TENNECOMP SYSTEMS

TP Card Manual

September 1, 1972

TENNECOMP SYSTEMS INC.

795 OAK RIDGE TURNPIKE ■ OAK RIDGE, TENNESSEE 37830

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NOTE: TP-048 through TP-149 are Open.

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* NOTE: Cards listed in this index with a * preceding their numbers are not described in this manual.

INTRODUCTION

The purpose of this booklet is to document the standard Tennecomp P.C. boards. The modules run from TP-001 upward. Each module has a block diagram or logic diagram showing the connection of the fingers to the actual circuit, the power and ground connections, and other information, including signal names and locations, vital to the understanding of the module. Accompanying each module is a summary sheet which gives a brief description of module operation and pertinent information.

TP-001

TP-001-1 contains 100 KHz oscillator, a frequency divider and logic for interrogating the clock flag. The module is to be used in experiments where a real or live time clock is needed. External clock at S2 replaces the 100 KHz internal clock in the -2 version of the module.

The clock is gated before it is applied to the divider. A high level signal at Enable Clock clears the divider in all conditions.

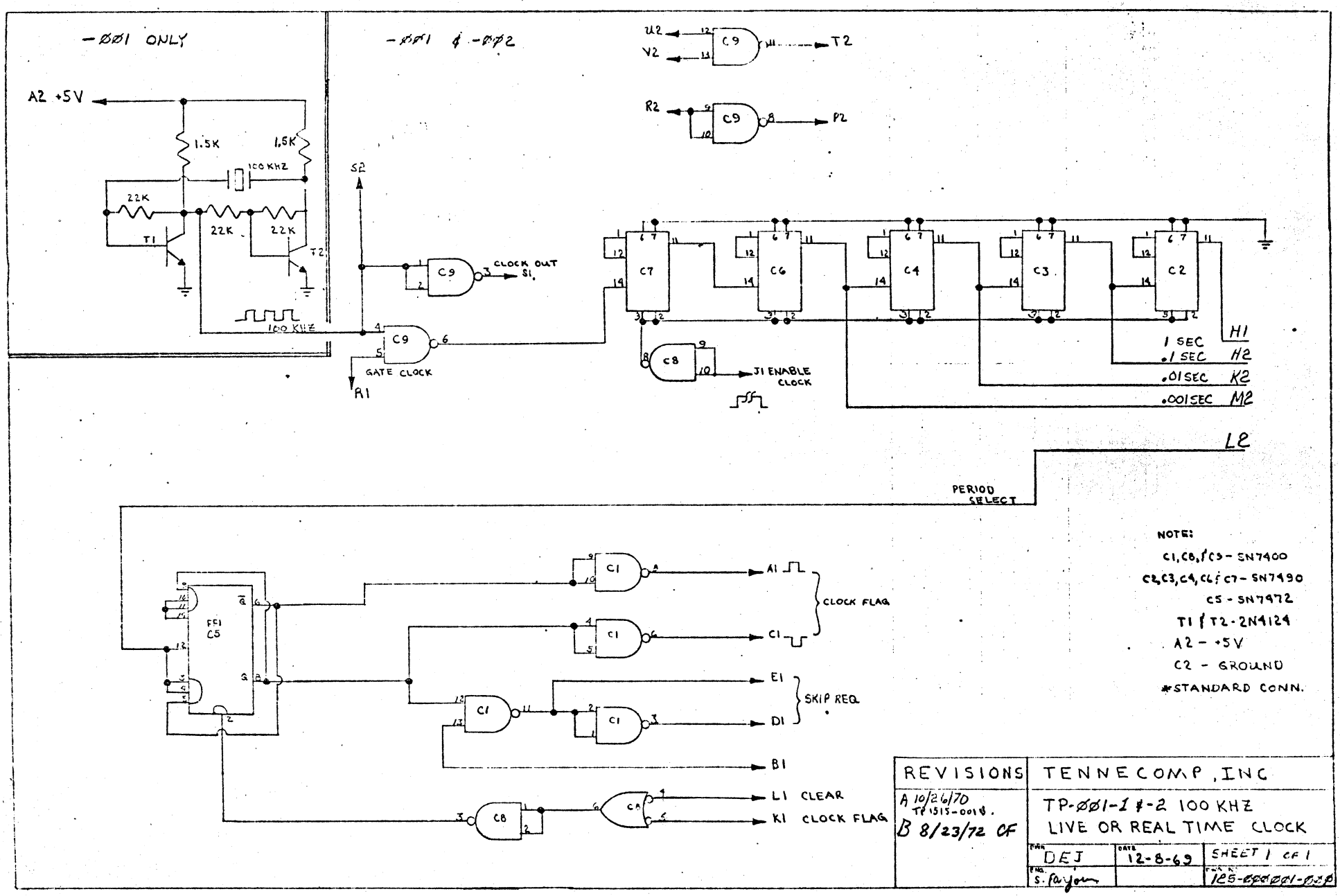
1 ms, 10 ms, .1 sec. and 1 sec. are tapped by connecting L2 to the appropriate pin—M2, K2, H2, H1, respectively—and the flag is raised with the negative transition of the signal from the divider. The clock flag may be cleared by applying a low level signal at L1 or K1. The clock flag is also internally gated with external IOT signals for easy connection to the skip bus, and both levels are available.

One inverter and one two-input NAND gate are also available.

Inputs: 1 unit load at all inputs; 2 unit loads at B1 IOT.

Outputs: E1, A1, T2, P2 capable of supplying 10 TTL unit loads each; D1, C1, and S1 supply 9 TTL loads each.

Card Format: A



NOTE:

C1, C8, & C9 - SN7400

C2, C3, C4, C6 & C7 - SN7490

C5 - SN7472

T1 & T2 - 2N4124

A2 - +5V

C2 - GROUND

*STANDARD CONN.

REVISIONS	TENNECOMP, INC
A 10/26/70 TP1515-0018. B 8/23/72 CF	TP-001-1 & -2 100 KHZ LIVE OR REAL TIME CLOCK
	DWN. DEJ — DATE 12-8-69 — SHEET 1 OF 1
	ENG. S. Fayon — TDR NO. 125-000001-000

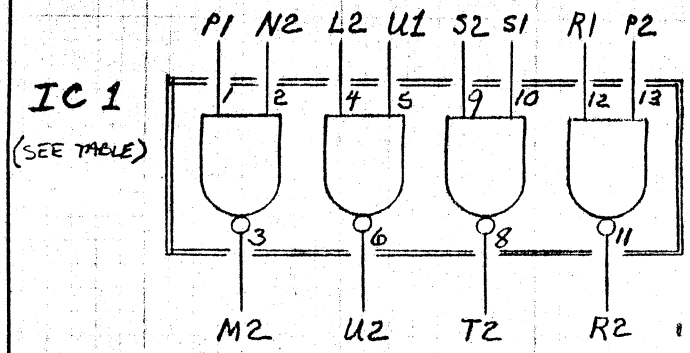
TP-002-n

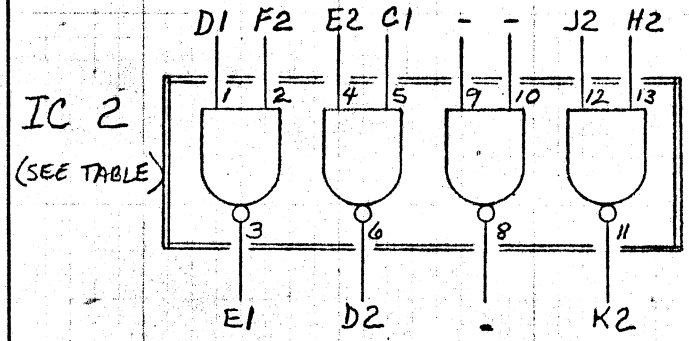
This general purpose card will accept 3 each 14-pin DIP integrated circuits. All logic pins are brought out to connector c except pins 8, 9, and 10 of IC2 and pin 3 and 11 of IC3. Power and ground pins are 14 and 7, respectively. In general, unused inputs must be tied to +3 volts. Pin V2 is provided on each card for this purpose. This pin can drive 40 inputs. Typical propagation delay is 15 ns. Card format is A.

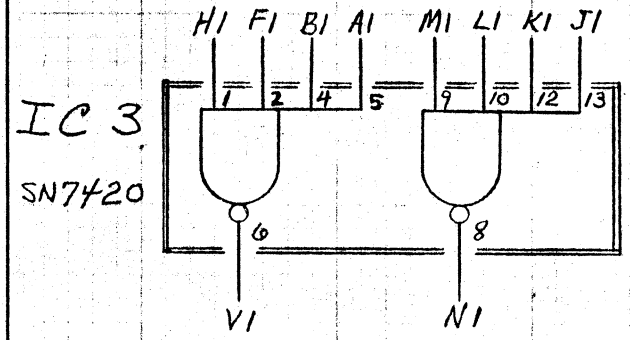
Dash Number	Input Loading (Unit Loads)			Output Drive (Unit Loads)			Power At +5 V (mA)	Description
	IC1	IC2	IC3	IC1	IC2	IC3		
1	1	1	1	10	10	10	40	NAND's 2x4, 7x2
2	1	1	1	10	10	10	50	NAND's 6x1, 3x2, 2x4
3	1	1	1	10	10	10	30	NAND's 3x2, 2x4, 1x8
4	*	1	1	*	10	10	100	Priority Gates + NAND's 3x2, 2x4
5	1	1	1	10	30	10	60	Power NAND's 3x2 + NAND's 4x2, 2x4
6	$\frac{1}{2}$	1	1	10	10	10	60	ST 4x2 + Open Collector 3x2 + NAND's 2x4
7	1	1	1	30	30	10	100	Power NAND's 7x2 + NAND's. 2x4
8	1	1	1	10	10	10	60	AND's 7x2 + NAND's 2x4
9	1	1	1	10	10	10	80	EX-OR (Open Collector) 7x2 + NAND's 2x4
10	1	1	1	10	10	10	70	OR 7x2 + NAND's 2x4
11	1	1	1	10	10	10	70	EX-OR 7 x 2 + NAND's 2 x 4
12	1	1	1	10	10	10	50	NAND 4x2I, NAND (0.6.) 3x2I, NOR 2x2I, 2 INV.
13	1	1	1	10	10	10	50	NAND (O.C.) 7x2I, NOR 2x2I, 2 INV.

(A unit load is defined as 1.6 mA into the gate.)

* See drawing.





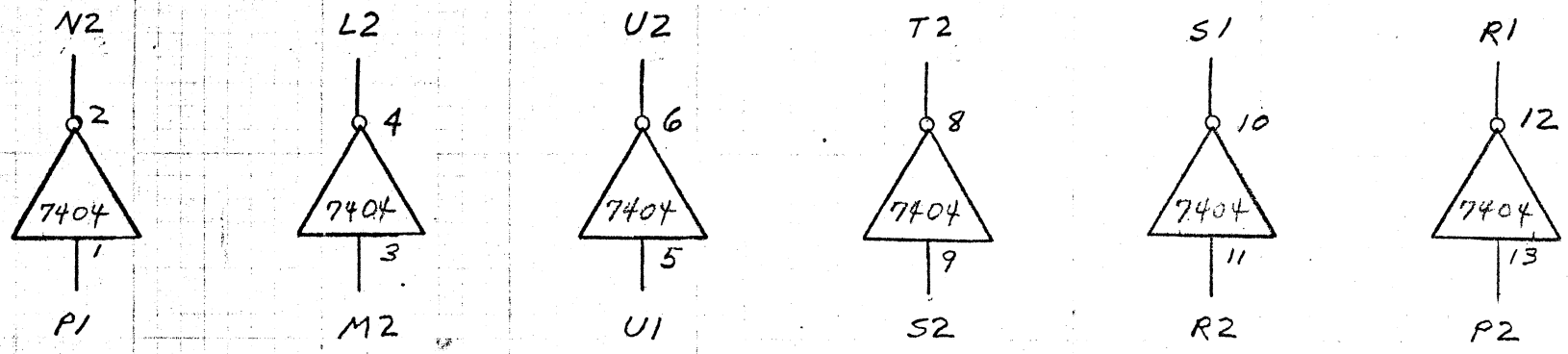


+3V — V2

CARD NUMBER	IC 1	IC 2
TP2-1	SN7400	SN7400
TP2-5	SN7400	SN7437
TP2-6	SN74132	SN7403
TP2-7	SN7437	SN7437

SN7400 2 INPUT NAND GATE
SN7403 2 INPUT NAND GATE -- OPEN COLLECTOR
SN7437 2 INPUT POWER NAND GATES (FAN OUT = 30)
SN74132 2 INPUT SCHMITT TRIGGER

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP002 GENERAL LOGIC		
	DESIGNED CF	APPROVED CF	SHEET 1 OF 1
	DRAWN CF	DATE 5/15/73	DWG. NO. 125-000002-001



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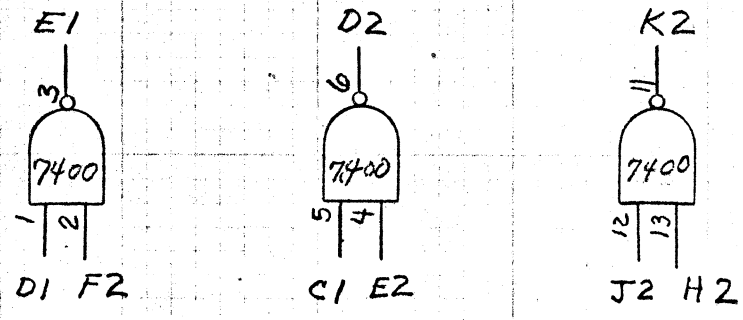
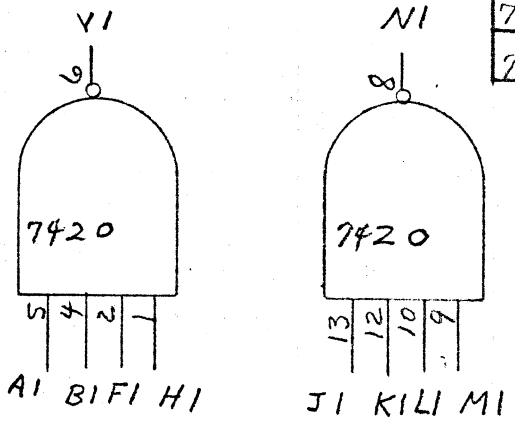
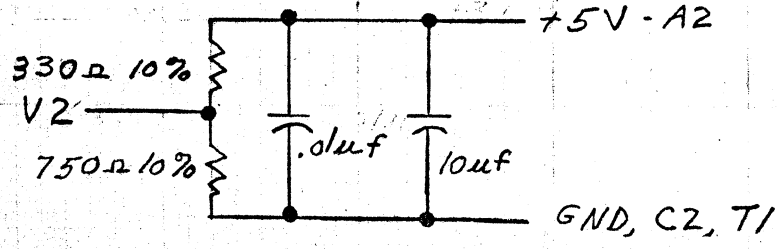
7420	T.I. 7420
7404	T.I 7404

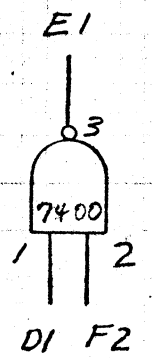


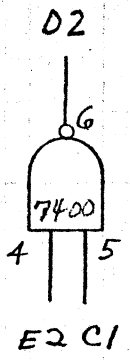


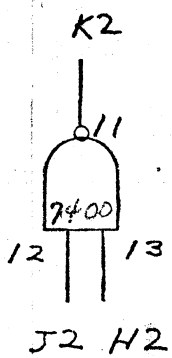


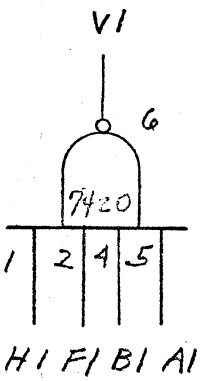
TP-0002A-E0

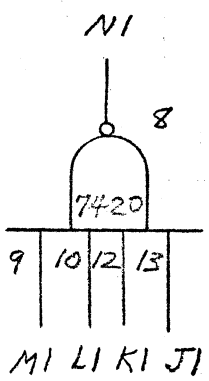
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-002-2 6 INVERTERS 3-2 INPUT NAND, 2-4 INPUT NAND		
	DESIGNED F.F.	APPROVED F.F.	SHEET 1 OF 1
	DRAWN G.T.	DATE 3-24-71	DWG. NO. 125-ab1an2-aa2

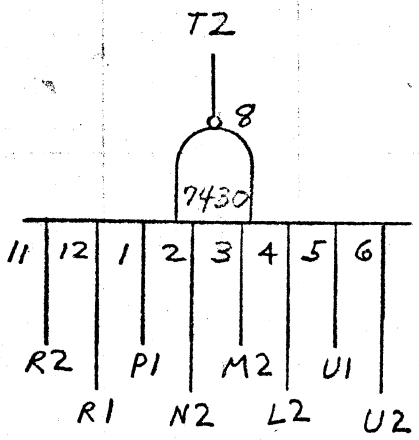












CODE	I. C. TYPE
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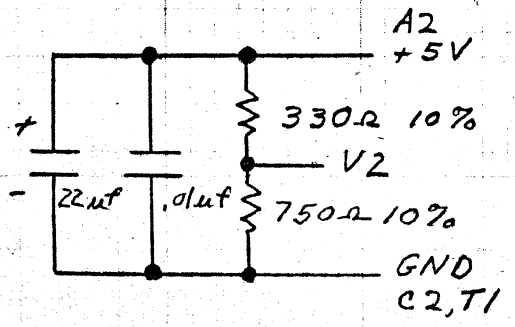
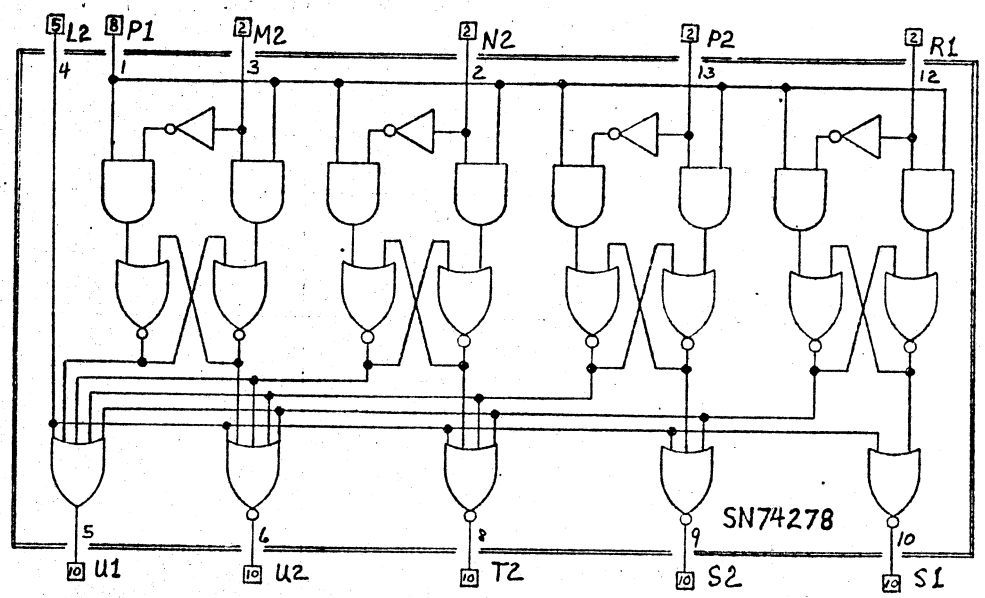
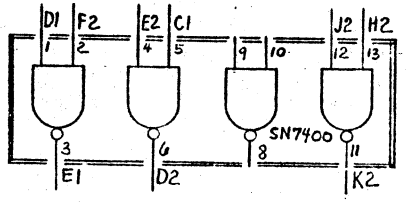
7420	T. I. 7420
7430	T. I 7430

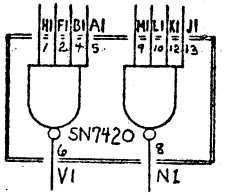


REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-002-3 3-2 INPUT NANDS 2-4 INPUT NANDS 1-8INPUT NAND		
	DESIGNED FF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 2-17-72	DWG. NO. 125-00002-003



+V — V2

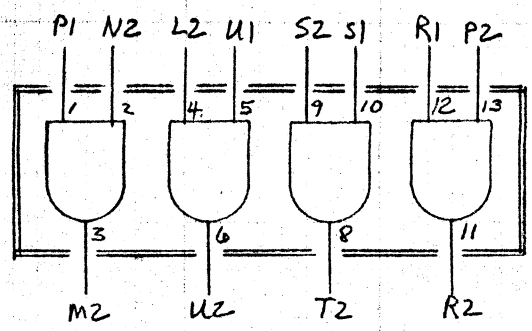


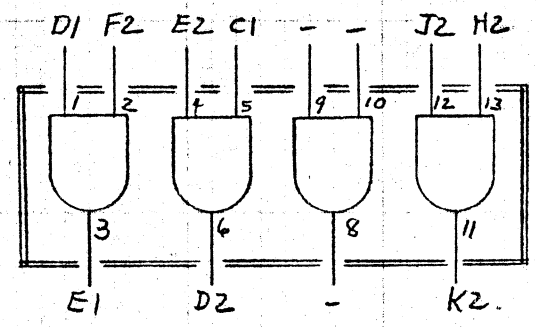


TP2-4

REVISIONS	TENNECOMP SYSTEMS, INC.		
	DESIGNED CF	APPROVED CF	SHEET 1 OF 1
	DRAWN CF	DATE 5/15/73	DWG. NO. 125-000002-004

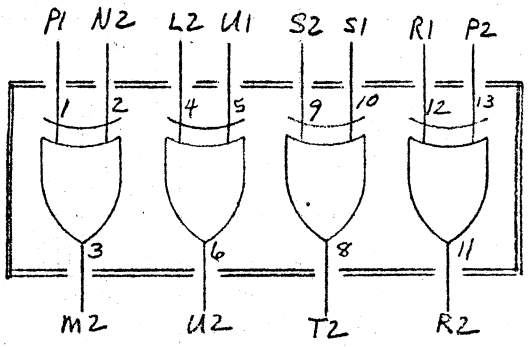
-8 ONLY

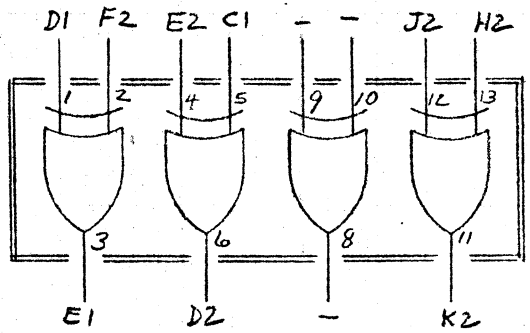




SN7408

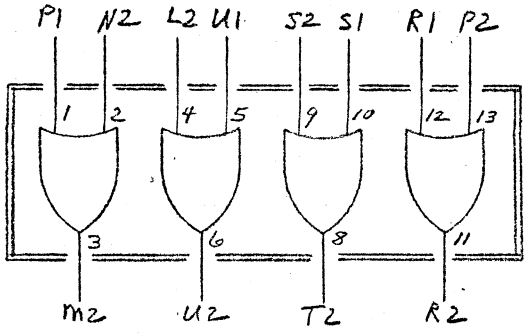
-4 ONLY

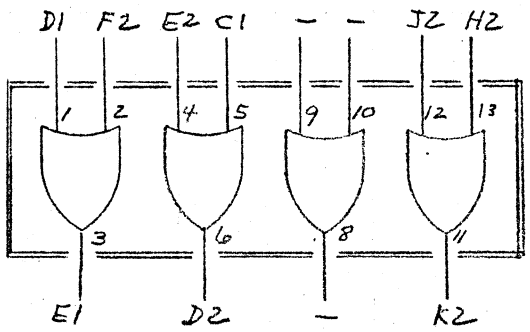




SN74136

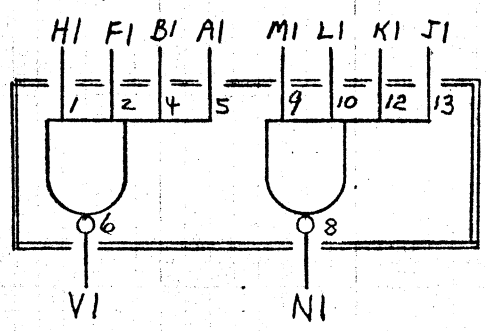
-10 ONLY





SN7432

-8, -9, -10

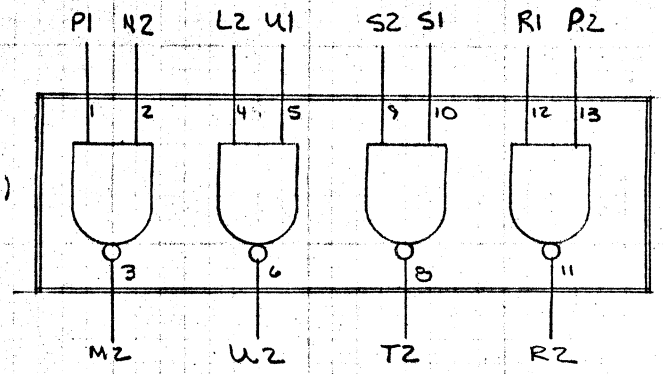


SN7420

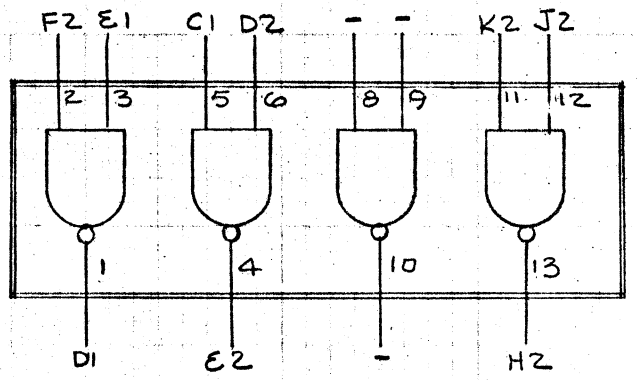
+3V —— V2

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP002 GENERAL LOGIC

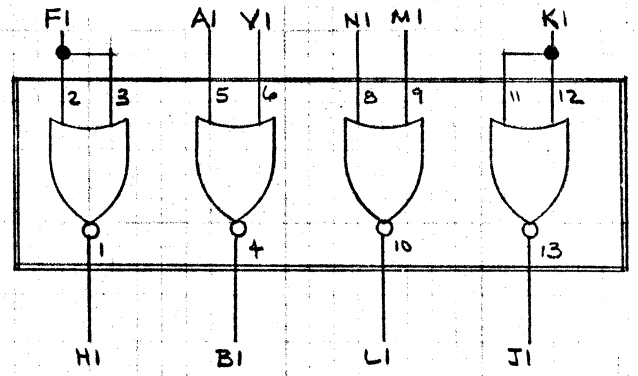
DESIGNED	APPROVED	SHEET 1 OF 1
CF	CF	
DRAWN	DATE	DWG. NO.
CF	5/15/73	125-000002-008



IC 1
(7400)



IC 2
(7401)



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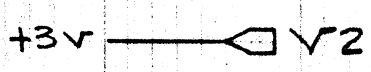
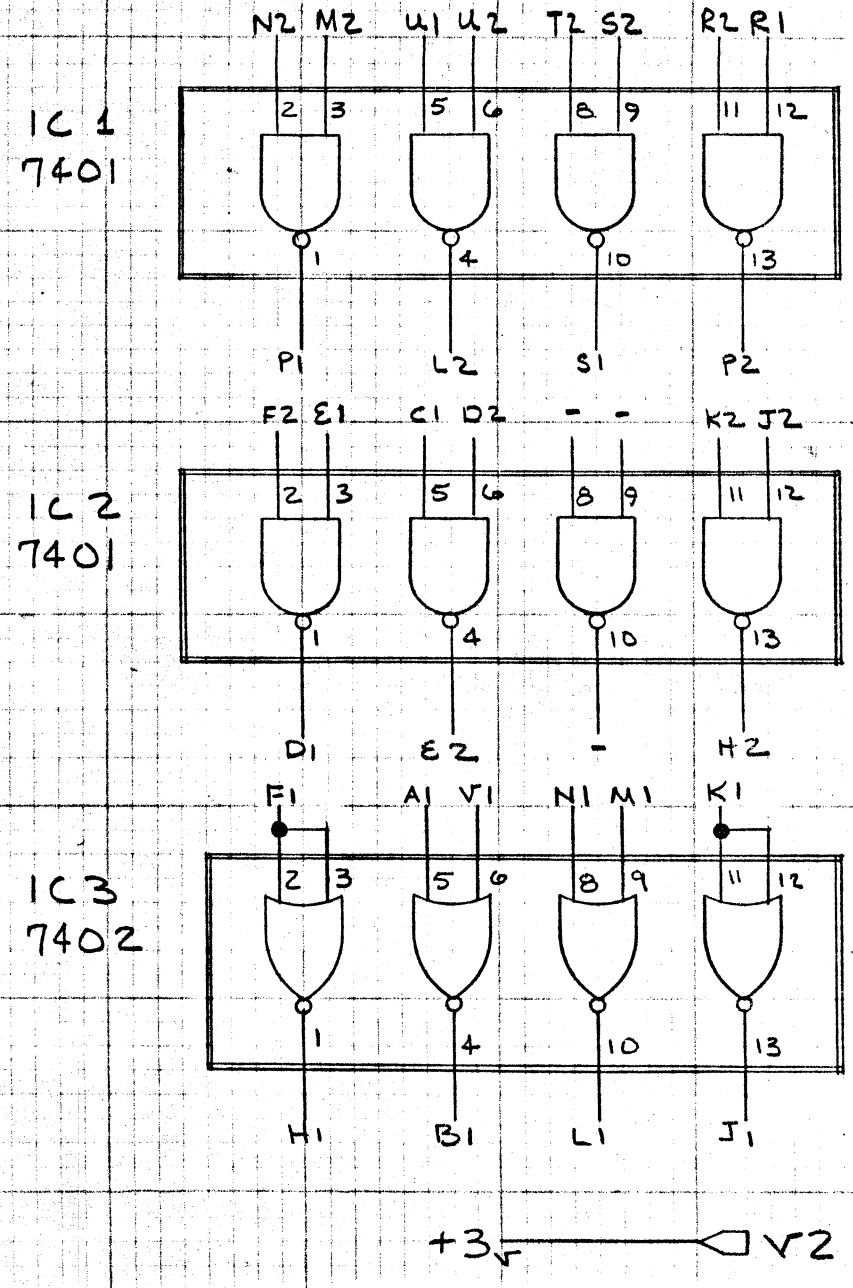
(7402)



SN 7400 - 2 INPUT NAND GATE
SN 7401 - 2 INPUT NAND GATE (OPEN COLLECTOR)
SN 7402 - 2 INPUT NOR GATE

NOTE -
AT ASSY., JUMPER PINS 2-3, 11-12 ON IC PAD 3 (ONLY) WITH 30 GA. WIRE.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP002-12 NAND 4X2I, NAND(O.C.)3X2I, NOR2X2I, 2 INV.		
	DESIGNED ADR	APPROVED	SHEET OF
	DRAWN	DATE 9/6/73	DWG. NO.



SN7401 - 2 INPUT NAND GATE (OPEN COLLECTOR)
SN7402 - 2 INPUT NOR GATE

NOTE -
AT ASSY., JUMPER PINS 2-3, 11-12 ON IC PAD 3 (ONLY) WITH 30 GA. WIRE.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP002-13 NAND (O.C.) 7X2I, NOR 2X2I, 2 INV.		
	DESIGNED ADR	APPROVED	SHEET OF
	DRAWN RCC	DATE 9-6-73	DWG. NO.

TP-003

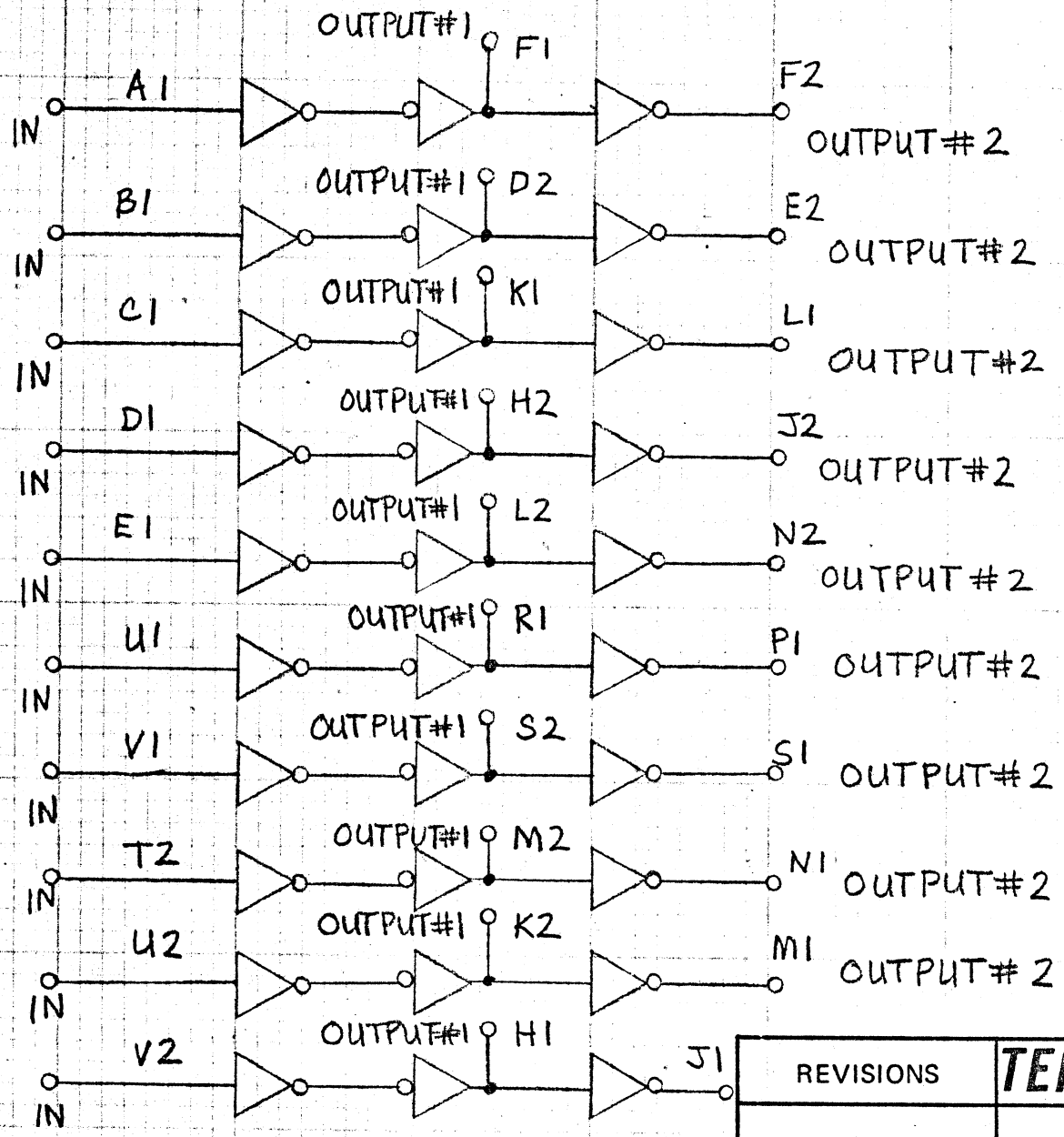
The TP-003 is a positive input/output receiver card for use with the PDP-15. It contains 10 high-input impedance circuits of at least 27 K ohm and input switching thresholds of about +1.5 volts. Each receiver has two outputs, one of the same polarity as the input, the other the inverse of the input. The receiver card can be used anywhere on the I/O bus, but power (B+) must be applied at all times, since the input impedance drops to 1 K ohm when power is off.

Inputs: The input impedance is 27 K ohm (min). Each input load current is 80 μA (max), and the threshold switching level is 1.4 to 1.6 volts.

Outputs: Output #1 fan out = 9 unit loads. Output #2 fan out = 10 unit loads. Output #2 delay = 50 nsec (from input).

Power: +5 volts at 170 mA (max)

Format: A



POWER + 5V A2
GROUND - C2, T1

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-003 RECEIVER		
	DESIGNED S. FAGIN	APPROVED S. FAGIN	SHEET 1 OF 1
	DRAWN GARY	DATE 10-30-70	DWG. NO. TP-0003A-E0

TP-004

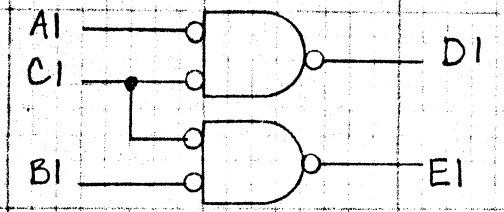
The TP-004 contains twelve two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Each driver can sink 100 mA at ground and allows a maximum output voltage of +20 volts. The output consists of an open collector NPN transistor.

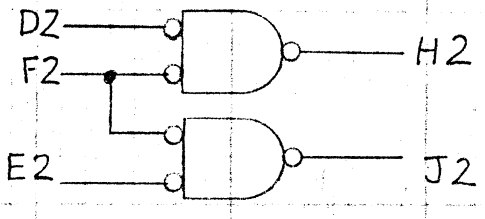
Inputs: Input levels are standard TTL levels of 0 volts and +2.4 volts. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All Other inputs present two unit loads.

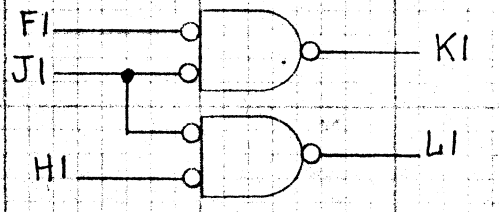
Outputs: A driver output will be at ground when both inputs are at ground. Output rise and fall (TTT) are typically 30 nsec when a 100 mA resistive load is connected to a driver output. Output voltage must not exceed +20 volts.

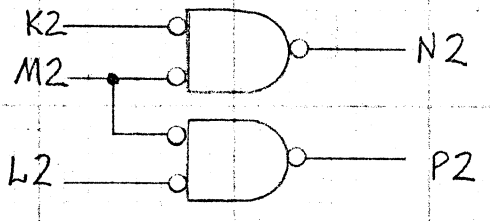
Power: +5 volts, 71 mA (max) plus external load.

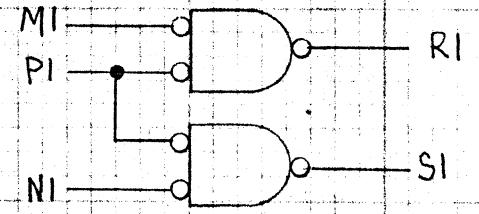
Format: A

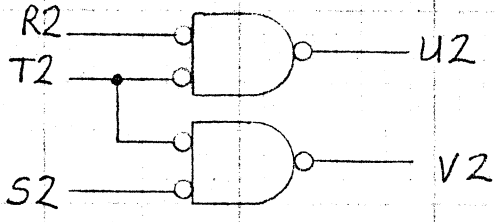






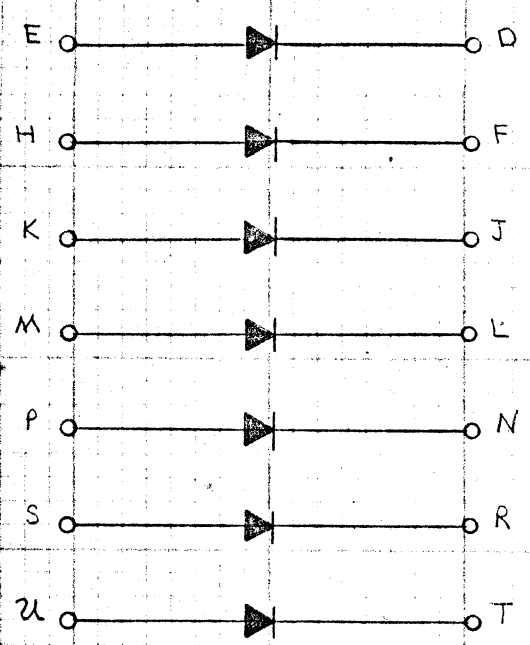






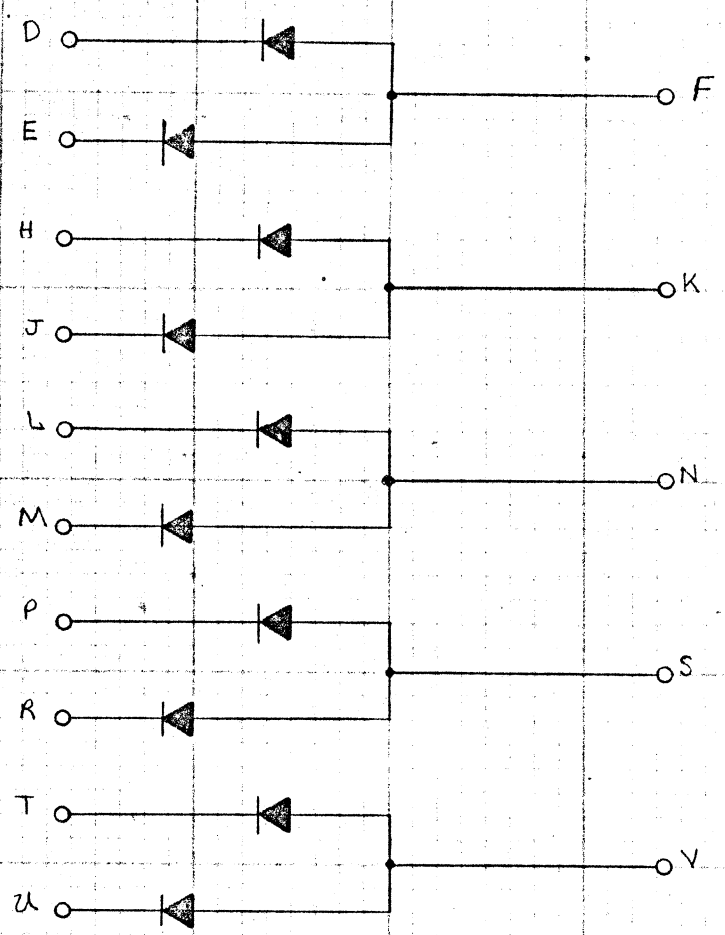
A2 +5VOLTS
C2, T1 GND.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-001 BUS DRIVER		
	DESIGNED S. FAYSON	APPROVED S Fayson	SHEET 1 OF 1
	DRAWN GARI	DATE 11-30-70	DWG. NO. TP-0001A EO



ALL DIODES IN281

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-005 DIODE NETWORK
	DESIGNED: S Parfon / APPROVED: F.P. / SHEET 1 OF 1
	DRAWN: D. Johnson / DATE: 5-20-70 / DWG. NO.



ALL DIODES 1N281

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-006 DIODE NETWORK
	DESIGNED: S. Fowler / APPROVED: F. F. [illegible] / SHEET 1 OF 1
	DRAWN: D. JOHNSON / DATE: / DWG. NO. [illegible]

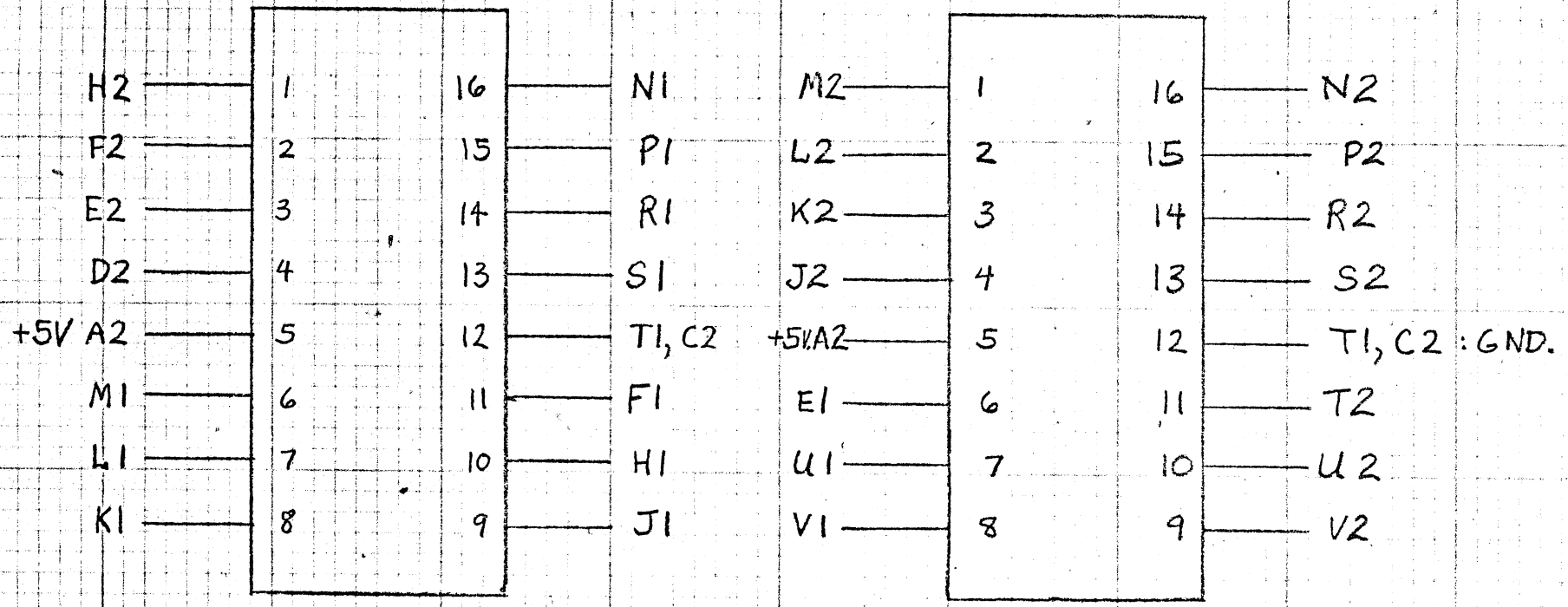
TP-007 Universal Card

This card can take any two 16 pins IC which has pin 5 as V and pin 12 as GRD. The card became very useful with the introduction of many MSI IC's which contain complex functions in one dual in-line package.

e.g.: With the 7475 IC, the card is used as an 8-bit latch register, while two 7483 make it an 8-bit adder/sub.

Format: A

Dash Number	Description
1	Two 4-bit Adder
2	Two 4-bit latch registers



VCC = A2
GND. = T1, C2

NOTE: USE 16 PIN INTERGRATED CIRCUIT WHICH HAS THE POWER ON PIN 5 AND THE GROUND ON PIN 12.

TP-007A-E0

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-007 UNIVERSAL		
	DESIGNED S. PARSONS	APPROVED S. Fanjoy	SHEET 1 OF 1
	DRAWN GARY	DATE 11-4-70	DWG. NO. 125-000007-000

TP-007-1 Two 4-Bit Adders

Two four-bit full adders are provided in this card. The adders may be used in medium to high speed, parallel add/serial carry applications. Each 4-bit full adder performs the additions of two four-bit binary numbers. Sum (Σ) outputs are provided for each bit, and the resultant carry is obtained from the last bit of each of these adders. Total carry time of the stage is typically 45 nsec and a maximum of 65 nsec.

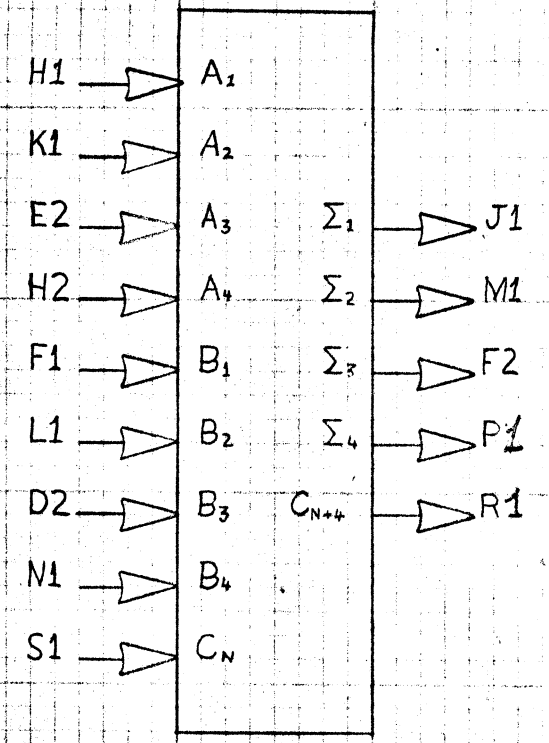
A4 (at pin H2 or M2) and B4 (at pin N1 or N2) are the most significant bits, while A1 and B1 are the least significant bits. C_n is the input carry from the previous stage; C_{n+4} is the output carry from the stage.

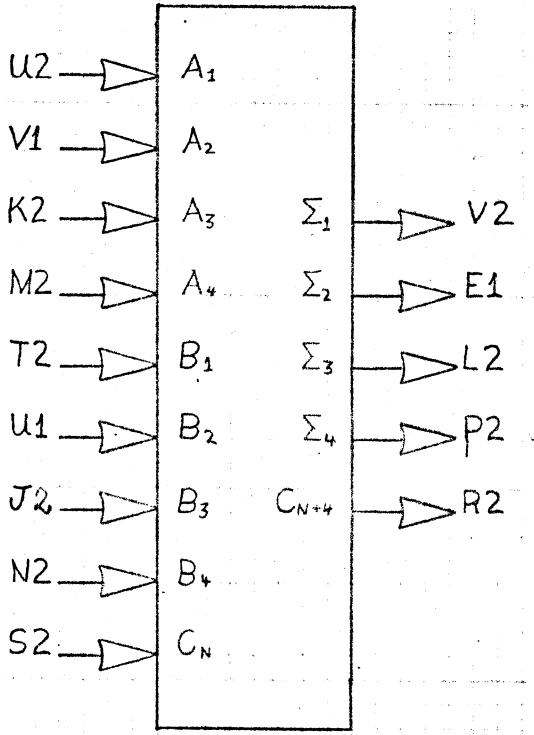
Inputs: H1, E2, F1, D2, U2, K2, T2, J2, S1 and S2 require 4 unit loads each. All other input represents one unit load (-1.6 mA max. at "0" level and 40 μA max. at the "1" level).

Outputs: Each output is capable of sinking 10 unit loads.

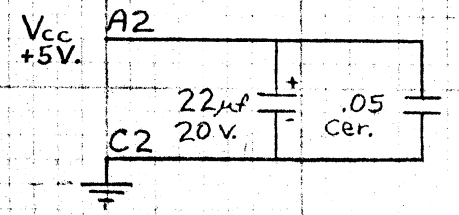
Note: IC's used are SN7483N or equivalent.

Format: A





V_{cc} = A2
GND = C2 & T1



NOTE: USE 7483N

TP-0007B-E0

REVISIONS	TENNECOMP SYSTEMS, INC.		
REVISED PER ECN 30 S. FAY REVISION B NOV. 5, 1970 G. Turner	TP-007-1 TWO 4-BIT ADDER		
	DESIGNED E. PARSONS	APPROVED S. Fay	SHEET 1 OF 1
	DRAWN J.A.L.	DATE	DWG. NO. 125-0000079-000

TP-007-2 Two 4-Bit Latch Registers

Four pairs of latches are available in this card - each pair having common clock input. Each latch provides complementary polarities at the output. Information present at a data input (e.g., F2, E2, etc.) is transferred to the output (N1, P1, etc.) when the clock is high, and the output will follow the data input as long as the clock remains high. When the clock goes low, the information that was present at the data input at the time the transition occurred is retained at the output until the clock is permitted to go high.

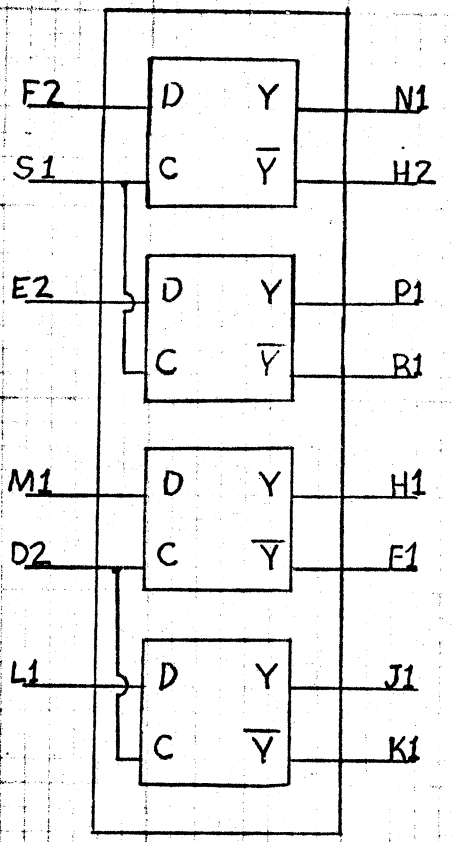
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

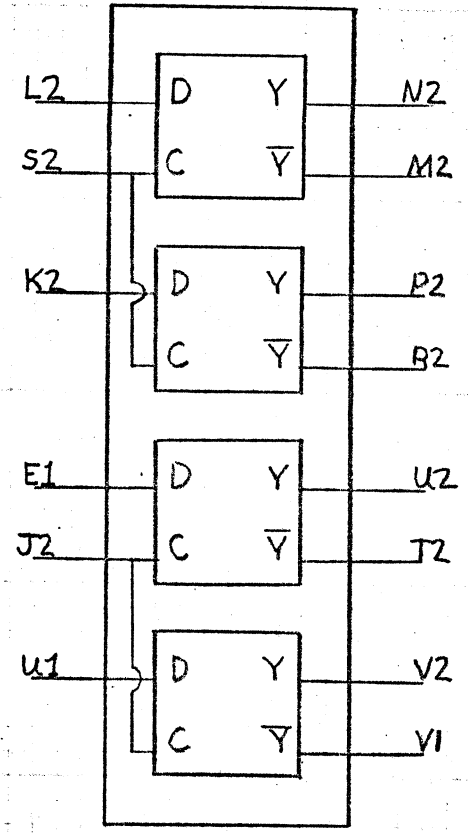
Inputs: Each data input presents 2 unit loads. Each clock input presents 4 unit loads.

Outputs: Each output provides fan-out of ten unit loads.

NOTE: IC's used are SN7475N or equivalent.

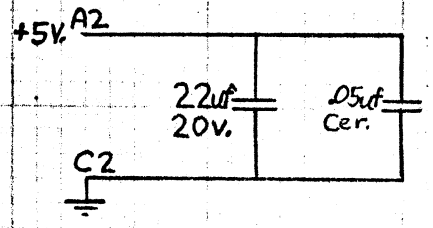
Format: A





Vcc = A2

GND = C2 + T1



I. C. 15 7475

TP-0007C-E0

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-007-2 TWO 4-BIT LATCH REG.		
	DESIGNED S. FARSCHI	APPROVED S. Farjam	SHEET 1 OF 1
	DRAWN J.A.L.	DATE 10-29-70	DWG. NO. 125-000007-000

TP-008 8-Bit Buffer Shift Register

The TP-008 is a general purpose, 8-bit buffer/shift register. Provision is made for gating single-ended parallel load from two different sources. The module is divided into two 4-bit registers, each having separate "Load", "clock" and "clear". However, this division may be modified into two blocks of 5 bit and 3 bit registers by patching on the module.

When "Load A" input is high, word A (J1, F2, J2, D1) is applied to the flip-flops. High level on "Load B" input causes word B (E1, K2, H1, H2) to be selected. The selected word is shifted to the output terminals (C1, D2, E2, L1) on the negative going edge of the clock pulse. A high level at the Direct "Clear" input clears the register at all input combinations.

Right and left shift may be performed by selective wiring of the outputs to the inputs. Connections of C1, D2, E2 to F2, J2, D1, respectively, while "load A" is high will cause a right shift on the negative going edge of the clock. In this case, J1 will serve as the serial input and L1 as the serial output.

Connecting L1, E2, D2 to H1, K2, E1, respectively, with "Load B" high will cause left shift on the negative going edge of the clock. However, in this case, H2 will serve as the serial input, and C1 as the serial output.

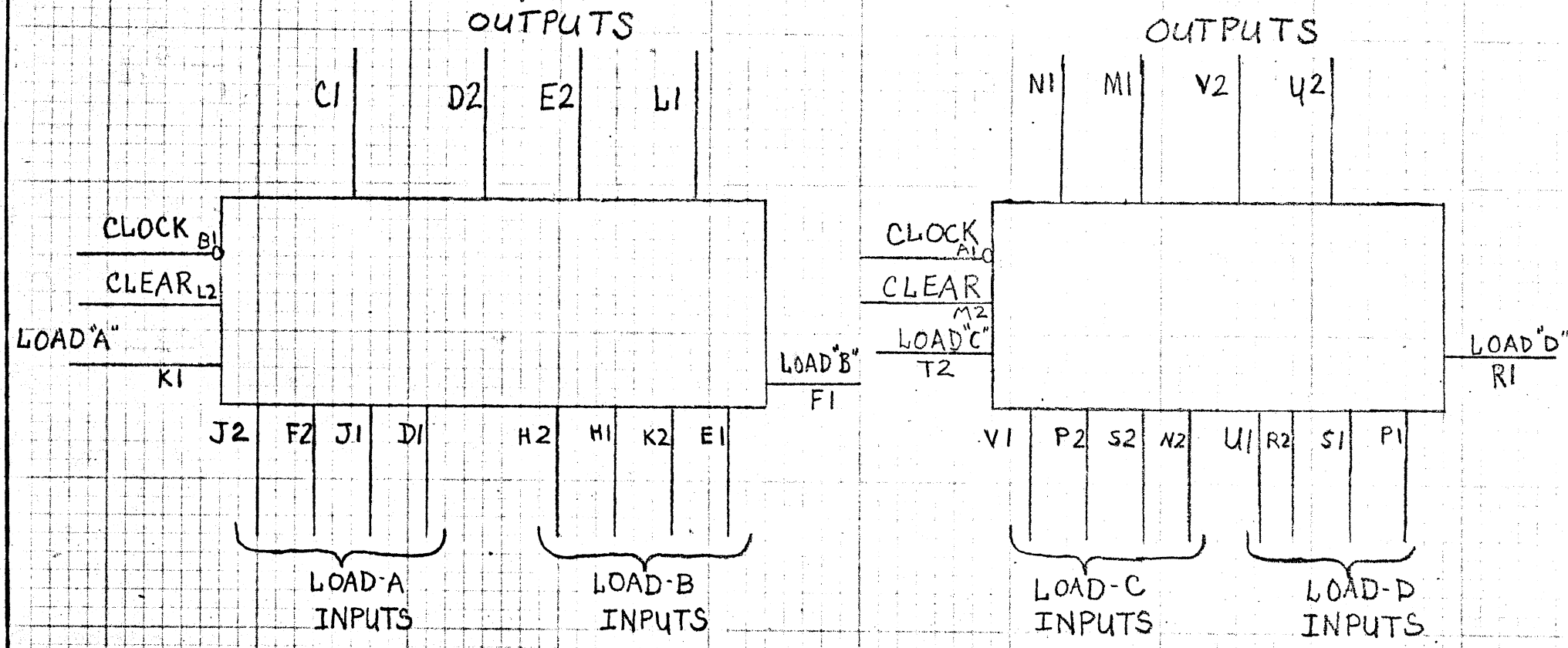
Data shifted or parallel loaded into the TP-008 will appear on the outputs within 55 nsec (max) of the clock pulse negative going edge threshold. "Load" and "Data" must be present at least 50 nsec prior to the clock pulse. Propagation delay from the leading edge of a "Clear" pulse to the output is 40 nsec max.

Inputs: Data inputs, "clock" and "clear" present one unit load each. "Load A" and "Load B" inputs present 4 unit loads in the standard division (4-4), and 5 unit loads in the 5-3 division.

"Load C" and "Load D" present 4 unit loads each on the standard division (4-4) and 3 unit loads each on the 5-3 division.

Outputs: Parallel outputs are capable of driving 10 unit loads each.

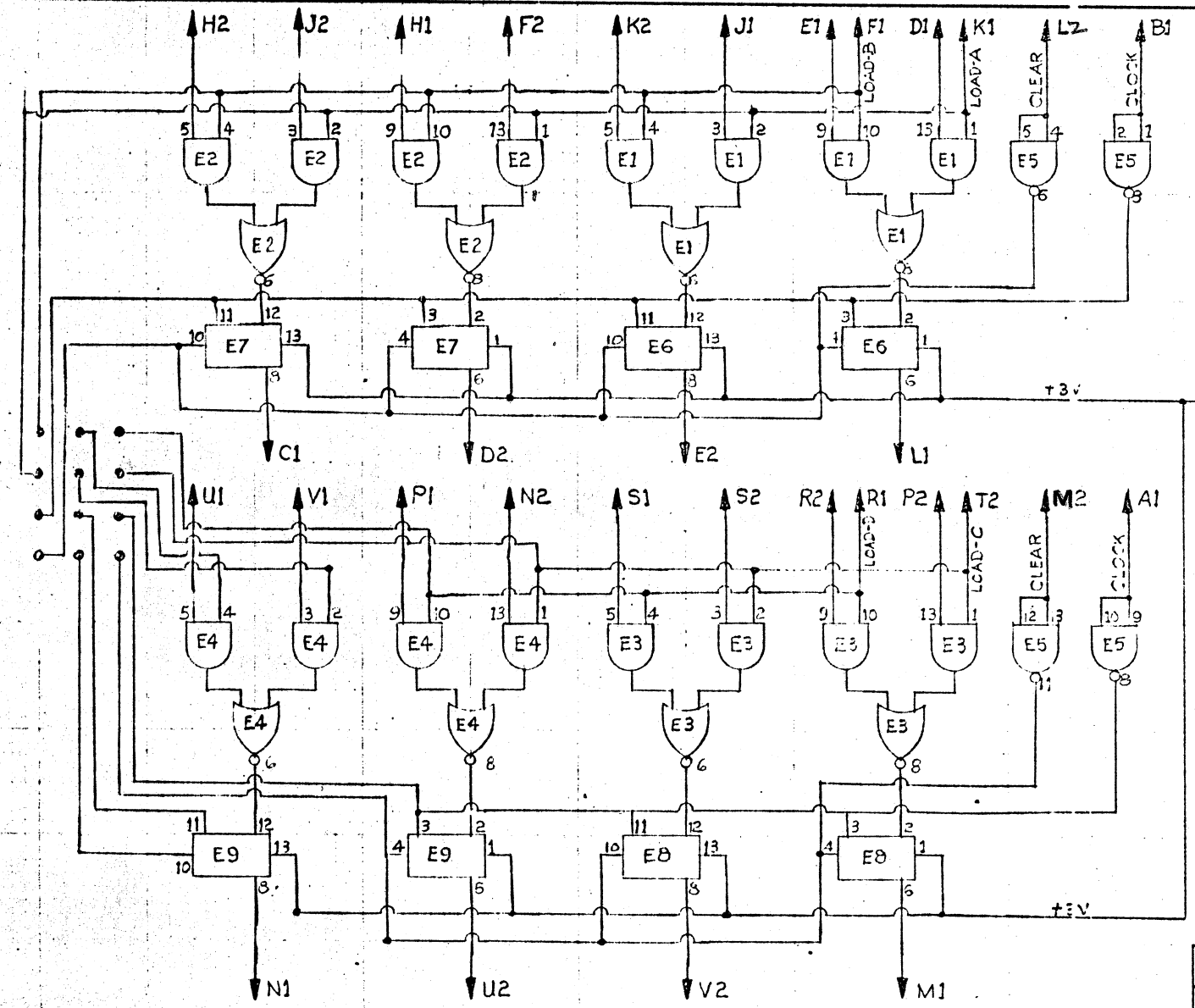
Power: +5 volts, 184 ma (max).

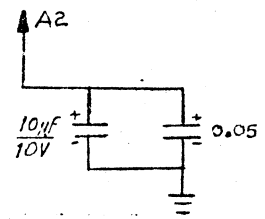


POWER +5 VOLTS — A2
GROUND —— C2-T1

NOTE: THE STANDARD DIVISON IS TWO SETS OF FOUR FLIP-FLOPS EACH. BY PATCH WIRING ON THE CARD THE DIVISON COULD BE CHANGED TO A SET OF FIVE AND THREE.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-008 8 BIT BUFFER SHIFT REGISTER		
	DESIGNED	APPROVED	SHEET 1 OF 1
	DRAWN GARI	DATE 10-29-70	DWG. NO.





NOTES:- E1 – E4 = SN7451N
E5 = SN7400N
E6 – E9 = SN7474N

REVISIONS	TENNECOMP SYSTEMS, INC
	TP008
	4 BIT BUFFER SHIFT REGISTER
	DESIGNED / APPROVED / SHEET / OF /
	DRAWN / DATE 8-12-70 / SCALE NONE

TP-009

This module provides general-purpose gating and is most commonly used for decoding, comparison, and control. The module performs the NAND function $\overline{A \cdot B \cdot C \cdot D}$.

TP-009— Six, four-input NAND gates.

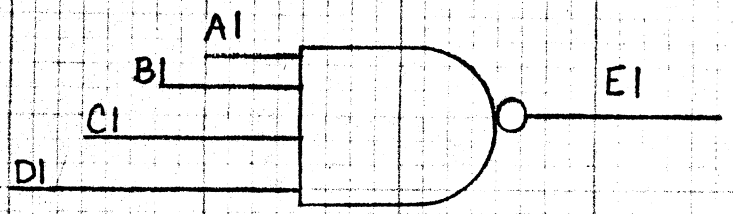
Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the TP-009, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads.

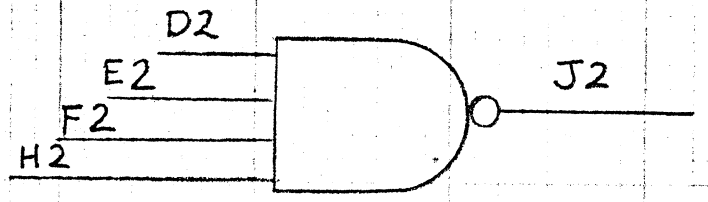
Typical propagation delay of the gates is 15 nsec.

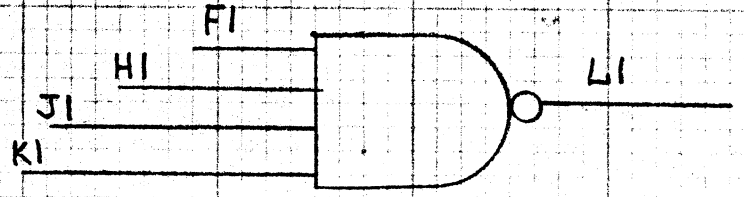
Inputs: Each input presents one unit load.

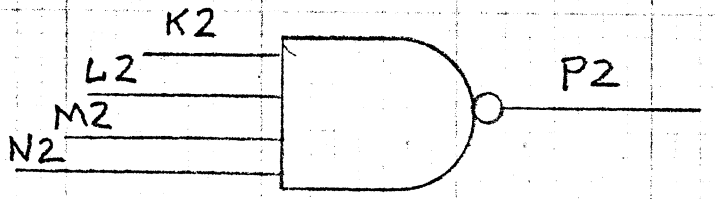
Outputs: Each output is capable of supplying 10 unit loads.

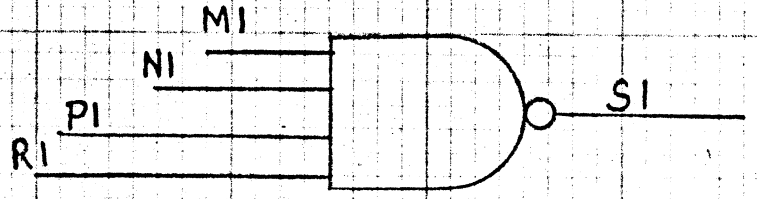
Power: 41 ma. + Max. current at 5 volts.

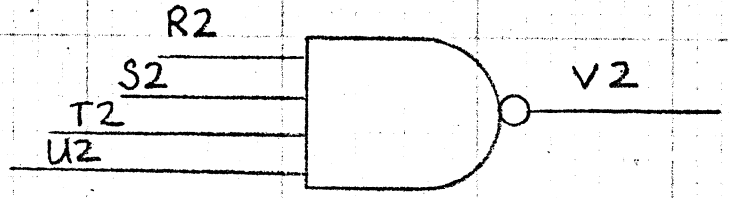












POWER +5 VOLTS — A2
GROUND — C2, T1
+3 VOLTS — U1, V1, UNUSED INPUTS

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-009 4-INPUT NAND GATES		
	DESIGNED [illegible]	APPROVED S. Farjoun	SHEET 1 OF 1
	DRAWN GARI	DATE 10-30-70	DWG. NO. TP-0[illegible]

TP-010 Universal

This card can take any two 16 pins IC which has pin 8 as GRD and pin 16 as V_{cc}. The card became very useful with the introduction of many MSI IC's which contain complex functions in one dual in-line package.

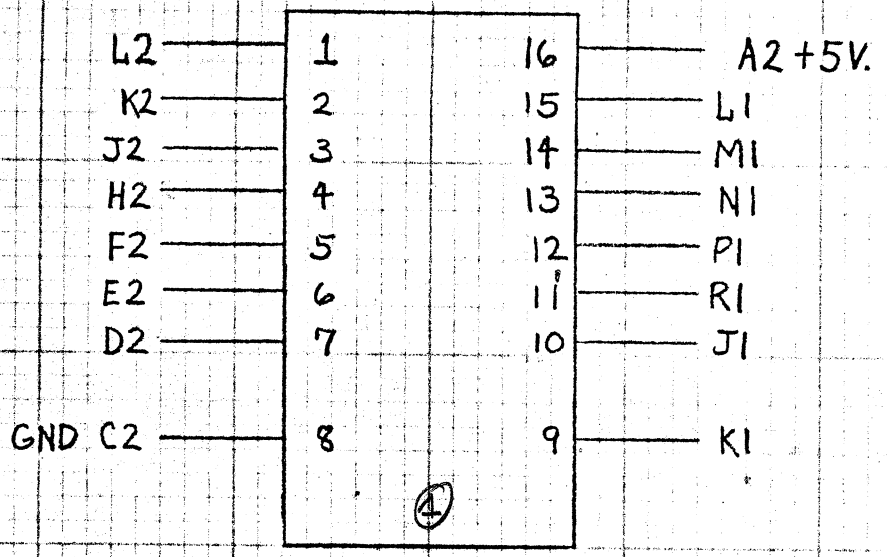
The card can also take the 14 pin IC, which has pin 7 as GRD and pin 14 as V_{cc}. In this case, pin 8 on the card should be connected to pin 7 on both IC's.

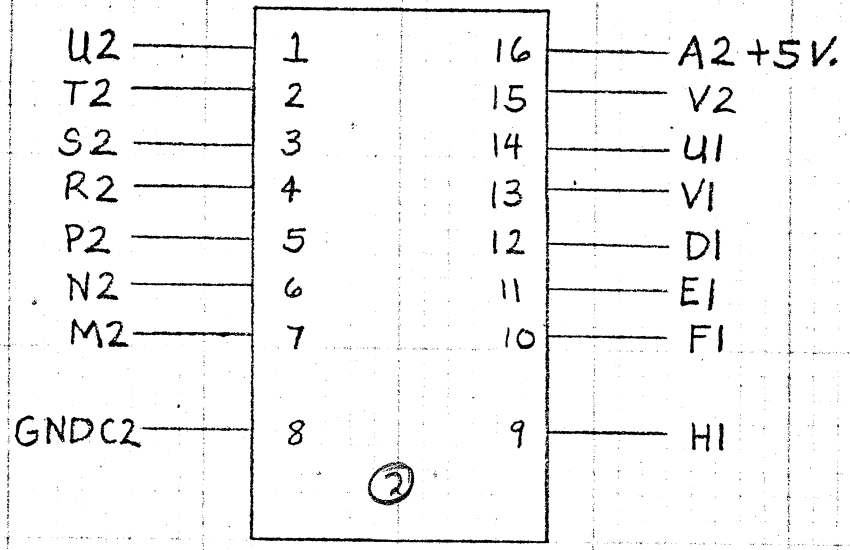
Pin S1 is available as a source of +3 volts for connection to unused inputs. The drive capability of this source is 30 unit loads.

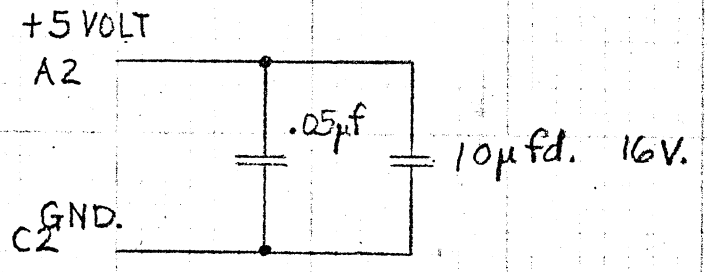
Format: A

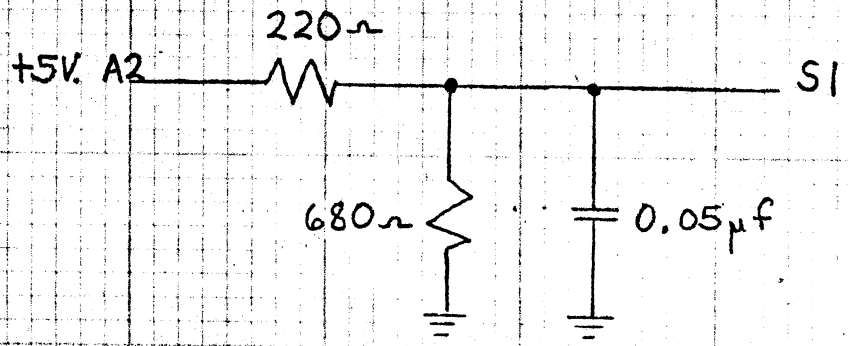
Dash Number	Name
1	Dual 4-bit Counter/Storage
2	Six 3-input or Gates
3	Four D-type Flip-Flops
4	Two one-shots
5	Dual 4-Bit Multiplexer
6	Dual 4-Bit Presetable Decade Counter
7	Quad Schmitt Triggers
8	Dual Non-inverting 1-of-8 Line Decoder
9	Mixed Schmitt triggers and Open Collector Gates
10	Dual 4x4 Register File (SN74170)
11	Dual Quad D-Register (SN74175)
12	Dual Hex D-Register (SN74174)
13	4 Line to 10 Line Decoder + Hex Inverter

Dash Number		Name
14		Dual Synchronous 4-bit Counters (SN74163)
15		Dual 4-line To 10-line Decoders (SN7442)
16		SP380A + SN7400
17		Quad Single Shot
18		8 2 NAND Unibus Drivers (N8881)
19	②	ONE OF 8 Decoder MC4048P (MOT)
	①	45 stage Binary Counter DM 8681N (NS)









NOTE: USE INTERGRATED CIRCUIT WHICH HAS PIN 8 GND. AND PIN 16 VCC.

TP-0010A-E0

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010 UNIVERSAL		
	DESIGNED: S. Fankhouser	APPROVED: S. Fankhouser	SHEET 1 OF 1
	DRAWN: GARY	DATE: 11-4-70	DWG. NO.: 125-000010-000

TP-010-I Dual 4-Bit Presettable Counter

Two 4-bit presettable counters make up this module. Each counter contains separated one flip flop and three cascaded flip flops, which may be connected to obtain a modulo sixteen counter. Each counter features strobed single-ended parallel entry capability with a separate Reset which is common to all four bits of the counter.

To implement the count function, the individual flip flops were made to exhibit J-K characteristics with a charge storage clocking scheme. Change of state is effected on the negative transition edge of the clock pulse. The clock pulse amplitude must be at least 2.6 volts for at least 25 ns, fall time, independent of pulse width, must be less than 75 ns. The maximum allowable input pulse repetition rates to "Clock 1" (J1, F1) is 35 MHz, while 20 MHz is the maximum allowable at "Clock 2" (E2, N2).

When data strobe (L2) is low, parallel data present at data input (H2, P2, J2, N1) are transmitted to the respective counter outputs. Data transfer is accomplished in parallel fashion with strobe active for 30 ns or more. The DATA STROBE is direct coupled and, therefore, is not sensitive to rise and fall times and is dominant over "Clock 1" and "Clock 2" inputs. RESET, when at "0" level, clears all flip-flops. Total reset may be accomplished in less than 30 ns. The activation of RESET ("0") dominates both Clock and Strobe and, therefore, may be used as a count inhibit command. Clocking transition may be accepted typically 20 ns following the entry of parallel data or the activation of RESET.

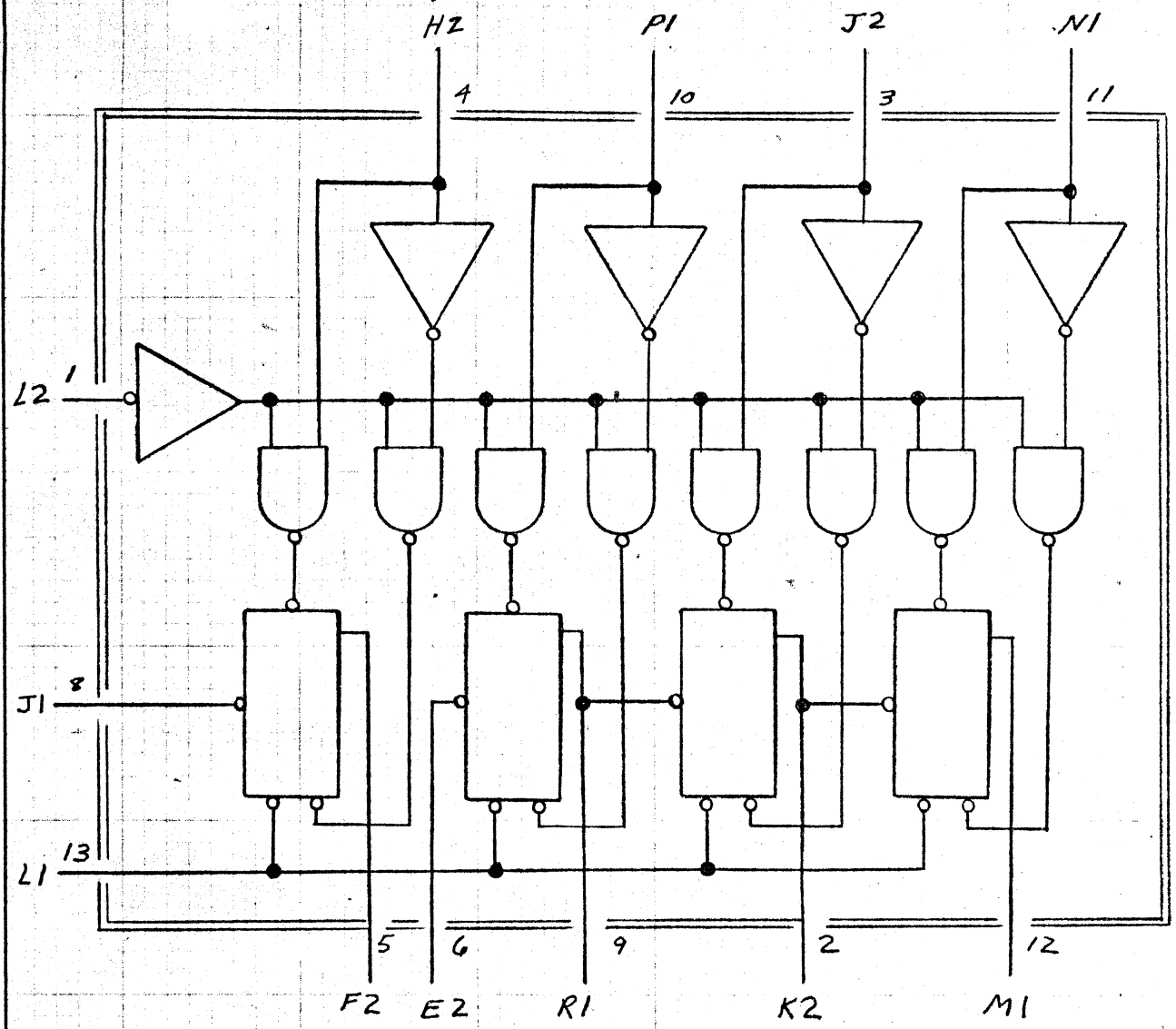
Inputs: DATA STROBE (L2, U2) and DATA IN (H2, P1, J2, N1; R2, D1, S2, V1) present 1 unit load.

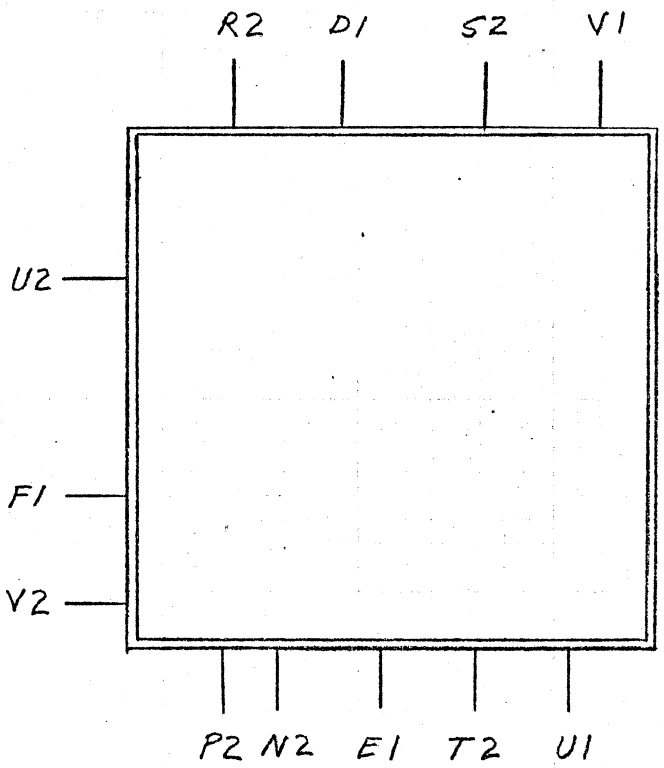
RESET (L1, V2) presents 2 unit loads.

CLOCK 1 and CLOCK 2 (J1, F1; E2, N2) present 3 unit loads each.

Outputs: R1, K2, E1, T2 can sink 6.4 ma each. F2, M1, P2, U1 can sink 9.4 ma each.

Note: S1 - Unused +3 v. input supplies 40 unit loads.





IC IS SYGNETICS 8281

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010-1 DUAL 4 BIT COUNTER / STORAGE		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO. 114-000010-001

TP-010-2 OR Gates

This module provides general purpose gating for the TP series. The module contains six 3-input OR gates.

Unused inputs should be grounded. A source of +3 volts is available at pin S1.

Typical propagation delay is 15 nsec.

Inputs: Each input presents one unit load.

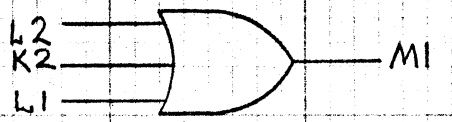
Outputs: Each output is capable of supplying 10 unit loads.

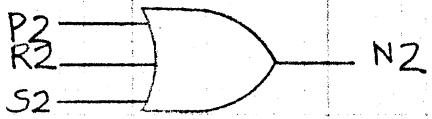
Power: +5 volts at ground.

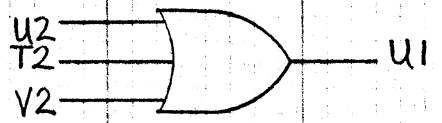
A2 - +5 V
C2-T1 GRD

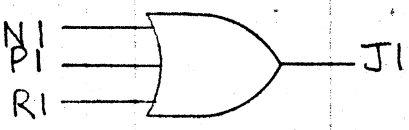
Format: A

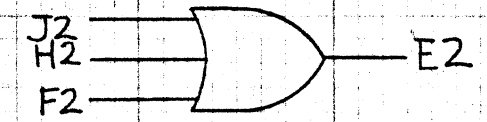
NOTE: IC's used are US7418A

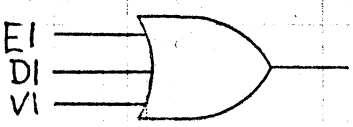












TP-0010C-E0

Note: VCC - A2

GND. - C2, T1

USE : US7418A.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TR010-2 3 INPUT OR GATES		
	DESIGNED: S. FARROW	APPROVED: S Farrow	SHEET 1 OF 1
	DRAWN: GARY	DATE: 1-18-71	DWG. NO.: 114-000010-002

TP-010-3 Quad D-Type Flip-Flops

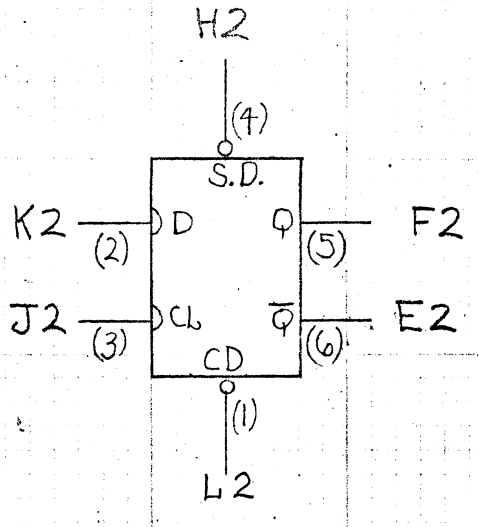
This module contains 4 independent D flip-flops with complementary outputs and direct set and clear. Input information is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going edge. Pin S1 supplies 40 unit loads at +3 volts.

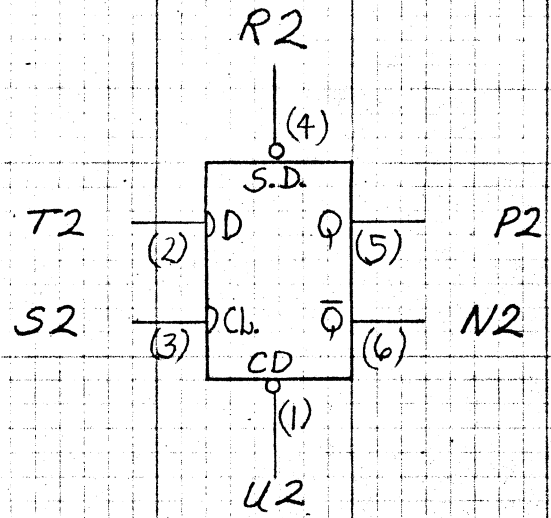
Input: PRESET or DATA - 1 unit load
CLOCK or CLEAR - 2 unit loads

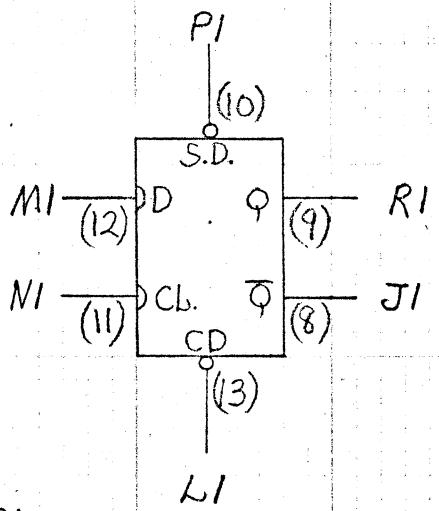
Output: Q and $\bar{Q}$ - 10 unit loads

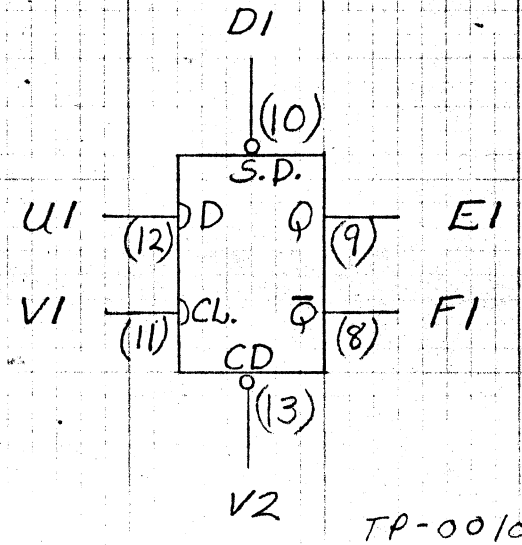
Power: +5 V @ 60 mA

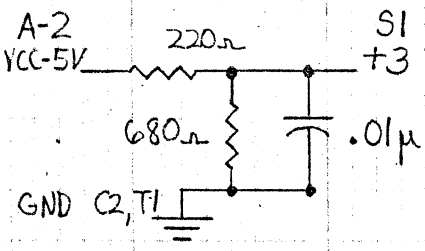
Format: A











I.C. 15 74 74

NOTE: CONNECT PIN 7 TO 8 ON I.C.s.

TP-0010D-E0

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010-3 4 D-TYPE FLIP FLOPS		
	DESIGNED S. FAJOUN	APPROVED S. Fajoun	SHEET 1 OF 1
	DRAWN GARI	DATE 3-24-71	DWG. NO. 114-000010-003

TP010-4 DUAL ONE-SHOT

The TP010-4 consists of two identical retriggerable one-shots. These one-shots feature DC and AC triggering, a clear input, and complimentary outputs.

The one-shots are capable of generating outputs from 40 ns to 10 ms.

TRUTH TABLE

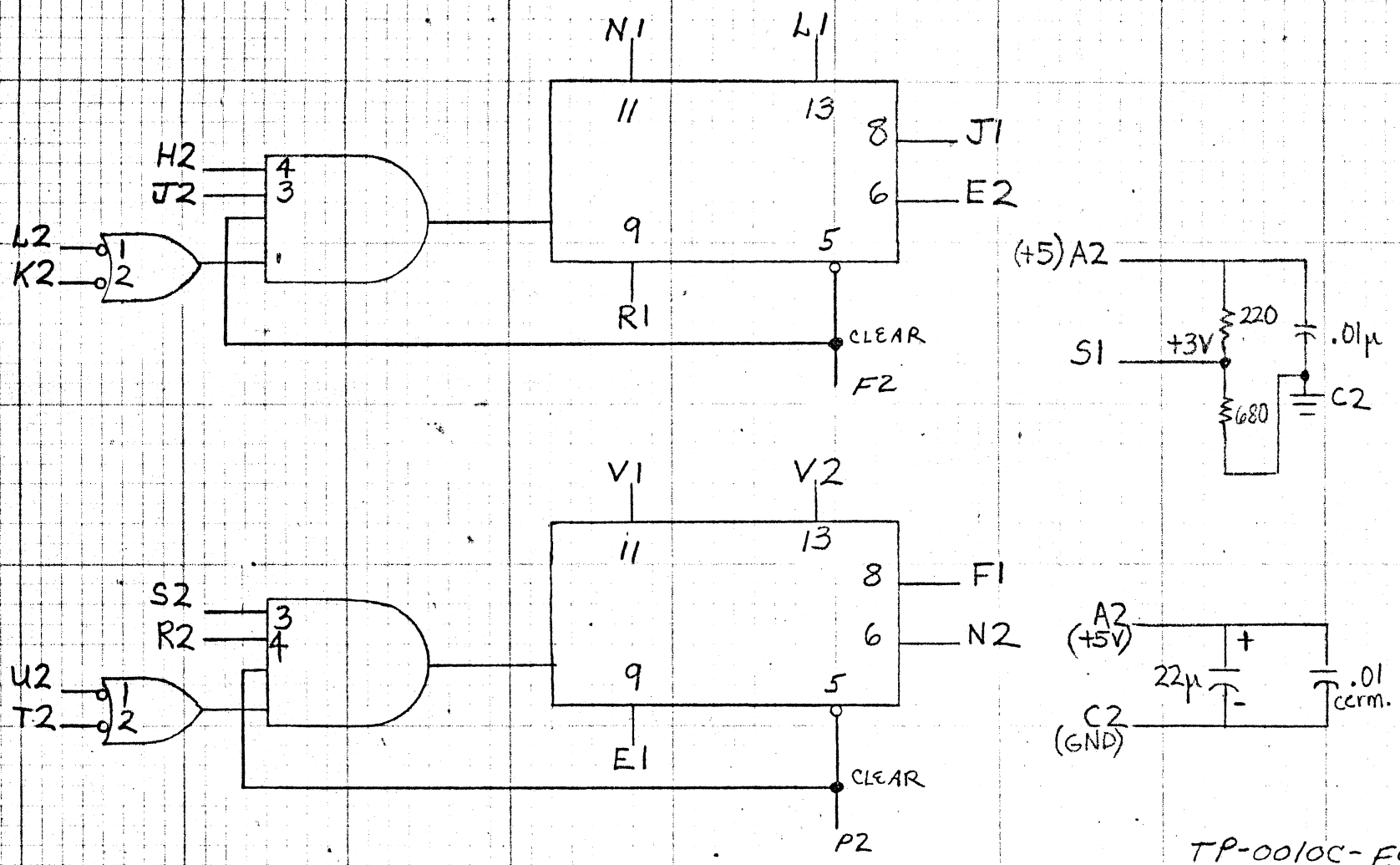
INPUT				OUTPUT	
L2/U2	K2/T2	H2/S2	J2/R2	J1/F1	E2/N2
H	H	-	-	L	H
-	-	L	-	L	H
-	-	-	L	L	H
L	-	H	H	L	H
L	-		H		
L	-	H			
H		H	H		
		H	H		
	H	H	H		

INPUTS: Each input is one TTL unit load.

OUTPUT: Each output can drive 10 TTL unit loads.

POWER: +5 V @ 112 ma

CARD FORMAT: A



TP-0010C-E0

IC: 74122

VCC ON PIN 14 IS +5 VOLTS FROM A2
GROUND ON PIN 7 FROM C2 AND T1

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010-4 TWO ONE SHOTS		
	DESIGNED: S. FARJOUN	APPROVED: S Farjoun	SHEET 1 OF 1
	DRAWN: GARI	DATE: 5-4-71	DWG. NO.: 114-00010-004

TP-010-5 2 Dual 4-Bit Multiplexer

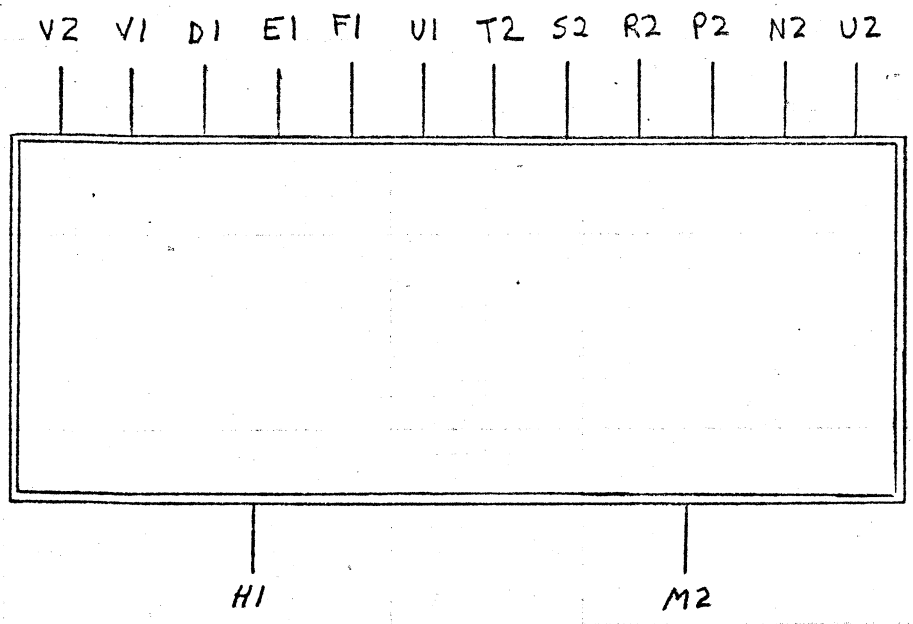
Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-ship, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

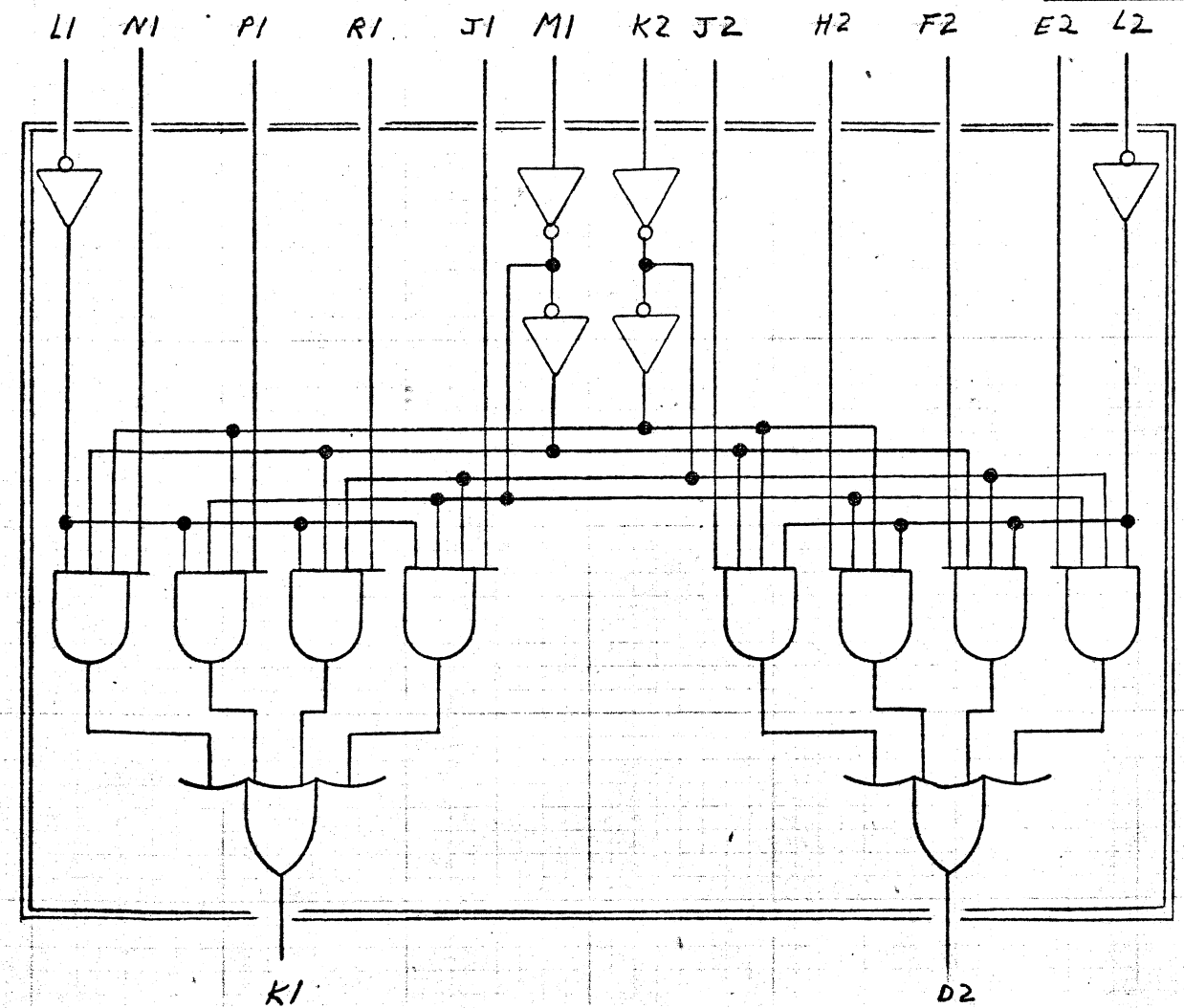
Input: All inputs 1 unit load.

Output: 10 unit loads

Power: 5 V@ 160 mA

Format: A





TENNECOMP SYSTEMS, INC.	TP-010-5 2-DUAL 4 BIT MULTIPLEXERS	DESIGNED	APPROVED	SHEET 1 OF 1
REVISIONS		DRAWN WJ+AD	DATE 2-18-72	DWG. NO. 1144-000010-305

TP-010-6 Dual 4-Bit Presettable Decade Counter

The 8290 Decade Counter provides a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The counter has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. The unit is provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

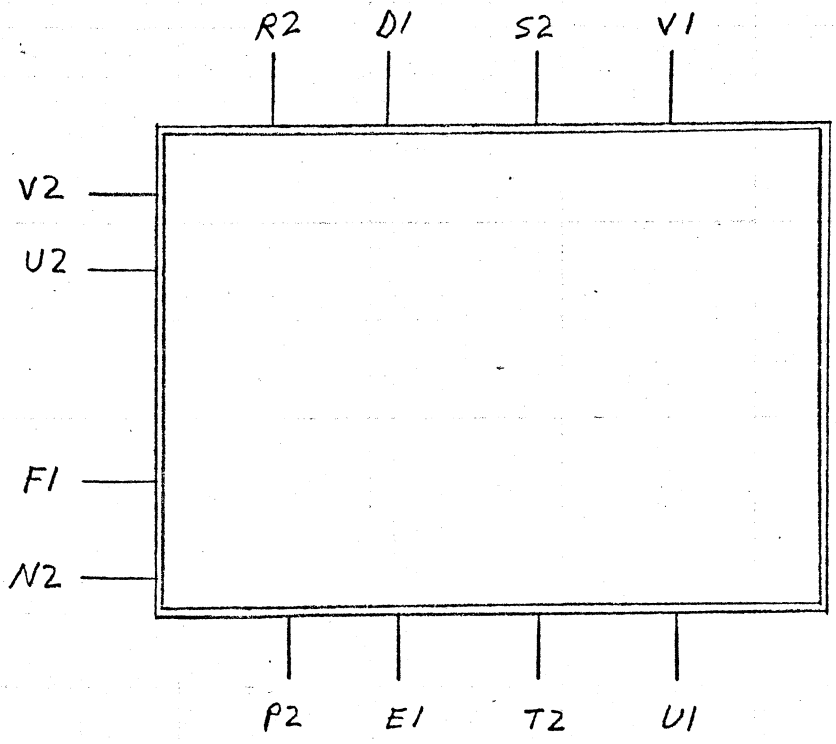
The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

Inputs: Clocks - 3 unit loads
Data Inputs - 1 unit load
Data Strobe - 1 unit load
Reset - 2 unit loads

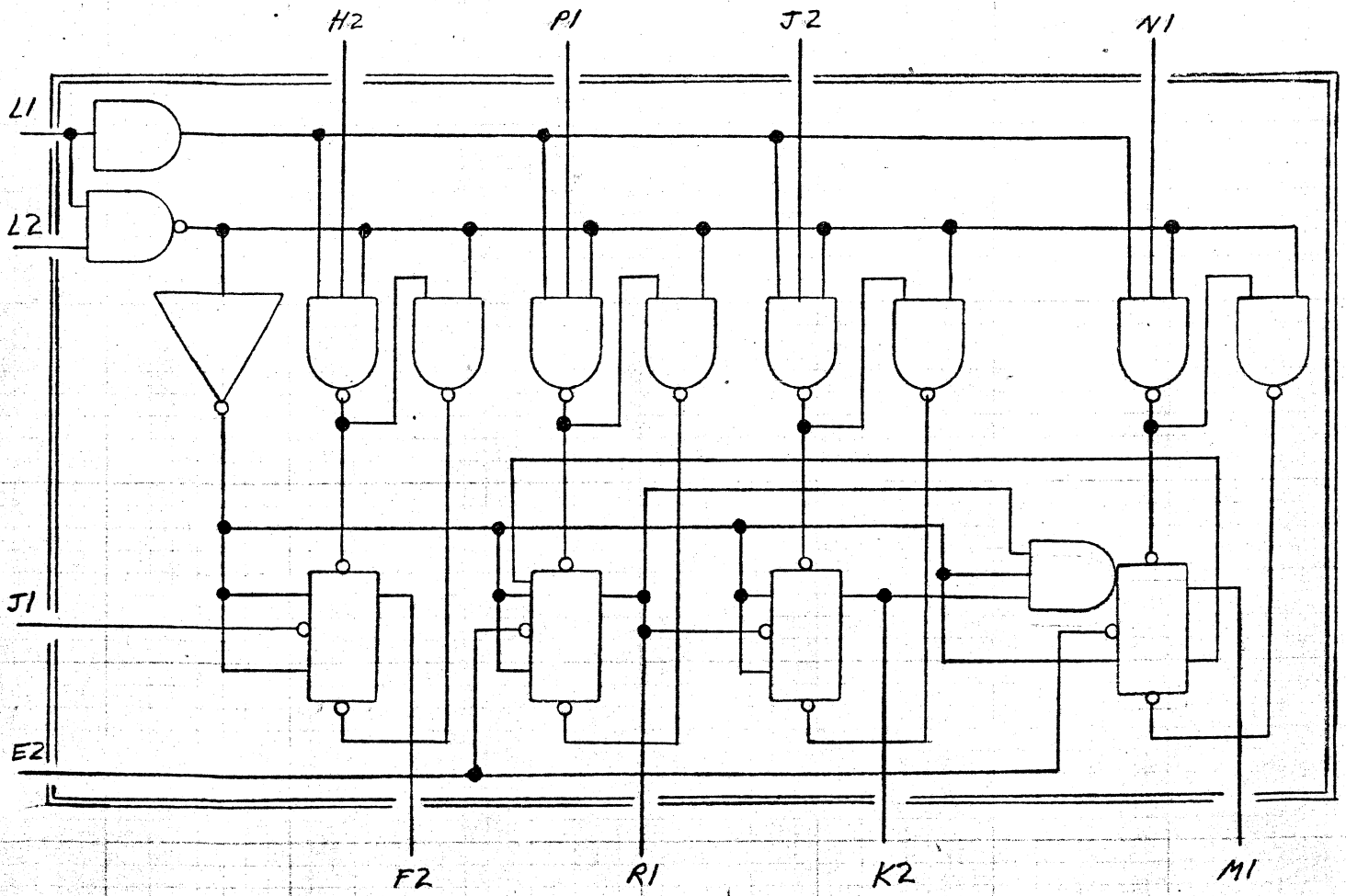
Outputs: Pins R1, K2, E1, T2 - 4 unit loads
Pins P2, U1, F2, M1 - 6 unit loads

Power: 5 V @ 100 mA

Format: A



REVISIONS	TENNECOMP SYSTEMS, INC.			
	TP-0100-6 DUAL 4 BIT PRESETTABLE DECADE COUNTER			
	DESIGNED	APPROVED	SHEET 1 OF 1	
	DRAWN	DATE 2-18-72	DWG. NO. 114-0030/0-006	



TP-010-7 Quad Schmitt Trigger

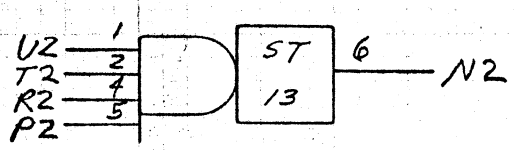
The TP-010-7 consists of two identical Schmitt triggers. Each Schmitt trigger has four inputs, which have different input thresholds for positive and negative going signals. The threshold difference is approximately 800 mv.

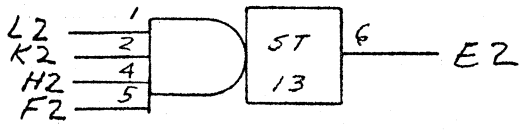
Inputs: Each input presents 1 TTL unit load.

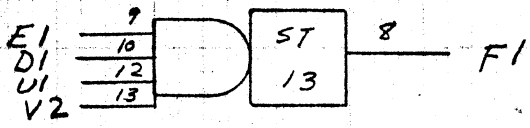
Output: Each output is capable of driving 10 TTL unit loads. The output is the inverse of the input.

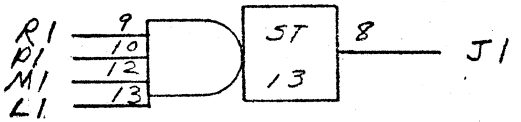
Power: +5 volts @ 64 mA max.

Card Format: A









I.C. 15 SN7413

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010-7 SCHMITT TRIGGERS		
	DESIGNED	APPROVED	SHEET / OF /
	DRAWN W. J.	DATE 2-18-72	DWG. NO. 11-1-000010-00

TP-010-8 1 of 8 Decoder

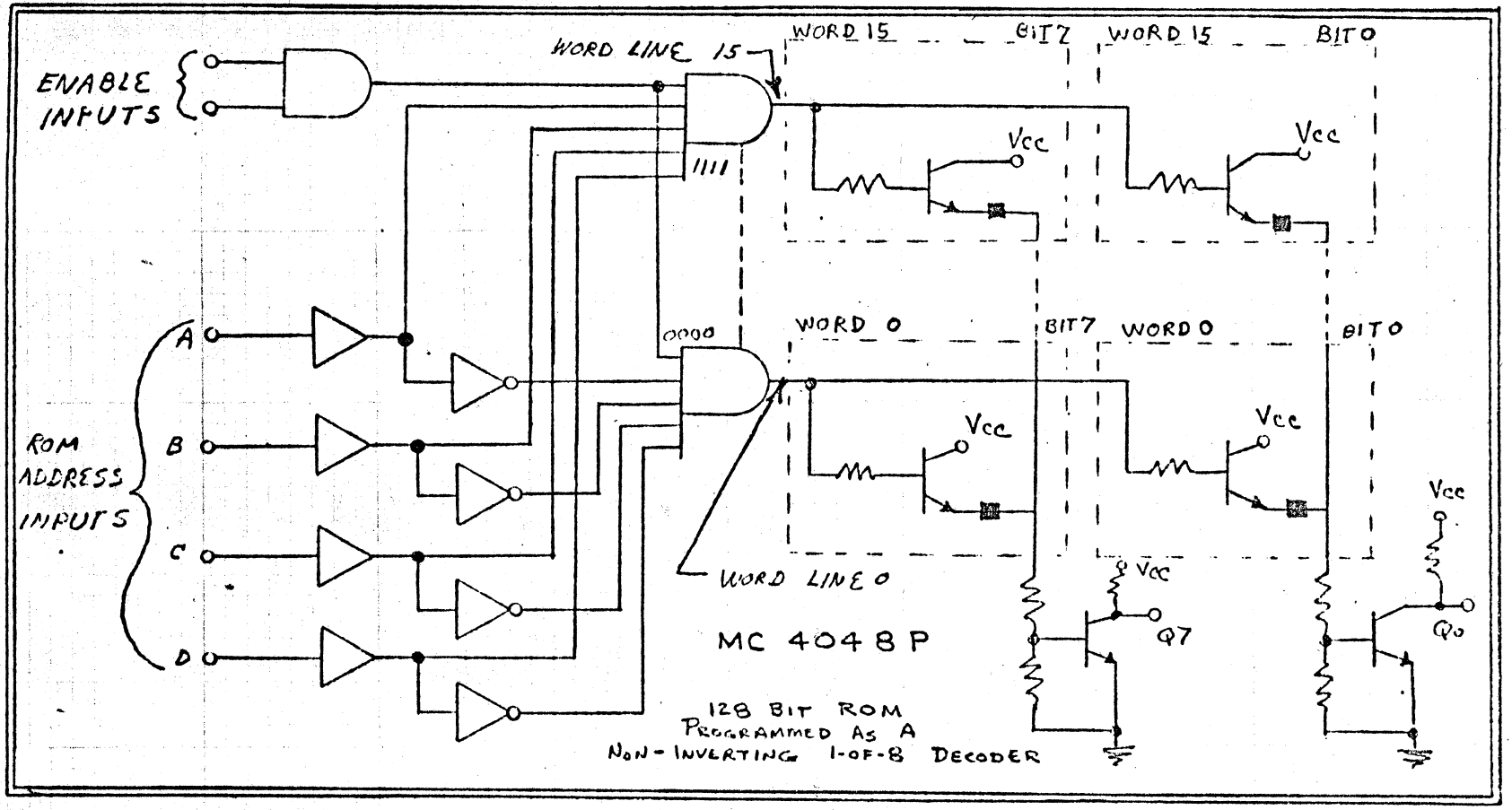
This card contains two standard formatted ROM coded to produce non-inverting one of eight.

Inputs: 1 unit load

Outputs: 10 unit loads

Power: 5 V @ 100 mA

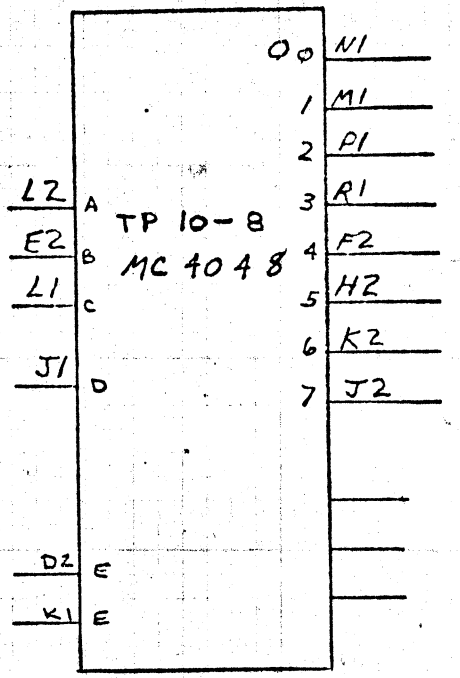
Format: A

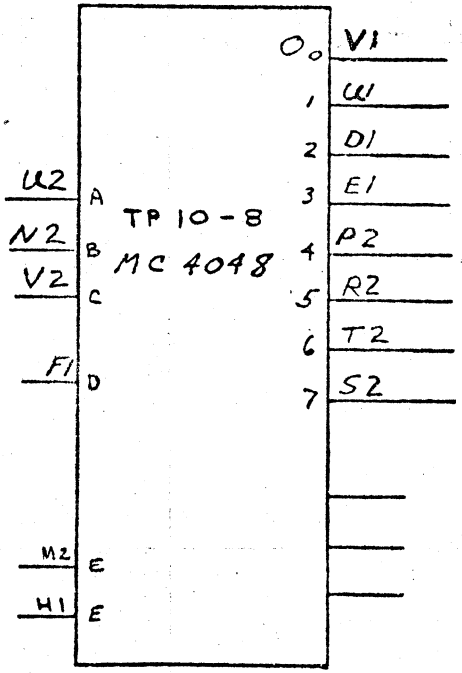


INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

MC 4048 P
TRUTH TABLE
(+ LOGIC)

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP010-8 1 OF 8 DECODER		
	DESIGNED AD-R	APPROVED	SHEET 1 OF 2
	DRAWN WS	DATE 3-17-72	DWG. NO. 114-000010-008

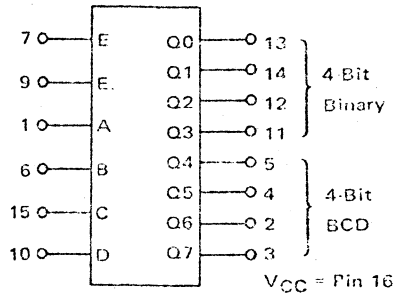




REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010 – 8 1 OF 8 DECODER		
	DESIGNED A D-R	APPROVED	SHEET 2 OF 2
	DRAWN W S	DATE 3-17-72	DWG. NO. 111-000010-009

DECODERS

MC4001
BCD-to-Binary/Binary-to-BCD Number Converter



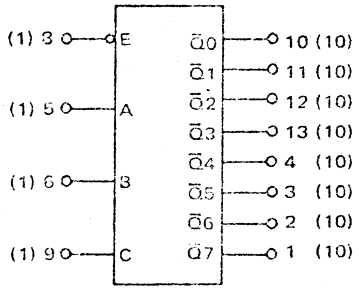
V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
				Binary to BCD				BCD to Binary			
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0	1	1	1	0
1	1	1	1	0	1	0	0	0	0	0	0

P_D = 300 mW typ/pkg

MC4006/MC4306
Binary to 1-of-8 Line Decoder

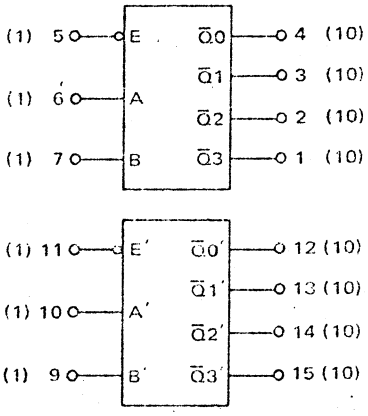


V_{CC} = Pin 14
Gnd = Pin 7

INPUT			OUTPUT							
C	B	A	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

t_{pd} = 14 ns typ
P_D = 100 mW typ/pkg

MC4007
Dual Binary to 1-of-4 Line Decoder



INPUT		OUTPUT			
B	A	3	2	1	0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

V_{CC} = Pin 16
Gnd = Pin 8

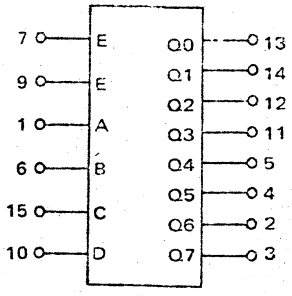
t_{pd} = 14 ns typ
P_D = 125 mW typ/pkg

MC4038
Inverting/Non-Inverting 1-of-8 Decoder

MC4040
Binary to 2-of-8 Decoder

MC4041
Single-Error Hamming Code Detector and Generator

MC4048
Non-Inverting 1-of-8 Decoder



V_{CC} = Pin 16
Gnd = Pin 8

ALL TYPES INPUT				MC4038 OUTPUT								MC4040 OUTPUT								MC4041 OUTPUT								MC4048 OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
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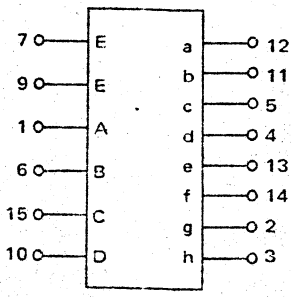
0	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	1	0	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

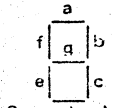
P_D = 240 mW typ/pkg — MC4038, MC4041, MC4048
= 200 mW typ/pkg — MC4040

MC4039
7-Segment Character Generator



V_{CC} = Pin 16
Gnd = Pin 8

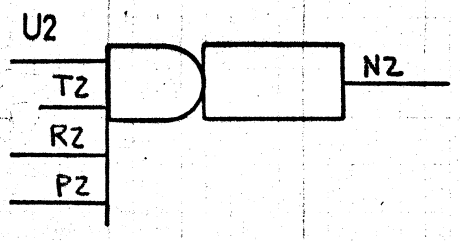
SEGMENT IDENTIFICATION

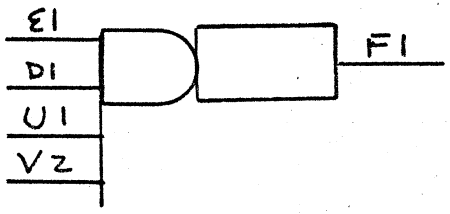


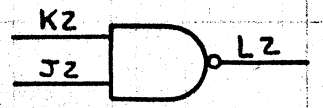
P_D = 240 mW typ/pkg

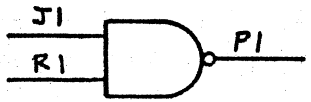
DIGIT	SEGMENTS ILLUMINATED	INPUT 3	2	1	0	OUTPUT a	b	c	d	e	f	g	h
0	a,b,c,d,e,f	0	0	0	0	0	0	0	0	0	0	1	1
1	b,c	0	0	0	1	1	0	0	1	1	1	1	1
2	a,b,d,e,g	0	0	1	0	0	0	1	0	0	1	0	1
3	a,b,c,d,g	0	0	1	1	0	0	0	0	1	1	0	1
4	b,c,f,g	0	1	0	0	1	0	0	1	1	0	0	1
5	a,c,d,f,g	0	1	0	1	0	1	0	0	1	0	0	1
6	c,d,e,f,g	0	1	1	0	1	1	0	0	0	0	0	1
7	a,b,c	0	1	1	1	0	0	0	1	1	1	1	1
8	a,b,c,d,e,f,g	1	0	0	0	0	0	0	0	0	0	0	1
9	a,b,c,f,g	1	0	0	1	0	0	0	1	1	0	0	1
NONE		1	0	1	0	1	1	1	1	1	1	1	1
0	h (Ext.)	1	0	1	1	1	1	1	1	1	1	1	0
NONE	g	1	1	0	0	1	1	1	1	1	1	0	1
NONE		1	1	0	1	1	1	1	1	1	1	1	1
NONE		1	1	1	0	1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1	1	1	1	1

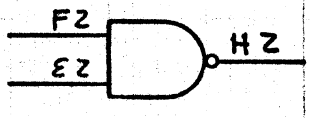
(continued)

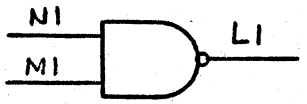












REVISIONS	TENNECOMP SYSTEMS, INC.		
	MIXED LOGIC SCHMIDT TRIGGER AND OPEN COLLECTOR GATES		
	DESIGNED	APPROVED	SHEET OF
	DRAWN WRC	DATE 5/1/73	DWG. NO.

TP-010-10

Dual 4x4 Register File

The SN74170 MSI 16-bit TTL register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W, is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement - data entry addressing separate from data read addressing and individual sense line - eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

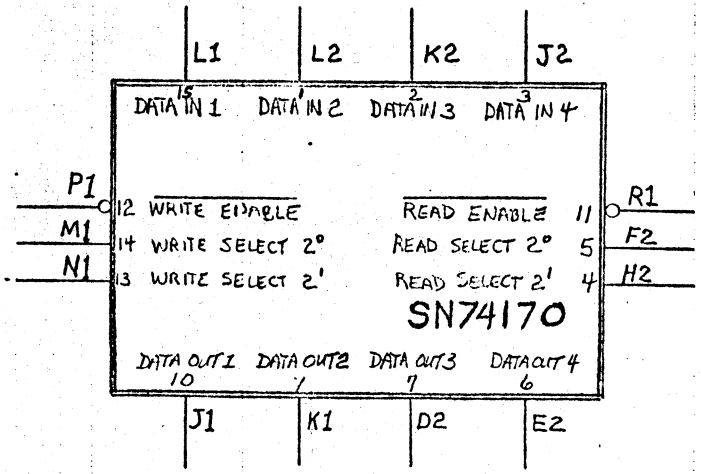
Power dissipation is typically 500 mW total or 5 mW per gate.

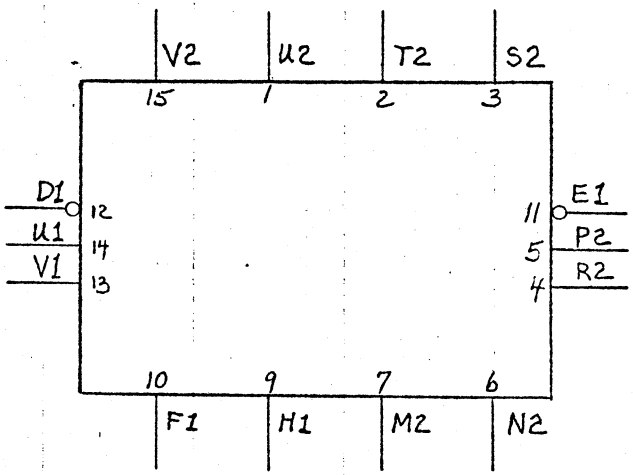
INPUT LOADING: 1 Unit Load Each

OUTPUT DRIVE: 10 Unit Loads

POWER: 220 mA at 5 VDC

FORMAT: A





TP 10-10

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-10 DUAL 4 X 4 REGISTER FILE		
	DESIGNED CF	APPROVED CF	SHEET 1 OF 1
	DRAWN CF	DATE 5/16/73	DWG. NO. [illegible]-000010-010

TP-010-11 Dual 4-Bit Register
TP-010-12 Dual 6-Bit Register

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the TP10-11 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

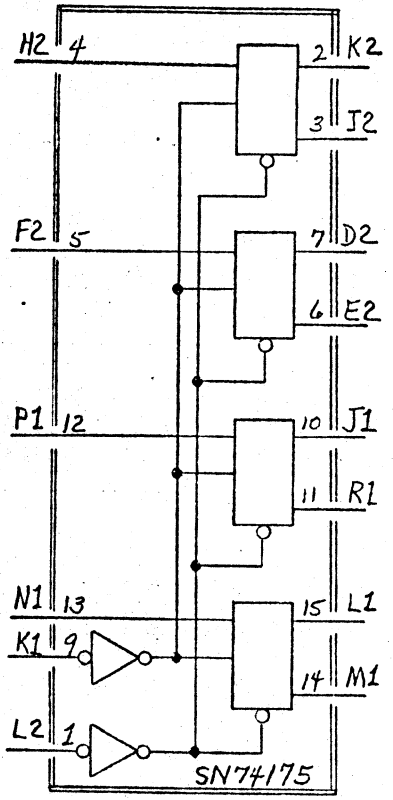
These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54/74 loads is available from each output at low logic levels, and to 20 loads at high logic levels to facilitate connection of unused inputs to used inputs. Maximum clock frequency is typically 35 megahertz, with a typical power dissipation of 38 milliwatts per flip-flop.

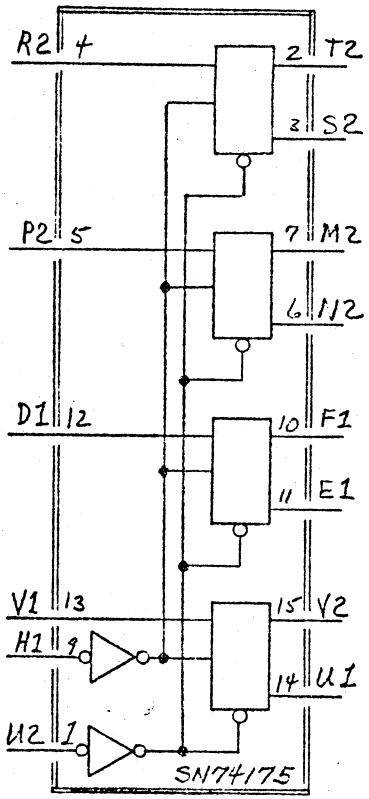
INPUT LOADING: 1 Unit Load

OUTPUT DRIVE: 10 Unit Loads

POWER: TP-10-11: 65 mA @ 5V
TP-10-12: 95 mA @ 5V

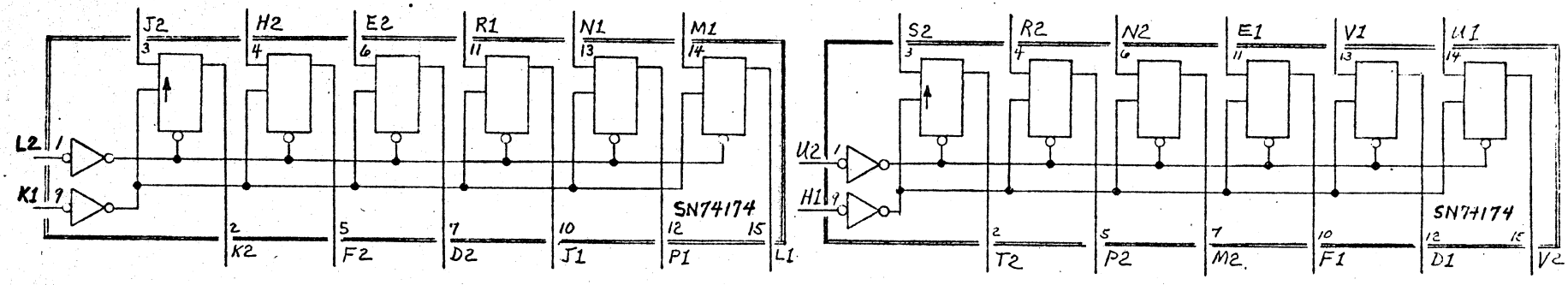
FORMAT: A





TP 10-11

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-11 DUAL 4 BIT REGISTER		
	DESIGNED CF	APPROVED CF	SHEET OF
	DRAWN CF	DATE 5/16/73	DWG. NO. 114-000010-011



TP 10-12

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-12 DUAL HEX REGISTER		
	DESIGNED CF	APPROVED CF	SHEET 1 OF 1
	DRAWN CF	DATE 5/16/73	DWG. NO. 114-000010-012

TP-010-13

4-Line to 10-Line Decoder (BCD)

The decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN7442 BCD-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. Full fan-out of 10 is available at all outputs.

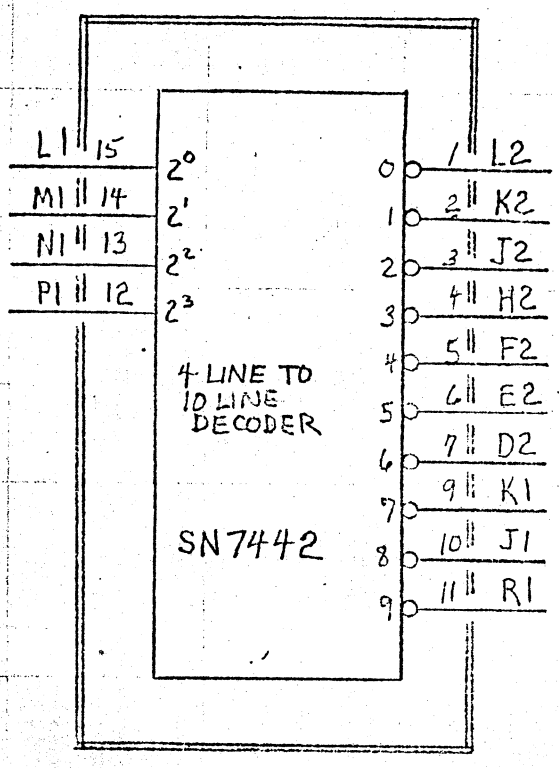
The TP-010-13 also contains 6 general purpose inverters.

INPUT LOADING: 1 Unit Load

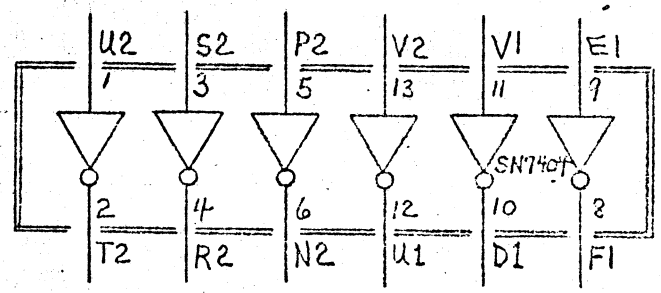
OUTPUT DRIVE: 10 Unit Loads

POWER: 50 mA @ 5V

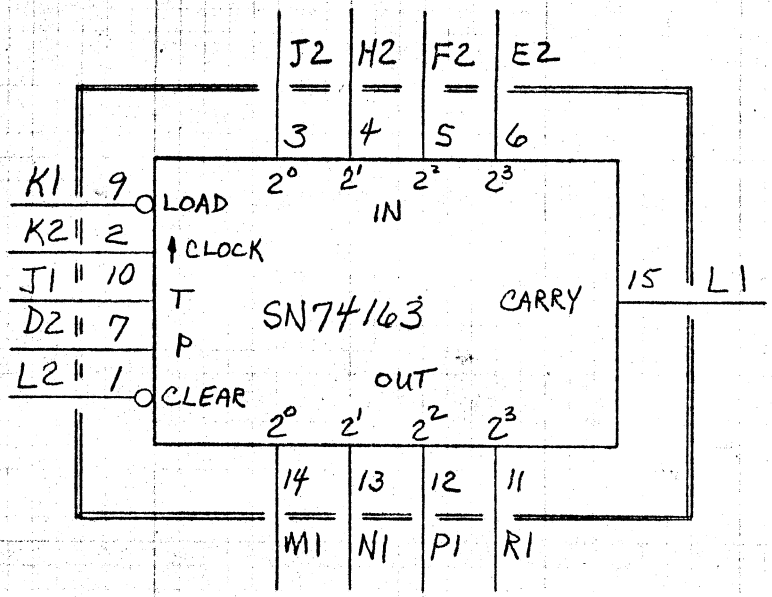
FORMAT: A

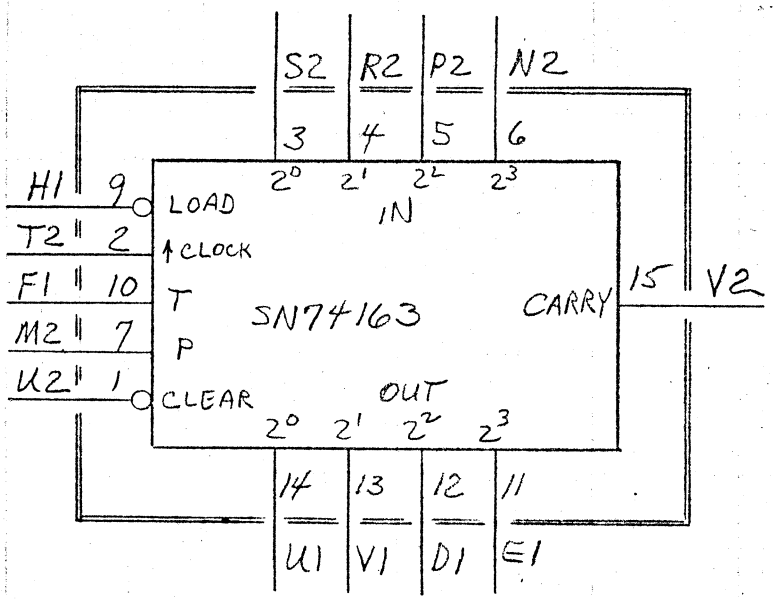


TP10-13

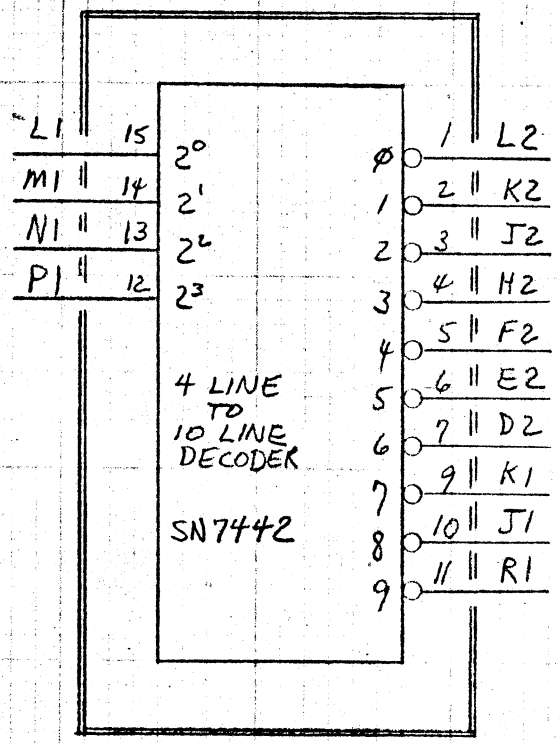


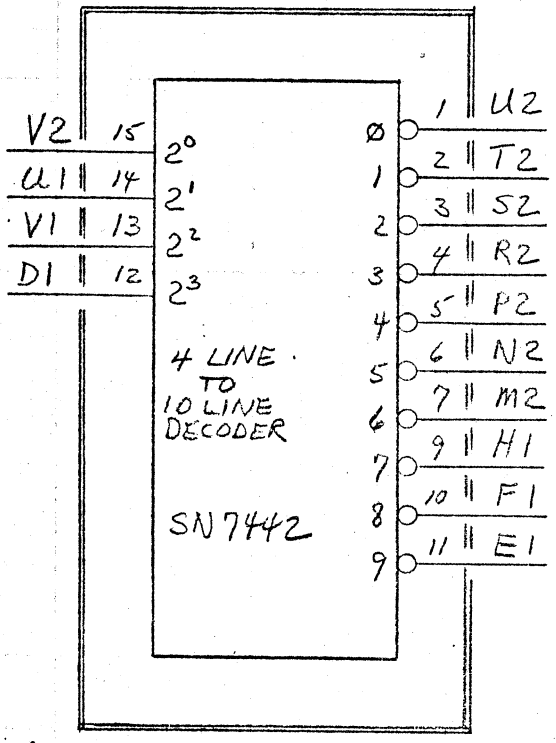
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-13 4 LINE TO 10 LINE DECODER		
	DESIGNED CF	APPROVED CF	SHEET 1 OF 1
	DRAWN CF	DATE 5/16/73	DWG. NO. 114-000010-013



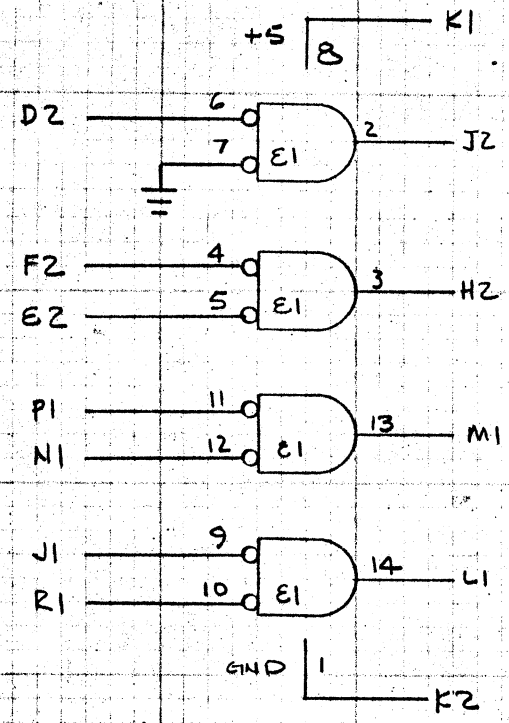


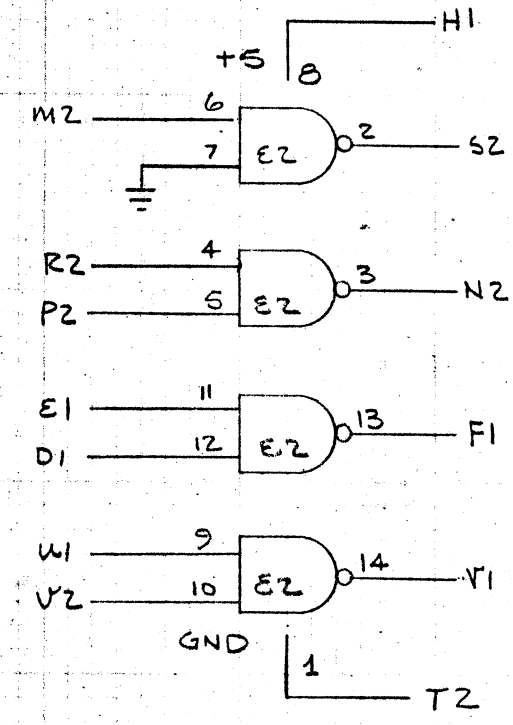
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-010-14 DUAL SYNCHRONOUS 4 BIT COUNTERS		
	DESIGNED CF	APPROVED	SHEET 1 OF 2
	DRAWN CF	DATE 6-6-73	DWG. NO. 114-000010-014

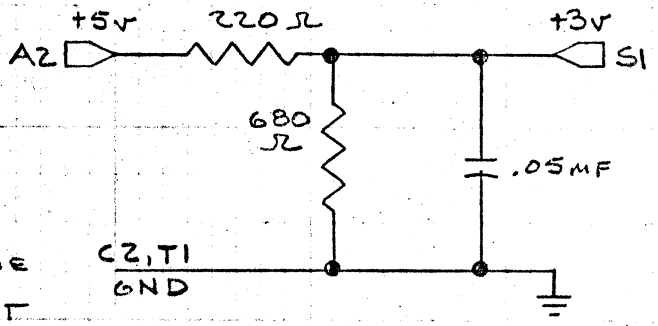


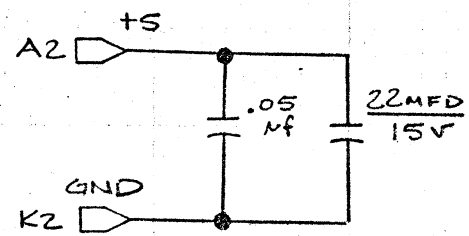


REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP 10-15 DUAL 4 LINE TO 10 LINE DECODERS		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN CF	DATE 6-6-73	DWG. NO. 114-000010-015





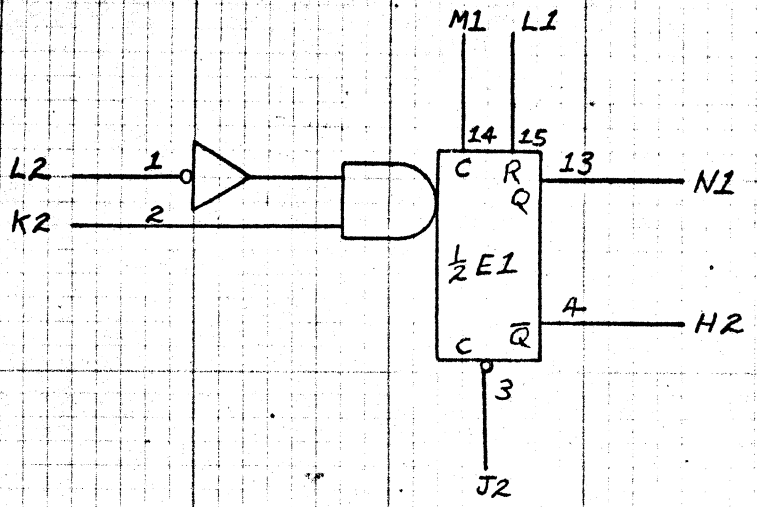


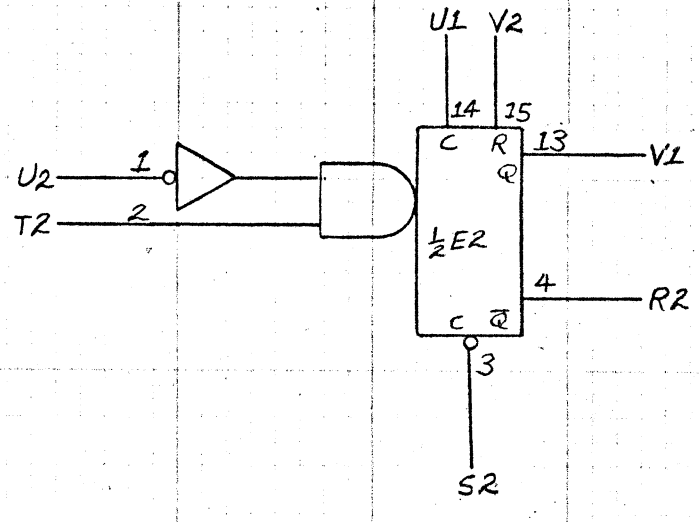


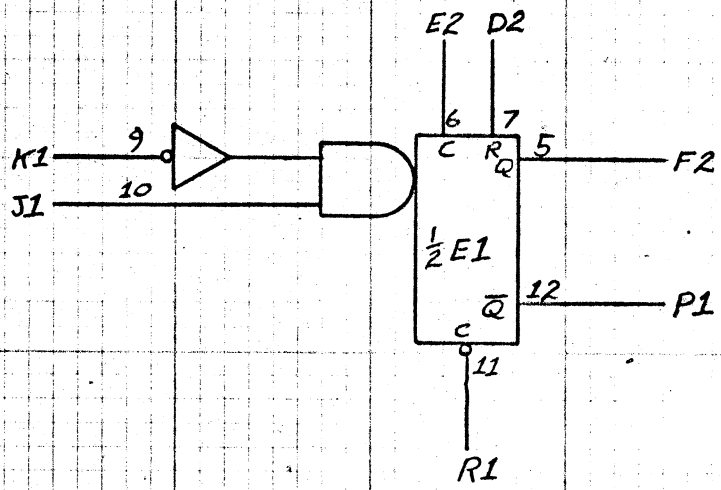
NOTES -

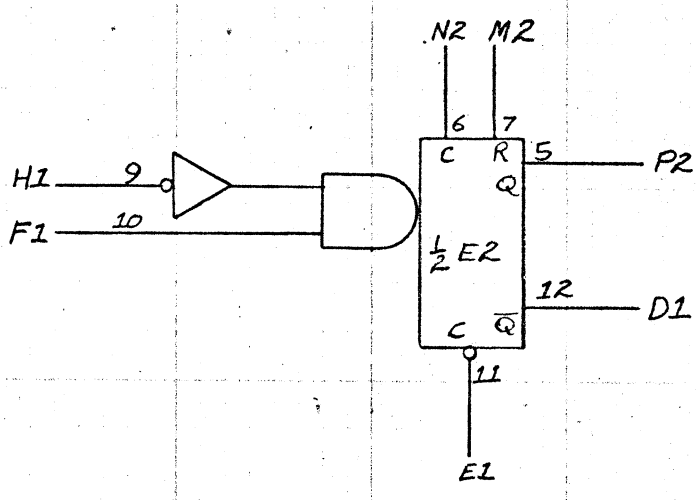
1. E1, E2 : SP-380
2. I.C.'s ARE SHIFTED ONE HOLE TO THE RIGHT DUE TO NON-STANDARD PINOUT OF SP-380. SEPERATE PINS MUST BE USED TO SUPPLY IC POWER & GROUND.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-16 8 BUS EXPANDER (4 X 1 NOR, 2 X 1 NOR) CRIMINEY BUS		
	DESIGNED ADR.	APPROVED	SHEET OF
	DRAWN	DATE 9/12/78	DWG. NO.



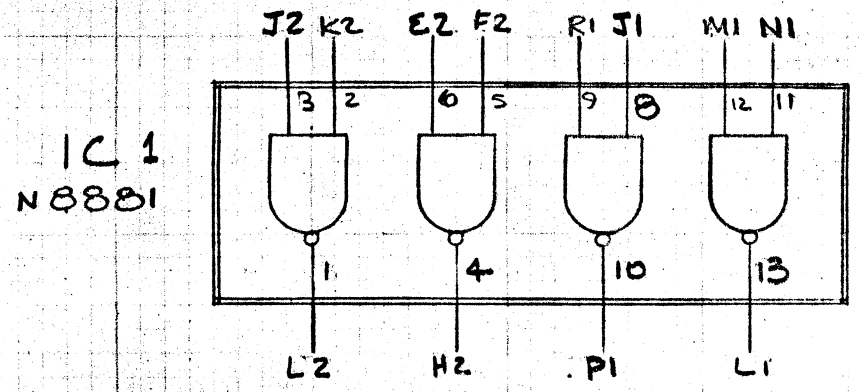


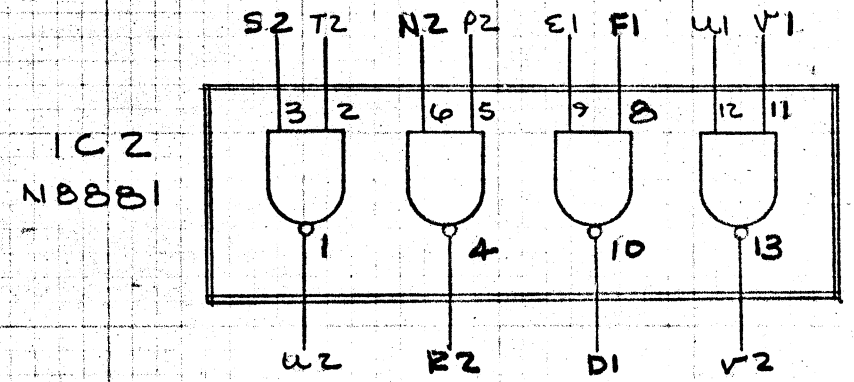


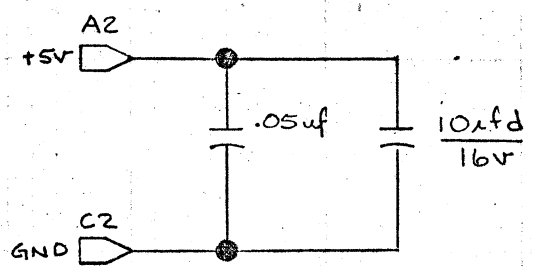


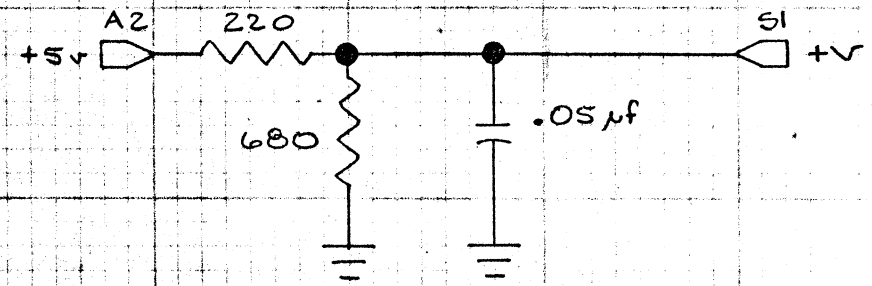
SN74123

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP10-17 UNIVERSAL CARD QUAD SINGLE SHOTS CRIMNEY BUS		
	DESIGNED AP	APPROVED W. Ward	SHEET / OF /
	DRAWN AP	DATE 4/19/73	DWG. NO.

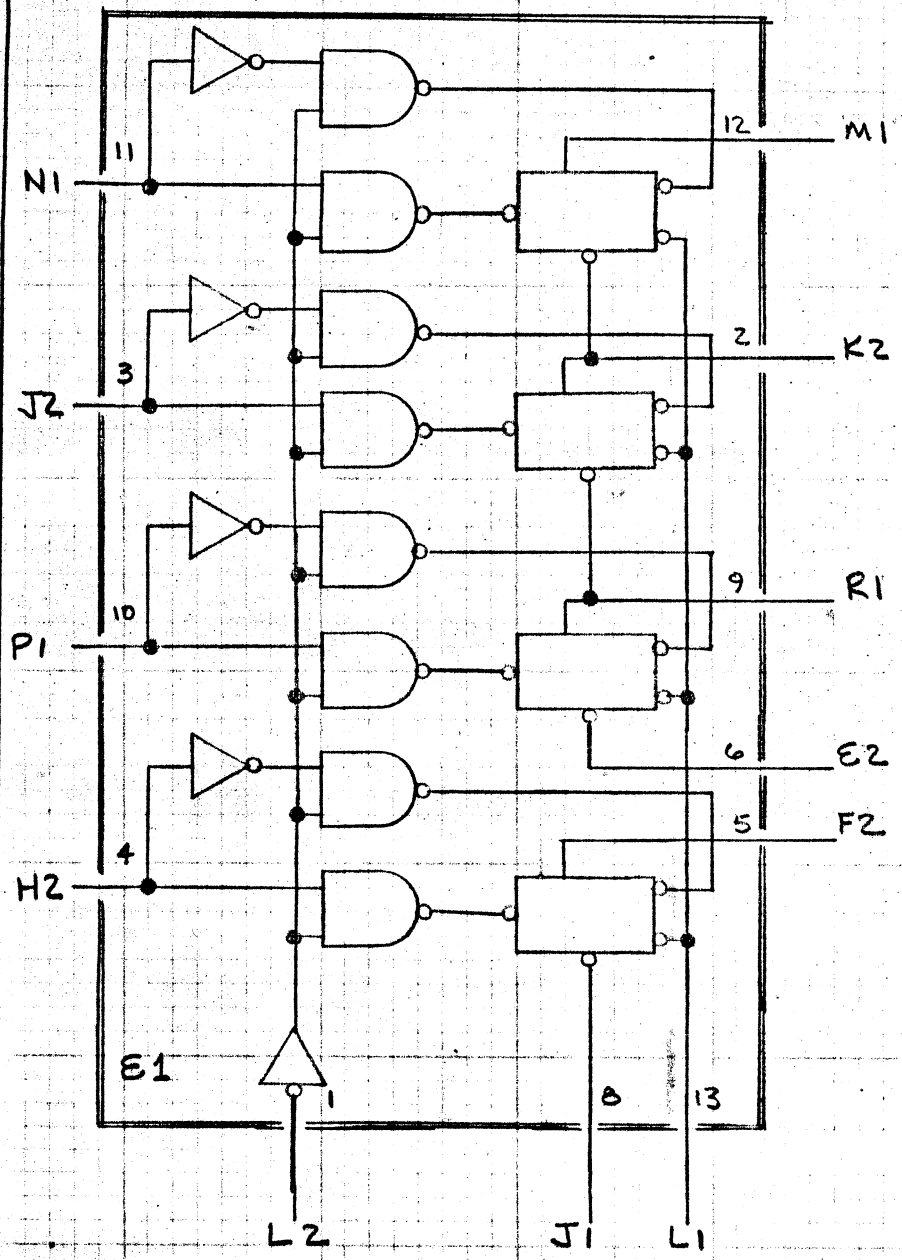


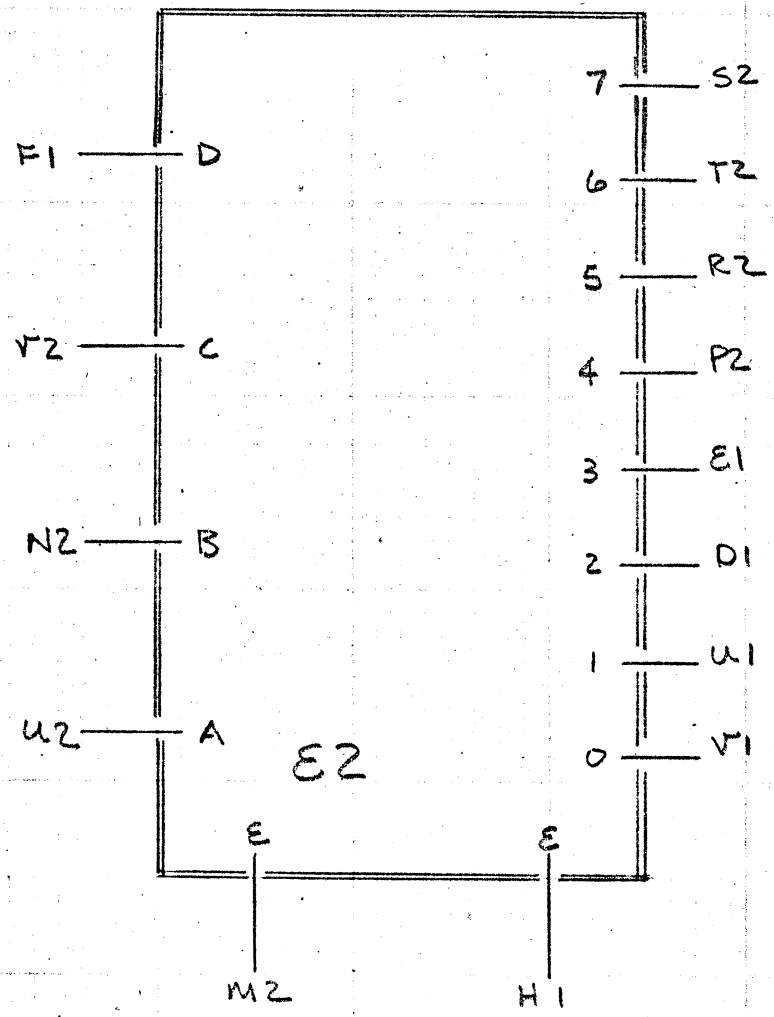






REVISIONS	TENNECOMP SYSTEMS, INC.
A - Corrected Pin Out 7/27/73 RJS	TP010-1B 8 NAND UNIBUS O.C. DRIVERS
	DESIGNED APE / APPROVED / SHEET 1 OF 1
	DRAWN R. Scott / DATE 9-6-73 / DWG. NO.





E1 - 8290

E2 - MC4048P (FOR DETAILED DESC.. OF THIS I.C. SEE TP010-8.)

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP 010-19 COUNTER & 1 OF 8 DECODER		
	DESIGNED	APPROVED W Hurd	SHEET 1 OF 1
	DRAWN R. Scott	DATE 9-14-73	DWG. NO.

TP-011

Ten Out of Thirteen Multiplexer

This module is a multiplexer scaler which accepts 13 inputs and has 10 outputs. The ten outputs are selected according to a 2-bit selection code at R1 and U1. STROBE input when high enables the multiplexer. When STROBE is in the "0" level state, all outputs are in the "0" state irrespective of the inputs. The ten least significant bits of the inputs will be transferred to the output when BIT SEL B,A are on "1","1" states, respectively, and the ten high significant inputs will be transferred to the outputs when BIT SEL B,A is in "0","0" level. (See the truth table).

Data propagation delay from input to output is typically 14 ns. Bit select delay is typically 22 ns, and the average input to output STROBE delay is 12 ns.

V1, S1 must be connected externally.

Inputs: R1, U1, V1, S1, J2, L2 present one unit load.

H2, P2 present two unit loads.

F2, R2 present 3 unit loads.

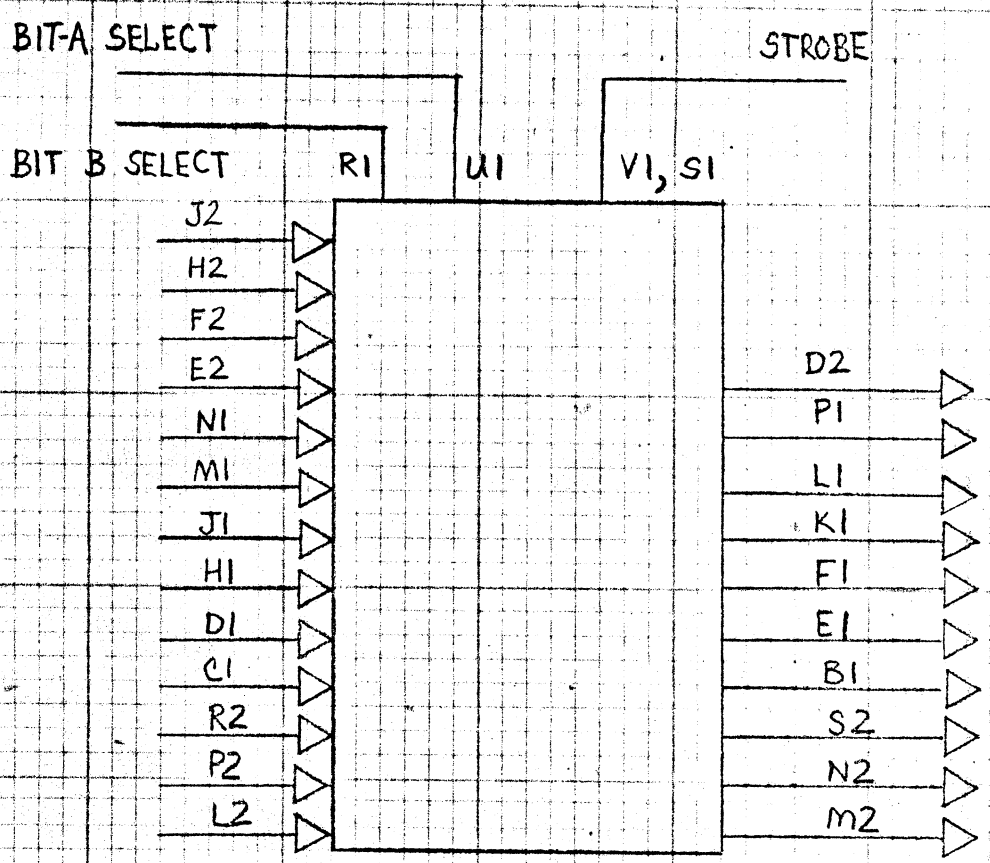
C1, D1, H1, J1, M1, N1, E2 present 4 unit loads each.

A1 - Unused input may serve as a source of +3 v., 40 unit loads.

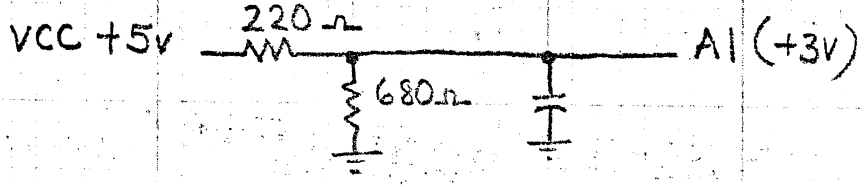
Outputs: 10 unit loads

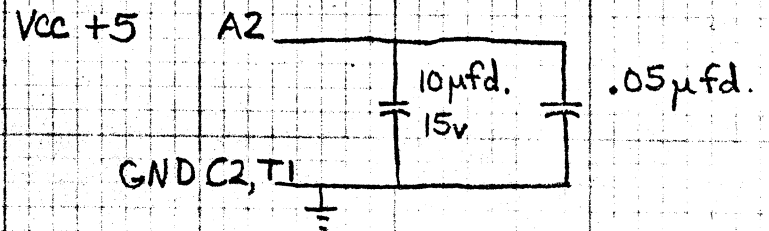
Power: 5 V @ 300 mA

Format: A

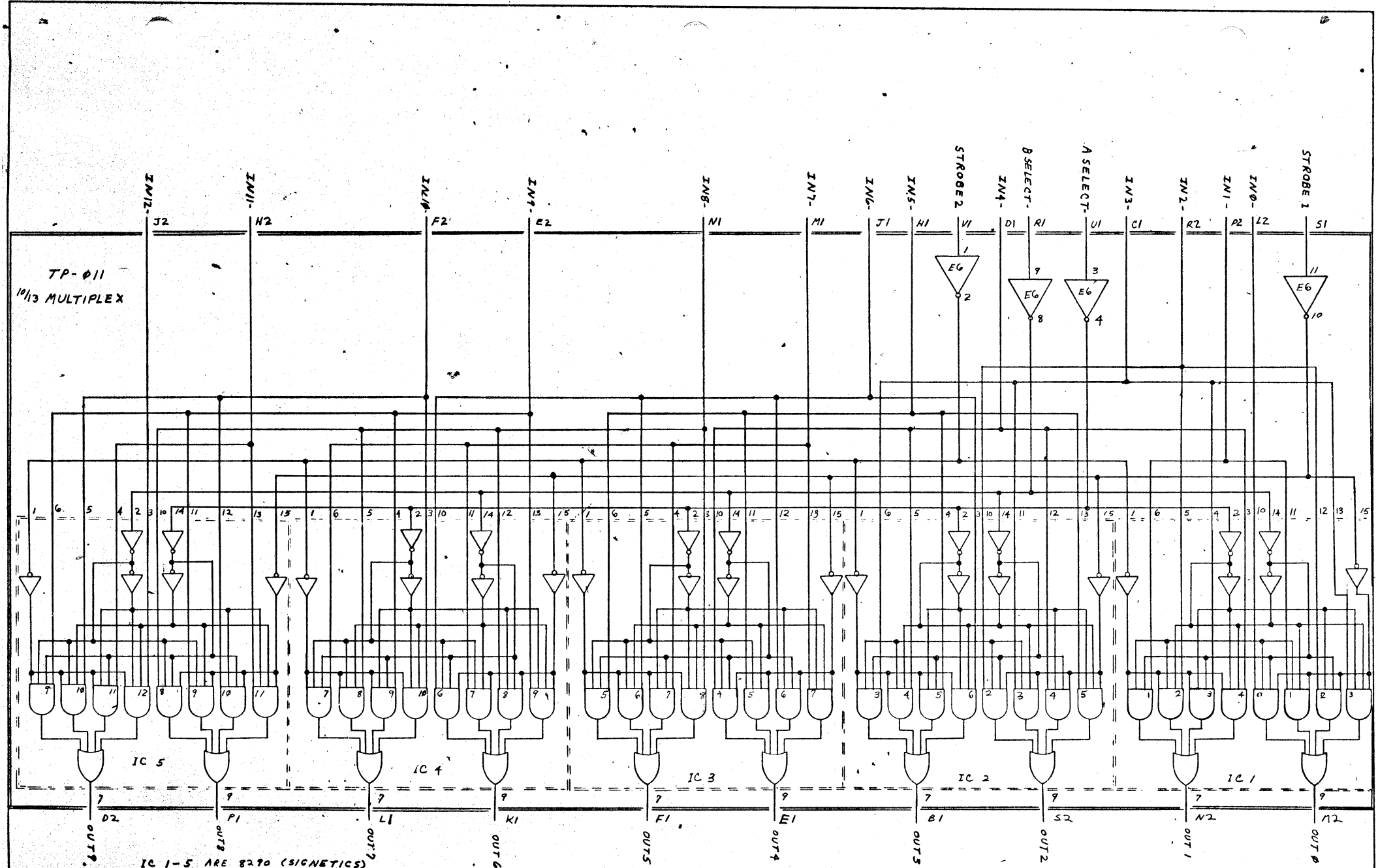


BIT SELECT "B, A"							
1	1	1	0	0	1	0	0
IN	OUT	IN	OUT	IN	OUT	IN	OUT
E2	D2	F2	D2	H2	D2	J2	D2
N1	P1	E2	P1	F2	P1	H2	P1
M1	L1	N1	L1	E2	L1	F2	L1
J1	K1	M1	K1	N1	K1	E2	K1
H1	F1	J1	F1	M1	F1	N1	F1
D1	E1	H1	E1	J1	E1	m1	E1
C1	B1	D1	B1	H1	B1	J1	B1
R2	S2	C1	S2	D1	S2	H1	S2
P2	N2	R2	N2	C1	N2	D1	N2
L2	M2	P2	M2	R2	M2	C1	M2





REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-011 TEN OUT OF THIRTEEN MULT.
	DESIGNED S. Ahlquist · APPROVED S. Ferguson · SHEET 1 OF 1
	DRAWN GARI · DATE 11-2-70 · DWG. NO. TP-011



IC 1-5 ARE 8290 (SIGNETICS)
IC 6 IS SN7404 (T.I.)

TP011- 10/13 MULTIPLEXOR

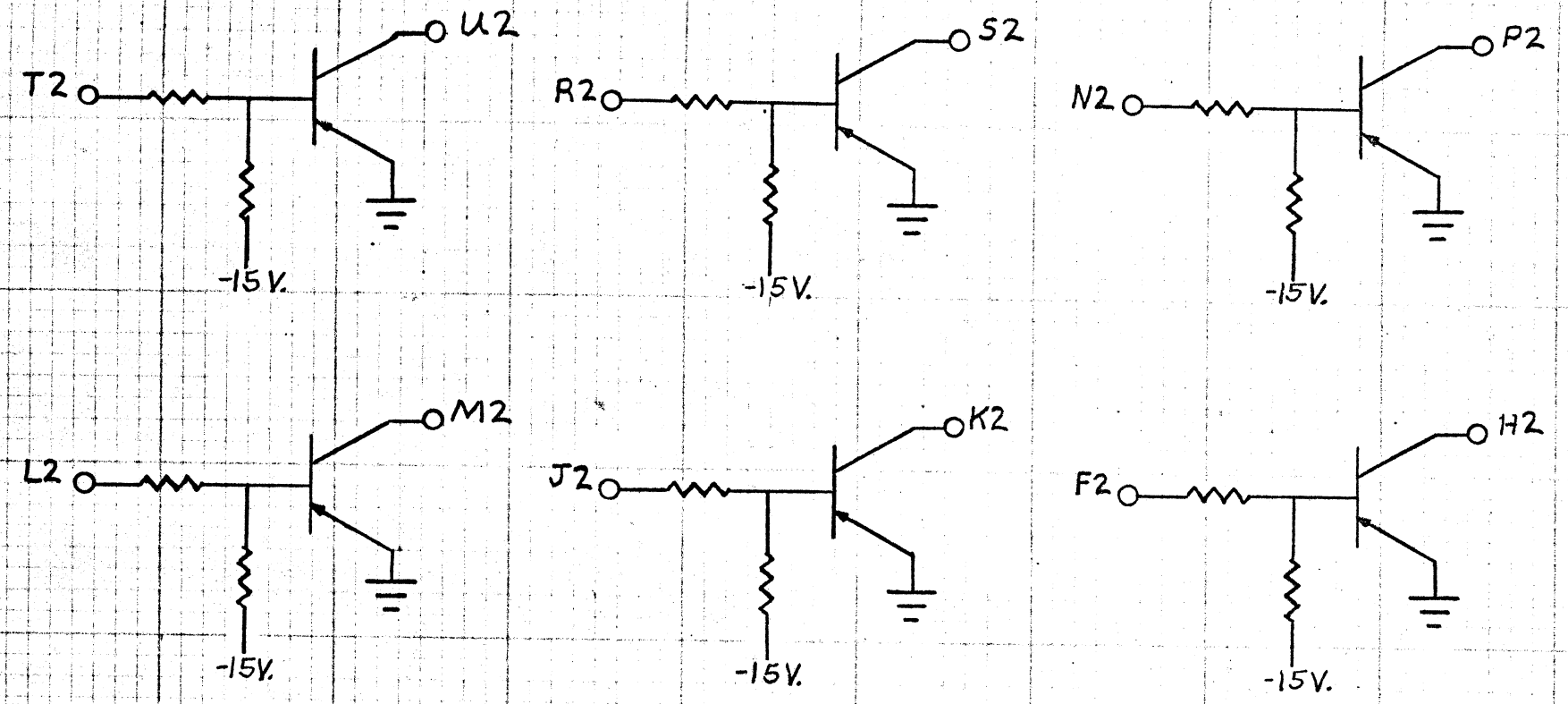
REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-011 - 10/13 MULTIPLEXOR CARD
	DESIGNED FF · APPROVED · SHEET / OF /
	DRAWN VJ · DATE 12-10-71 · DWG NO [illegible]

TP-012-1 TTL Input/Negative Driver

This card provides 7 circuits which convert standard positive logic TTL to negative logic. The outputs are open collector PNP transistors. Outputs are at ground with a +V input and open with a 0V input.

Inputs: 1 unit load

Outputs: Up to 100 mA



POWER
GND — C2 →
-15V. — B2 →

REVISIONS	TENNECOMP SYSTEMS, INC
	TTL INPUT 100 MA NEG. DRIVER TP-012
	DESIGNED: S. FARRAR / APPROVED: / SHEET 1 OF 1
	DRAWN: J.A.L. / DATE: 8-27-70 / DWG. NO. TP-0012A-EC

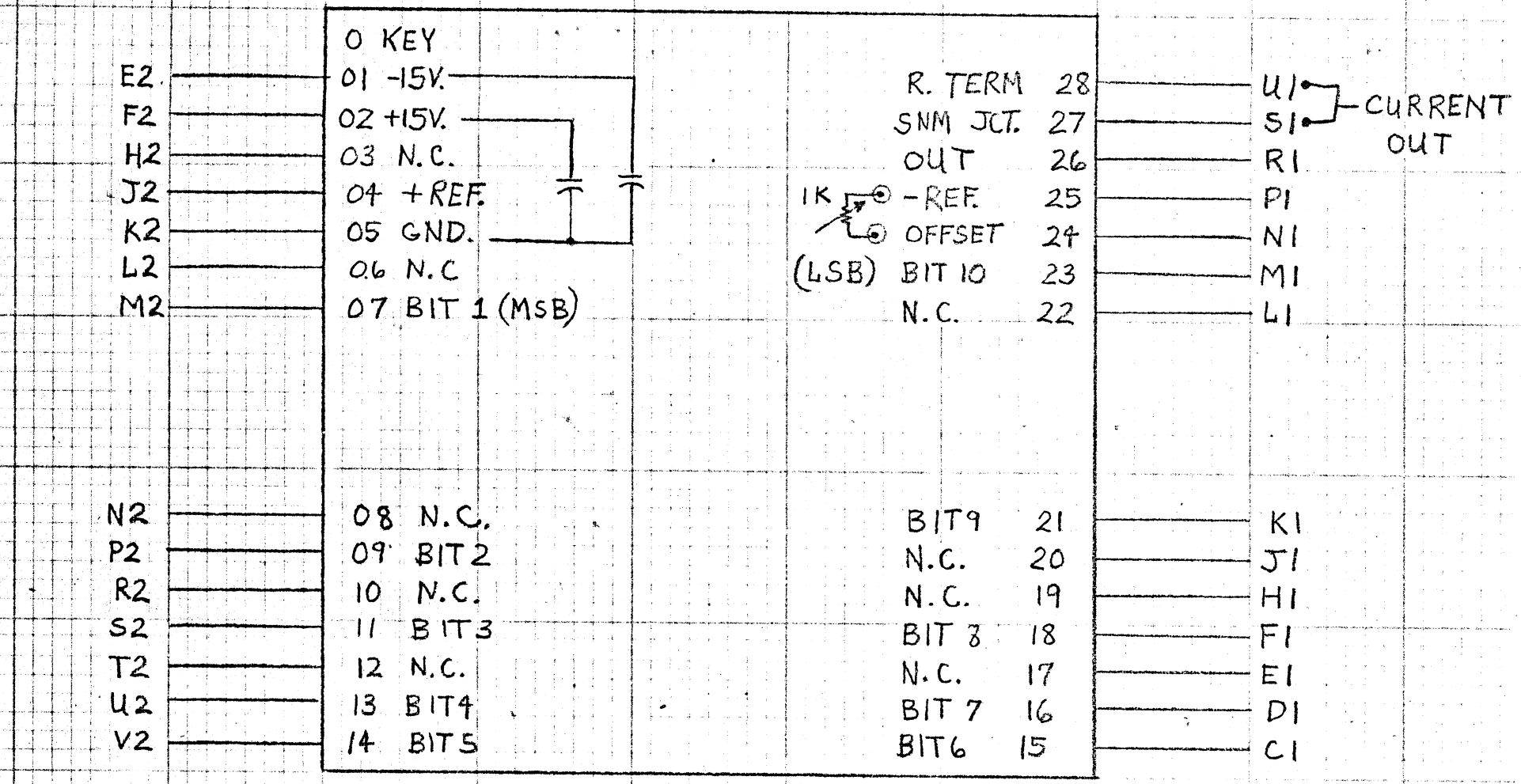
TP-015 DAC

The TP-015 card is a universal card for Digital to Analog converters. Below is a summary of specifications for all dash numbers. More detailed information is available on Analog Devices, Inc., data sheets for each of the DAC's.

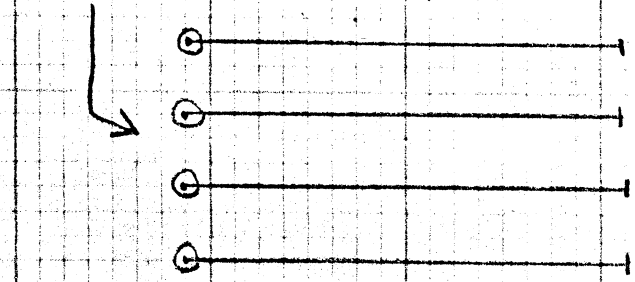
Dash Number	-1	-2	-3
DAC Part No.	MDA10H15	8484	MDA10Z110
Output Range	± 1 mA	0-2 mA	± 1 mA
Settling Time	300 ns	300 ns	300 ns
Resolution (Bits)	10	12	10

All DAC's require ±15 V. The 8484 is an Analog Devices modified DAC 12QZ.

ANALOG DEVICE'S MDA 10 H15

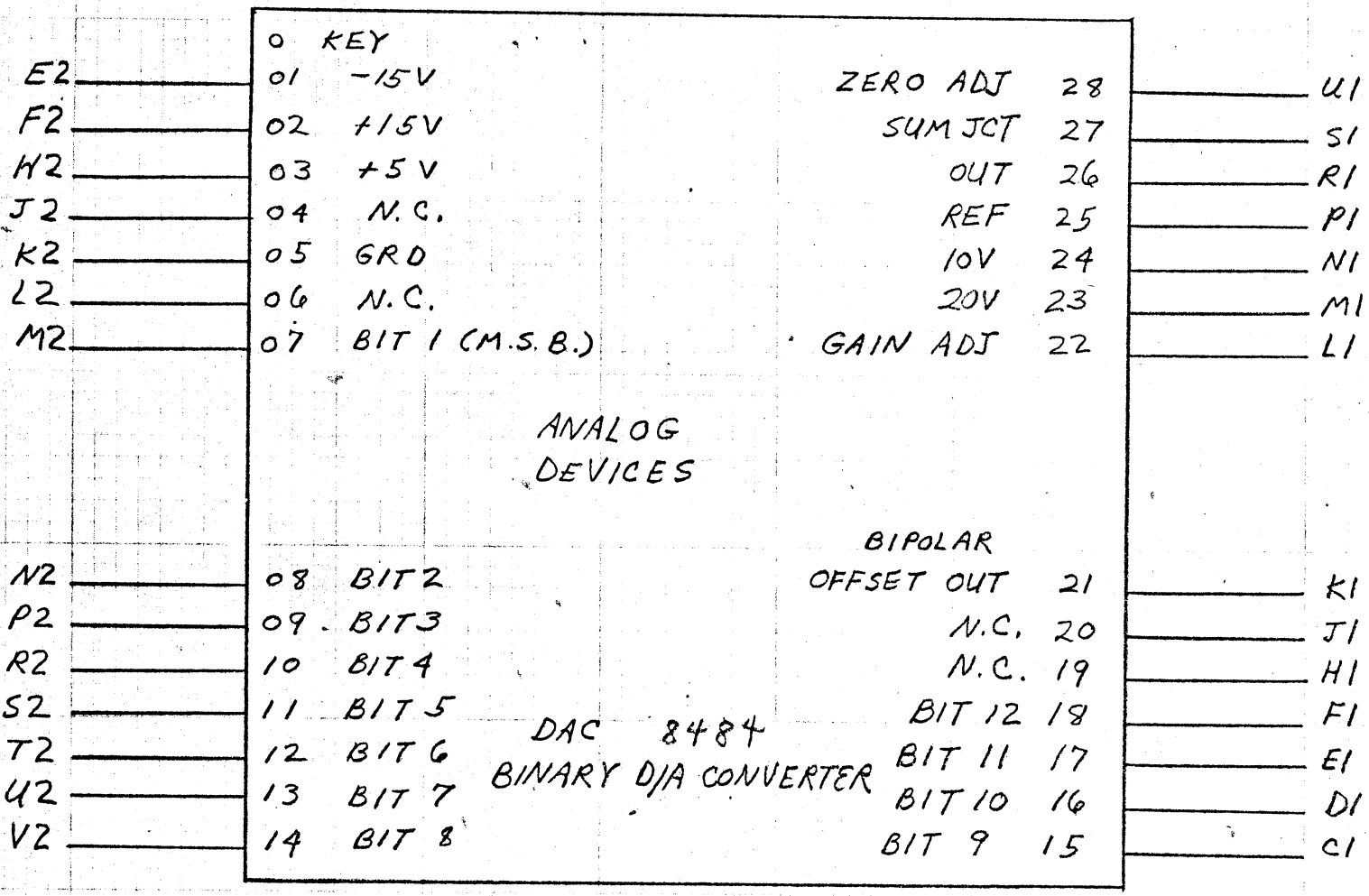


POINT ON P.C. FOR ADDITIONAL COMPONENTS

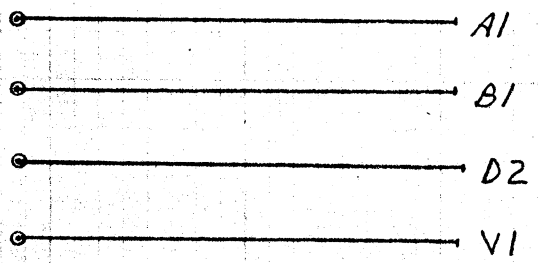


NOTE: C2 DIGITAL GND.

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-015-1 10 BIT D.A.C.
	DESIGNED: [illegible] APPROVED: S Fanfara SHEET 1 OF 1
	DRAWN: GARY DATE: 11-5-7 DWG. NO.

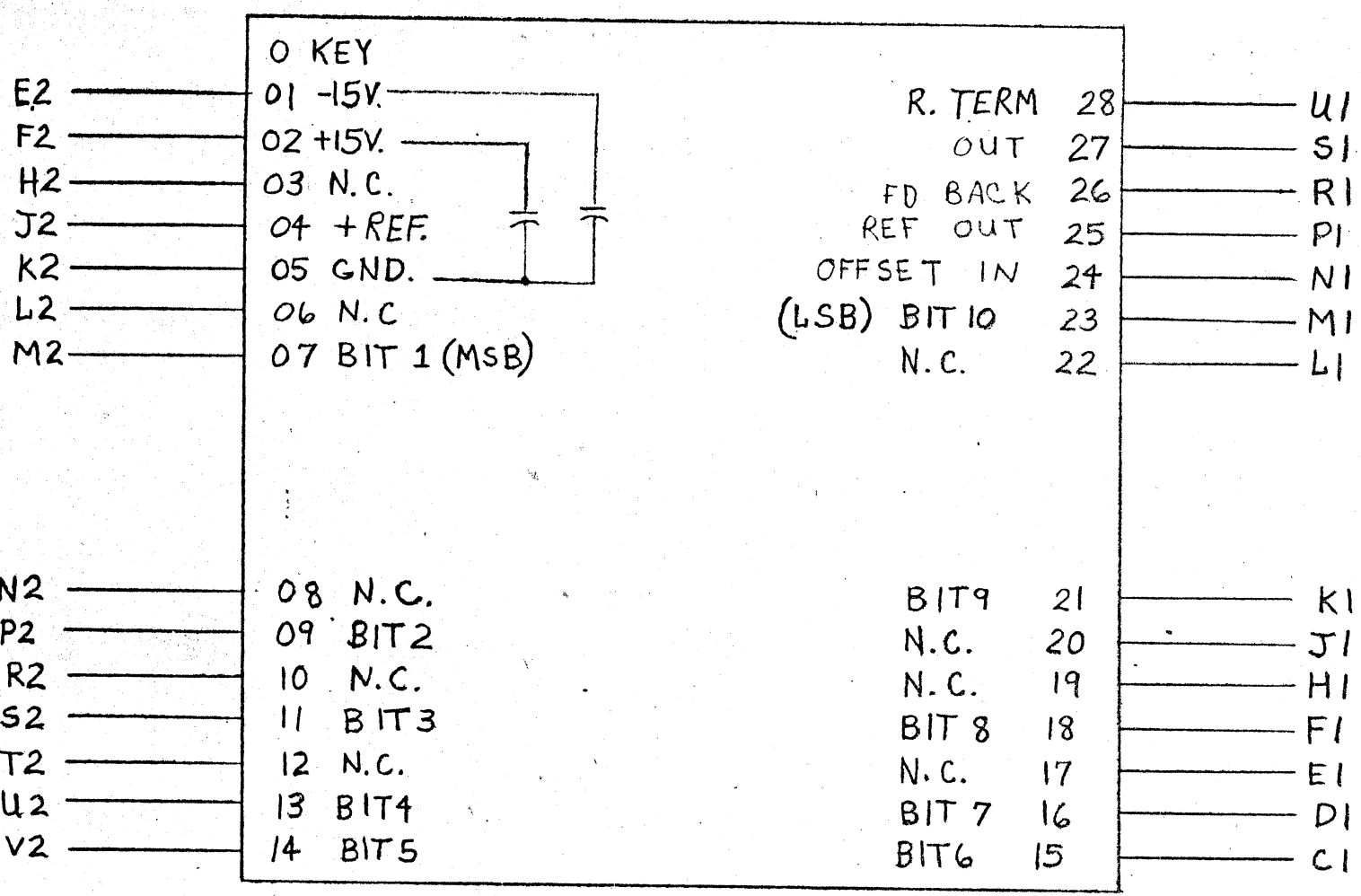


POINTS ON P.C. FOR ADDITIONAL COMPONENTS

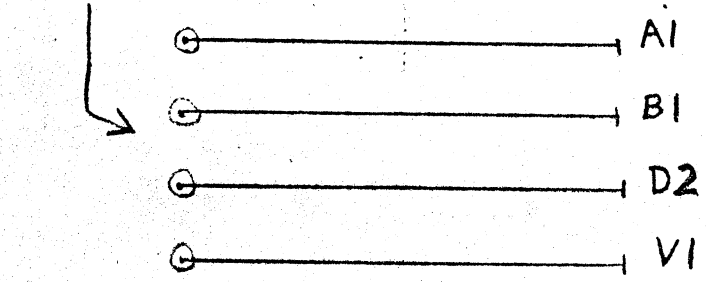


REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-015-2 12 BIT D.A.C.		
	DESIGNED ADR	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 3-14-72	DWG. NO.

ANALOG DEVICE'S MDA 10 Z -110



POINT ON P.C. FOR ADDITIONAL COMPONENTS



NOTE: C2 DIGITAL GND.

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP 15-3 10 BIT D.A.C.		
	DESIGNED	APPROVED S Pappas	SHEET 1 OF 1
	DRAWN GARY	DATE 11-5-7	DWG. NO.

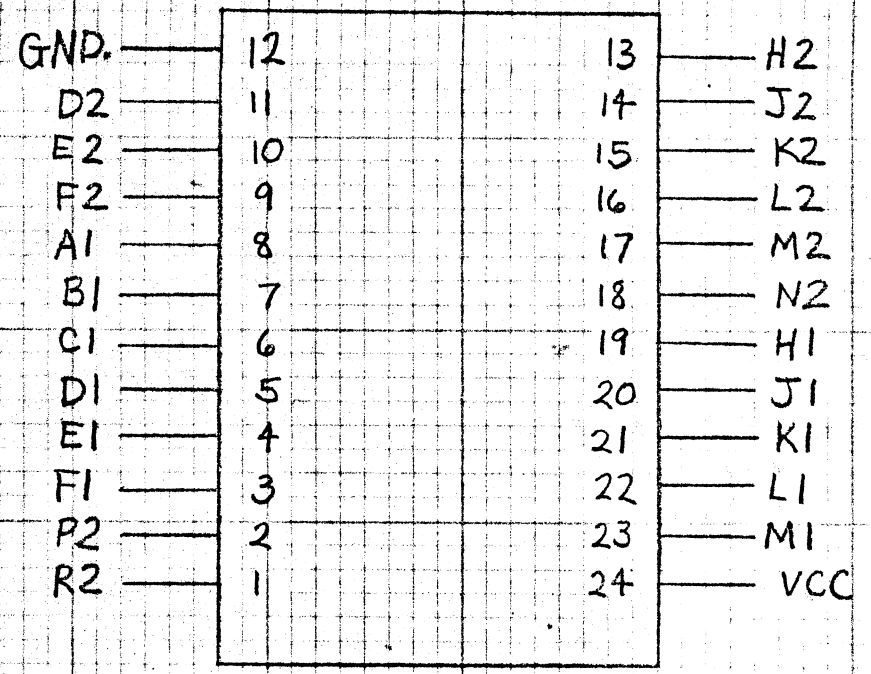
TP-016 Universal Card

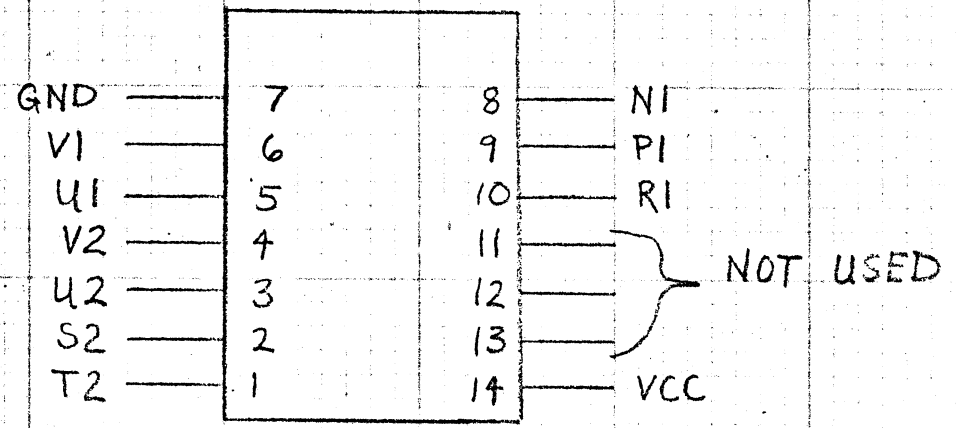
This card can take one 24-pin IC which has pin 12 as GRD and 24 as V_{cc}, and a 16-pin IC which has pin 7 as GRD and pin 14 as V_{cc}. For the 14-pin IC, only pins 1 through 11 are available at the output.

The card became very useful with the introduction of many MSI and LSI, which contain complex functions in dual in-line package.

Format: A

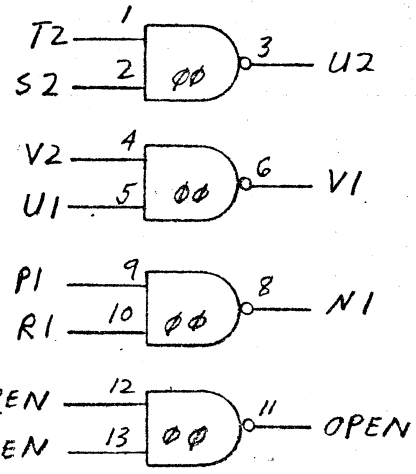
Dash Number	Description
1	Data Selector and 3 each 2-NAND
2	Data Selector and 3 Bus Drivers
3	Data Selector and 4 Inverters
4	Position Scaler and 3 each Open Collector
5	Position Scaler and 3 each 2-NOR

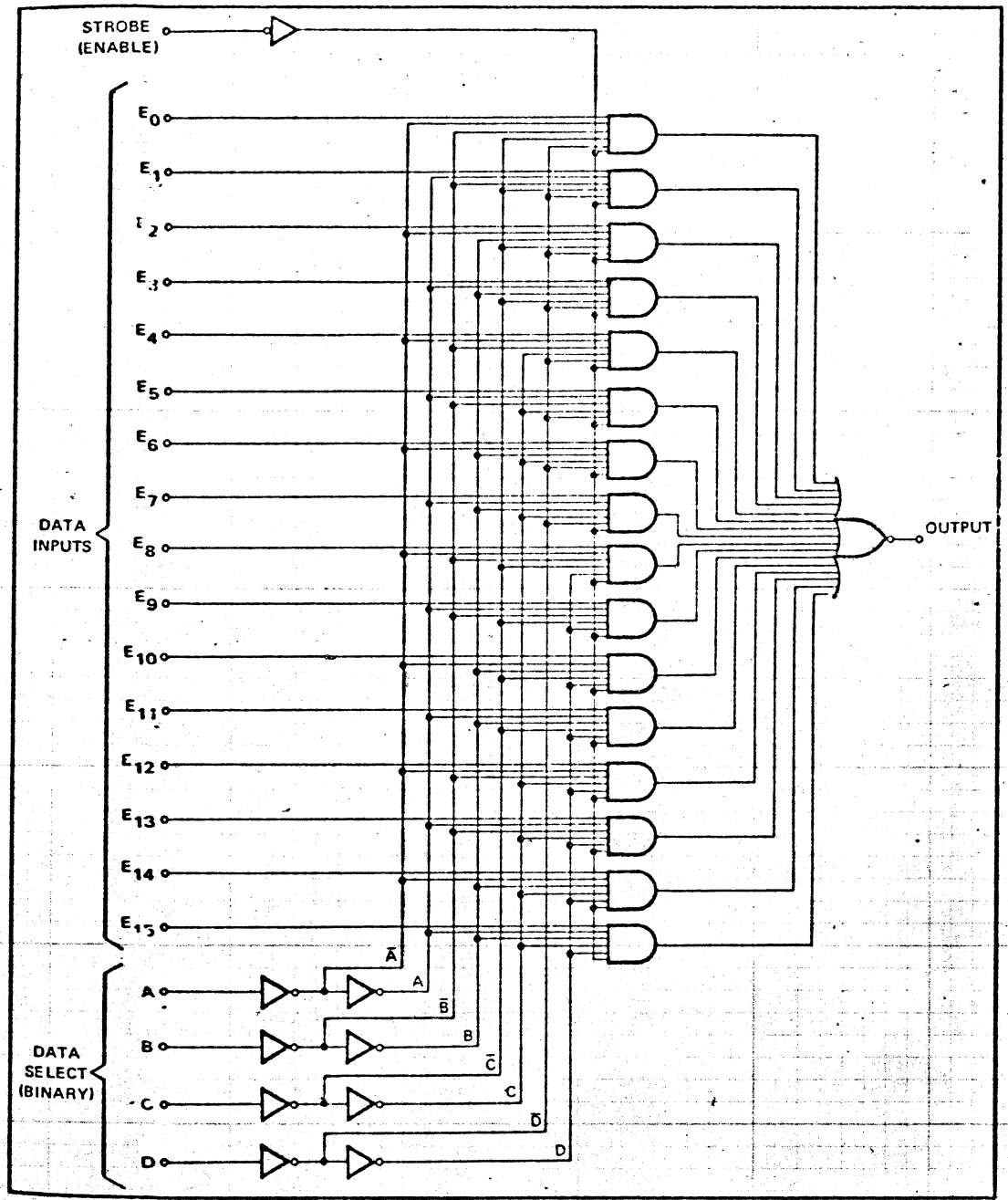




VCC - A2 +5 VOLTS
GND. - C2, T1

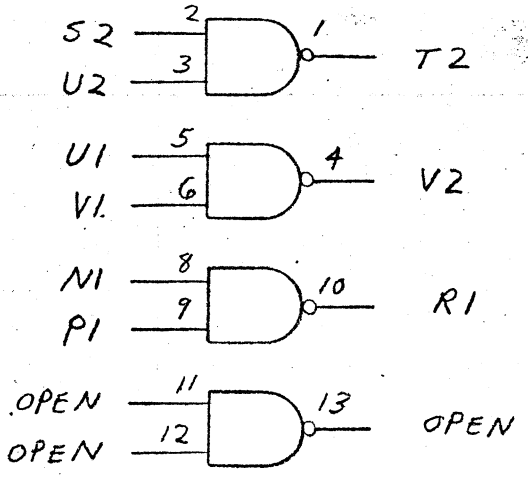
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-016 UNIVERSAL 24 PIN		
	DESIGNED S. MARTIN	APPROVED S. Fontana	SHEET 1 OF 1
	DRAWN GARY	DATE 11-5-70	DWG. NO. TP-00161-EC

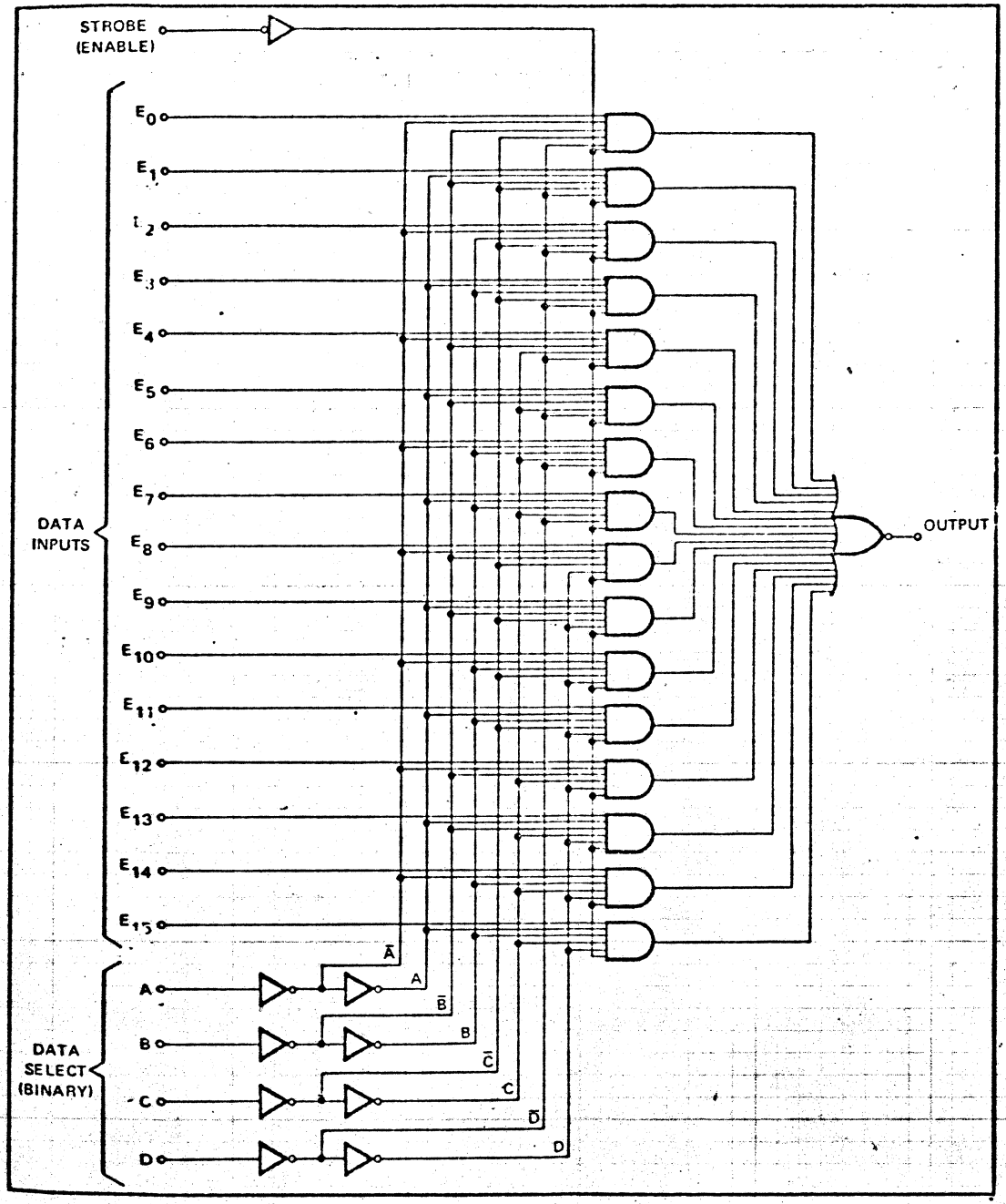




REVISIONS		TENNECOMP SYSTEMS, INC		
		TP-016-01	DESIGNED	APPROVED
			DRAWN WJT	DATE 2-22-72
			SHEET 2 OF 3	DWG. NO. 114-00016-000

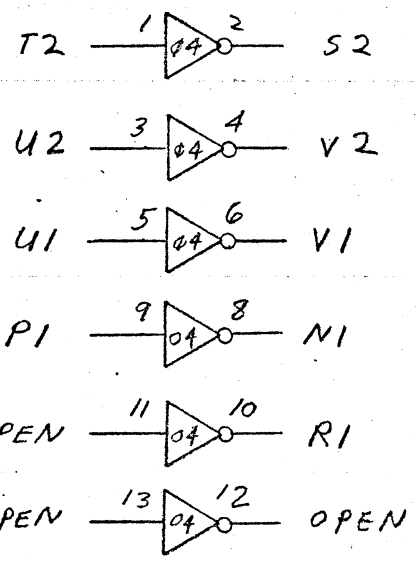
ICS ARE 74150 T.I.
AND 7400 T.I.

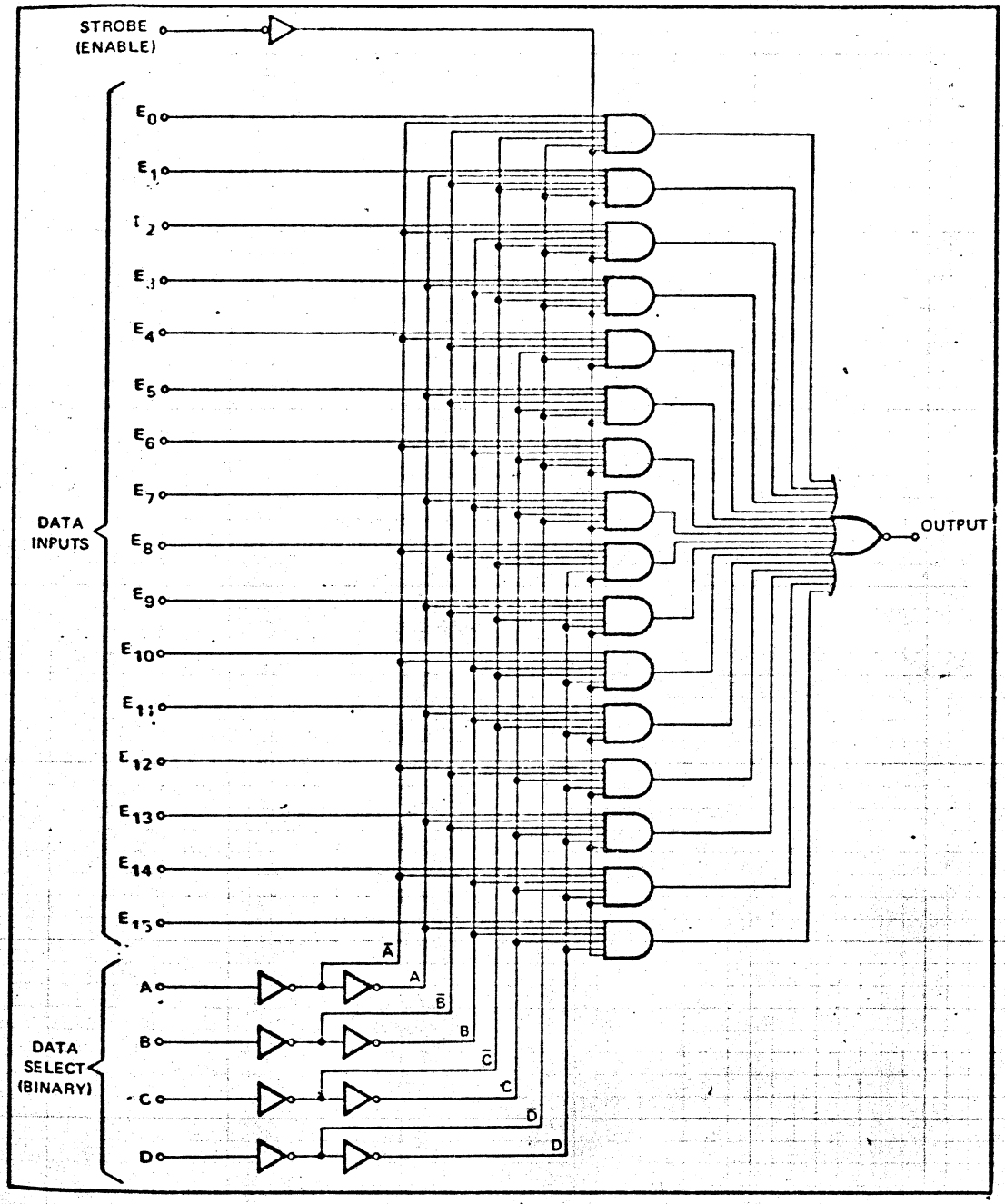




TENNECOMP SYSTEMS, INC.					
TP-016-P2				SHEET 2 OF 3	
	DESIGNED	APPROVED		DWG. NO.	
	DRAWN WT	DATE 2-22-72		114-00016-000	
REVISIONS					

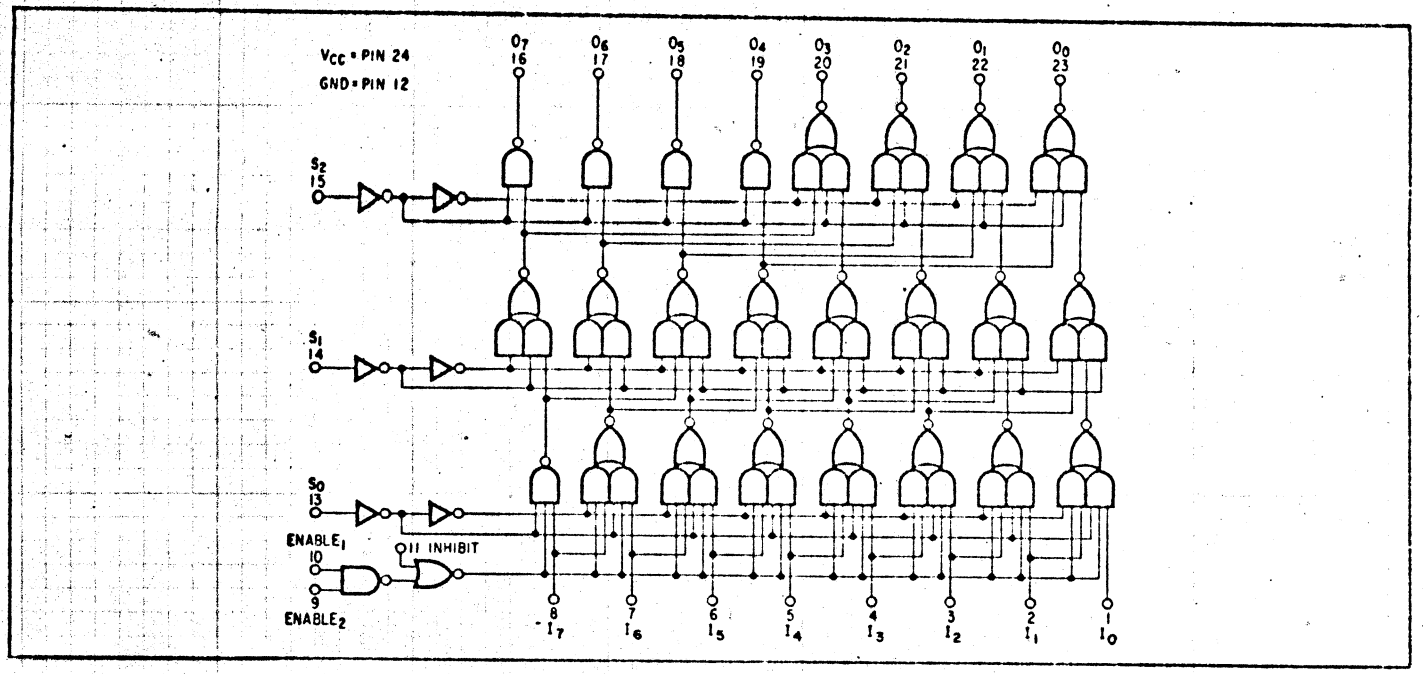
I.C.'S ARE 74150 T.I.
AND N8881 SIGNETICS





I.C.'S ARE 74150 T.I.
AND 7404 T.I.

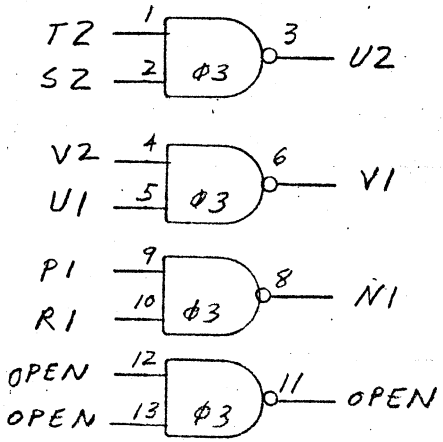
TENNECOMP SYSTEMS, INC.	TP-16-03	DESIGNED	APPROVED	SHEET 2 OF 3
REVISIONS		DRAWN WJ	DATE 2-22-72	DWG. NO. 114-00016-000



TRUTH TABLE
EIGHT BIT SCALER

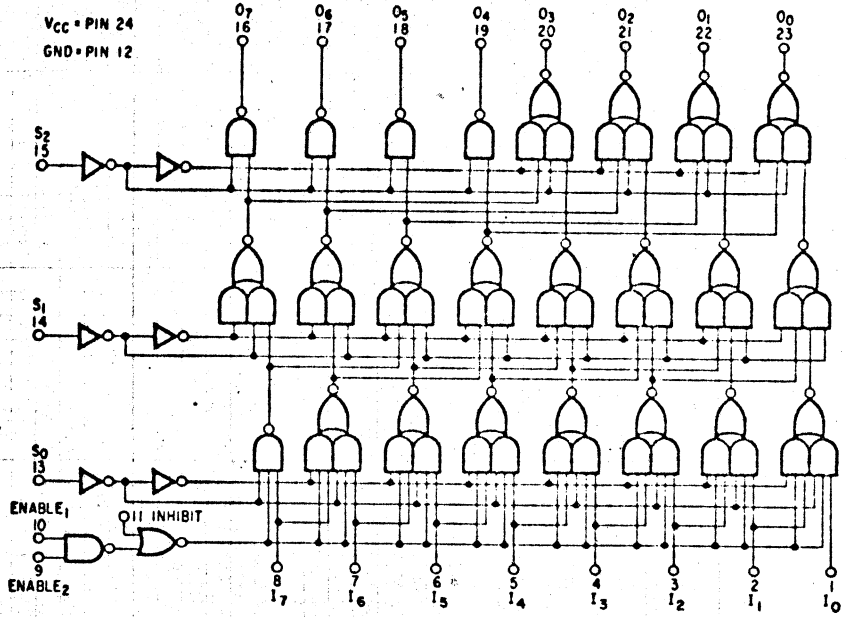
Inhibit	Enable 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
		0	0	0	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$
0	1	1	0	0	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1
0	1	0	1	0	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1
0	1	1	1	0	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1
0	1	0	0	1	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1
0	1	1	0	1	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1
0	1	0	1	1	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\overline{I}_7$	1	1	1	1	1	1	1
1	1	X	X	X	1	1	1	1	1	1	1	1
0	0	X	X	X	1	1	1	1	1	1	1	1

X INDICATES EITHER LOGIC "1" OR LOGIC "0" MAY BE PRESENT



I.C.'S ARE 8243 SYGNETICS
AND 7403 T.I.

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-16-04
	DESIGNED: — APPROVED: — SHEET 3 OF 3
	DRAWN: WJ DATE: 2-22-72 DWG. NO.: 114-00016-000

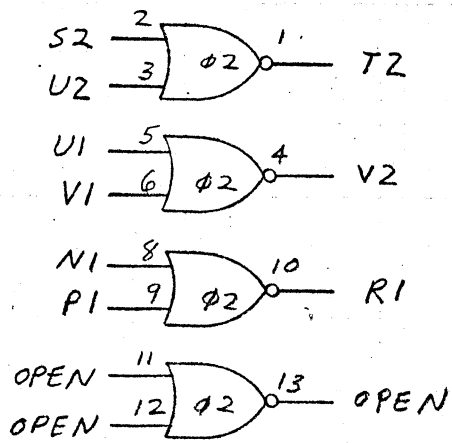


TRUTH TABLE

EIGHT BIT SCALER

Inhibit	Enable 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
		0	0	0	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$
0	1	1	0	0	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1
0	1	0	1	0	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1
0	1	1	1	0	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1
0	1	0	0	1	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1
0	1	1	0	1	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1
0	1	0	1	1	$\overline{I}_6$	$\overline{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\overline{I}_7$	1	1	1	1	1	1	1
1	1	X	X	X	1	1	1	1	1	1	1	1
0	0	X	X	X	1	1	1	1	1	1	1	1

X INDICATES EITHER LOGIC "1" OR LOGIC "0" MAY BE PRESENT



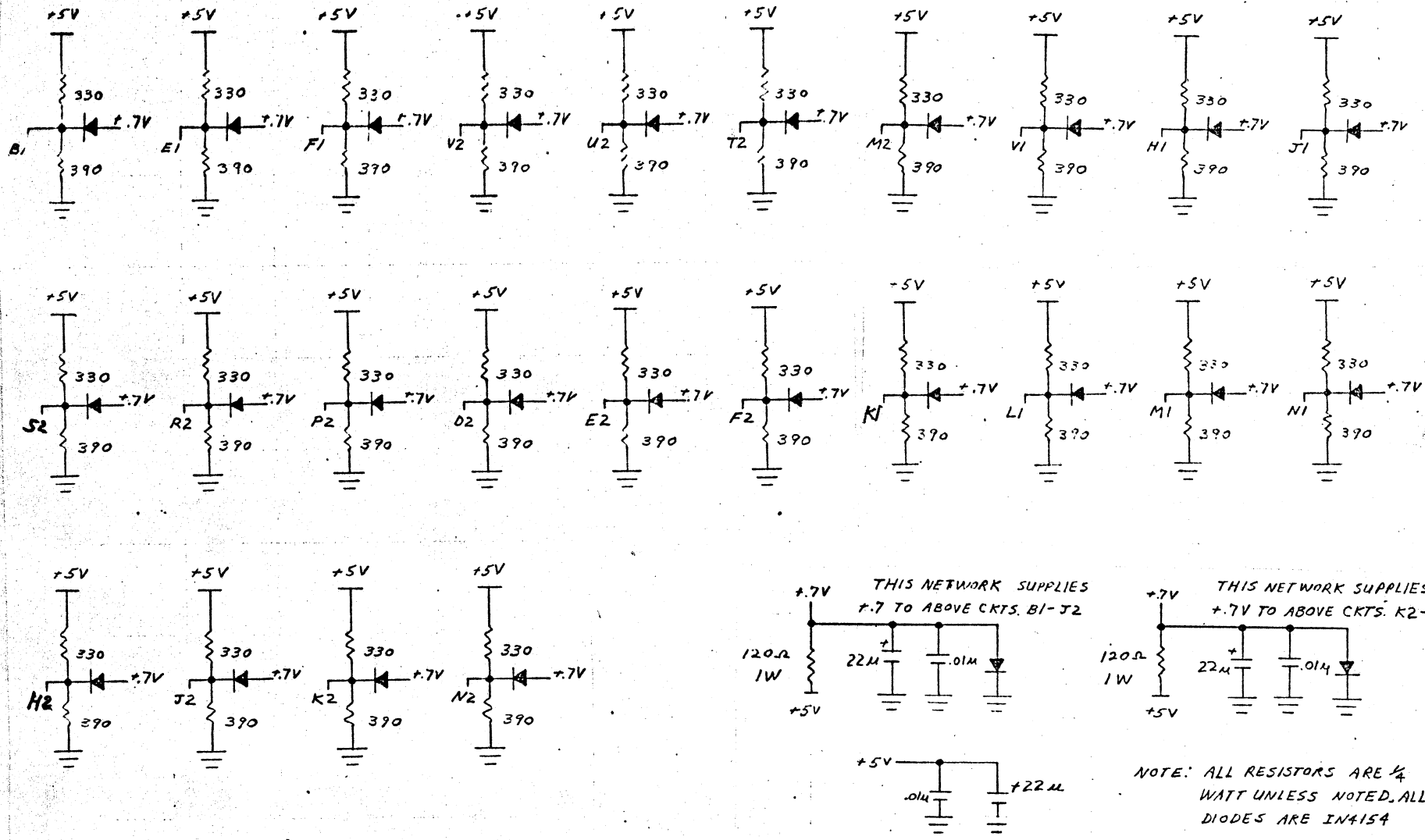
I.C.'S ARE 8243 SYGNETICS
AND 7402 T.I.

REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-16-Φ5
	DESIGNED: — APPROVED: — SHEET 3 OF 3
	DRAWN: WJ DATE: 2-22-72 DWG. NO.: 114-00016-000

TP-020 Resistor Card

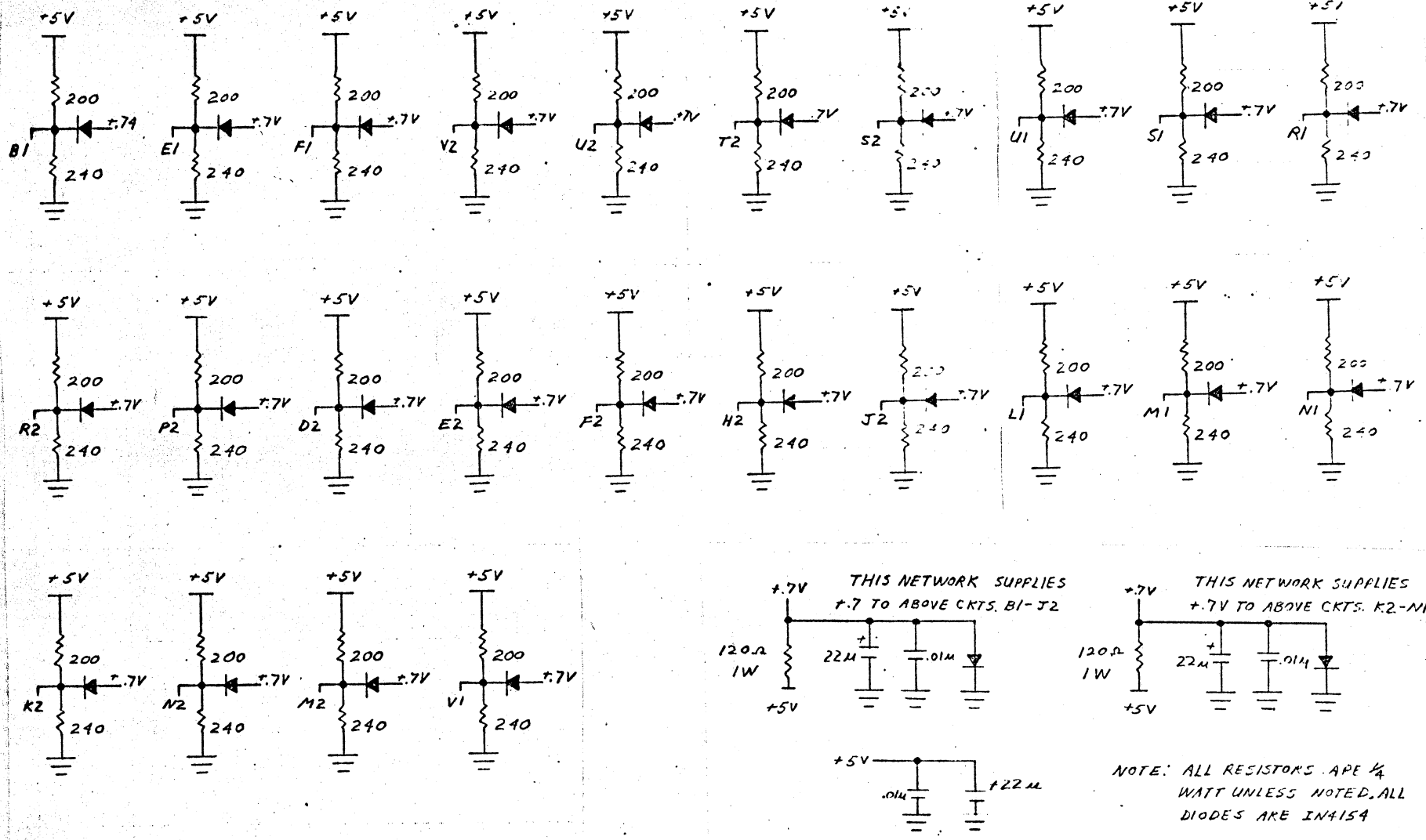
The TP-020 is a general purpose resistor card designed as a Nova Terminator for the TP-1371. Below is a summary of the variations available:

-1	Nova Terminator
-2	Nova Terminator
-3	FCP Bus Terminator
-4	Channel Selector
-5	ADC Terminator
-6	Display Intensity Control



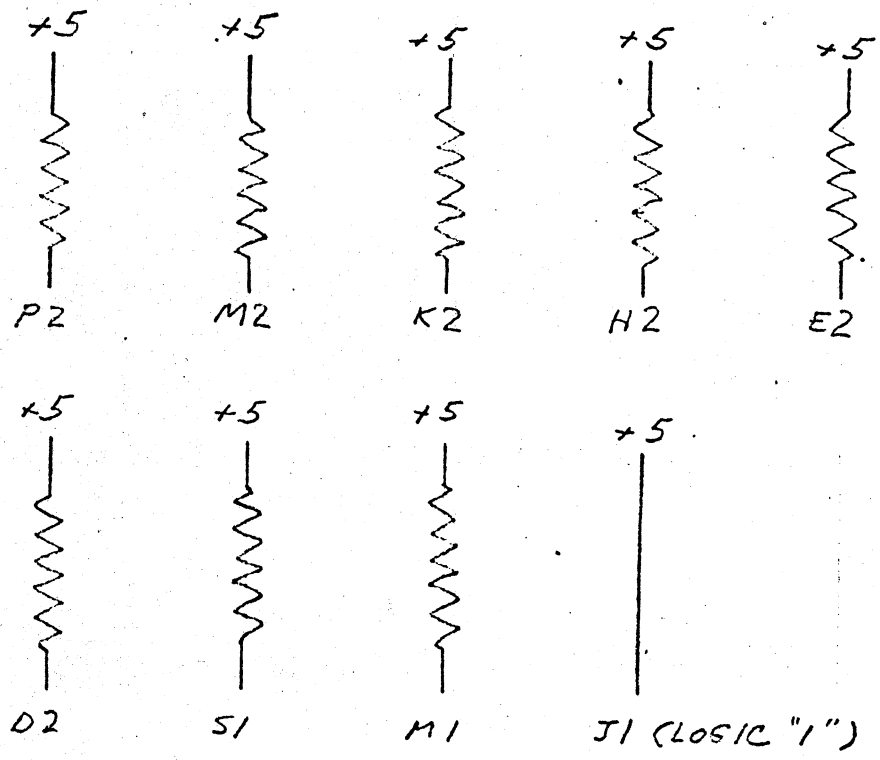
NOTE: ALL RESISTORS ARE ¼ WATT UNLESS NOTED. ALL DIODES ARE IN4154

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-020-1 NOVA TERMINATOR		
	DESIGNED FF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO.



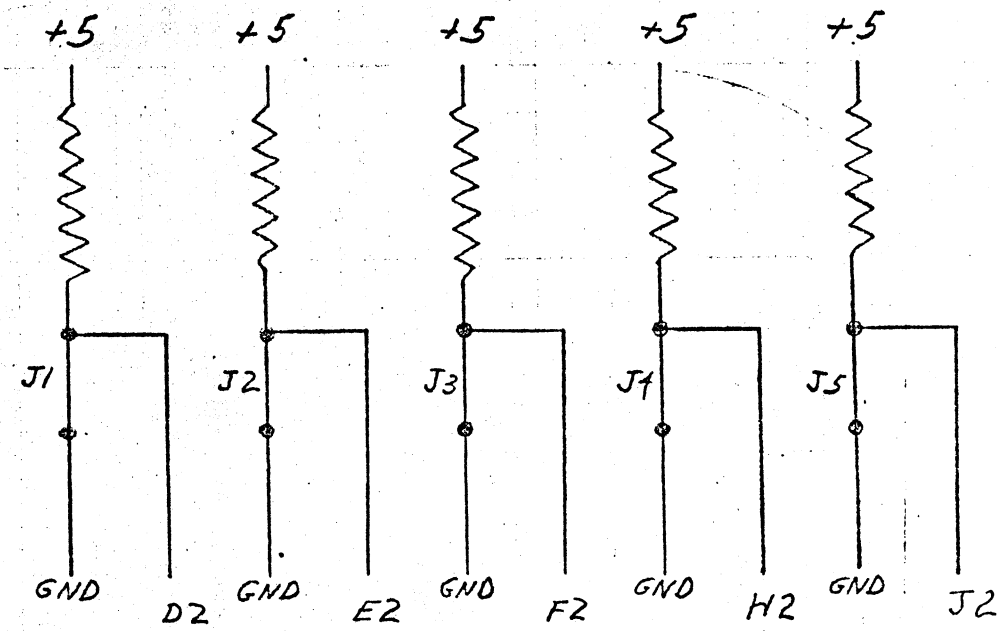
NOTE: ALL RESISTORS ARE 1/4 WATT UNLESS NOTED. ALL DIODES ARE IN4154

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-020-2 NOVA TERMINATOR		
	DESIGNED FF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO.



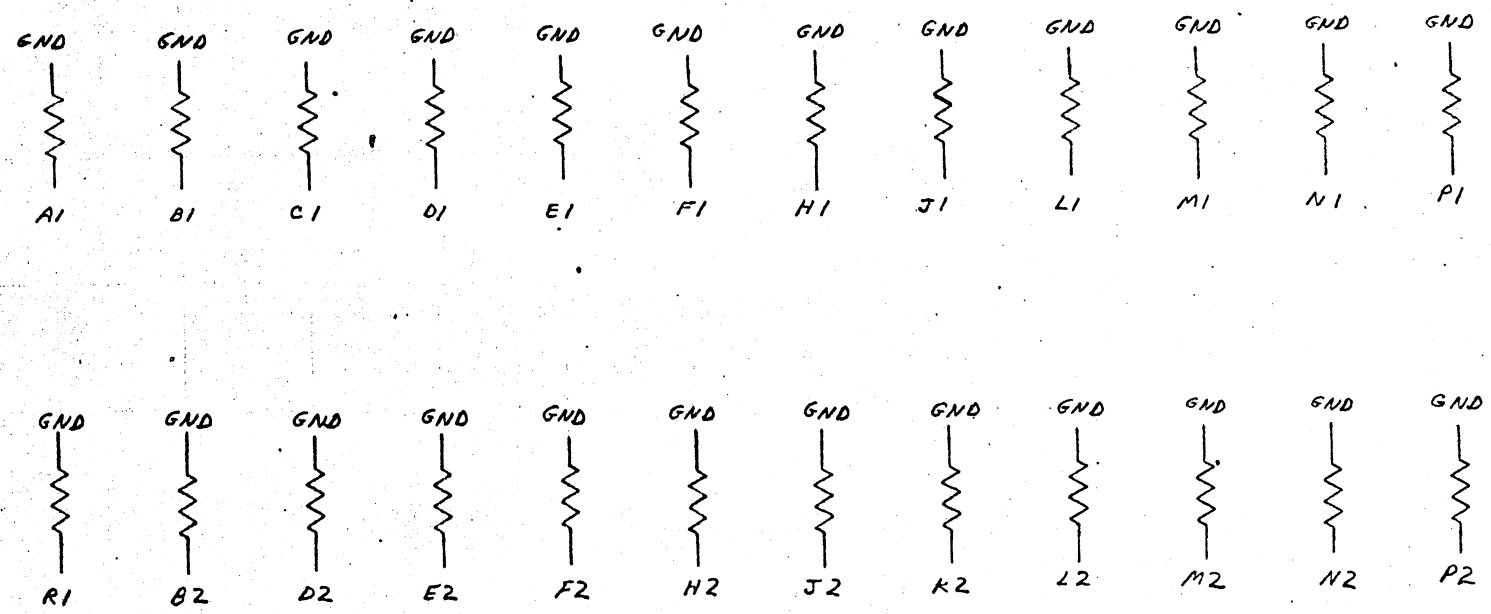
ALL RESISTORS 1 KΩ

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-020-3 FCP BUS TERMINATOR		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO.



ALL RESISTORS 1 KΩ

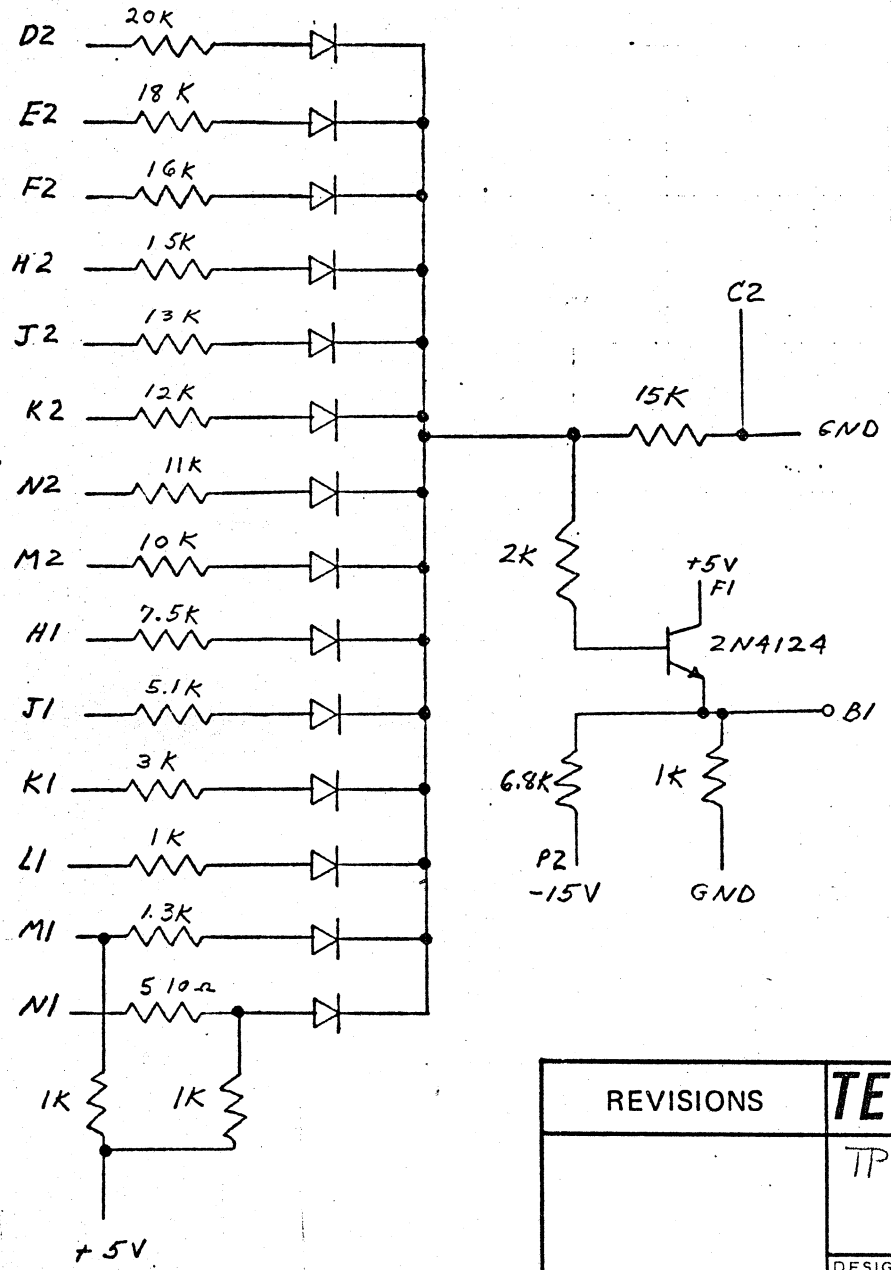
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-020-4 CHANNEL SELECT CARD		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO.



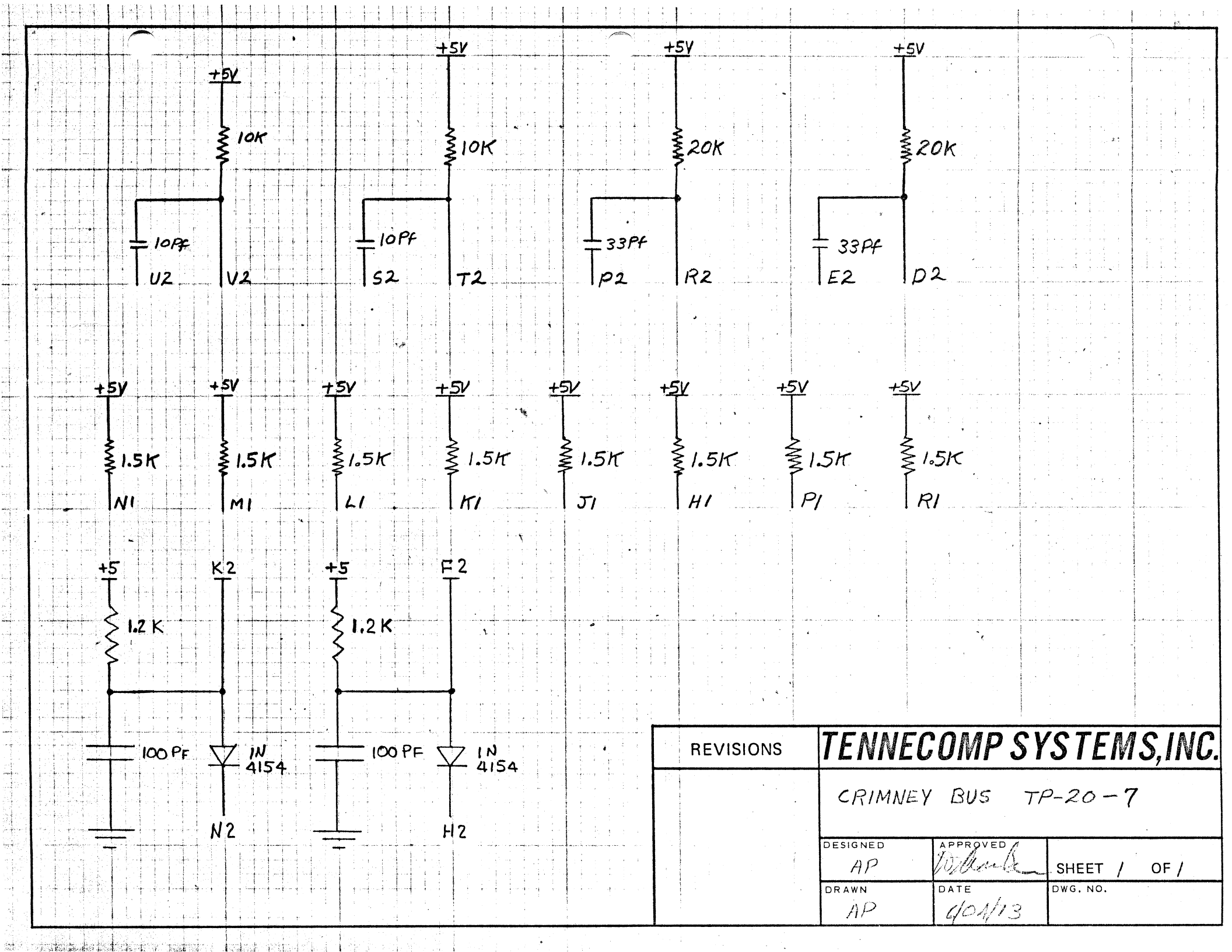
ALL RESISTORS 1K Ω

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-020-5 ADC TERMINATOR		
	DESIGNED WC	APPROVED	SHEET 1 OF 1
	DRAWN WJ	DATE 6-1-72	DWG. NO.

DIODES — IN281



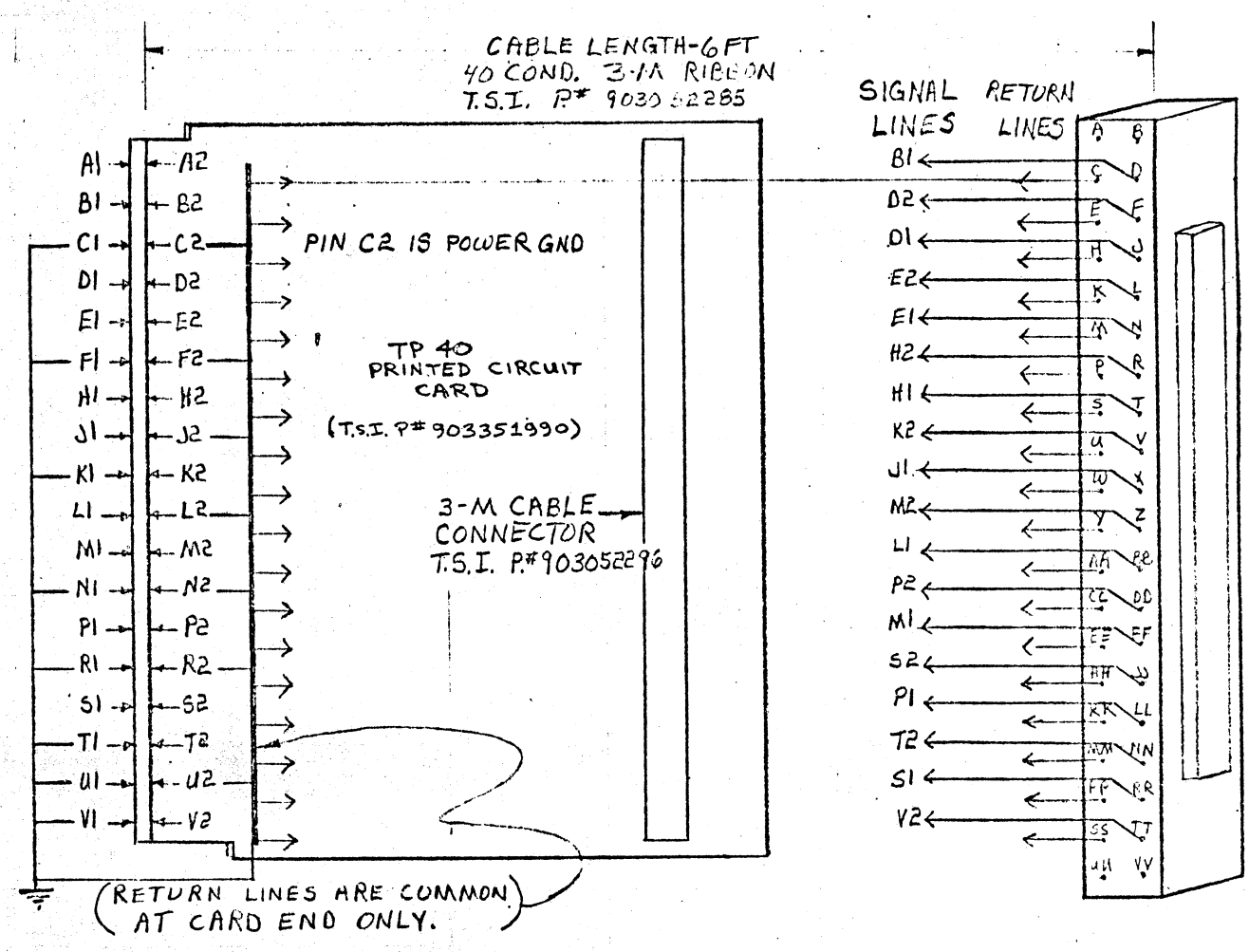
REVISIONS	TENNECOMP SYSTEMS, INC.
	TP-020-6 INTENSITY CONTROL
	DESIGNED: A D-R; APPROVED: ; SHEET 1 OF 1
	DRAWN: WJ; DATE: 6-1-72; DWG. NO.



REVISIONS	TENNECOMP SYSTEMS, INC.		
	CRIMNEY BUS TP-20-7		
	DESIGNED AP	APPROVED	SHEET 1 OF 1
	DRAWN AP	DATE 4/04/13	DWG. NO.

TP-040-1 3M Ribbon Connector Card

This card is used as a connector for 3M type ribbon. The card is a standard double-density DEC board with a 3M cable connector TSI part number 903-052296 at one end.



REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-040-1 3M RIBBON CONNECTOR CARD		
	DESIGNED FF	APPROVED	SHEET 1 OF 1
	DRAWN CF	DATE 8-24-72	DWG. NO.

TP-041-1 PDP-11 Address Decoder and Interrupt Control

This card is functionally the same as DEC's M105 and M782 boards. The card is a double-wide board with section A the M105 equivalent and Section B the M782 equivalent.

Detailed information on the use of this card may be found in DEC PDP-11 I/O Interface manuals.

TP-142-41 JUMPER LIST

Insert jumpers for good mechanical connection.

Do not solder.

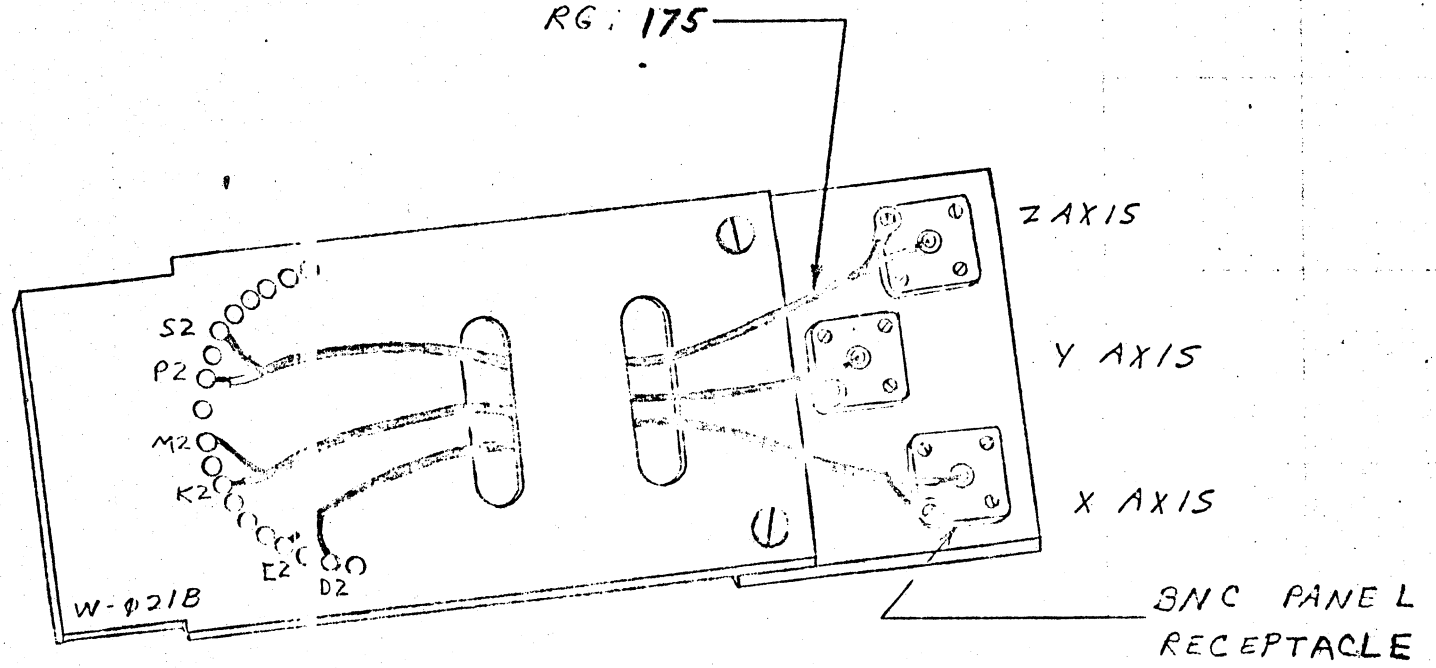
Device	Address	Vector	A SELECT JUMPERS (Jumper Center to 1 or 0) 12	11	10	9	8	7	6	5	4	3	VECTOR JUMPERS (Add Jumper if Marked) J_3	J_4	J_5	J_6	J_7
Functional Control Panel	16405X	31X	0	1	0	0	0	0	0	1	0	1		*	X		
Display 1	16406X	30X	0	1	0	0	0	0	0	1	1	0	X	*	X		
Display 2	16407X	32X	0	1	0	0	0	0	0	1	1	1	X		X		
ADD 1 Interface	16410X	33X	0	1	0	0	0	0	1	0	0	0			X		
LIST Mode	16411X	33X	0	1	0	0	0	0	1	0	0	1			X		
Live Time Clock	16412X	30X	0	1	0	0	0	0	1	0	1	0	X	*	X		

* Use insulation on this jumper.

2/8/73

TP-044-1 Display Cable Connector Card

This card contains 3 BNC connectors mounted on an extended W-021 DEC board. Both the center conductor and the shield are connected to individual pins to enable isolated grounds. This card is designed for use on Tennecomp display systems.



DISPLAY CABLE D5

REVISIONS	TENNECOMP SYSTEMS, INC
	TF-44 DISPLAY CABLE CARD
	DESIGNED FF / APPROVED / SHEET 1 OF 1
	DRAWN WJ / DATE 12-10-71 / DWG. NO. 141-07[illegible]02

TP-45 ±15 V Analog Power Supply

This card contains a single power supply module for ±15 Volt operation. The specifications for each of the cards are summarized below:

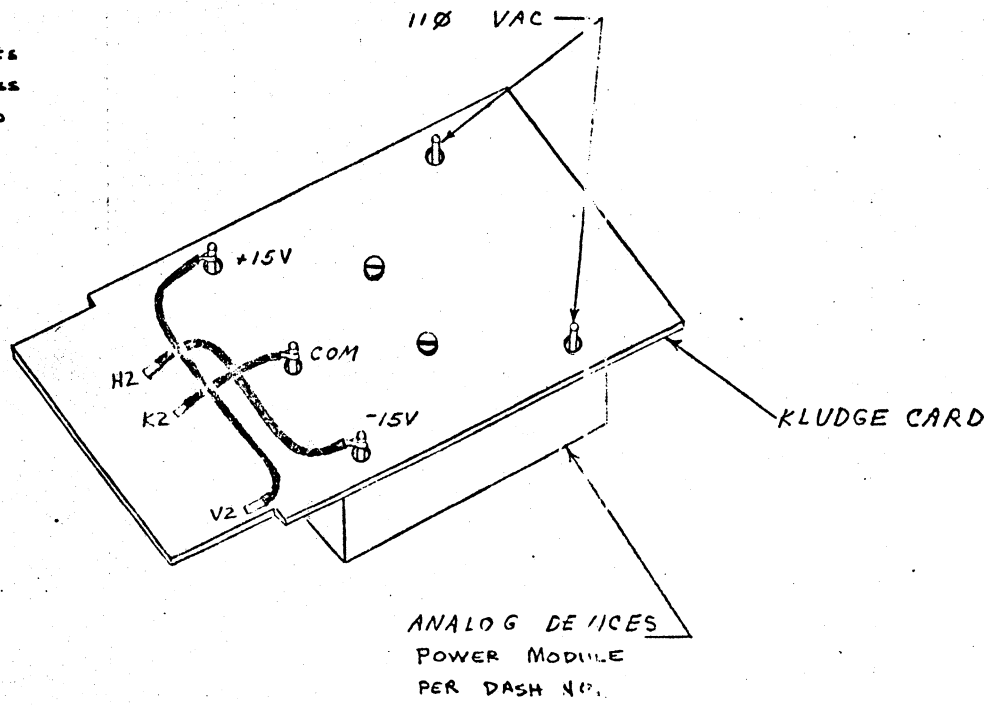
Card	mA	Analog Devices Part No.
TP-045-1	100	902
TP-045-2	50	904

SPECIFICATION SUMMARY

	900 SERIES, GENERAL PURPOSE	
	±15VDC Dual Op Amp Supply	
Model	904	902
Rated Output Voltage	±15VDC @ ±50mA	±15VDC @ ±100mA
Rated Input Voltage	105VAC to 125VAC[1] 50Hz to 400Hz	
Output Error (max)	+200mV, -0mV	+300mV, -0mV[1]
Regulation		
105 to 125VAC	0.1%	0.05%
Load, 0 to 100%	0.1%	0.1%
Temperature Coefficient (/°C)	0.015%	0.015%
Operating Temperature (°C)	0 to +71[2]	0 to +71[2]
Warm Up Drift	37mV (max)	45mV (max)
Ripple & Noise (max)	0.5mV rms	0.5mV rms
Short Circuit Protected	all outputs	

NOTE:

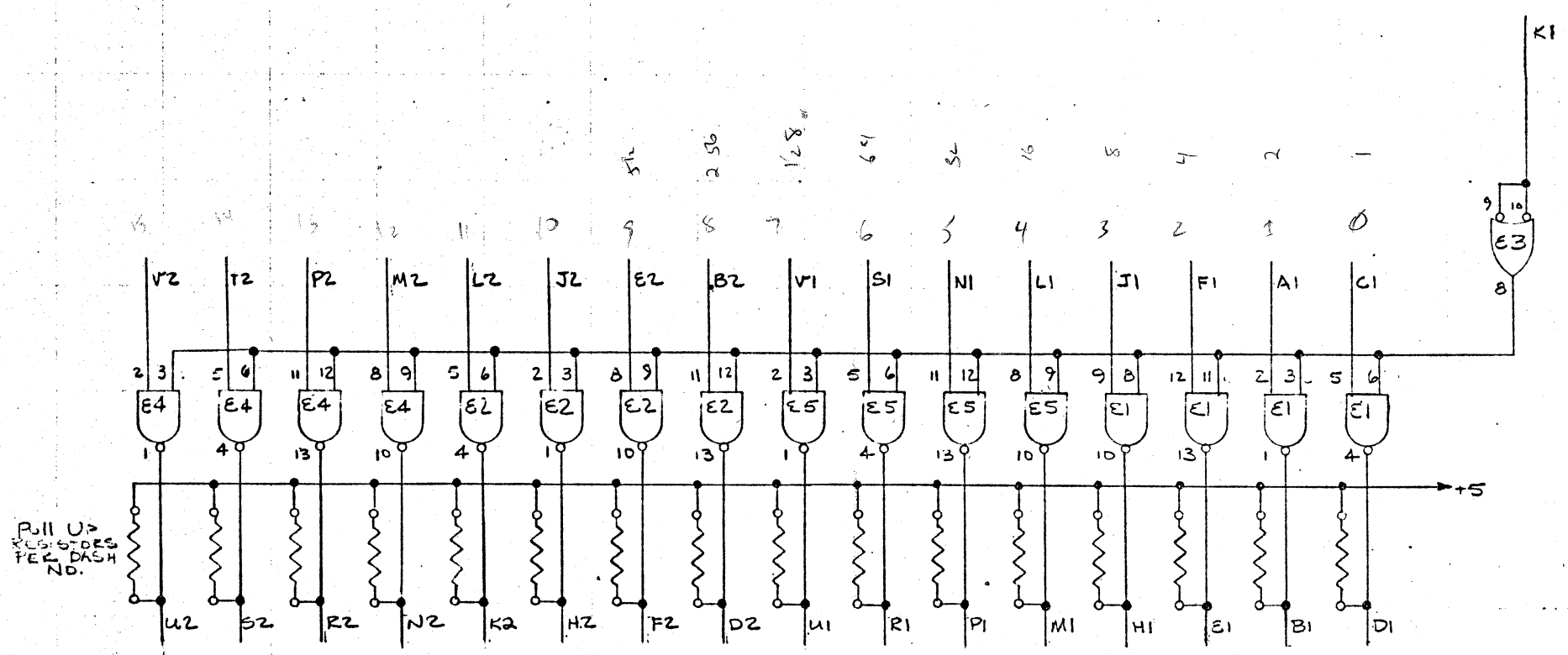
THIS CARD REQUIRES CLEARANCE IN EXCESS OF ONE STANDARD CARD SLOT.



± 15 V. POWER SUPPLY CARD

TP 45 -1	100 MILLIAMPS	(ANALOG DEVICES MODEL 902)
-2	50 MILLIAMPS	(ANALOG DEVICES MODEL 904)

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-45 ±15 V. P.S.		
	DESIGNED	APPROVED	SHEET 1 OF 1
	DRAWN	DATE 12-13-71	DWG NO.



	E1,2,4,5	E3	Pull Up Resistors
-1	7401	7437	None
-2	8881	7437	None
-3	7401	7437	1K Ω

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	TP-046-1,2,3
	DESIGNED / APPROVED / SHEET OF
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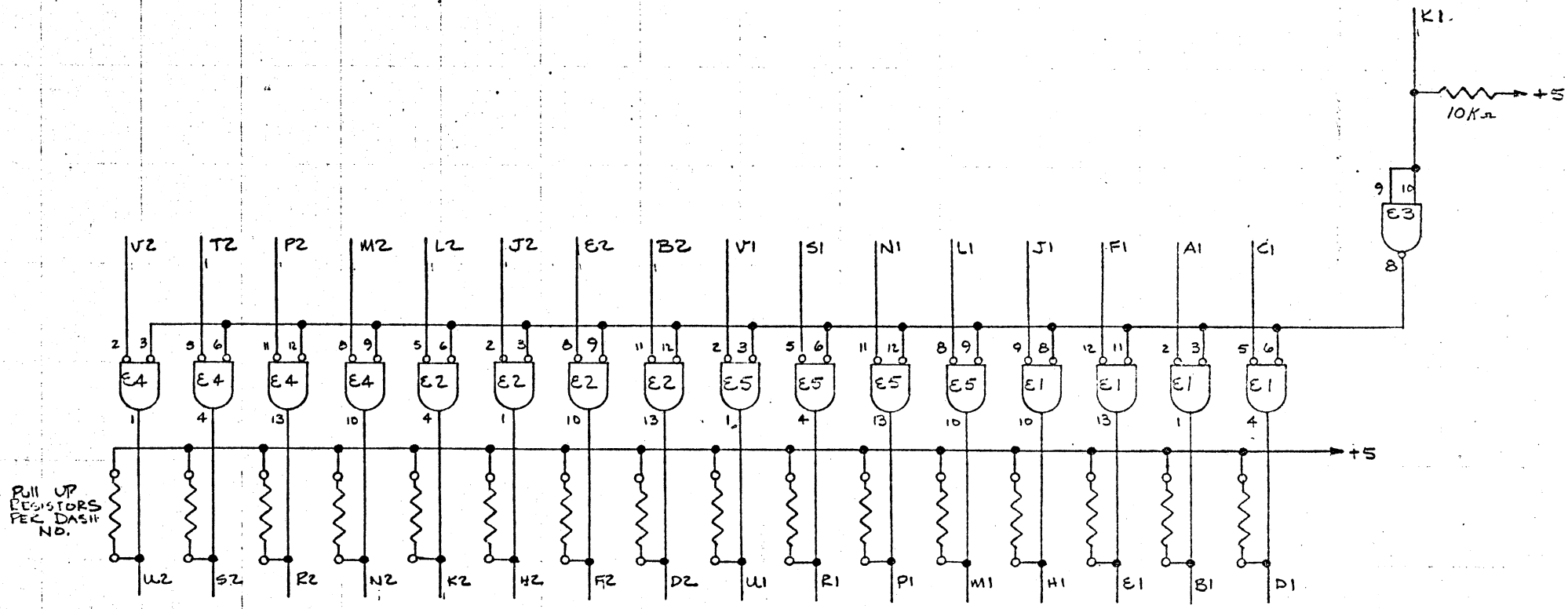

	E1,2,4,5	E3	Pull UP Resistors
-4	7402	7437	NONE

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	TP-046-4

DESIGNED	APPROVED	SHEET OF
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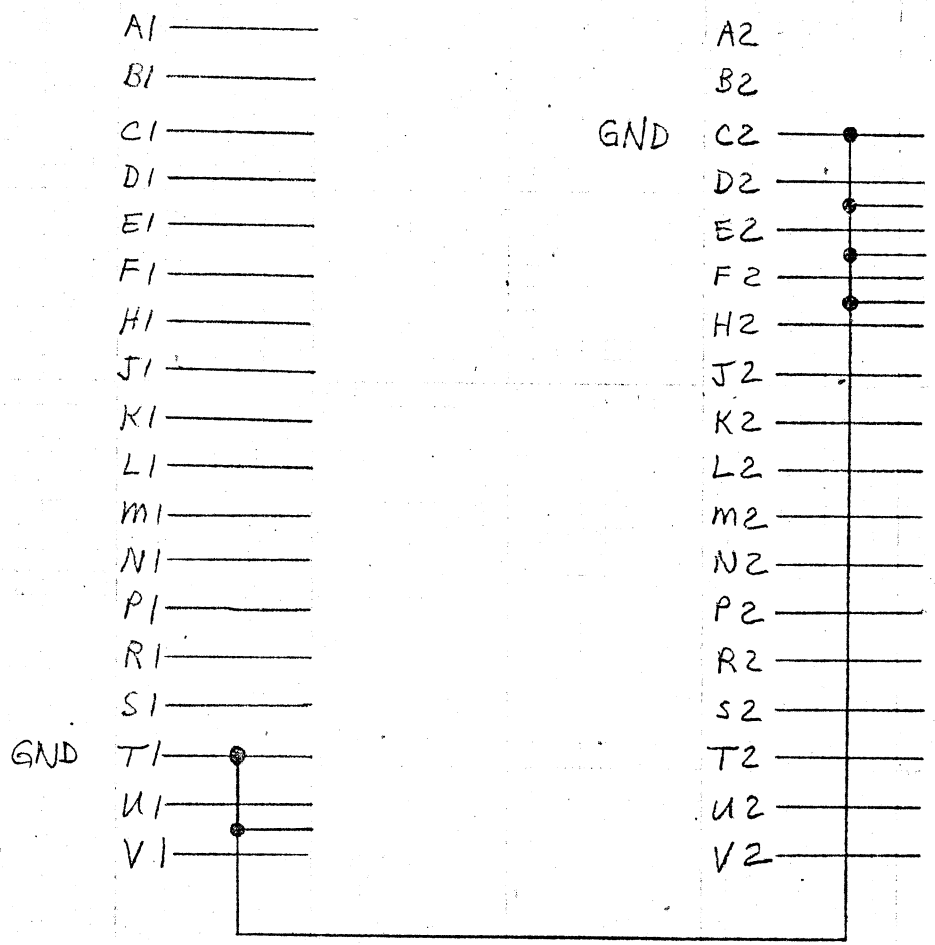
TP-049

32-Signal Ribbon Connector Card
2 Ground Pins
2 Unused

This card is used for interconnecting signals between modules. There are only 6 ground wires in the cable; therefore, it is not recommended for critical timing or strobes.



REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-049 CONNECTOR BOARD		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN CF	DATE 6-6-73	DWG. NO. 125-000049-000

TP-150-1 A/D Converter

The TP-150-1 is a 12-bit A/D converter card using Analog Devices model ADC-12QM. The converter has 3 selectable ranges as shown in Table 1 below. Converter specifications are summarized in Table 2 below.

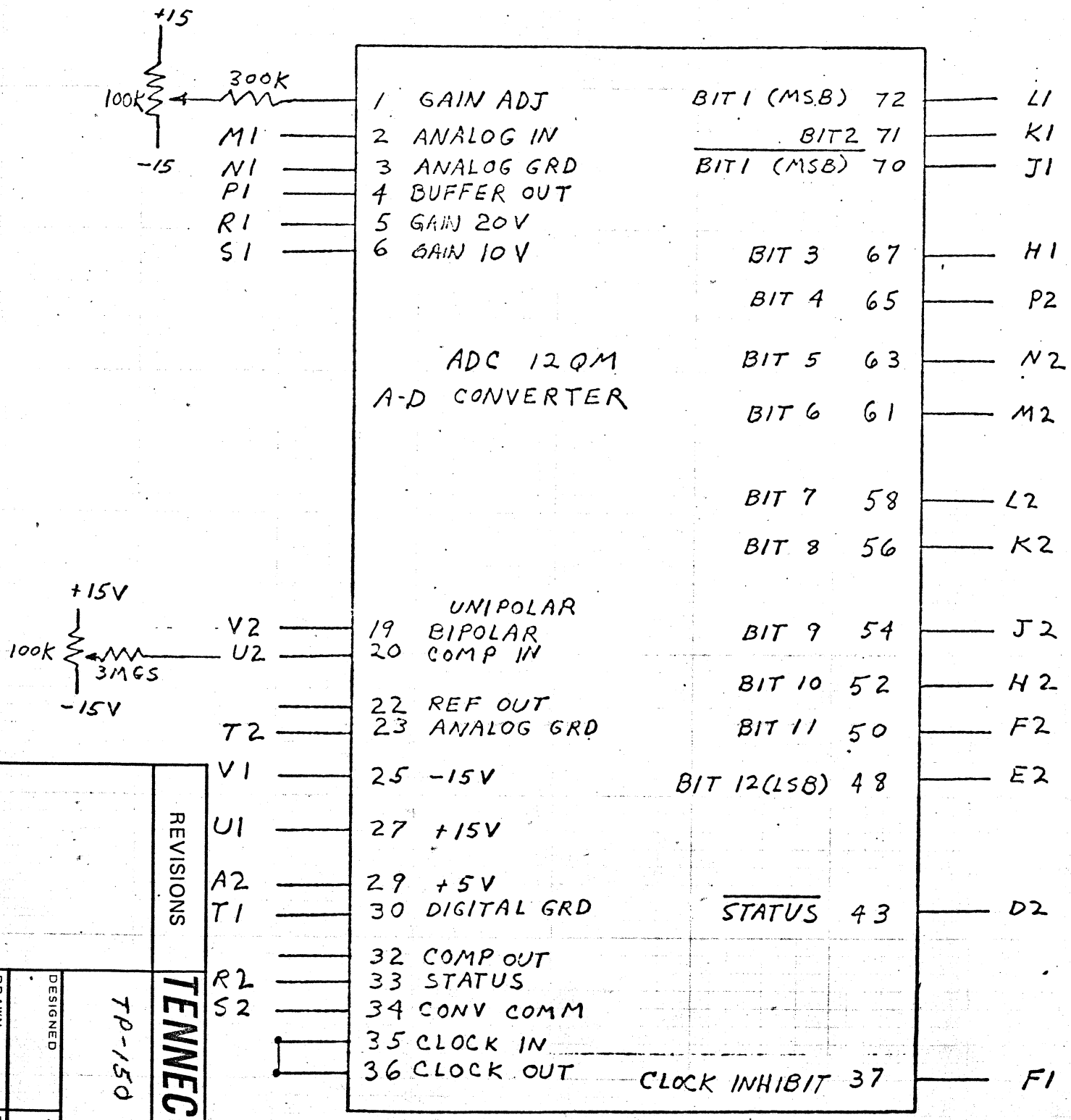
Table 1

Connection	Range
P1-S1, V2-U2	± 5 V
P1-R1, V2-U2	±10 V
P1-R1, V2-T2	+10 V

Table 2

Specification Summary - ADC-12QM

Model	ADC-12QM
Resolution, Bits	12
Linearity Error	$\pm\frac{1}{2}$ LSB
Analog Input Ranges (Volts)	±5, ±10, +10
Input Impedance (without Buffer)	About 2.5K
Conversion Time	25 μs
Digital Control Inputs & Outputs	TTL/DTL Compatible
Data Outputs	TTL Positive True
Output Code	Binary
Status or Busy Output	"1" During Conversion
Temperature Coefficient	
Gain (of Reading)	5 ppm/°C
Offset (Unipolar)	50 μV/°C
(Bipolar)	75 μV/°C
Power Required	+15 V @ 25 mA
	-15 V @ 35 mA
	+5 V @ 300 mA



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DRAWN	DESIGNED	TP-150 ADC 12 QM
DATE	APPROVED	TENNECOMP SYSTEMS, INC.
DWG. NO. 114-3150-000	SHEET OF	

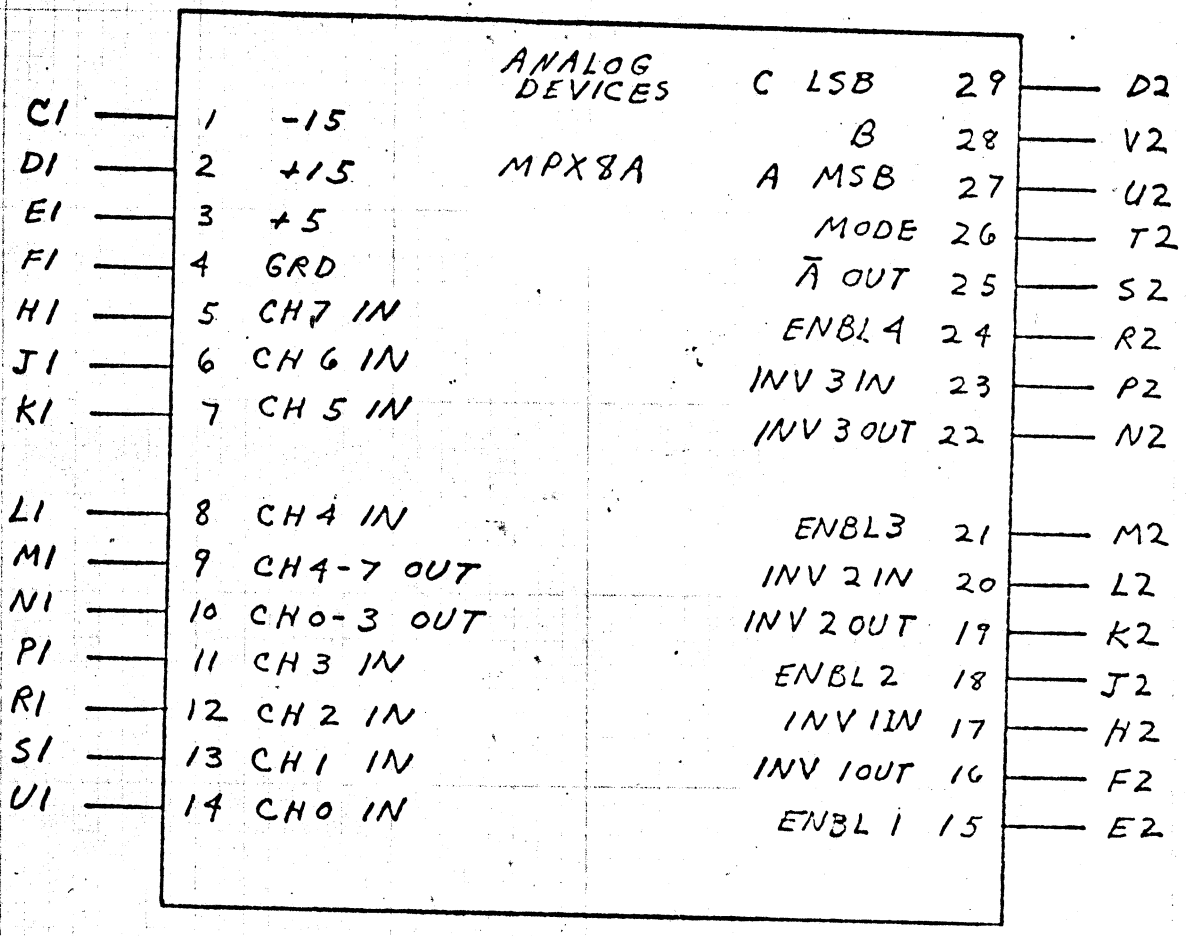
TP-151-1 Multiplexer

The TP-151-1 uses the Analog Devices model MPX-8A multiplexer, which is a high-speed multi-pole switch design to allow the time-sharing of a single digital processor by a number of analog circuits. This card may be used either with A/D converters to acquire data from a number of sources, or with D/A converters to distribute data to a number of receptors.

The MPX-8A is a high-speed 8-channel MOSFET multiplexer complete with binary address control logic. The logic provides usage in 4-channel differential mode, as well as providing all needed logic elements for expansion to 64 channels.

Specification Summary

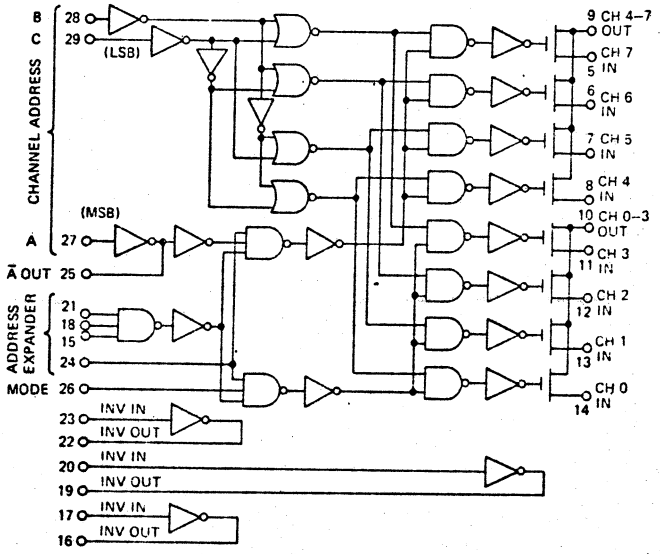
Model	MPX-8A
Channels	
Single-Ended	8
Differential	4
Voltage Range	
Rated Operation	±10 V
Overload Protection	±15 V
Transfer Error	.01%
Settling to 0.01%	<2 μs
Cross Channel Coupling	-80 dB
Common Mode Rejection	
DC	120 dB
60 Hz	106 dB
Channel Addressing	Binary Code
Address Logic	TTL Compatible/Positive True
Power Requirement	+15 V, ±1 V@ 6.2 mA
	-15 V, -1 V, +0 V@ 4 mA
	+5 V, ±10%@ 102 mA



-01 ONLY

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-151-1 MULTIPLEXER		
	DESIGNED	APPROVED	SHEET OF
	DRAWN	DATE	DWG. NO. 114-000151-001

LOGIC FLOW DIAGRAM: MPX-8A



TP-151-2 Sample and Hold

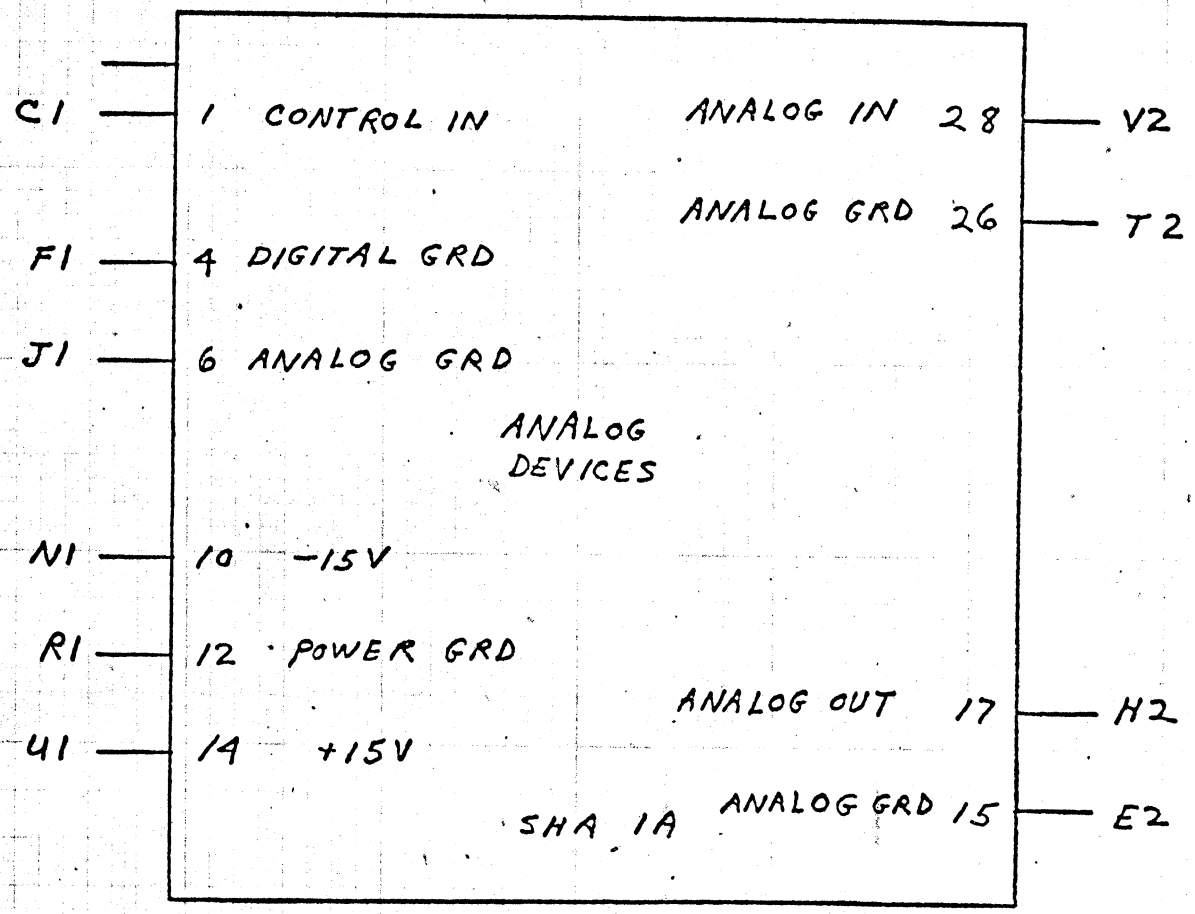
SHA-1A

The SHA-1A is intended for high accuracy operation at high speed. It settles to 0.01% in under 5 μsec; output droop in "HOLD" is 50 μV/μsec.

A specification summary is given below:

SPECIFICATION SUMMARY

Model	SHA-1A
Range	±10V
Gain	1
Gain Error	+0% - 0.05%
Linearity Error	2mV max over ±10V signal range
Input Impedance	10^{12} ohms
Acquisition Time	5μs to 0.01%
Aperture Delay	40ns
Aperture Jitter	5ns
Droop Rate	50μV/ms max
Mode Control	TTL Positive True
Logic Level in "Sample" Mode	"1"
Power Required ±15V @	15mA

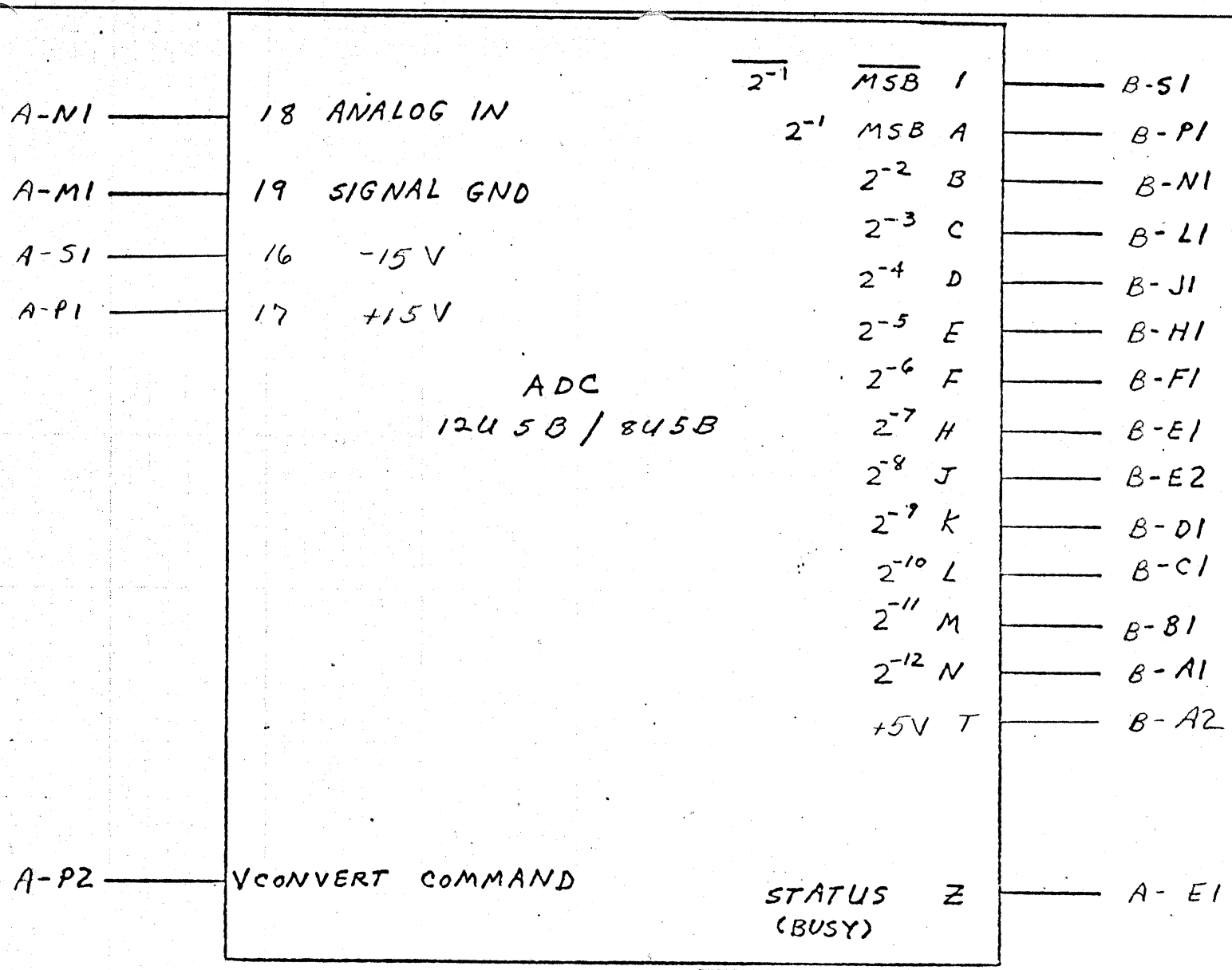


-02 ONLY

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP-151-2 SHA 1A		
	DESIGNED	APPROVED	SHEET OF
	DRAWN	DATE	DWG. NO. 114-000151-000

TP-152-1 ADC Connector

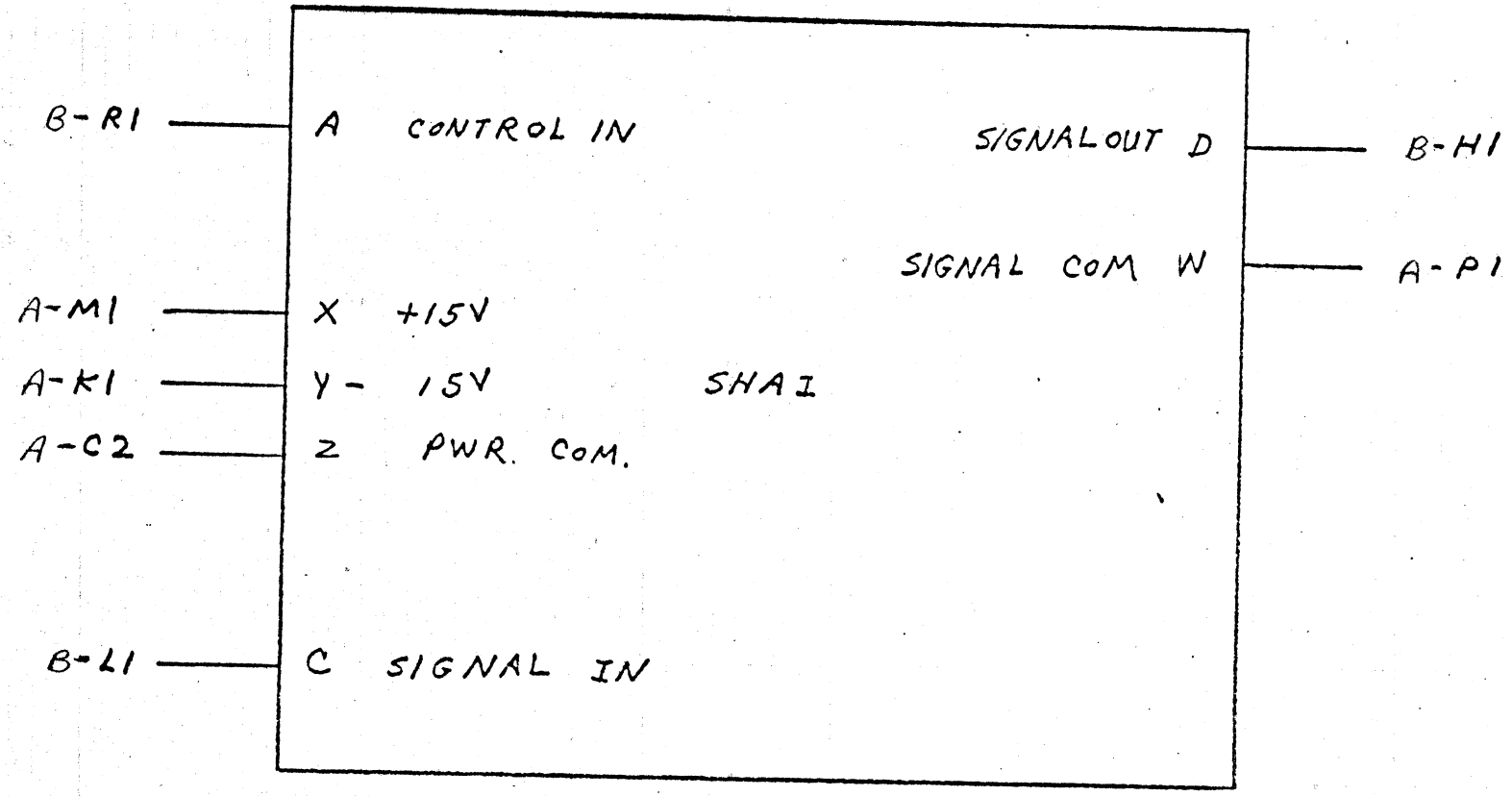
This is a double-wide connector card designed to mate with Analog Devices ADC 12U5B or ADC 8U5B A/D converters.



REVISIONS	TENNECOMP SYSTEMS, INC.		
	TF-152 ADC 1245B/ADC 845B		
	DESIGNED	APPROVED	SHEET OF
	DRAWN	DATE	DWG. NO. 114-000152-000

TP-153-1 Sample and Hold

This is a double-wide connector board designed to mate with Analog Devices model SHA1 Sample and Hold.

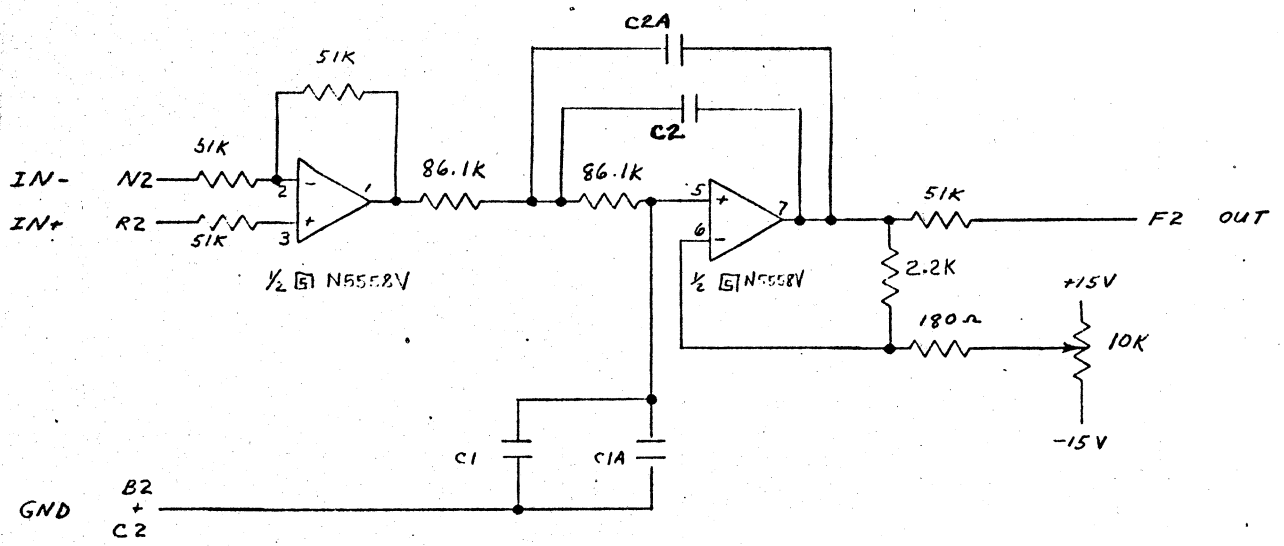


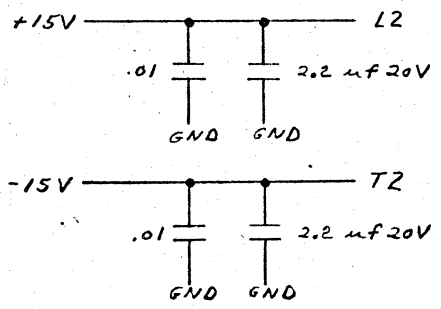
REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP 153-1 SHA I		
	DESIGNED	APPROVED	SHEET OF
	DRAWN	DATE	DWG. NO. 114-00515 3-000

TP-154 Filter

The card is a low pass active, 2-pole Butterworth filter with cut-off frequencies of 50, 500, 1K, and 5KHz, according to the table on the following page. The 001 version has no filter but is a bypass card connecting the input directly to the output. The filter characteristics are as follows:

F_{co} Accuracy: ± 3%
Rolloff: 12 db/octave
Gain in Pass Band: 0 ± .5 db
Signal Level in Pass Band: ± 10 V max.
Input Impedance: 51 K ohm floating differential
Output Impedance: 50 ohms max.
Output Current: ± 10 mA max.
DC Offset Adjustment Range: ± 200 mV
Power Requirements: ± 12 to ± 18 V; nom ± 15 @ 10 mA max.





CARD NUMBER	TYPE OF FILTER	TYPICAL CAPACITOR VALUES			
		C1	C1A	C2	C2A
TP-154-2	50 HZ	.01 μf	.015 μf	.047 μf	3680 pf
TP-154-3	500 HZ	110 pf	2500 pf	2200 pf	3000 pf
TP-154-4	1 KHZ	910 pf	1200 pf	100 pf	2500 pf
TP-154-5	5 KHZ	20 pf	240 pf	510 pf	10 pf
TP-154-1	NONE	-	-	-	-

NOTE: 1. ALL UNUSED PINS ARE TIED TO GROUND PLANE.
2. ON FILTER BYPASS CARDS, NO COMPONENTS ARE USED; JUMPERS ARE CONNECTED BETWEEN R2 AND F2 AND BETWEEN N2 AND C2. (TP-154-1 ONLY)
3. FILTER USED IS MULTIMETRICS INDUSTRIES SPECIAL DESIGN FOR TENNECOMP DATED 1-25-72

REVISIONS	TENNECOMP SYSTEMS, INC.		
	TP 154 FILTER		
	DESIGNED CF	APPROVED	SHEET 1 OF 1
	DRAWN CF	DATE 8-31-72	DWG. NO.