TP-5000

SYSTEMS MANUAL

TENNECOMP SYSTEMS INC.

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TP-5000

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December, 1972

201-000141

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1.0 INTRODUCTION

1.1 Purpose of Manual

The purpose of this manual is to assist in the operation and maintenance of the Tennecomp Systems TP-5000 Pulse Height Analysis System. It is intended that the user of this manual have at his disposal the system logic drawings, purchased component service manuals, program listings and listed reference documentation.

This manual presumes that the user of this manual who is performing hardware maintenance is familiar with TTL logic design. The hardware descriptions are intended to give the maintenance personnel an understanding of the functional operation and does not attempt to give a "cook book" repair description.

In a like manner, the software description presumes that the person working in detail on the software has a ready knowledge of the PDP-11 and its assembly language.

The operating procedures presume that the operator has neither hardware nor software experience, but that he does have a knowledge of "set-up" of the experiment that he is running.

1.2 General Description of System

The Tennecomp Systems TP-5000 Pulse Height Analysis System is an integrated series of computer-based modules for data acquisition, display and manipulation. It is based on the Digital Equipment Corporation's PDP-11 computer family. Peripheral modules are added to the system to perform the required functions. The UNIBUS hardware structure of the PDP-11 provides a standardized data exchange path between all system components. This permits expansion with a minimum of effort and allows the user to "build" his system to almost any level of sophistication.

The basic functions of the system are:

1.2.1 Sampling an analog signal or signals, digitizing the information, and storing the results in the computer memory, either as digital representations of the input pulse voltage or as a spectrum of the number of occurrences of pulses as a function of pulse height (histogram).

1.2.2 Manipulating the stored results to select areas of interest prior to display or storage in permanent form.

1.2.3 Presenting the data on an oscilloscope, teleprinter, or plotter for real time guidance of the experimenter.

1.2.4 Storing the data on magnetic tape or disc for retrieval at a later time or for transfer to a larger computer.

1.3 Specifications

1.3.1 ADC Subsystem

The ADC subsystem is designed to accommodate the Tennelec PACE system or a number of Wilkenson-type ADC's.

Two modes are available for data transfer from the ADC to the computer. In the ADD 1 mode, a count distribution is automatically accumulated in core memory. In the LIST mode, digital data is brought directly into a memory buffer, where the computer may manipulate the data and create a count distribution. Data may also be dumped on a pulse-by-pulse basis onto magnetic tape or disc.

Standard interface modules are available to implement the ADD 1 and LIST modes, to combine up to 8 digital input sources, to keep track of real and live time, and to permit various coincidence requirements to be placed on input events.

1.3.2 Central Processing Unit (CPU)

The CPU provides the logical and arithmetic capability for controlling the system and manipulating the data. Any PDP-11 family CPU may be used.

1.3.3 Memory

Magnetic core memory provides storage for data and program instructions. From 8K to 32K of 16-bit word core memory can be furnished, in 4K increments. The standard TP-5000 utilization of core is 6K for the control and manipulation programs and $1\frac{1}{2}$,16-bit words for each pulse height count channel. Standard TP-5000 nuclear programs require at least 12K of core memory and provide at least 4K,$1\frac{1}{2}$-word channels for data storage.

1.3.4 Magnetic Tape

Magnetic tape may be used to store ADD 1 mode count distributions, LIST mode data, or programs. IBM-compatible magnetic tape provides communication with off-line computers for post-experiment data analysis.

1.3.5 Disc Storage Unit

A disc storage unit provides the capability for computer control using an advanced disc operating system (DOS) executive. Such a system simplifies development and execution of user programs. Seldom-used subroutines may be stored on disc,

thus freeing core memory for other uses. A FORTRAN capability is included. All standard PDP-11 configurations compatible with the DOS may be used in the TP-5000 system.

1.3.6 Scope, Light Pen, and X-Y Plotter

Different experimenters require different displays. In the TP-5000 display control, Tennecomp Systems has provided features designed to satisfy most applications. The design provides high brightness, flicker-free display of a large number of points with low burden on the CPU. The display is normally continuously regenerated from data contained in memory. A storage scope capability is provided as an option, but it limits the display flexibility, particularly when a light pen is used.

An oscilloscope display with light pen is the primary "window" through which an experimenter obtains a feeling for his experiment and by which he exercises control of the experiment during its progress. The TP-5000 display is a general purpose computer display which has character and vector generation capabilities. Standard computer display features are augmented by a special digital logic organization which permits display of one-dimensional data and two-dimensional data with a rotatable isometric or contour presentation. Sixteen brightness levels, including 2 black levels, are provided. Regions for integration and printout can be selected with the light pen. Graphical data (for background subtraction) can be entered into the system by light pen "sketching". The X-Y plotter is a graphical option which can be used to output the scope display in hard copy form.

1.3.7 Teleprinter

A Teletype printer provides hard copy data output. The teleprinter keyboard is used by some TP-5000 programs for input of control information. A 165-character per second line printer may be used to augment the teleprinter and is particularly valuable for data dumps and for program preparation.

1.3.8 Functional Control Panel

The functional control panel allows control of the system through a centralized group of switches and lights labelled to match the operator's requirements.

This approach provides great flexibility. The positions of the switches are "read" by the program and interpreted as the user desires. For example, a pushbutton labelled "START" can enable an ADC, begin a real time and live time clock, and light a panel lamp to indicate that the ADC is in operation. Other switches may select appropriate data-taking or display modes. The functional control panel has no direct connection with any other peripheral module in the system. Its only link is by means of the CPU.

1.3.9 Cartridge Tape Unit

Some method must be provided for loading system programs into the memory. The Teletype paper tape reader may be used for this purpose in a minimal system, but use of paper tape is slow and awkward. The Tennecomp Systems TP-1371 Cartridge Tape Unit provides rapid program loading and dumping and retrieval of data. It also allows editing and assembling to be done directly from magnetic tape and offers an operating speed higher than that of a high speed paper tape reader/punch.

1.3.10 CAMAC Interfacing

Although the principal function of high speed digitizing and display can presently be served better by direct interfacing to the UNIBUS, many secondary tasks such as the interfacing of scalers and experiment control using low speed ADC's, DAC's, and control lines, can be efficiently handled by commercially available CAMAC modules. Tennecomp Systems can supply complete CAMAC subsystems or interfaces to existing CAMAC systems. The basic interface provides a CAMAC Branch Highway controller conforming to the EUR 4600e ESONE specification. Bidirectional data transfers of 8, 16, or 24 bits may be made between any CAMAC crate device and the PDP-11.

1.3.11 Other Peripherals

A major objective of the TP-5000 system is to provide a modular approach, with all modules connected to the PDP-11 UNIBUS in a standardized manner. This system design permits the user to add peripherals manufactured by Digital Equipment Corporation or independent peripheral manufacturers. The user may also make his own special modules using the logical building blocks supplied by DEC.

1.3.12 Software

Specific data analysis programs are described in the software section. Additional standard programs will be added periodically. Custom software is also available.

1.4 List of References

The following documents are required for the detailed maintenance and understanding of the TP-5000:

1. PDP-11 Unibus Interface Manual (DEC-11-HIAB-D).
2. DEC Logic Handbook, 1971 or 1972.
3. PDP-11 Paper Tape Software (DEC-11-GGPB-D).
4. Processor Handbook, PDP-11/20, PDP-11/15, PDP-11R20.

5. Peripherals and Interfacing Handbook, PDP-11
6. Tennelec PACE system
7. Operating and Service Manual for Hewlett-Packard 1300A - Publication No. 02608-2
8. Operating and Service Manual Modifications, Model 1300A/Option H86 - Hewlett-Packard

2.0 INSTALLATION

The TP-5000 has been designed to provide the user with an optimum system by providing a great deal of modularity and flexibility. This modularity and flexibility also lends itself to potential installation difficulties, since there are a greater number of places to connect cables incorrectly. History has continually shown that greater than 75% of start-up problems are associated with cables being in the wrong place, inverted or loose. A separate section has been provided to describe all cables, their location, and their orientation.

2.1 Power Requirements

The TP-5000 requires 20 amps of 115 ±10 VAC, 60 ±1 cycle, single phase. The cable and connector supplied with the system is rated at 20 amps. A safety ground is provided in the cable and must be connected to prevent accidental shocks.

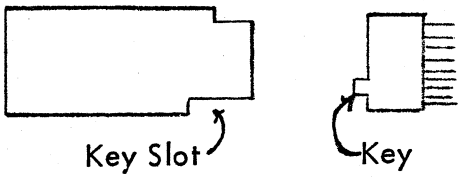
The input power is switched by a 30 amp circuit breaker which can be used as a power on/off switch. Both sides of the AC power lines are switched by this breaker.

2.2 Visual Inspection

It is a necessity to inspect a system visually after it has been moved and reinstalled. It is also wise to inspect the system periodically to catch potential problems.

2.2.1 Logic Cards

All logic cards should be seated firmly in their connectors. All cards are oriented the same direction, with the components coming off the right side, looking at the card side of the logic frame. The cards have a keying slot at the bottom which meshes with the key of the connector when properly inserted. A card that is upside-down will not fit flat in its connector. The holding force of the connector system is adequate to hold the cards reliably under normal circumstances. If the system is to be trucked, it is recommended that it be carried on its back, or that the cards be secured in some fashion.



2.2.2 Wire Wrap Pins

The rear door normally protects the wire wrap pins. If by chance the rear door is removed for servicing, extreme care should be taken to prevent damaging the pins. After servicing or installation, a visual check should be made of the wire wrap pins

to ascertain that none are shorted. The pins are reasonably soft and can usually be straightened with long-nose pliars. In the event a pin breaks off, it can be replaced individually.

2.2.3 Cables

Since cables are often heavy and stiff, they are logical candidates to give problems when a system is moved. When checking cables, check the following:

(1) The cable should be seated properly.

(2) The cable should not snag when the swing frame is opened and closed.

(3) The cables should not be pinched when the swing frame and doors are in their closed positions.

(4) The cables should be checked for wear at the point where there is motion or rubbing.

(5) The cables should not be resting upon logic cards since their weight might cause the card to come loose.

(6) Cables should not be allowed to come in contact with moving parts such as fans or motors.

2.2.4 Controls

Whenever the system has been moved, it is always wise to verify that all switches are in their correct positions.

(1) AC Power

The following switches control AC power to the system:

(a) Circuit breaker at the bottom front of the system.

(b) Looking inside the system rack from the rear at the left side, just below the display, there are two Weber power strips. Each strip has a Power On/Off switch that should be On.

(c) The Hewlett-Packard display has a power switch at the lower left front, or the Tektronix display has a pull "on" near the upper right hand corner of the display screen.

(d) The ADC system has a power switch on the front right mounting rail.

Since all subunits are connected to the Weber power strips and the Weber strips are plugges into the front circuit breaker, the entire system will come on with the circuit breaker if the switches in (b), (c), and (d) are in the ON position.

(2) Operational Controls

The following controls are in addition to the controls required to operate a specific program:

(a) PACE System

TC 501 - The Convert/Stop switch should be in the Convert position.

TC 520 - The Run/Stop switch should be in the Run position.

The Channel Mode switches should be set to their appropriate positions. The remaining switches on the PACE are dependent on the type of source and setup. The operator is referred to the Tennelec PACE system manual for the setup.

(b) Wilkenson ADC (Northern Scientific) Analyze/Stop in Analyze Coincidence/Anti-Coincidence position depends on desired mode.

(c) ADC Test Panel

All ADC simulation switches should be in the UP position, (on-line).

The appropriate patch plug must be inserted in the patch receptables.

(d) ADC Input Panel (Wilkenson)

Select desired mode for those parameters to be used. All other parameters switch to OFF position. Insert appropriate patch plug.

(e) ADC Input Panel (PACE)

Insert appropriate patch plug. "Run" output should be connected to appropriate gate inputs and busy outputs from PACE connected to busy inputs on ADC panel.

(f) Display

Intensity: The intensity control should be turned down (counter-clockwise) until the dot is not visible under ambient conditions.

Focus: When a display is present, the focus can be adjusted to the satisfaction of the operator.

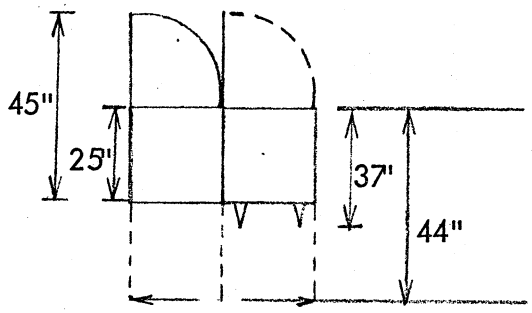
The selector at the rear of the display should be in the DC position.

The AC switch at the bottom rear should be in the 115 volt position.

2.3 Physical Mounting

2.3.1 The TP-5000 with a PDP-11 measures 72 inches high, 25 inches deep, and 41 inches wide. The CPU portion of the cabinet has stabilizing feet which extend an additional 12 inches in the front.

A top view illustrating the floor space occupied by the system and required for servicing is shown below:



2.3.2 Cooling

The TP-5000 is capable of operating reliably in an ambient environment of 0° to 50° C, provided the built-in fans are not blocked and the filters are kept properly cleaned. Cooling air enters at the base of the rack and exits at the top.

2.4 External Cables

All external cables for the TP-5000 terminate at the ADC.

2.5 Cables and Cable Routing

Those cables that have paddle connectors are to be oriented the same as the logic cards. The cable is attached to the component side (right side, looking from card end) and the long slot is at the bottom.

2.5.1 ADC Cable

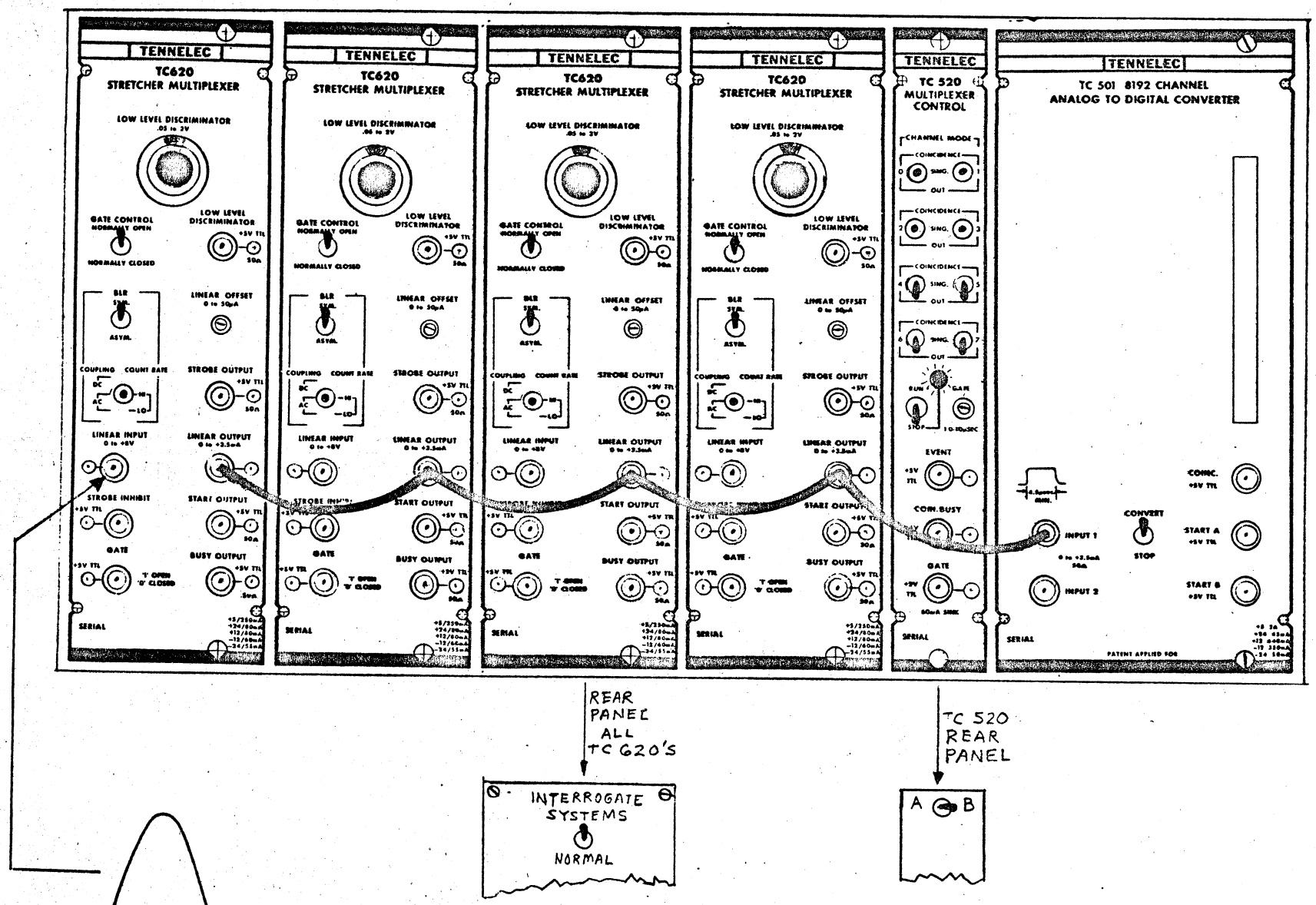
(a) PACE

This cable mounts at the upper left of the back of the PACE system. It is polarized and, therefore, cannot be mounted in the wrong direction. It is difficult to reach, however, and should be firmly seated with its retaining clips snapped into place. The other end of this cable mounts in the ADD-1 interface at card slot 1F1 and when the ADC input panel has been provided, the cable mounts in slot A1 of the control panel module.

(b) Wilkenson

Each Wilkenson ADC is provided with a cable that mates on the rear of the ADC and the other end terminates at a slot provided at the rear of the ADC input panel.

If only a single Wilkenson ADC has been provided, the input panel will be eliminated and the single cable will be mounted in slot 1F1 of the Add-One interface.



TENNELEC PACE SYSTEM

SINGLES OPERATION

Figure 2.5.1-1

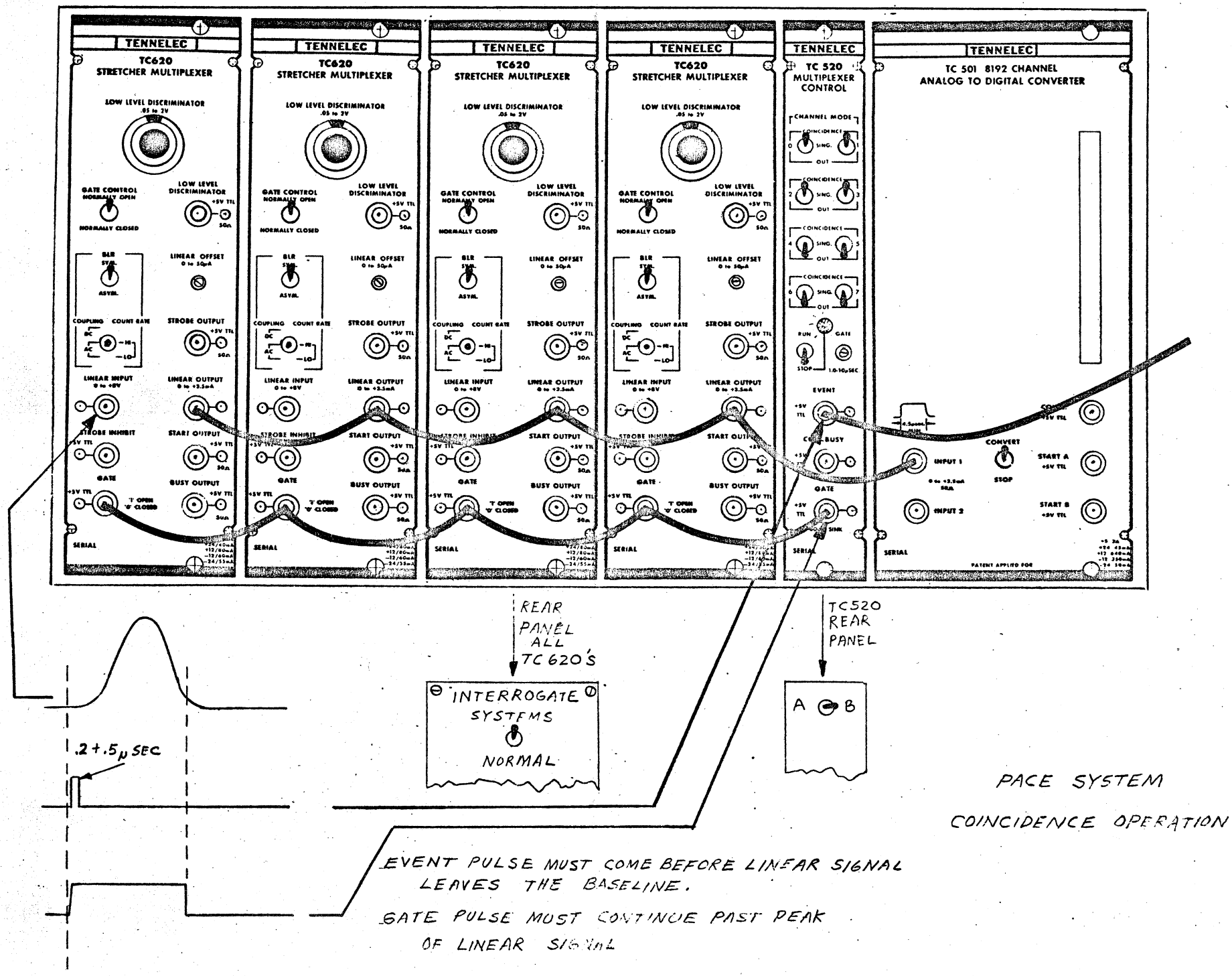

TENNELEC
TC620
STRETCHER MULTIPLEXER
LOW LEVEL DISCRIMINATOR
.05 to 2V
GATE CONTROL
NORMALLY OPEN
NORMALLY CLOSED
LOW LEVEL DISCRIMINATOR
+5V TTL
50Ω
BLR
SYM.
ASYM.
LINEAR OFFSET
0 to 50μA
COUPLING
DC
AC
COUNT RATE
IN
LO
STROBE OUTPUT
LINEAR INPUT
0 to +8V
LINEAR OUTPUT
0 to +2.5mA
STROBE INHIBIT
START OUTPUT
GATE
BUSY OUTPUT
'1' OPEN
'0' CLOSED
SERIAL
TC 520
MULTIPLEXER
CONTROL
CHANNEL MODE
COINCIDENCE
SING.
OUT
RUN
STOP
GATE
1.0-10μSEC
EVENT
BUSY
SINK
TC 501 8192 CHANNEL
ANALOG TO DIGITAL CONVERTER
INPUT 1
INPUT 2
CONVERT
START A
START B
PATENT APPLIED FOR
REAR
PANEL
ALL
TC 620's
INTERROGATE
SYSTEMS
NORMAL
TC520
REAR
PANEL
A
B
.2 + .5μ SEC
EVENT PULSE MUST COME BEFORE LINEAR SIGNAL
LEAVES THE BASELINE.
GATE PULSE MUST CONTINUE PAST PEAK
OF LINEAR SIGNAL
PACE SYSTEM
COINCIDENCE OPERATION

Figure 2.5.1-2

2.5.2 Live Time Clock

The Live Time Clock cable has 5 coax cables terminated at one end with BNC coaxial connectors; at the other end, it is terminated with a Paddle connector. The BNC connectors are attached to the back side of the input panel at those feedthroughs closest to the appropriate Busy outputs. Each cable is a different length; and if the lengths are attached in logical order, the appropriate Busy will be connected correctly to the Live Time Clock Interface. The other end of the cable is plugged into connector slot 1C4 of the Live Time Clock interface.

2.5.3 ADC Input Panel

The ADC Input Panel will have the ADC cables mentioned in paragraph 2.5.2. In addition, there will be a cable coming from the live time clock, a cable going to the ADC interface; and for the Wilkenson system, a cable going to Coincident Control Module.

2.5.4 Functional Control Panel

The Functional Control Panel has a double flat ribbon cable that originates on the control panel interface card in the Control Panel Interface slots 1C1 and 1D1, and terminates at the Functional Control Panel in slot A7.

2.5.5 Display

There are three coax cables between the display interface and the display. The cables are permanently attached at the interface and are connected via BNC connectors at the display. The cables are cut to length, so there should not be any difficulty in keeping the cables attached to the appropriate connector. The X deflection originates in the display interface at 3B4S1; the Y deflection originates at 1D1U1; and the Z deflection originates at 3C2B1.

2.5.6 Light Pen

The light pen is connected with a flat ribbon cable that mounts in the slot at the rear of the light pen chassis and connects to slot 3A4 in the display interface.

3.0 SOFTWARE

3.1 Introduction

This section describes the operation of the standard system software. Descriptions are included for the paper tape input/output versions of the TP-5001 (one-parameter), TP-5002 (two-parameter), and TP-5003 (Multiple region of interest) programs. Any modifications to a particular program are noted following the main description. Such modifications might include drivers for specific peripheral devices.

3.2 TP-5001 SPECTRUM STRIPPING PROGRAM

The Tennecomp Systems TP-5001 Spectrum Stripping Program is a basic data acquisition and analysis program for single parameter nuclear pulse-height applications. Real or live time data may be acquired. Displays are available in full, overlay, or expanded display modes. Movable cursors are provided to define regions for analysis, output, or expanded displays. Data may be stored and retrieved via paper tape with listing of desired regions of interest on the teleprinter. Operator interaction and system control are provided through the functional control panel and the light pen. The Tennecomp Systems TP-5001 program is specifically designed for complex spectrum stripping by means of light pen sketching.

3.2.1 Data Acquisition: The TP-5001 Spectrum Stripping Program acquires data from the ADC system. Provisions are made for storing 8192 channels of data with the maximum count per channel of 1,048,575. Data count overflows result in termination of the data acquisition. The program allows the operator to specify the data channel origin in increments of 256 channels with the length of the data segment selectable by patch panels. Timing of data acquisition may be controlled by the system real time clock or by individual live time clocks for each input. When data-taking is terminated, the live time expired for each input will be printed, along with the actual real time elapsed. The time unit for real and live time counting is 0.1 second.

3.2.2 Display Modes: The display of data is independent of the data acquisition. Data for display may be selected from any 256, 512, 1024, 2048, or 4096-channel subgroup of the data field beginning at multiples of 256 channels. The number of channels selected is variable from 256 channels to 4096 channels in increments of 256 channels. Any subgroup of the data field may be overlaid on any other subgroup of equal length. The contents of the overlaid subgroup of data channels may be added to or subtracted from the contents of the other subgroup of data channels. Any region of the data field may be expanded for further study or any 128-channel region selected as the region of interest for spectrum stripping. The TP-5001 program display is operational only when the MAIN TRACE toggle switch is set. Therefore, the MAIN TRACE toggle switch should remain in the ON position, except for the selection of new origin and length parameters.

a. Main Trace Mode: When the MAIN TRACE toggle switch is in the ON position, and the EXPAND, OVERLAY, and STRIP toggle switches are in the OFF position, the data channels specified by the origin and length settings are displayed. The origin and length parameters are selected, and the MAIN TRACE toggle switch is reset.

b. Overlay Mode: When the MAIN TRACE and OVERLAY toggle switches are in the ON position, and the EXPAND and STRIP toggle switches are in the OFF position, the MAIN TRACE display is overlaid with the data channels specified by the current origin and MAIN TRACE length settings. The contents of the OVERLAY data channels may be added to or subtracted from the contents of the MAIN TRACE data channels with the ADD or SUBTRACT pushbuttons. The result of the addition or subtraction is stored in the MAIN TRACE data channels.

c. Expand Mode: When the MAIN TRACE and EXPAND toggle switches are in the ON position and the OVERLAY and STRIP toggle switches are in the OFF position, the region defined by the lower and upper cursors in the MAIN TRACE display is expanded. If the OVERLAY toggle switch is in the ON position, the MAIN TRACE expanded display is overlaid with the corresponding channels of the OVERLAY display. The two vertical cursors provided in the EXPAND display mode may be positioned to mark a region of interest independent of the region specified in the MAIN TRACE display.

d. Strip Mode: When the MAIN TRACE and STRIP toggle switches are in the ON position, the 128-channel region of interest beginning with the channel specified by the lower cursor in the MAIN TRACE display is displayed as the FOREGROUND curve. The BACKGROUND curve is initially set equal to the FOREGROUND curve. The DIFFERENCE curve is automatically calculated to be the difference between the FOREGROUND and BACKGROUND curves (zero if BACKGROUND is greater than the FOREGROUND). The tracking cross may be moved by pointing the light pen at the cross and dragging it around the screen. The tracking cross will jump to the FOREGROUND curve when the light pen is pointed to the curve. The path of the tracking cross is entered into the BACKGROUND curve when the pressure-sensitive light pen tip is pressed against the screen. The data curves are displayed from separate buffer regions in memory so that spectrum stripping operations do not modify the channel contents in the data field. The buffer regions are reinitialized when the STRIP toggle switch is reset.

The control dots on the right of the screen perform the following functions when the light pen is pointed to them:

C AND A	Prints out the centroid (to the nearest 0.1 channel) and the area of the DIFFERENCE curve.
F ON	The FOREGROUND curve is displayed.
F OFF	The FOREGROUND curve is not displayed.
B ON	The BACKGROUND curve is displayed.
B OFF	The BACKGROUND Curve is not displayed.
D ON	The DIFFERENCE curve is displayed.
D OFF	The DIFFERENCE curve is not displayed.
B=0 RIGHT	The BACKGROUND curve is zeroed to the right of the tracking cross.
B=0 LEFT	The BACKGROUND curve is set equal to the DIFFERENCE curve.

B=D	The BACKGROUND and DIFFERENCE curves are exchanged.
F=B	The FOREGROUND curve is set equal to the BACKGROUND curve.
B=F	The BACKGROUND curve is set equal to the FOREGROUND curve.

A method of analysis of a spectrum shall be as follows:

Upon initialization, a region of interest is brought into the FOREGROUND curve, and the same data is transferred to the BACKGROUND curve. The difference shown by the DIFFERENCE curve is then zero. The background of a peak is sketched in by hand with the light pen into the BACKGROUND curve. The DIFFERENCE curve then contains a single peak. The area and centroid of the DIFFERENCE curve is then calculated and output by pointing the light pen at the top control dot on the right of the display screen. Now the BACKGROUND curve contains the original spectrum with the analyzed peak subtracted. In preparation for the analysis of the next peak, the BACKGROUND curve is transferred to the FOREGROUND curve by pointing the light pen at the second control dot from the bottom on the right of the display screen. The difference shown by the DIFFERENCE curve is again zero. As before, the background of the second peak is sketched into the BACKGROUND curve with the light pen and analysis proceeds as before until all peaks have been analyzed.

3.2.3 Functional Control Panel Description: Operator interaction and system control are provided through the functional control panel and light pen. With the exception of the file identification for optional Disc, DECtape, or Magtape handlers, all input parameters are entered from the functional control panel or indicated with the light pen by means of moveable vertical cursors, control dots, or sketching. A detailed description of the functional control panel labels follows.

PUSHBUTTONS:

(0) START ADC: Enables the ADC system to acquire data with each ADC input storing data in the prespecified data region. The real or live time count time is specified by the left bank of decimal entry (thumbwheel) switches in 0.1 second increments. In the case of live time counting, data acquisition will be terminated when any ADC input has timed out, when the STOP function is requested, or when any channel overflows (exceeds 1,048,575 counts).

(1) SET ORIGIN: Specifies the data origin for the ADC input specified by thumbwheel switch 9. The ADC inputs are numbered 0 through 2. The data origin is calculated as being the sum of the ORIGIN rotary switch setting and the settings of the 2048/0 and 4096/0 toggle switches. Thus, any ADC input can have its origin set to any 256-channel subgroup in the 8192 channels available for data acquisition.

(2) INTEGRATE: Sums and prints the number of counts contained in the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND displays. The output format for the printout consists of the lower cursor channel number, the upper cursor channel number, and the integrated number of counts.

(3) PRINT: Prints the contents of the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND displays onto the printout device (normally the teleprinter). The output format consists of a channel number followed by eight channel contents.

(4) EXECUTE: Executes the function specified by the EXECUTE rotary switch when pressed. If conflicting functions are requested, the most recent function is ignored, except in the case of the STOP command.

(5) ADD: Adds the contents of the channels specified by the OVERLAY display to the contents of the corresponding channels specified by the MAIN TRACE display.

(6) SUBTRACT: Subtracts the contents of the channels specified by the OVERLAY display from the corresponding channels specified by the MAIN TRACE display. If any subtraction results in a negative value, a zero will be stored in the channel.

(7) ZERO: Zeros the contents of the channels specified by the MAIN TRACE display.

ROTARY SWITCHES:

(0) EXECUTE: Selects the function to be executed when the EXECUTE pushbutton is pressed.

STOP disables the ADC system and clocks. The live time expired for each ADC input is printed along with the total real time on the teleprinter.

PUNCHA, PUNCHB, AND READB refer to the paper tape system and are described in a later section.

(1) ORIGIN: In conjunction with toggle switches 1 and 2, specifies the channel origin for the MAIN TRACE and OVERLAY displays. When the SET ORIGIN pushbuttons is pressed, the current setting of the ORIGIN rotary switch in conjunction with toggle switches 1 and 2 are used to set the channel origin for data acquisition. The number of channels specified by this switch is added to the settings of toggle switches 1 (0 or 2048) and 2 (0 or 4096).

(2) LENGTH: Selects the number of channels to be displayed for the MAIN TRACE and OVERLAY displays.

(3) SCALE: Selects the number of counts full scale for the MAIN TRACE, OVERLAY, EXPAND, and STRIP displays.

TOGGLE SWITCHES:

(0) REAL/LIVE: Selects either the real time clock or the live time clocks for timing of data acquisition when the START ADC pushbutton is pressed. Thumbwheel switches 0 - 4 determine the length of time for data acquisition, real or live time.

(1) 2048/0: In conjunction with rotary switch 1, specifies the channel origin for the MAIN TRACE or OVERLAY displays, as well as the data origin for the ADC input specified by thumbwheel switch 9 when the SET ORIGIN pushbutton is pressed. The number of channels specified by rotary switch 1 is added to the toggle switch setting to obtain the actual channel origin.

(2) 4096/0: Identical to (1) in function.

(3) NOT USED.

(4) MAIN TRACE ON/OFF: Initiates the display of data channels specified by the origin setting and the LENGTH switch (rotary switch 2). The origin and length settings for the MAIN TRACE display remain fixed until the toggle switch is reset.

(5) OVERLAY ON/OFF: Overlays the MAIN TRACE display with the data channels specified by the current origin setting and the MAIN TRACE length setting.

(6) EXPAND ON/OFF: Expands the region marked by the lower and upper vertical cursors in the MAIN TRACE display. If the OVERLAY display toggle switch is ON, the OVERLAY display will also be expanded.

(7) STRIP ON/OFF: Enters the spectrum stripping mode with the 128-channel region beginning with the channel marked by the lower cursor in the MAIN TRACE display. The spectrum stripping display is initialized each time the toggle switch is reset.

DECIMAL THUMBWHEEL SWITCHES:

(0-4) ADC TIME: Specifies the real or live time count time for the ADC system. Data acquisition will begin when the START ADC pushbutton is depressed and will continue until either the STOP function is selected, a channel overflows, the real time has elapsed, or in the case of live time counting, when any ADC input has timed out.

(5-8) NOT USED.

(9) ADC INPUT SELECT: Selects the ADC input for which the channel origin is to be set when the SET ORIGIN pushbutton is pressed. Only the selection of inputs 0 through 2 is valid.

STATUS LAMPS:

(0) LIVE: Indicates data acquisition in live time.

(1) REAL: Indicates data acquisition in real time.

(2-6) NOT USED.

3.2.4 Paper Tape System: Functions are provided for the output of data onto paper tape in binary and ASCII formats. Data may be input from paper tape in binary format only.

The following functions are available for paper tape input and output:

PUNCHA — Outputs the contents of the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND display modes onto paper tape in ASCII format. The paper tape data format is the same as the printed data format produced by the PRINT pushbutton.

PUNCHB — Outputs the contents of the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND display modes onto paper tape in binary format. The paper tape data format consists of the initial channel number, the number of channels, the HI channel data (most significant 8 bits), the LO channel data (least significant 16 bits), and checksum. The punched checksum is the 8 least significant bits of the sum of all data characters punched.

READB — Reads binary format paper tape produced by the PUNCHB function. An error message is printed if data is read incorrectly or if no paper tape is in the reader. Data is read into the same region of interest specified when the binary tape was punched.

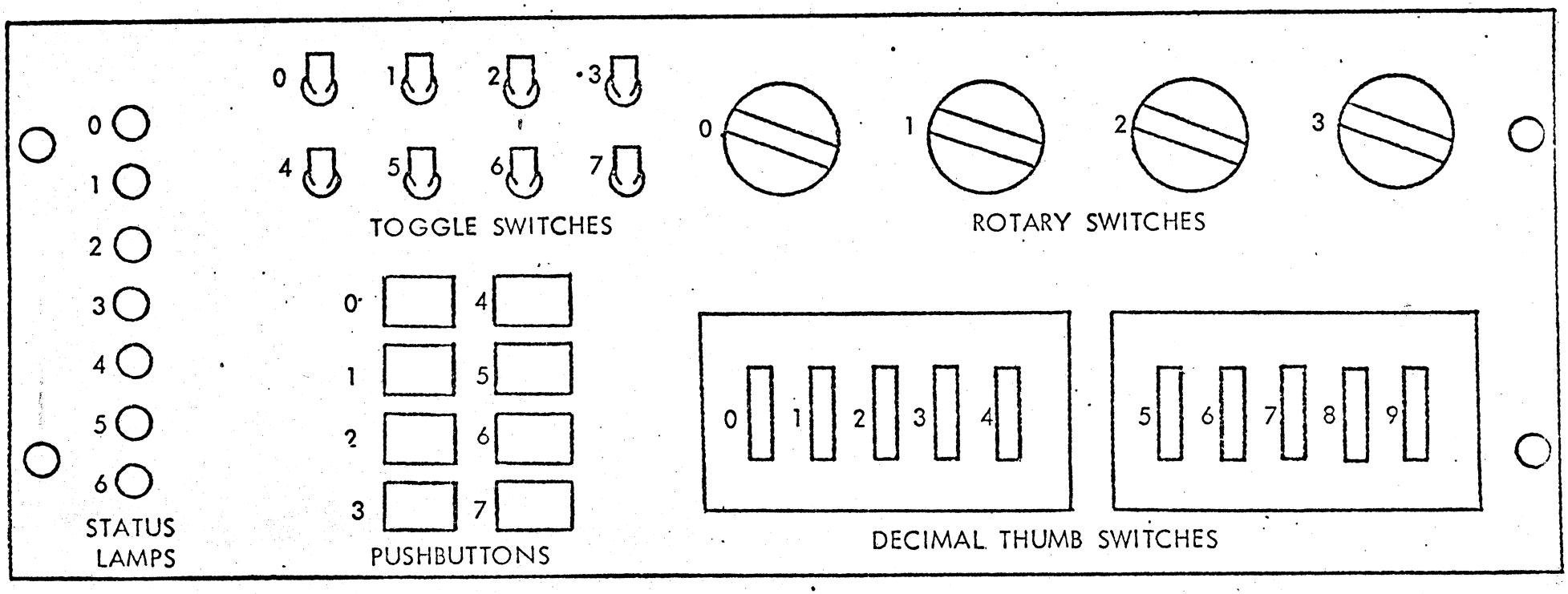


Figure 1.

TP-5347 Functional Control Panel

DECIMAL THUMB SWITCHES:

(0-4) ADC 1 TIME: Specifies the real-time or live-time count time for ADC 1.

(5-9) ADC 2 TIME: Specifies the real-time or live-time count time for ADC 2.

(3) SCALE: Selects the number of counts full scale for the MAIN TRACE, OVERLAY, and EXPAND displays.

STATUS LAMPS:

(0-2) NOT USED.

(3) ADC1 LIVE: On during ADC 1 live-time data acquisition.

(4) ADC1 REAL: On during ADC 1 real-time data acquisition.

(5) ADC2 LIVE: On during ADC 2 live-time data acquisition.

(6) ADC2 REAL: On during ADC 2 real-time data acquisition.

TOGGLE SWITCHES:

(0) REAL/LIVE: Selects either the real-time clock or live-time clocks for timing of data acquisition.

(1) 2048/0: In conjunction with rotary switch 1, specifies the channel origin for the MAIN TRACE and OVERLAY displays. The number of channels specified by rotary switch 1 is added to the toggle switch setting to obtain the display origin.

(2) 4096/0 Identical in function to (1).

(3) NOT USED.

(4) MAIN TRACE ON/OFF: Initiates the display of data channels specified by the origin setting and the LENGTH switch (rotary switch 2). The origin and length settings for the MAIN TRACE display remain fixed until the toggle switch is reset.

(5) OVERLAY ON/OFF: Overlays the MAIN TRACE display with the data channels specified by the current origin setting and the MAIN TRACE length setting.

(6) EXPAND ON/OFF: Expands the region marked by the lower and upper cursors in the MAIN TRACE display.

(7) BASELINE ON or OFF: Initiates the display of a straight line between the intersections of the two vertical cursors with the data curve. The baseline display is operative only in the EXPAND display mode.

ROTARY SWITCHES:

(0) EXECUTE: Selects the function to be executed when the EXECUTE pushbutton (pushbutton 4) is pressed.

STOP disables the ADC's and clocks. The time expired for each ADC is printed on the teleprinter.

CALIB performs a conversion gain and zero offset calculation based on two known energy peaks.

PUNCHA, PUNCHB, and READB refer to the paper tape system and are described in a later section.

(1) ORIGIN: In conjunction with toggle switch 1, specifies the channel origin for the MAIN TRACE and OVERLAY displays. The number of channels specified by this switch is added to the setting of toggle switch 1 to obtain the display origin.

(2) PEAK (LENGTH): Specifies the peak reference number assigned to the region of interest displayed when the SET PEAK pushbutton (pushbutton 6) is pressed. In automatic analysis, specifies the number of preset regions of interest to be analyzed.

Selects the number of channels to be displayed for the MAIN TRACE and OVERLAY displays.

3.5.6 Paper Tape System:

Functions are provided for the output of data onto paper tape in binary and ASCII formats. Data may be input from paper tape in binary format only.

The following functions are available for paper tape input and output:

PUNCHA — Outputs the contents of the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND display modes onto paper tape in ASCII format. The paper tape data format is the same as the printed data format produced by the PRINT pushbutton.

PUNCHB — Outputs the contents of the region of interest marked by the two vertical cursors in the MAIN TRACE or EXPAND display modes onto paper tape in binary format. The paper tape data format consists of the initial channel number, the number of channels, the HI channel data (most significant 8 bits), the LO channel data (least significant 16 bits), and checksum. The punched checksum is the 8 least significant bits of the sum of all data characters punched.

READB — Reads binary format paper tape produced by the PUNCHB function. An error message is printed if data is read incorrectly or if no paper tape is in the reader. Data is read into the same region of interest specified when the binary tape was punched.

3.6 Hybrid Computer Control and Ultrafast Processing Software (HYCCUPS) System.

3.6.1 THE PROBLEM

The problem is that typical PHA system users are chemists or physicists who wish to use their time for chemistry or physics rather than for computer science. Such a user requires a system which can be used without expending a great deal of effort on program development and which does not require sophisticated programmers. In the past, it has become painfully apparent to users that the programming expense on a computer PHA system (with a modest hardware cost of, say, $40,000) has been two or three man-years over the first 5 years of usage. The programming expense can easily be greater than the cost of the hardware, to say nothing of the time lost from physics or chemistry projects.

3.6.2 PREVIOUS SOLUTIONS

(a) The use of high level languages (such as FORTRAN) which reduce the program preparation effort. This has been successful on larger (>$200,000) systems, but the use of FORTRAN on smaller systems has run into problems. As commonly implemented by the manufacturer of the computer, the FORTRAN language gobbles up memory. Furthermore, a very complex operating system is required which requires complex system interaction with supporting peripherals when assembling, loading, and on input/output. Thus, the FORTRAN programmer is not freed from complex programming, but must deal with sophisticated interactions between software components.

(b) The use of an interpretive language (such as BASIC or FOCAL) which is oriented toward "hands-on" program development and debugging. This does succeed in reducing programming time by an order of magnitude; however, it is too slow for real time PHA device interaction. Even a simple task such as clearing a 4096 channel spectrum requires about 40 seconds, compared with .2 second for FORTRAN or .1 second for hand-coded machine language.

(c) Purchase a set of "canned" application programs which are used with no modification or with only minor modifications. This effectively destroys inherent system flexibility.

(d) Obtain the services of a programmer solely dedicated to the operation of the system.

3.6.3 POSSIBILITIES

(a) Extend the capabilities of the manufacturer-supplied FORTRAN so that real time interaction and device control is possible within the FORTRAN framework without the use of a complex operating system.

(b) Extend the capabilities of the interpretive language by speeding up execution and/or by providing efficiently-coded non-interpretive subroutines.

(c) Provide a dual task foreground/background mode whereby the real time device control is done in efficient coding, while the detailed analysis portion of the task is done in a simpler language.

Since its inception in 1967, Tennecomp Systems has specialized in custom PHA systems for physics and chemistry. Our users generally have sophisticated requirements which cannot be met by standard commercial systems. In the course of development of systems based upon PDP-8's, PDP-9's, PDP-15's and PDP-11's, we produced systems which used all of the above possibilities and gained extensive experience in their actual field use. We closely observed the way the users interacted with the systems.

3.6.4 THE SOLUTION

Although several manufacturers have implemented some of the above possibilities, Tennecomp Systems has optimized, by a process of evolution, a balanced programming system to provide maximum versatility for PHA applications with minimum programming effort. The solution is HYCCUPS - its key features are:

(a) Division of the programming into two separate tasks - an ultrafast foreground task and an interactive background task.

(b) The foreground task is programmed in a subset of FORTRAN called FORTRAN-m. All device handlers and executive functions can be programmed in FORTRAN-m. There is no necessity for sophisticated assembly language coding or for complex operating systems.

(c) The background task is programmed in FOCAL-11, an elementary interpretive language conceived by Rick Merrill and offered by Digital Equipment Corporation.

(d) There is a complete logical separation between the foreground and background tasks. The exclusive Tennecomp Systems Functional Control Panel is used to control the foreground task. Thus, one may be acquiring and displaying data by means of the foreground "control panel" oriented FORTRAN-m program while running an independent FOCAL-11 program simultaneously. The organization of the TP-5000 requires only a small amount of central processor attention to the PHA functions. FOCAL-11 is interrupted for a few microseconds when the CPU is required to service the foreground program.

(e) HYCCUPS is optimized for modest-sized systems (approx. $40,000) and for PHA applications, where every dollar of price must count. The FOCAL portion requires 6 to 8 thousand words of core memory, but the resulting saving in programming time more than compensates for the cost of the additional memory.

3.6.5 THE ADVANTAGES

The HYCCUPS system offers a variety of levels of interaction:

(a) On the simplest level, the conventional PHA functions of Start, Clear, Set Live or Real Time, Display, etc., can be controlled from the Functional Control Panel exactly like a conventional hard-wired PHA system.

(b) On the next level of sophistication, the user may utilize a FOCAL applications program which activates the control panel functions by means of simple statements which have been added to the FOCAL commands. FOCAL may recognize a number of commands such as "ANALYZE", "START", "SCAN", "AUTO", etc., and branch to a section which carries on a dialogue with the operator.

(c) At the next level of sophistication, FOCAL may interact with FORTRAN-m coded routines. For example, a FORTRAN-m routine may be used by the foreground task to qualify coincident events for writing on magnetic tape. A simple FOCAL program allows the qualification "restriction bounds", to be altered from the teletype while observing the effect on the display.

(d) At the final level of sophistication, the user can write additional modules in assembly language and can couple these to the foreground or background tasks.

Thus, HYCCUPS puts the entire system resources at the disposal of the user in incremental stages without requiring that he master complex programming conventions before he can get started.

3.7 Extensions to DEC FOCAL

FOCAL-HYC is the name given to the extensions to DEC's FOCAL-11 language.

The standard FOCAL-11 features include the following elements:

Sample Commands	Description
ASK X,Y,Z	User types a value for each variable.
COMMENT	Lines beginning with C ignored.
DO 2.1	Execute line 2.1; return to next line.
ERASE 2.1	Erase line 2.1.
MODIFY 2.1	Edit any character on line.
FOR i=x,y,z	Do next command for i=x to z in steps of y.
GOTO 3.4	Starts stored program at line 3.4.
IF (X) L1,L2,L3	If X≤0, go to L1; if X=0, go to L2;
IF (X) L1,L2	if X≥0, go to L3; otherwise, go to
IF (X) L1	next command.
QUIT	Returns control to the user.
RETURN	Terminates DO subroutines.
SET X=1+2	Defines X and assigns the value 3.
TYPE A+1	Evaluates the expression & types its value.
WRITE	Types out the stored program text.
X FSTP(N)	Executes function.
SET Z = FSTP(N)	Executes function and assigns result to Z.

Standard Functions	Description
FSQT( )	Square Root
FABS( )	Absolute Value
FSGN( )	Sign Part of Expression
FITR( )	Integer Part of Expression
FEXP( )	Natural Base to Power
FLOG( )	Natural Log
FSBR(4.0,X)	One arg user defined subroutine.
FX(1,A)	Returns data from UNIBUS octal address A.
FX(0,A,M)	Returns with the bit by bit logical product (AND) at Unibus octal address A and the bits of M.
FX(-1,A,D)	Puts D into Unibus octal address A.

Standard I/O	
OPERATE P	Selects High Speed Punch.
OPERATE R	Selects High Speed Reader.
OPERATE T	Selects Teletype printer/punch.
OPERATE K	Selects Teletype Keyboard/reader.
OPERATE L	Selects Line Printer.

The new functions added to make up FOCAL-HYC are:

Function	Description
FADC(N,T)	Enables ADC No. N for T seconds live time.
FSTP(N)	Disables ADC No. N and returns elapsed time.
FTIM(N)	Returns elapsed time only.
FPSH(N)	Returns non-zero value if panel button N is pushed.
FRSW(N)	Returns position of rotary switch N on panel.
FZER(LOW,HI)	Zeroes data channel contents from LOW to HI.
FCUR(N)	Returns position of upper or lower cursor.
FCUR(N,I)	Sets upper or lower cursor to channel I.
FMAC(CHAN)	Returns contents of CHAN.
FMAC(CHAN,DATA)	Stores Data in CHAN.
FPPL(C,S,X,Y)	Point plotting function.
FNORM(LO1,HI1, LO2,HI2,A,B)	Multiply spectrum #1 by B, add A, and put in spectrum #2.
FSUM(LO,HI)	Integrate from channel LOW to HI.
FSMO(LO,HI)	Smooths from channel LO to HI.
FUNS(LO,HI)	Un-smooths from channel LO to HI.
FORG(N,P)	Sets origin for ADC No. N to 128P.

Commands	Description
OPERATE C	Selects Display Scope Numeric
LIBRARY	Allows input or output of programs and data.

3.8 FOCAL-HYC Library Input/Output

The FOCAL-HYC Library commands allow the user to create and recall named files containing programs or data. The files use ASCII data mode and are consistent with the PDP-11 DOS conventions. They can be manipulated by such programs as PIP and EDITOR.

Command	Description
*LIBRARY OPEN NAME	Initializes file NAME for output on the mass storage device.
*LIBRARY WRITE 4.1	Causes line 4.1 to be added to file.
4.0	Causes group 4 to be added to file.
ALL	Entire indirect program added to file.
*LIBRARY CLOSE	Completes file output and enters file name into library mass storage device directory.
*LIBRARY KILL	Allows "LIBRARY" mode to be left without finishing and closing the file.
*LIBRARY IN NAME	Searches for file NAME. Inputs file as FOCAL text until end-of-file is encountered.
*LIBRARY STORE NAME	Causes output from all TYPE commands to be written into the data file until the file is closed by a LIBRARY CLOSE command. The exclamation point (!) must appear in the TYPE command before information is transferred to the output buffer.
*LIBRARY ASK NAME	Opens the file NAME for input. All ask commands will cause data to be read from the file until the file is closed by a LIBRARY CLOSE command. The data for each ASK statement must be terminated by a "!".
*LIBRARY DELETE NAME	Selectively deletes FOCAL created files from library storage device.
*LIBRARY LIST	Lists names of all FOCAL files on library storage device.

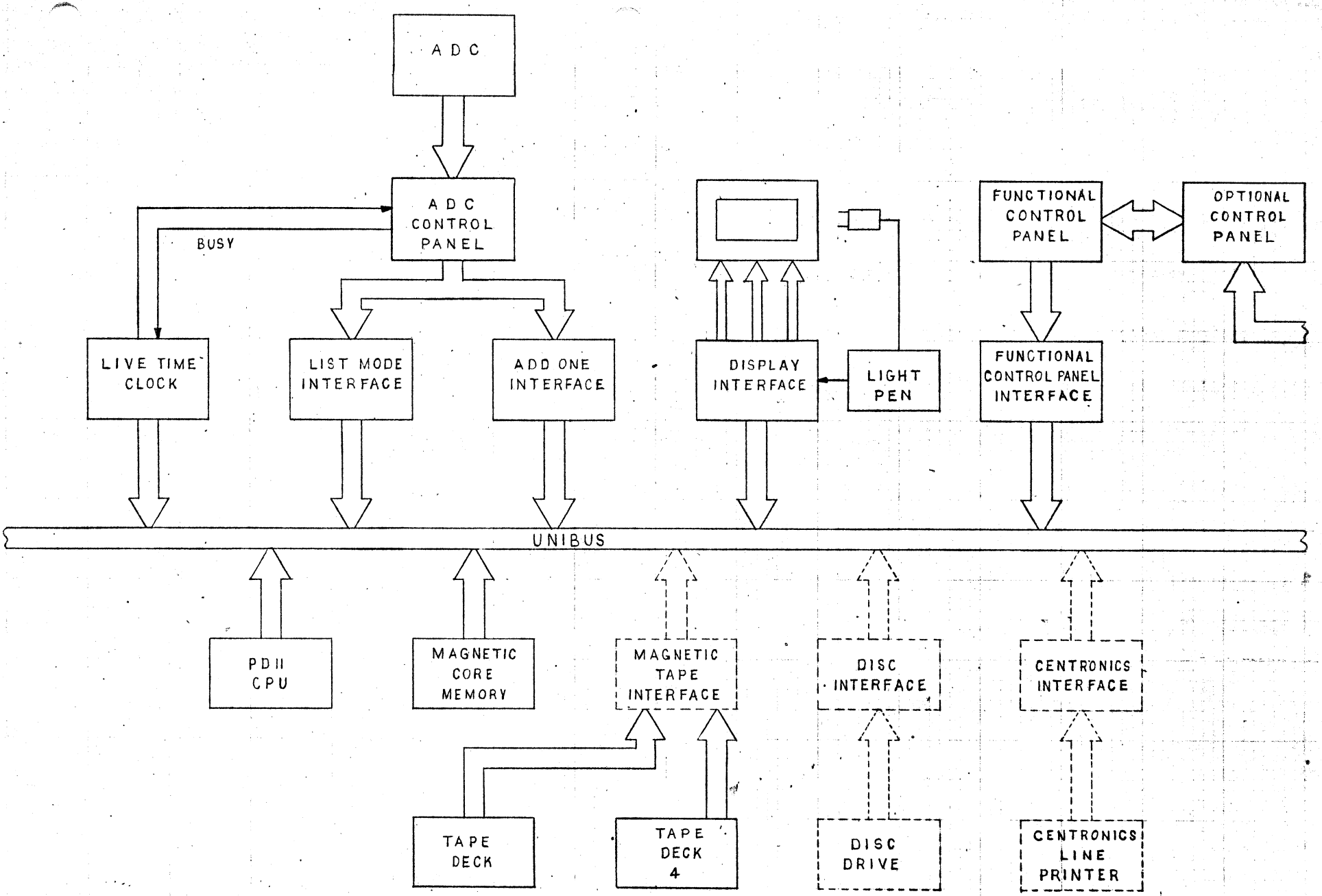

ADC
ADC CONTROL PANEL
BUSY
LIVE TIME CLOCK
LIST MODE INTERFACE
ADD ONE INTERFACE
DISPLAY INTERFACE
LIGHT PEN
FUNCTIONAL CONTROL PANEL
OPTIONAL CONTROL PANEL
FUNCTIONAL CONTROL PANEL INTERFACE
UNIBUS
PDII CPU
MAGNETIC CORE MEMORY
MAGNETIC TAPE INTERFACE
DISC INTERFACE
CENTRONICS INTERFACE
TAPE DECK
TAPE DECK 4
DISC DRIVE
CENTRONICS LINE PRINTER

FIG. 4.1-1.

4.0 THEORY OF OPERATION

4.1 System

4.1.1 Overall Interaction

This section contains descriptive information to aid in the understanding and maintenance of the TP-5000. Since the system is essentially a collection of specially designed peripherals, the descriptive discussion treats each peripheral separately. The basic ingredient that brings these peripherals together as a working system is the system software. This method provides the user with sophistication and flexibility not possible with a hardware-controlled system.

Section 3 discusses the operating procedures and, as such, provides the best understanding of the system working as a whole.

Figure 4.1-1 illustrates the basic data flow in the TP-5000 system. The display can be initialized and thus will pull data directly from memory without additional intervention of the CPU.
Also, the ADC can be initialized and will transfer data to the memory without CPU intervention. The Live Time Clocks are gated counters which are normally controlled by the "Busy" outputs of the stretchers and supply an interrupt to the CPU after program-selected number of counts have been accumulated. Since there can be up to 8 clock inputs, the CPU must read the clock flags whenever an interrupt occurs to determine which clock has caused the interrupt.

The Functional Control Panel can be examined by the software to determine which, if any, switch has been activated and can light any or all indicators. Actuation of the pushbutton switches will cause an interrupt.

4.1.2 Logic Drawing Standards

Tennecomp Systems has adopted a variation of MIL Standard 806B as its logic drawing standard in an effort to make troubleshooting of Tennecomp equipment as convenient as possible. This standard is reproduced here and should be reviewed before using the supplied logic drawings.

4.1.2.1 General

4.1.2.1.1 Purpose

This standard establishes minimum requirements for the preparation of logic drawings generated by Tennecomp Systems, Inc. Adherence to these standards enhances the interchange of information contained on the engineer's drawings.

4.1.2.2 Formal Drawing Format

4.1.2.2.1 Drawing Size

Logic designs will be drawn on standard Tennecomp title block, "C" size (12 x 22) drawing paper. The designer will leave a minimum $\frac{1}{2}$ inch clearance between any notation and the printed border.

4.1.2.2.2 Standard Reserved Areas

Notations will be located in the lower left corner of the drawing.

4.1.2.2.3 Titles

The title should be descriptive of the function contained on the logic drawing and does not need to define the drawing as a logic drawing.

4.1.2.2.4 Numbering

Multiple sheets that contain contiguous logic information can have the same drawing number. Each sheet must contain the drawing number and the sheet number.

4.1.2.3 Logic Symbols

It is the intention of this standard to adhere to MIL-STD-806B wherever practicable.

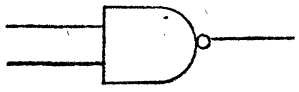
4.1.2.3.1 Symbol Size

Symbols will be drawn with the half-size MIL-STD-806 Logic Symbol Template.

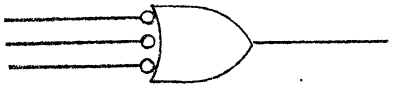
4.1.2.3.2 Symbol Definitions (for TTL Logic)

Tennecomp TTL logic is defined as high true logic. The basic design element is, by this definition, classified as a NAND gate. Logic interpretations for "AND" and "OR" logic are shown in the following figures. In

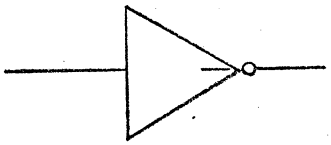
general, the logic notations supplied by Texas Instruments adhere closely to 806B standards and can be used as a reference.



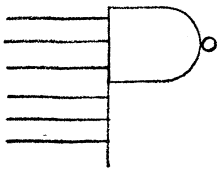
AND



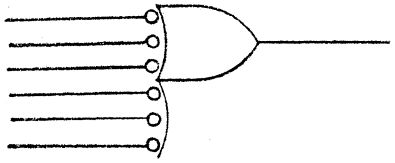
OR



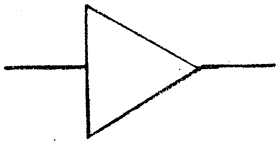
INVERTER



6 INPUT AND

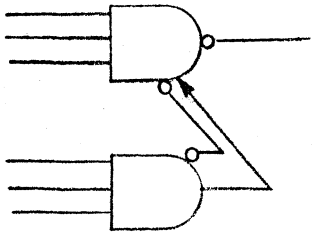


6 INPUT OR



BUFFER

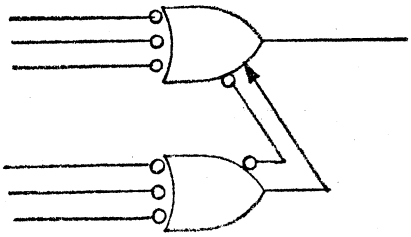
EXPANDABLE



EXPANDER

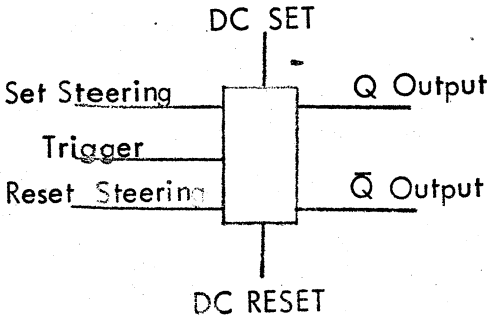
EXPANDED AND

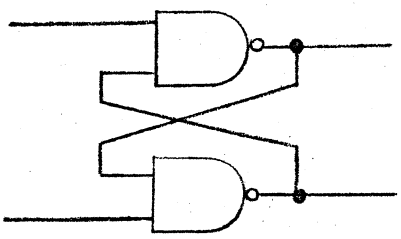
EXPANDABLE



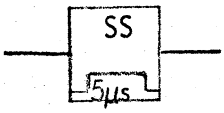
EXPANDER

EXPANDED OR

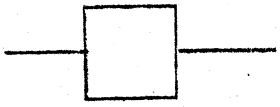




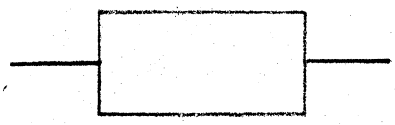
NAND LATCH



SINGLE SHOT



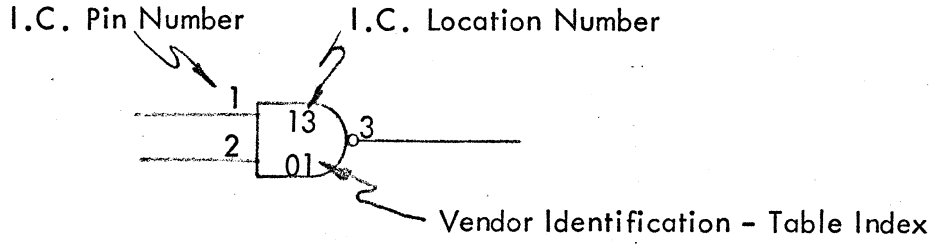
SCHMITT TRIGGER



GENERAL SYMBOL

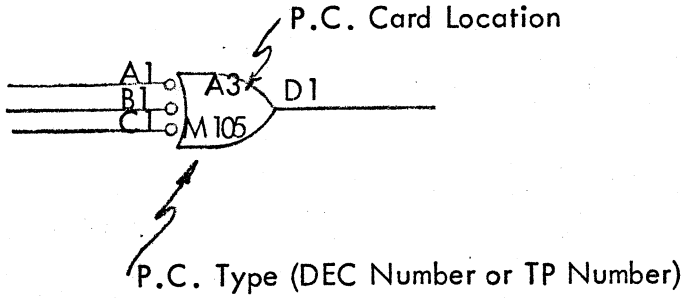
4.1.2.3.3 Logic Symbol Tag Information

The following information will be contained within and around the standard logic symbol on functional boards:

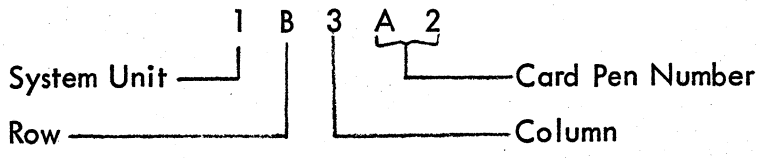


ID	VENDOR IDENTIFICATION
01	TI 7401

(1) When the logic is composed of universal P.C. boards, the following tagging information will be supplied:



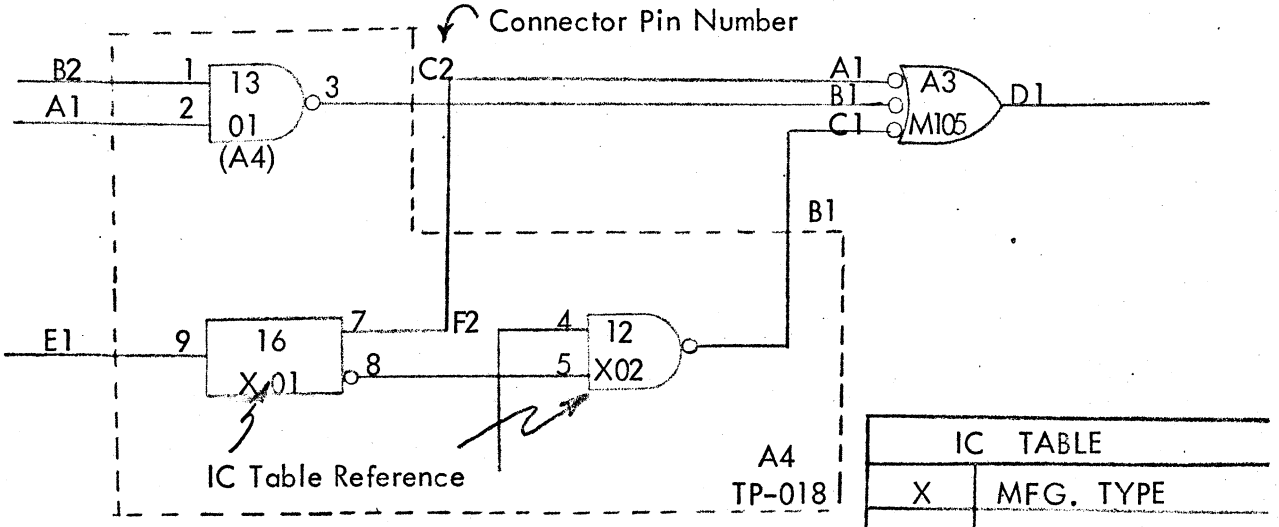
P.C. card location designations will be established in the following manner: Looking from the card side, the first row of connectors are designated A, the second B, etc. The right column will be designated 1, the second column 2, etc. If more than one system unit is involved, the right-most system unit is designated as 1, the second as 2, etc. The total designation will be assembled as follows:



When a card extends beyond a single card slot, it will carry all the used card slot designations. Card Designations for cards in the first system unit may drop the system unit designation.

When a number of interfaces are mounted on a common frame, each interface is designated independently and will be identified in some other manner.

(2) When the logic implemented is mixed or is of a non-Texas Instruments or DEC type, the following designations will be used:



IC TABLE	
X	MFG. TYPE
01	TI 7401
02	TI 7402
X01	National B030
X02	Sprague SP1042

4.1.2.3.4 Signal Lines

The intention of the logic drawing is to provide information as clearly as possible. It is the responsibility of the designer to determine when signal lines are to be drawn or when they are named only. The test is not for designers' convenience, but for which provides the greater clarity.

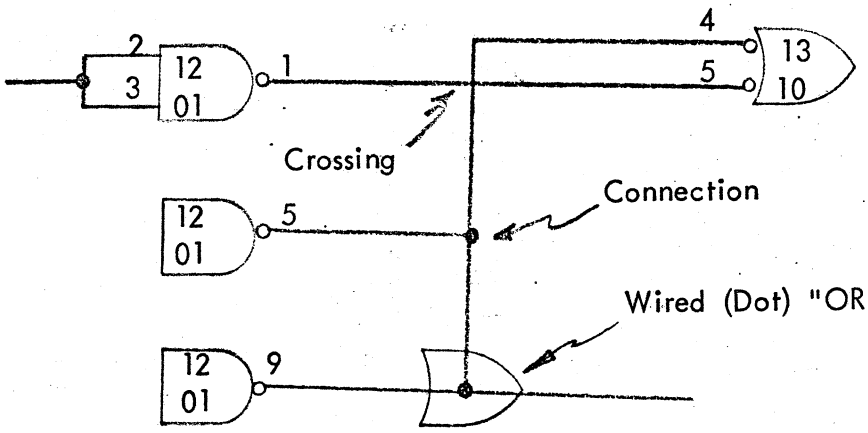
(1) Crossings and Connections

All wiring interconnections will be shown with a filled dot. Crossings will not have any special designations. Wire "OR" gates

should be shown according to 806B standards. Arrowheads can be drawn on the wiring where they add clarity to the drawing. They should not be drawn touching logic symbols.

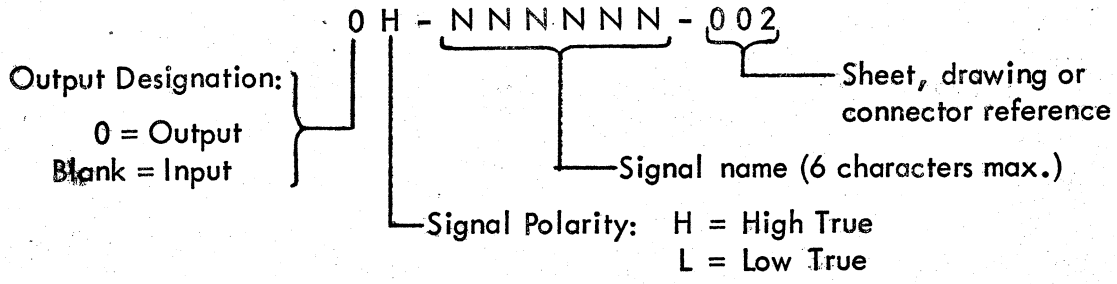
Descriptive signals can also be drawn near the wiring.

Signal names must meet the requirements under section 4.1.2.4.



4.1.2.4 Interdrawing References

It is imperative that interdrawing references be standardized in a format that permits following signals between drawings. Interdrawing references will be of the format:



Output signals will not be forward-referenced except in cases where the interface is to an element that is not normally included as the logic set (i.e., switches, mechanisms, etc.).

4.1.2.4.2 Signals that are named but do not leave the drawing. These signals will be of the format:

O H - N N N N N N

4.1.2.4.2 Signals that interconnect to drawings of the same drawing number but different sheets:

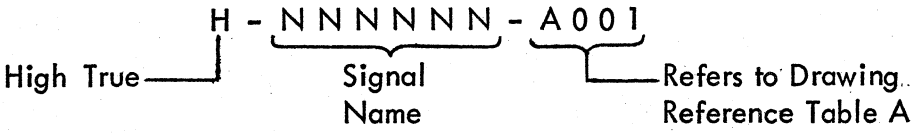
4.1.2.4.3 Several letters and numbers have ambiguous forms and will be differentiated as follows:

Letter	Number
O	ø
Z	2
I	1

Extra care should be exercised in drawing the following characters:

4 vs. A
5 vs. S
8 vs. B

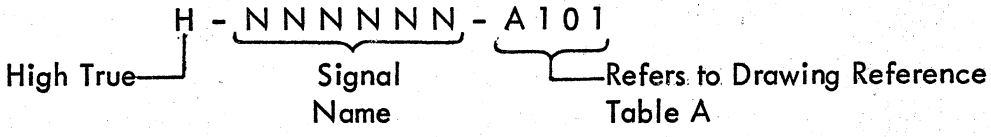
Signals between logic drawings of different numbers:



DRAWING REFERENCE TABLE A

Designation	Drawing	Sheet
000	103-000007-002	6
001	103-000013-000	2

4.1.2.4.4 Signals between Tennecomp drawings and other vendors:



DRAWING REFERENCE TABLE A

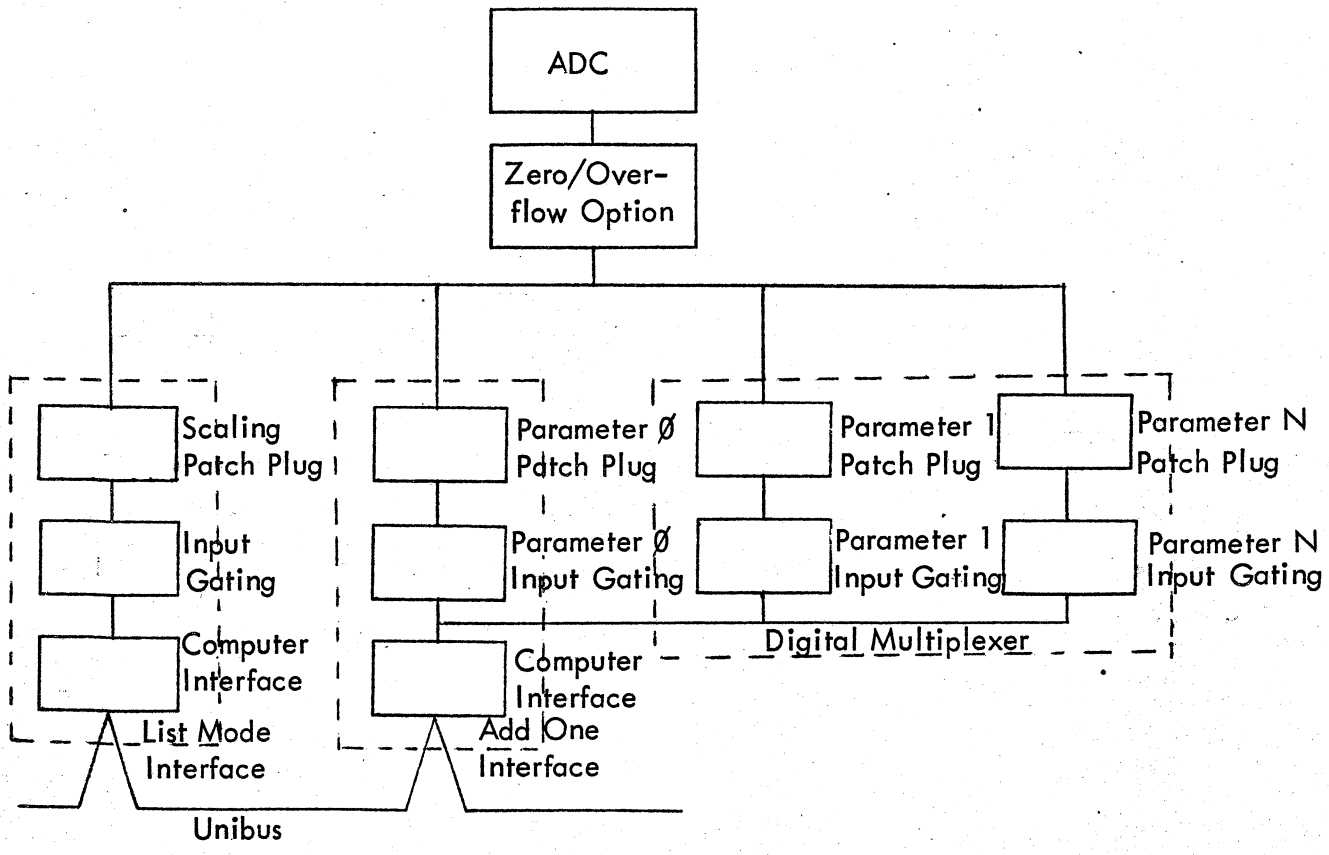
Designation	Drawing	Sheet
000		
001		
101	DEC 142371 Omnibus	2
102	KENNEDY #13-112H1-3	1

4.1.2.4.5 Customer Interconnects

Customer interconnects should be pulled together in a common area and clearly marked as such. In addition to the forementioned interconnection standards, additional English comments may be appropriate in the customer interconnect area.

4.2 ADC Subsystem

The ADC subsystem is made up of a number of subunits. The configuration of the subunits is shown below. Each unit is described in further detail in the following sections.



4.2.1 PACE ADC

Although the PACE system is described in greater detail in the PACE manual, this section highlights some aspects that relate directly to its use in the ADC subsystem.

Data and control signals are carried between the ADC and the interface on a multiconductor cable. Logic in both units is a TI type 7400 TTL circuit. A list of the signals used and their descriptions is given below:

Line	Description
DATA Line $2^0 - 2^{12}$	These data bit lines are high for a logic one.
OVERFLOW	This signal indicates that regardless of the encoded value on the data lines, the input signal exceeded full scale.
ZERO	This signal indicates that regardless of the encoded value on the data lines, the input signal did not exceed the low level discriminator threshold.
COINCIDENCE	This signal occurs when the PACE is used in Coincident mode and indicates that the current encoded data is part of a coincident group.
Channel ID $2^0 - 2^2$	These three bits indicate in binary which of the up to 8 stretchers supplied the currently encoded data.
Halt Request	This is an input signal to the PACE and is used to indicate to the PACE that it should go from the Run mode to the Stop mode. The PACE will not stop until all stretchers waiting with data when the signal is initiated have had their contents encoded and accepted by the interface.
Halt Grant	This signal indicates that the PACE is in the Stop mode.
Store	Indicates that Wilkenson type ADC has an encoded event ready.
Clear	Signal sent from interface to clear Wilkenson ADC.

Although most of the interfacing signals are fairly standard, the end of conversion signal is handled a little differently in a PACE in that it performs two functions simultaneously. When the signal goes from the zero (high) to the one (low) state, it indicates that the PACE has a new encoded data word ready for the interface. The interface can now prevent the PACE from advancing to the next conversion by holding the line at the one state until it is ready. When the interface is ready, it releases the line and the PACE will interrupt the transition from the one state to the zero state as an indicator that it can begin encoding a new data word if it needs to. All data and control signals except Halt Grant will be stable before the signal is generated.

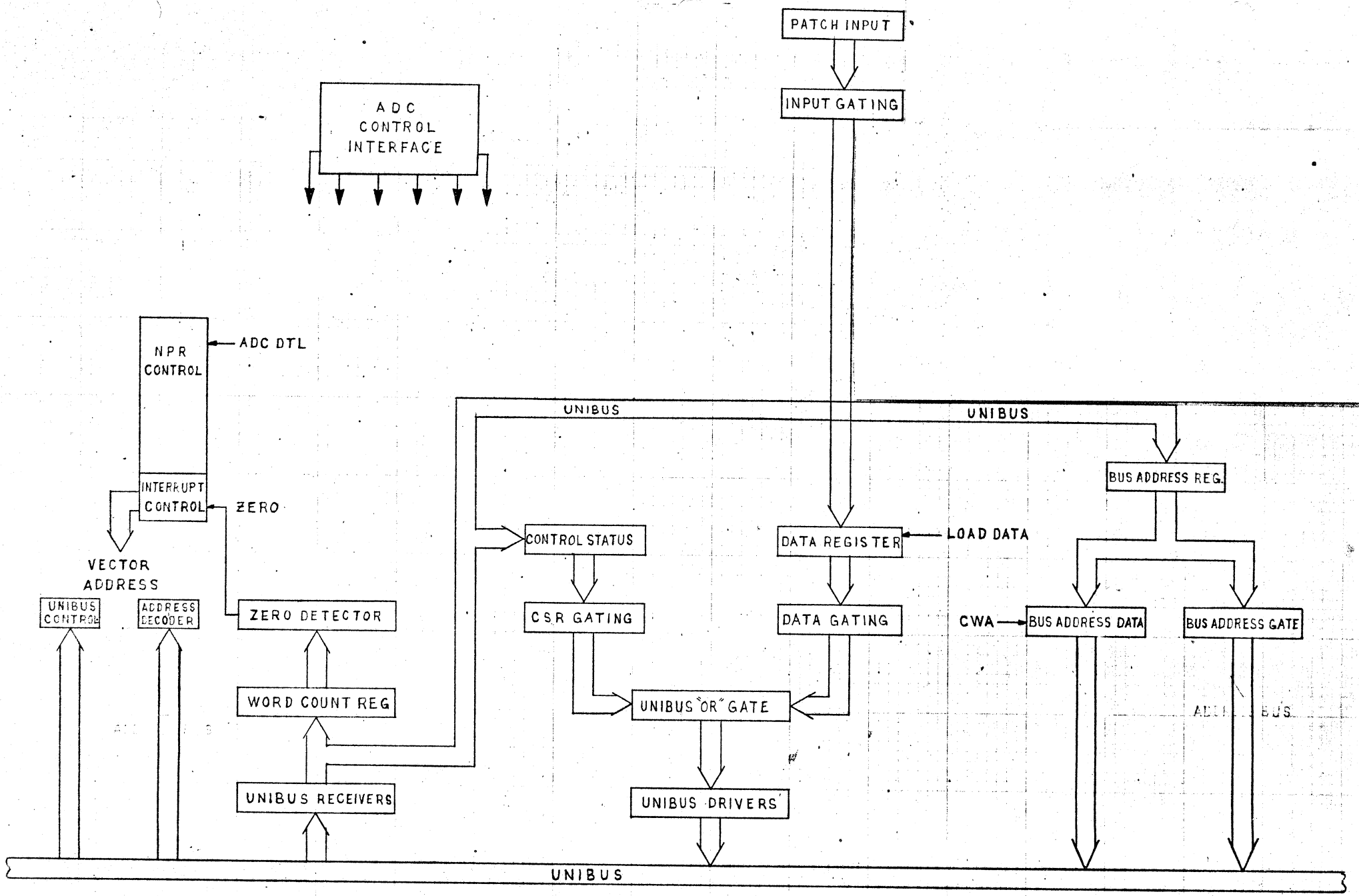

PATCH INPUT
INPUT GATING
ADC
CONTROL
INTERFACE
NPR
CONTROL
ADC DTL
INTERRUPT
CONTROL
ZERO
VECTOR
ADDRESS
UNIBUS
CONTROL
ADDRESS
DECODER
ZERO DETECTOR
WORD COUNT REG
UNIBUS RECEIVERS
UNIBUS
CONTROL STATUS
CSR GATING
UNIBUS "OR" GATE
UNIBUS DRIVERS
UNIBUS
DATA REGISTER
LOAD DATA
DATA GATING
UNIBUS
BUS ADDRESS REG.
CWA
BUS ADDRESS DATA
BUS ADDRESS GATE
UNIBUS

FIG 4.2.2-1

Since there are numerous controls on the front of the PACE, the following discussion will deal only with those related to the interface. A layout of the PACE front panel is given in figure 4.2-2 as a reference.

The recommended procedure for bringing up power on the PACE is to place the Run/Stop switch on the TC 520 in the down, or Stop, position. The Convert/Stop switch on the TC 501 should be in the "Convert" position. After power is applied, the Run/Stop switch on the TC 520 can be returned to the Run position. If the PACE has come up properly, the Stop indicator should be lit. The Channel Mode switch for the desired channels can be set at any time; however, they will not be read by the PACE unless it has been returned to the Stop position either by the Run/Stop switch or by a Halt Request from the interface.

Stretchers must be used in order. The PACE system will not work properly if a lower numbered stretcher is switched "out".

CAUTION!! The Linear outputs of the Stretchers must be connected to the input of the TC 501 with the jumper cable supplied with the PACE system.

Whenever servicing the PACE system, it should be remembered that AC is supplied by two AC cables.

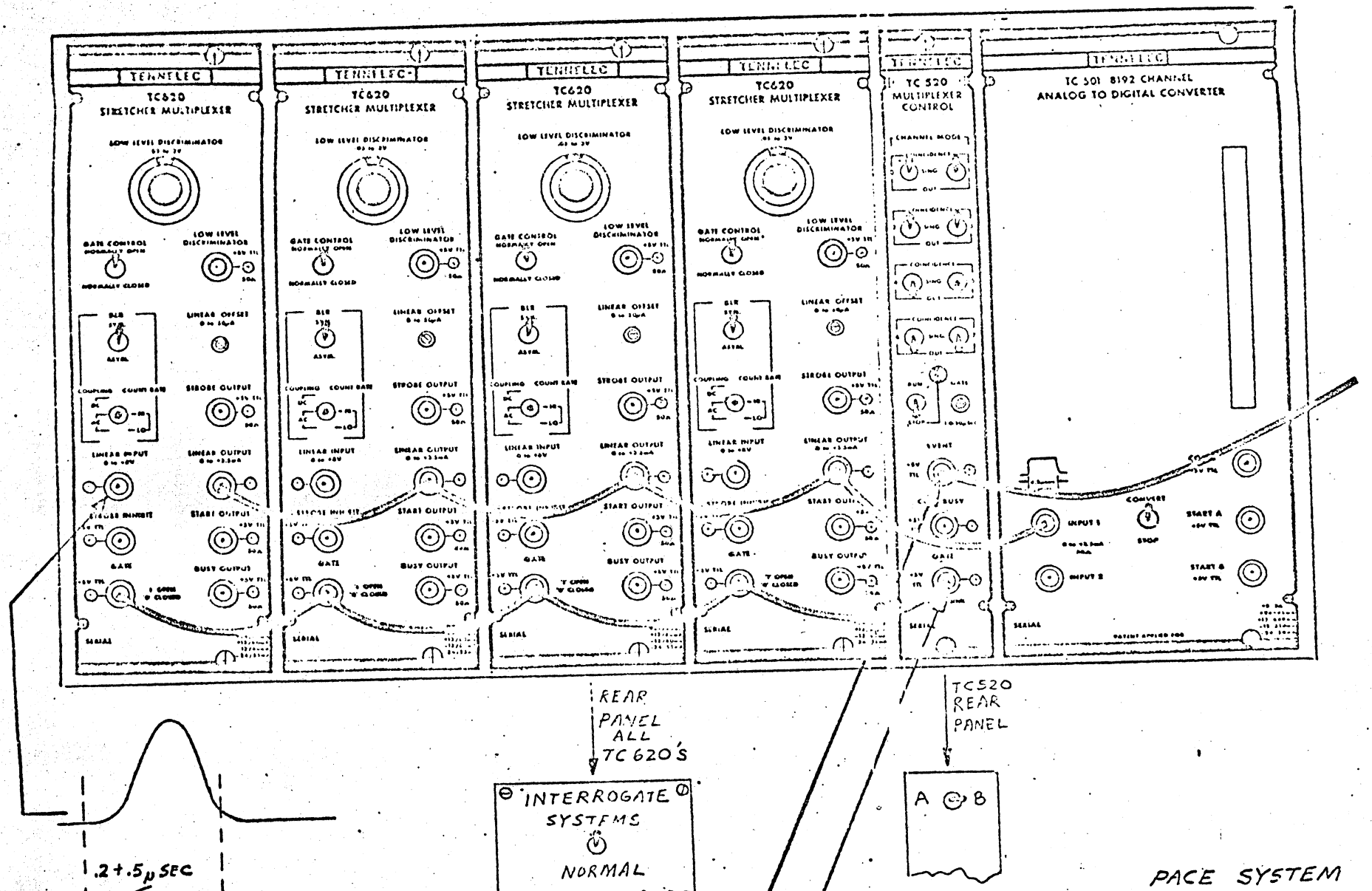
4.2.2 LIST Interface

4.2.2.1 General Description

The LIST interface permits the non-processor request transfer of data from an analog-to-digital converter to program selectable areas of PDP-11 memory. The ADC input to the interface can be in parallel with an ADD 1 interface.

A block diagram of the LIST interface is shown in Figure 4.2.2-1. The interface uses the NPR techniques recommended in the DEC PDP-11 Unibus Interface Manual (Second Edition). This manual should be studied to understand the timing associated with the computer interface.

As part of the initialization of the interface, the software must set up the Word Count with the two's complement of the number of words to be transferred and with the starting memory location for the data. An ADC Enable can now be given, and transfers of data will automatically take place to memory. An interrupt will be generated when the Word Count reaches zero.



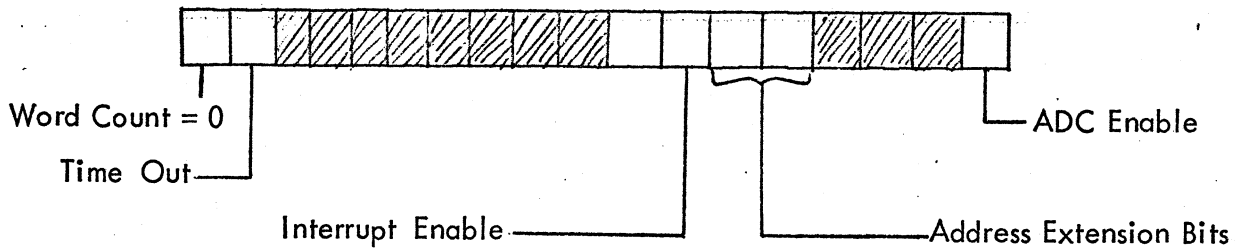
PACE SYSTEM

COINCIDENCE OPERATION

Fig. 2

4.2.2.2 Control Status Register

The format of the Control Status Register is shown below:



Those areas that contain slashes are not used. The CSR can be loaded and stored under program request.

4.2.2.3 Data Register

The input data register has been designed to accommodate a digital multiplexer. This multiplexer would permit adding additional ADC inputs. A decoding matrix permits the selection of specific data words from the PACE system. This will permit the selection of Coincidence words in the presence of singles data or the selection of a single channel out of the eight possible channels.

The selected data word is transferred into the Data Register, where it is held until the next data word is presented.

4.2.2.4 Timing and Control

The Timing and Control logic is primarily concerned with the computer transfers. It is initiated by the End of Conversion signal from the PACE ADC. Until the transfer is completed, the End of Conversion signal will be held in its logic one state, indicating to the PACE that the transfer is not completed. When the transfer is complete, the PACE End of Conversion will be permitted to return to logic zero and the interface is ready for the next transfer. The Bus Address is advanced at the end of the transfer cycle, and the Word Count is advanced at the beginning of the transfer cycle.

4.2.2.5 Address Select Codes

The following select codes have been assigned to the LIST interface:

Control Status Word (Load and Store)	764110
Data Register (Store only)	764112
Bus Address Register (Load and Store)	764114
Word Count Register (Load and Store)	764116

The interrupt vector address is 334 and will occur at priority level 4.

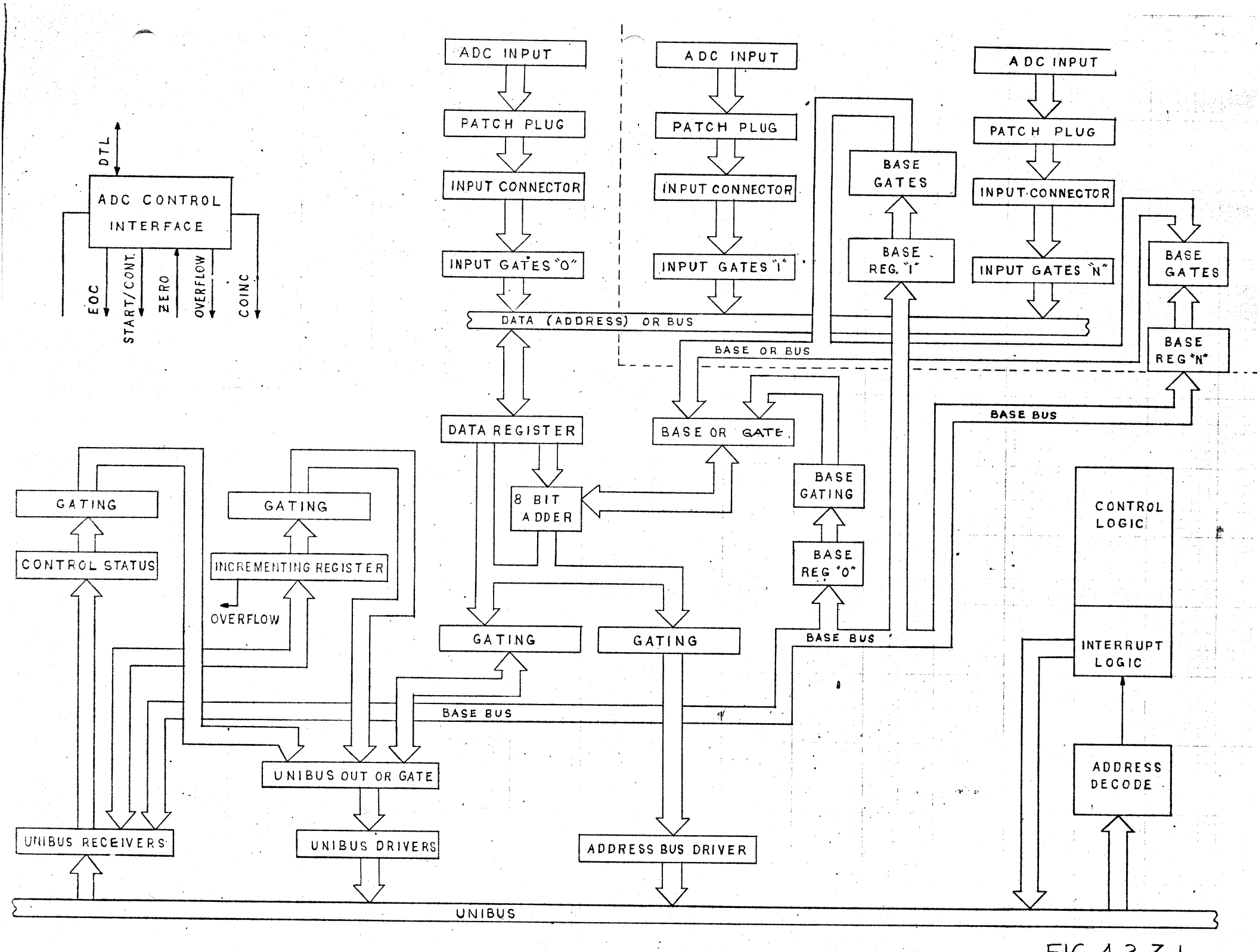

DTL
ADC CONTROL INTERFACE
EOC
START/CONT.
ZERO
OVERFLOW
COINC
ADC INPUT
PATCH PLUG
INPUT CONNECTOR
INPUT GATES "0"
ADC INPUT
PATCH PLUG
INPUT CONNECTOR
INPUT GATES "1"
ADC INPUT
PATCH PLUG
INPUT CONNECTOR
INPUT GATES "N"
BASE GATES
BASE REG. "1"
BASE GATES
BASE REG "N"
DATA (ADDRESS) OR BUS
BASE OR BUS
BASE BUS
DATA REGISTER
BASE OR GATE
8 BIT ADDER
BASE GATING
BASE REG "0"
GATING
CONTROL STATUS
GATING
INCREMENTING REGISTER
OVERFLOW
GATING
GATING
BASE BUS
CONTROL LOGIC
INTERRUPT LOGIC
BASE BUS
UNIBUS OUT OR GATE
ADDRESS DECODE
UNIBUS RECEIVERS
UNIBUS DRIVERS
ADDRESS BUS DRIVER
UNIBUS

FIG 4.2.3-1

4.2.3 ADD One Interface

4.2.3.1 General Description

The ADD One interface is designed to permit spectrum generation by taking data from a nuclear ADC. The interface operates on a non-processor request basis to reduce the CPU overhead and maintain high input rates.

A general block diagram of the ADD One interface is shown in Figure 4.2.3-1. The ADC input could come directly from an ADC, although it usually is pre-scaled in the optional patch plug or ADC test panel. The interface has been designed to accommodate an optional digital multiplexer which permits the interface to handle more than one ADC or additional scaling patch plugs.

The ADC data is used in the generation of a memory address. The contents of the addressed memory is automatically accessed, incremented and restored in memory each time a new encoded output is transmitted by the ADC. The address generated by the ADC can be modified under program control to pre-assign the area in memory where the spectrum will be located.

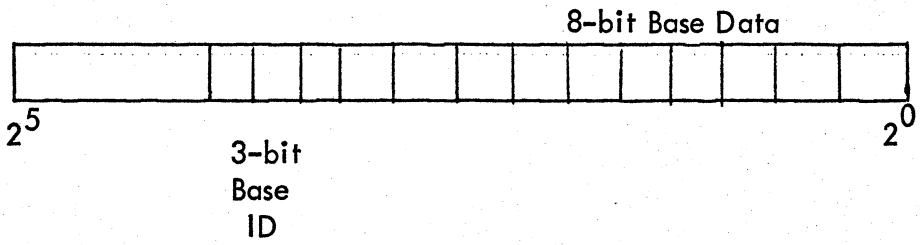
4.2.3.2 Detailed Description

4.2.3.2.1 Inputs

Sixteen data lines are provided as inputs to the interface. These lines are gated by open collector type NAND gates which permit easy expansion of additional gates. The gates are enabled by three input address decoders. The gated data is stored in a 16-bit data register. Optional inputs can be used to zero the data register selectively or to set it to all ones. The least significant 8 bits of the data register are used directly as address bits, while the most significant 8 bits are used as one input to a full adder, whose other input is the contents of a base register. The output of the adder forms the most significant 8 bits of the address. Not only are the above formed address bits applied to the address portion of the Unibus, but they can also be gated onto the data bus under program control.

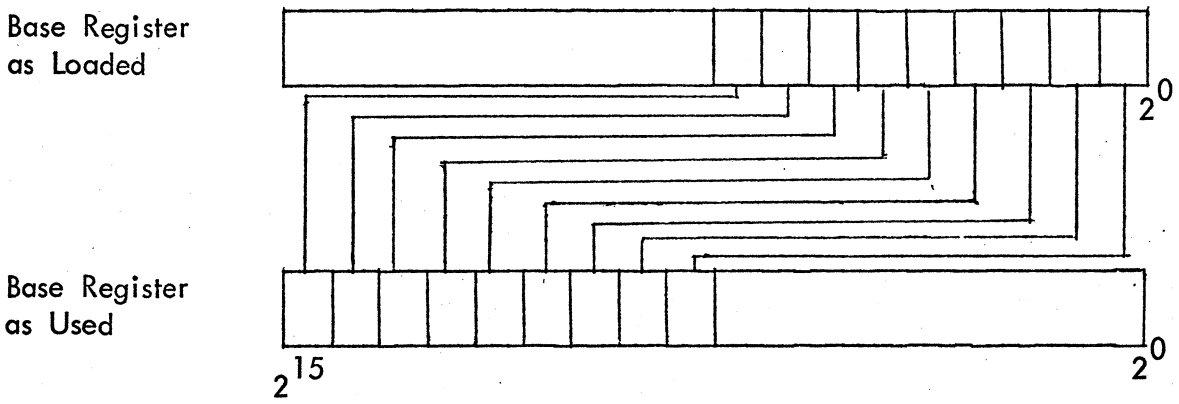
4.2.3.2.2 Base Register

The 8-bit base register is loaded under program control. The format of the word as it appears on the Unibus is shown below:



When the optional digital multiplexer is used, there is an additional base register for each additional input channel. The 3-bit base ID is used to select the base register to be loaded.

Although the base register data is located in the least significant byte, it actually is used in the formation of the most significant half of the address word.



Whenever the addition of the base register to the data register causes wrap-around, there is no hardware indication. It should also be noted that the generation of an address exceeding the size of the existing memory will cause a time-out interrupt.

4.2.3.2.3 Increment Register

The increment register is a 16-bit ripple counter. The register is reset at the beginning of any cycle. After the address is generated from the ADC output, the increment register is loaded from the address generated. The ripple counter is incremented by one; and after a sufficient delay (200 nanoseconds), the incremented word is loaded into memory at the same location. After incrementing the register, the incremented word is checked to see if the count is rolling over 64K counts. This overflow when it occurs will enable an interrupt which will permit the software accumulation of overflow counts.

4.2.3.2.4 Control Status Register

The format of the Control Status register is consistent with the recommended format established by DEC:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Function
0	ADC Enable
1 & 2	Must be "0"
3	"1" - Multiscale; "0" - Add One
4 & 5	Address Extension for Systems Exceeding 64K
6	Interrupt Enable
7 - 13	Not used - must be "0"
14	Time Out Interrupt
15	Increment Register Overflow

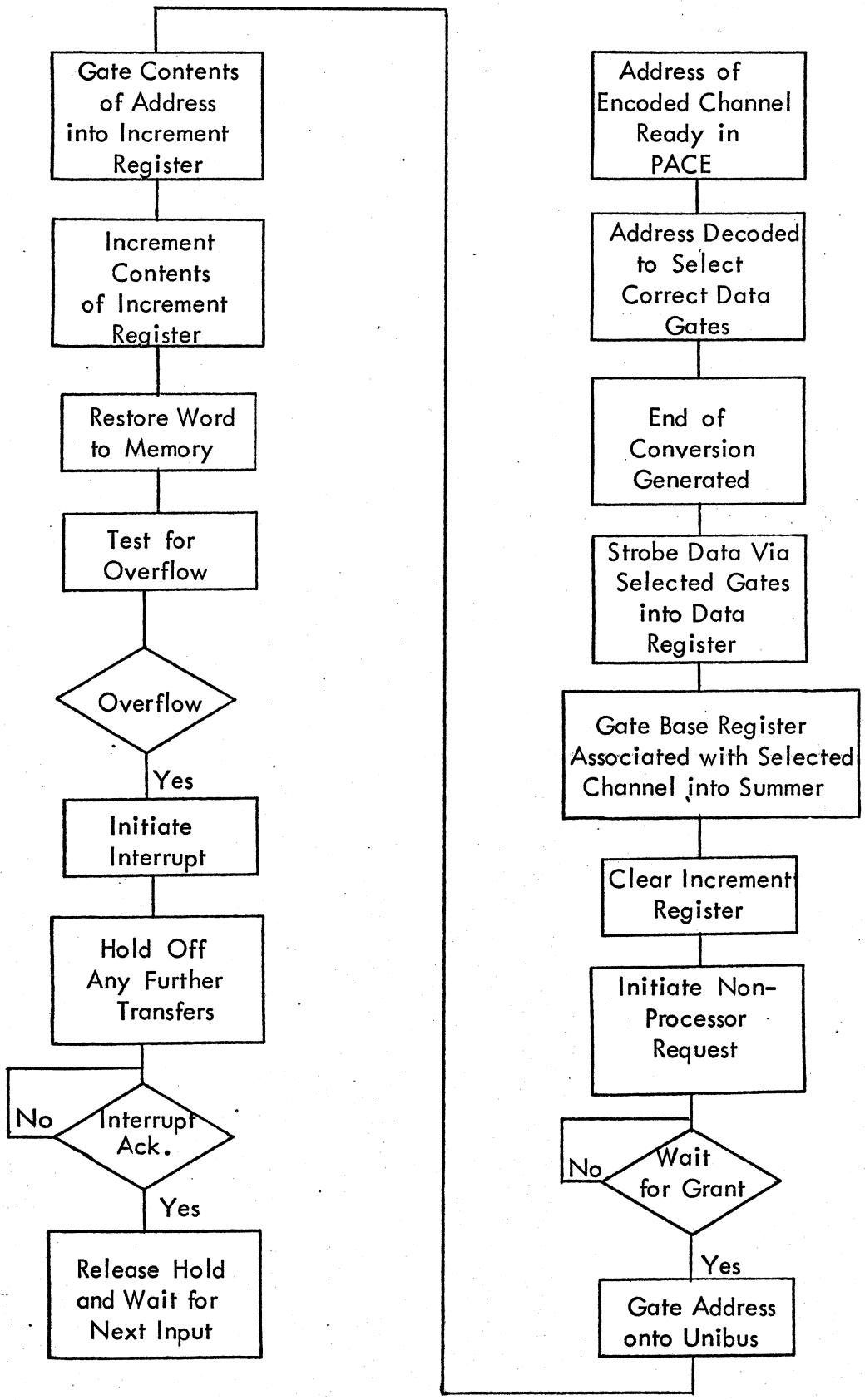
The Control Status Register is loaded and stored using normal CPU instructions. The Increment Overflow and the Time Out Interrupt flags can be reset by loading the register with these bits set to zero.

4.2.3.2.5 Timing and Control

The timing and control provides both the interface to the DEC Unibus and the interface to the ADC. The Unibus interface is the recommended DATIP interface as described by the DEC PDP-11 Unibus manual. Since this manual is readily available, it is recommended that it be used as a reference in studying and maintaining this interface.

The Tennecomp card TP-41 replaces the DEC M782 interrupt card and the M105 address decoder.

The interface begins its NPR operation whenever the end-of-conversion signal is received from the PACE. The leading edge of this signal generates an NPR request and strobes data via the appropriate data gates into the data register. The receipt of the Non-Processor Grant initiates the transfer sequence. This sequence is shown in the flow chart below:


Gate Contents of Address into Increment Register
Increment Contents of Increment Register
Restore Word to Memory
Test for Overflow
Overflow
Yes
Initiate Interrupt
Hold Off Any Further Transfers
No
Interrupt Ack.
Yes
Release Hold and Wait for Next Input
Address of Encoded Channel Ready in PACE
Address Decoded to Select Correct Data Gates
End of Conversion Generated
Strobe Data Via Selected Gates into Data Register
Gate Base Register Associated with Selected Channel into Summer
Clear Increment Register
Initiate Non-Processor Request
No
Wait for Grant
Yes
Gate Address onto Unibus

Although there are several one-shots in the timing and control logic, they are all relatively non-critical. The one-shot associated with the End-of-Conversion (D1 on drawing 114-000130, Sheet 1) signal is merely a pulse generator to strobe the input data and clear the increment register. It can be adjusted anywhere from 50 nanoseconds to 1 microsecond. The one-shot 2F3 (drawing 114-000130, Sheet 1) is probably the most critical in the interface. This one-shot does several things. Its leading edge increments the increment register. The pulse width enables the overflow test logic and, therefore, must be greater than the maximum ripple time of the increment register. The trailing edge starts the second part of the DATIP/DATO transfer. If the pulse is too wide, it will cause the interface to consume more time than necessary. It nominally should be about 400 nanoseconds. The one-shot 2F3 on drawing 114-000130, Sheet 2, is used to generate a pulse at the end of the first part of the transfer cycle to change the input/output request lines (C0, C1) from input to output. Again, this one-shot is not critical and can be adjusted anywhere from 50 nanoseconds to 500 nanoseconds.

4.2.4 ADD One Multiplexer

The ADD One Multiplexer gives the interface the capability of processing additional inputs without adding any significant amount of timing and control logic. The multiplexer consists of additional input gates for each additional input. It also has a base register for each additional input. A channel ID decoder decodes the channel ID bits from the ADC to determine which set of gates and which base register should be used for the current transfer. The interface logic is not affected by the decoding process and will cycle through its transfer operation regardless of which channel is selected.

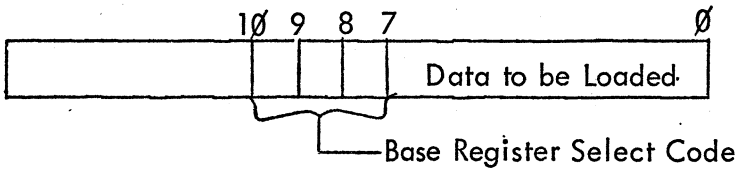
The base registers are identical in function to the base register in the interface. They are loaded in the same manner. The selection of the base register to be loaded will depend upon the 2^8, 2^9, and 2^{10} bits of the base load word. The implementation of the multiplexing functions is made with open collector gates whose outputs are "wired-ored".

4.2.4.1 Address Select Codes

The following address select codes have been assigned to the ADD One Interface:

Control Status Register (Read and Write)	764100
Current Word Address (Read only)	764102
Base Register (Write only)	764104

The format of the Base Register word is shown below:



Increment Register (Read and Write) 764106

The interrupt vector will point to address 330.

4.2.5 Input Test Panel

The optional Input Test Panel provides both a patch panel for one input channel and a means of simulating, via switches, inputs from an ADC. All input test panel switches are on the input side of the patch panel, and therefore will be modified by the patch plug in the same way as actual input data.

In the up position, the switches connect the input into the system. This is the normal position for all switches in the normal operating mode. In the center position, the switches provide a logic "0" to the system input. In the down position, the switches gate a logic "1" to the system input.

The switches labeled 0 thru 15 are associated with data inputs, depending on the scale factor determined by the patch plug. The switch number can be related to the binary power of the input. Switches labeled 14, 15 and 16 are reasonably interpreted as channel ID bits. Bit 17 is the "overflow" bit, and bit 18 is the "zero" bit. The unlabeled switch at the extreme right permits the simulation of the end-of-conversion signal from the ADC. In the center position, the simulated end-of-conversion rate is 1KC; and in the down position, the rate is 100KC.

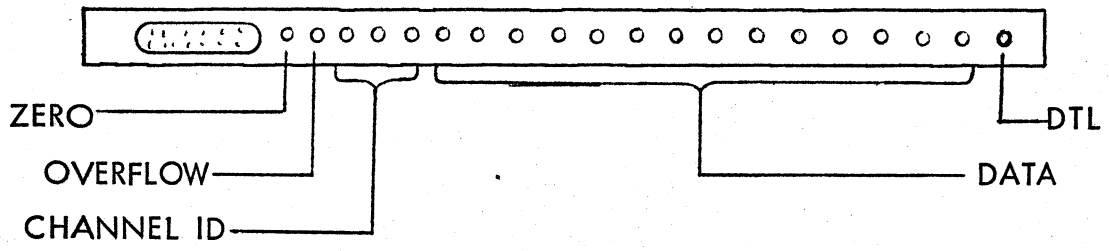


Figure 4.2.5-1 Input Test Panel

4.2.6 Input Patch Panel and Multiplexer

The input patch panel and multiplexer provides the operator control and flexibility in the use of his ADC. The panel provides the following functions:

Start/Stop Control: The BNC connectors labeled GATE are used to start and stop individual stretchers using the GATE inputs of the stretchers. When connected to the stretcher, these signals will start and stop the stretcher when the appropriate stretcher live time clock is enabled or disabled.

Busy: The BUSY BNC connector is used to gate the TP-5000 live time clock. These lines are normally attached to the busy outputs of the individual stretchers.

Run Indicators: These indicators are optionally used on some systems to indicate which stretchers are enabled.

Patch Plugs: There is a patch plug associated with each stretcher and one additional patch plug associated with the List interface. The patch plugs allow the operator to scale data individually for each stretcher and to enable the stretchers to be gated into the Add One interface.

A block diagram of the input patch panel is shown in Figure 4.2.6-1

The zero and overflow gates are controlled by the zero and overflow signals generated by the ADC. If a data word is accompanied by a zero signal, the data lines will be cleared to all zeros. If the data word is accompanied by an overflow signal, the data lines are set to all ones. The input gates are open collector circuits that can be OR tied at their outputs. Each gate has a unique enabling gate. The gates are preconditioned for channel ID codes associated with a particular stretcher. Their inputs are made available at the patch plug so that other signals can also be used as gating signals.

Control of the Add One interface and control of the List interface are independent of each other. The List interface will execute a cycle whenever the conditions required by its patch plug enabling gate are satisfied and there is an End of Conversion pulse from the ADC. If the interface was not previously busy, the encoded word is placed in a buffer register and the ADC is released as far as the List interface is concerned. If, however, the interface is busy with a previous word, it will not release the ADC until it is able to transfer the new word. The operation is the same for the Add One interface. Both interfaces have to release the ADC before it is free to encode a new value. Both interfaces can store the same word. The order in which they take the word is inconsequential.

Only one patch plug has been provided for the List interface since it is customary to store data in the list at full resolution. The Add One operation, however, often involves storing data at various resolutions and therefore provides a separate patch plug for each stretcher. It is not necessary to store only data in the data fields. It is possible and

reasonable to store Channel ID with data in the list; and it is possible to use Channel ID in the Add One interface to provide additional steering of data. Zero and Overflow signals are also available at the patch plug and could be used with the data. A maximum of 16 data bits can be stored in the list, and 13* data bits can be used as an address by the Add One interface.

* 15 bits can be used as an address by the Add One interface - See modification to Add-1 interface. (A. Baldwin 1975)

4.2.7 Display

4.2.7.1 General

The TP-5600 is a fast, multi-function display system which interfaces directly with the DEC PDP-11 computer. The display controller generates analog positioning voltages with a vertical resolution of 1 part in 1024, and a horizontal resolution of 1 part in 4096. The standard output medium is an 8" x 10" CRT display, with provisions for up to 4 selectable monitors, including storage displays and X-Y plotters.

The major data transfer mode is via "NPR" (Non-Processor Request) block transfer at a 125 KHz rate, though individual points can be displayed under program control. The display utilizes the PDP-11 Unibus only during the data transfer portion of a display cycle, leaving the bus free for processor operations during the balance of the cycle. Using a CRT display, 14 levels of intensity are available such that each point can be displayed at an individually assigned intensity level, or an entire block of data can be displayed at a single program-controlled intensity. The CRT display option is fully interfaced with the TP-1465 Light Pen for operator interaction with the graphic display.

4.2.7.2 Display Modes

4.2.7.2.1 Program Controlled (PR - Processor Request) Display Transfer

Display PR transfers provide a means for point-by-point displays under continuous program control. Each time the Y position register is loaded, the displacement is set, and then a point is plotted. The X position is not modified by this transfer. The Z register is loaded depending upon the state of the Command and Status Register (CSR) Intensity Control Bit.

4.2.7.2.2 Non-Processor Request (NPR) Display Transfer

Display NPR transfers provide for a continuous, high-speed output of a predetermined number of data points. All of the display registers are initialized to set up the transfer; then the "GO" bit of the CSR is set to initiate the transfer. No additional program intervention is required. At the termination of the NPR block transfer, the display indicates the "done" status by clearing the CSR "GO" bit (HALT condition) and setting the CSR "Display Ready" bit. Though all NPR transfers operate in this same manner, there are four different formats for memory data transfers.

4.2.7.2.3 NPR Modes

(1) MODE 0

Twenty-four bits of information are transferred from memory to the display in two memory cycles. One 16-bit word of data is transferred into the least significant bits of the 20-bit Memory Data Register from the memory address specified by Current Memory Address #1 Register (CMA1). The second memory cycle transfers one 8-bit byte from the memory address specified by Current Memory Address #2 Register. The least significant 4 bits of this byte go to the most significant 4 bits of the 20-bit Data Register. The most significant 4 bits of the byte contain intensity information. CMA1, CMA2, and Word Count (WDCNT) registers are incremented and then the point is displayed. After the end of the display time, auto X

and Y position incrementation occurs according to the appropriate STEP register values, followed by a request for a new NPR data point transfer. This process continues until all data points have been displayed. This mode is used to display scaled data histograms where the data range is from zero to $2^{20}-1$.

(2) MODE 1

One 16-bit word of information is transferred to the display from the address specified by CMA1. The least significant 11 bits go to the least significant bits of the 20-bit Data Register. The remaining data bits in the register are cleared to "zero". The 4 most significant bits contain intensity information. The remaining bit, when set, inhibits the auto X position increment at the end of that display cycle. CMA1 and WDCNT are incremented, and Y position is incremented by Y Step value.

This mode is used to display scaled data histograms where the data range is from zero to $2^{11}-1$; and for symbol generation using the X Step Inhibit feature.

(3) MODE 2 (Intensity Only)

One 8-bit byte of information is transferred to the display from the address specified by CMA1. The most significant 4 bits are intensity information. The remaining bits are ignored. CMA1 and WDCNT are incremented, and X and Y positions are incremented by the corresponding Step Register values.

This mode is used for "raster-scan" displays with intensity modulation (video). This can be referred to as a contour display.

(4) MODE 3 (X-Y)

Two 16-bit words of information are transferred to the display in two memory cycles. The first word is transferred from the address specified by CMA1; the LS 12 bits go to X position. CMA1 is then incremented by one word, and the next memory word is transferred from that address. The LS 10 bits go to the Y position register, and the 4 MS bits are the intensity information. Thus, the memory data list for Mode 3 consists of sequential word pairs (X, then Y), which form X-Y coordinate points.

This mode can be referred to as the X-Y, or linear, mode and is useful for displaying plots generated by two independent variables.

4.2.7.3 Block Diagram Description

The Display System Block Diagram shows the major portions of the display and briefly outlines the system data flow paths.

4.2.7.3.1 Unibus

The I/O line for the PDP-11 computer is the "Unibus", and it consists of parallel address, data, and control signal lines. In order to minimize loading effects, the input and output lines for the Command and Status Register, X Position Register, Y Position Register, Intensity Register, and X,Y Step Register, are buffered from the Unibus. The signals going to the Unibus from these registers are multiplexed by a 4-way data selector, and signals coming from the computer via the bus lines are distributed from a common line receiver.

Sheet 1 of the block diagram shows the Control and Status Register (CSR), I/O function select logic (address selectors), the basic timing block, interrupt controls, and non-processor transfer control registers.

4.2.7.3.2 Control and Status Register (CSR)

The CSR receives information from the bus master (CPU) which sets the various system operating parameters, such as NPR transfer mode, vertical data scale, monitor selection, and intensity register mode. Upon interrogation, it also transmits back to the computer the status of various display functions, such as "GO" - NPR transfer in progress, display ready, light pen hit, and light pen tip switch depressed.

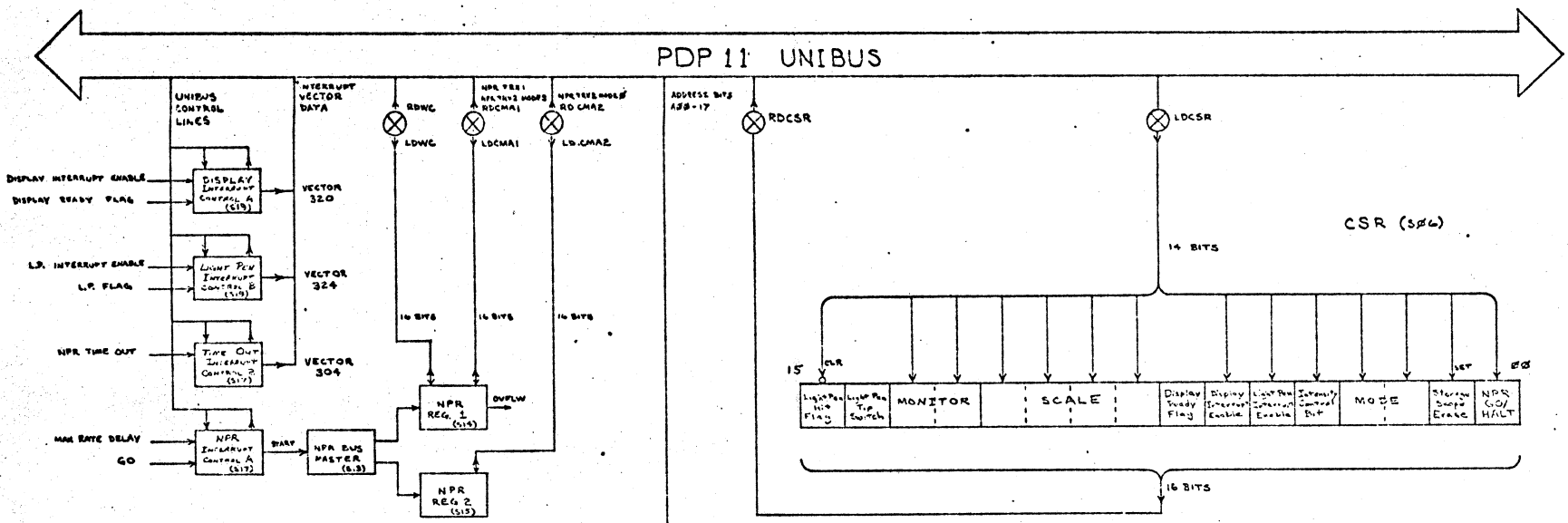
4.2.7.3.3 Address Selectors

The address selectors decode the particular I/O function to be performed, distribute the appropriate control signals to the designated display function.

4.2.7.3.4 Interrupt Controls

The interrupt control sections conditionally demand processor action, depending upon the status of the controlled function. The unique vector addresses specify the memory address which references the central processor to the interrupt handling program.

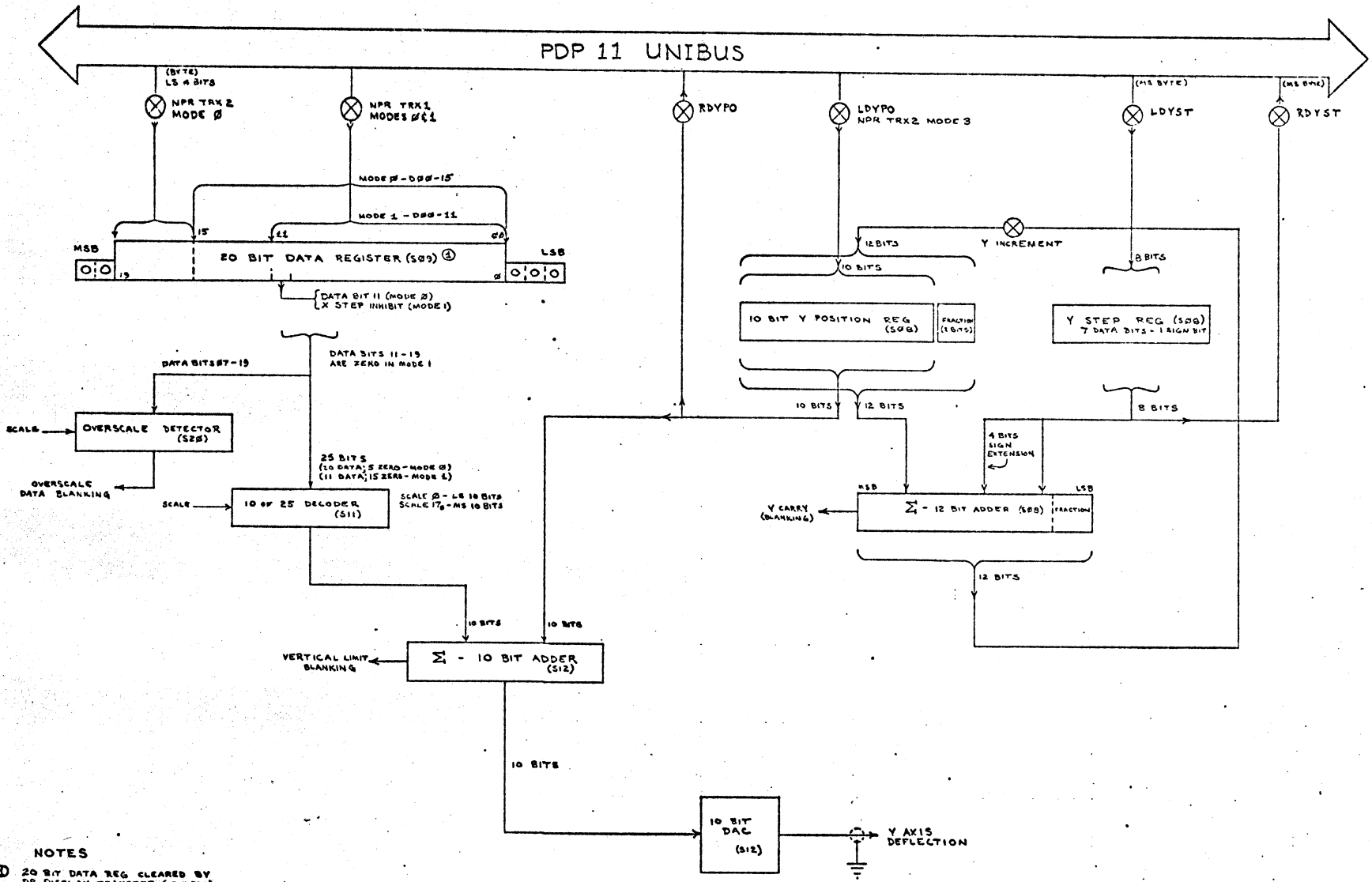
The NPR Interrupt Control initiates a non-processor interrupt for each data point transfer when the "GO" bit of the CSR is set and at the end of each displayed point. The maximum data transfer rate can be slowed down



NOTES:

"S" NUMBERS REFER TO SHEET NUMBERS OF SCHEMATIC 114-000120-000

REVISIONS	TENNECOMP SYSTEMS, I
	PDP 11 DISPLAY SYSTEM
	BLOCK DIAGRAM - CONTROL, STATUS, E
	DESIGNED: DTP — APPD BY: — SHEET 1 OF
	DRAWN: DTP — DATE: — SCALE:



NOTES

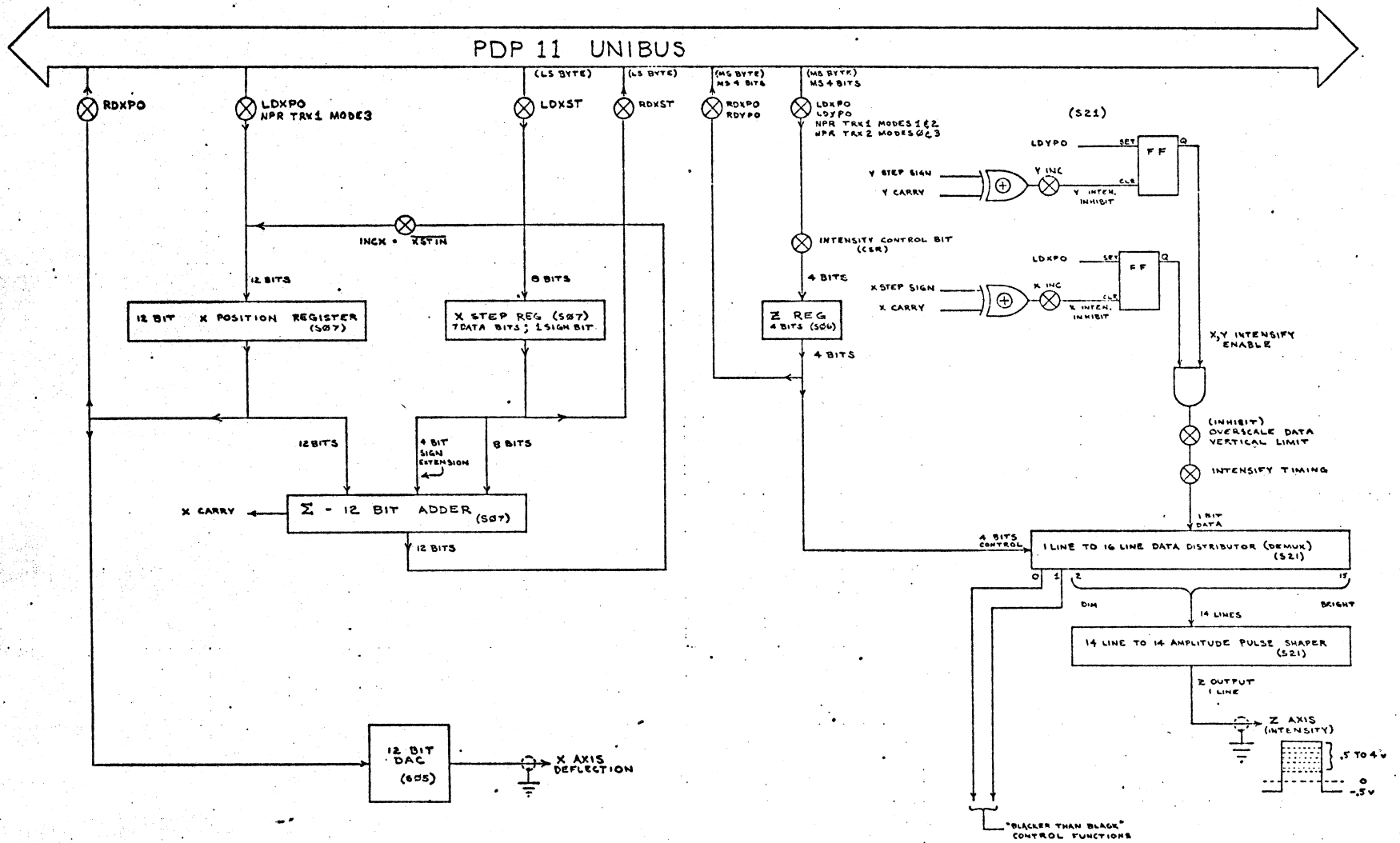
① 20 BIT DATA REG CLEARED BY PR DISPLAY TRANSFER (LD 7 P06); MODE 2 ; MODE 3. BITS 12-19 ONLY CLEARED BY MODE 1. BIT 11 IS DATA IN MODE Ø ; X STEP INHIBIT IN MODE 1 (D11 = Ø).

"S" NUMBERS REFER TO SHEET NUMBERS OF SCHEMATIC 114-000120-000

MS - MOST SIGNIFICANT (8-BIT)

LS - LEAST SIGNIFICANT (8-BIT)

REVISIONS	TENNECOMP SYSTEMS, IN
	PDP 11 DISPLAY SYSTEM
	BLOCK DIAGRAM - Y AXIS
	DESIGNED DSR · SHEET 2 OF 3
	DRAWN DSR · SIZE



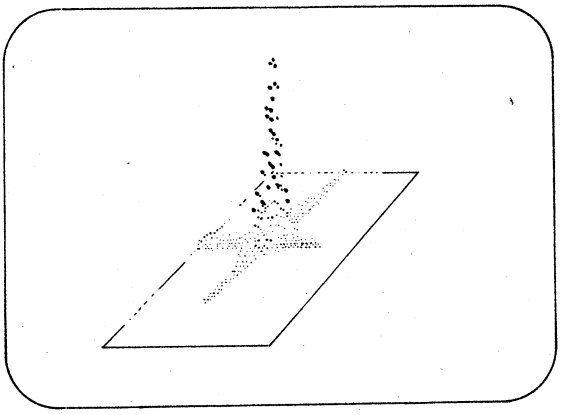
REVISIONS	TENNECOMP SYSTEMS,
	PDP 11 DISPLAY SYSTEM
	BLOCK DIAGRAM - X & Z AXES
	SHEET 3 OF

by "MAX RATE DELAY" to prevent the display from "loading down" the bus when other NPR devices require maximum bus-time utilization. When the NPR interrupt is granted by the processor, the start signal initiates a bus data transfer under the control of the display bus master circuitry. Appropriate control functions are applied to the NPR transfer registers, which specify the memory addresses from which data is to be transferred, and which also log the number of transfers which have occurred. After the predetermined number of data points, "OVFLW" (Word Count Overflow) returns the CSR to the HALT mode, terminating the NPR transfer.

4.2.7.3.5 Display Y-axis Circuitry (Sheet 2)

The basic function of the Y-axis circuitry is as follows:

Ten adjacent bits are selected as data from a 25-bit data register under the control of the CSR Scale setting. The data is then added to the Y-position information to determine the resultant Y displacement of the displayed point. In the NPR mode, after each point is displayed, the Y position is incremented by the value of Y-STEP. This can be best illustrated by an isometric display, such as Figure 4.2.7.3-4, below:



Isometric Mode

The 25-bit data register consists of a 20-bit memory data register with two leading and three trailing "hardwired" zeroes.

Twenty-bit Data Register: This register is used in NPR transfer modes 0 and 1. Mode 0 loads all 20 bits with memory data; mode 1 loads 11 bits with memory data, setting the remaining 9 bits to zero. In this mode, one additional bit transferred from memory controls the automatic X-step function described under the X axis circuitry.

Ten of Twenty-five Decoder: This circuit scales the data by selecting the significance of the 10 bits of data to be displayed. The range of scaling is from 2^7 full scale to 2^{20} full scale; and 2^{20} half and quarter scale. The initialized scale setting of the CSR is for 2^{10} full scale.

4.2.7.3.6 Y Position and Y Step Registers

The basic Y Position register is a straightforward 10-bit register which controls the Y baseline displacement. This corresponds to the displacement of the displayed point in program-controlled transfers and NPR mode 2 and 3 transfers. Mode 0 and 1 NPR transfers sum 10 bits of data with Y position to determine the displacement.

A two-bit extension of the Y Position register is used in conjunction with the Y STEP register to give an apparent step resolution of one part in 4096. If the Y STEP were set such that Y STEP = 1, every fourth Y axis increment would shift the displacement by one point. Y STEP can be set either positive or negative in the range of 0 to 2^7-1 in unity increments.

4.2.7.3.7 Overscale Data Detector

The overscale data detector is a series of shifting gates which detect the presence of a "one" bit in any bit position of the 20-bit data register more significant than the 10 bits selected as display data. This indicates that the magnitude of the data is higher than is indicated by the scaled data, and an appropriate logic signal is generated. This signal, along with the vertical limit and Y carry blanking signals, is processed by the Z axis logic to prevent "rollover" (see Z axis).

4.2.7.3.8 X Position and Step (Sheet 3)

The X Position register is a 12-bit register which controls the X axis displacement of a displayed point in all operating modes. The step register controls the automatic X increment with a resolution of 1 part in 4096. The X step can be set either positive or negative in the range of 0 to 2^7-1 in unity increments. The automatic X increment can be inhibited during Mode 1 NPR transfers by setting bit 11 of the memory data. This feature is especially useful for character generation.

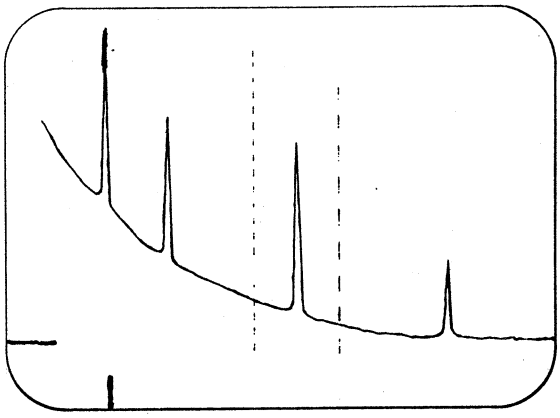
The X carry signal indicating displacement beyond the 12-bit range is processed by the Z axis logic to prevent "rollover".

4.2.7.3.9 Z Axis

The Z axis circuitry has two main functions: to determine the intensity level of each displayed point, and to prevent "rollover" phenomena.

4.2.7.3.10 Rollover

The bounds of the display matrix are 10 bits for the Y axis and 12 bits for the X axis. Since these displacements are the result of the sum of two or more terms, the result can possibly exceed the display bounds. When this happens, the bits which cause the excess are ignored by the displacement generating digital/analog converters. Thus, an X displacement of 12345_8 is exactly equivalent to 02345_8, producing 2 data values for a single displayed displacement. As is illustrated in Figure 4.2.7.3-5, continuous lines going off the top of the screen reappear at the bottom, while lines going off the right edge reappear on the left. To prevent the resultant ambiguity, any rollover condition is detected and blanked out by the Z axis circuitry.



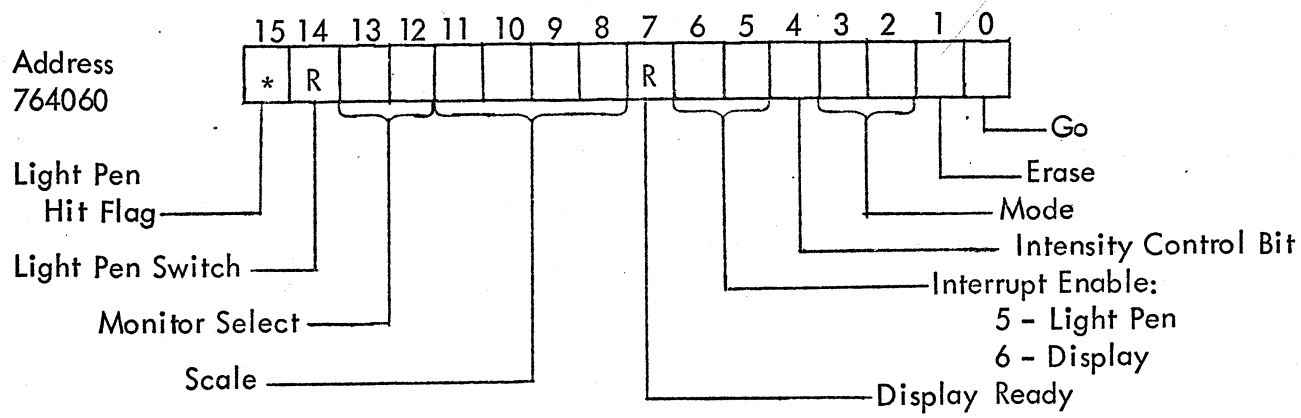
4.2.7.3.11 Z Register

The Z register, or Intensity Register, controls the intensity of every point displayed. For program-controlled and NPR mode 3 transfers, it occupies the most significant 4 bits of the X Position and Y Position words. During modes 0, 1, and 2 NPR transfers, the Z register accepts memory data. The loading of this register is conditional. If the intensity control bit of the CSR is set to "one", the Z register is loaded during the appropriate transfer. If the intensity control bit is reset to "zero", the contents of the Z register cannot be modified; and all successive points will be plotted at the constant, unmodified intensity level.

4.2.7.3.12 Intensity Generation

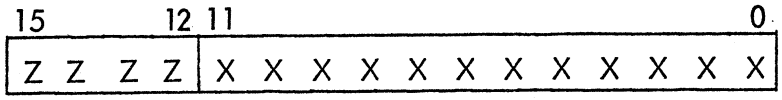
Intensity generation occurs by decoding the 16 possible intensity codes from the Z register. Of these, 14 codes (2 through 15) amplitude modulate the Z axis intensification pulse. Two codes, 0 and 1, do not generate intensification, but are logical control functions which can be used to control such parameters as "pen up" on X-Y chart recorders, and are referred to as "blacker than black".

Command and Status Register (DSPCSR):



BITS:		Initialize
0	GO: When set, initiates NPR transfer. Can be cleared by program, but normally cleared by end of NPR block or Light Pen Hit (when L.P. interrupt enabled).	0
1	ERASE: Used to initiate a storage display erase cycle.	0
2-3	MODE: Sets the NPR transfer mode.	00
4	INTENSITY CONTROL: When cleared, the Intensity Register contents cannot be modified. When set, the Intensity Register is updated with each NPR, load X Position, or load Y Position data transfer.	1
5	LIGHT PEN INTERRUPT ENABLE: Vector - 320; Priority - 5 Enables Light Pen Hit Flag to halt an NPR transfer and generate a Light Pen interrupt. When cleared, the Light Pen Hit Flag does not terminate an NPR transfer.	0
6	DISPLAY INTERRUPT ENABLE: Vector - 324; Priority - 4 Enables the Display Ready Flag to generate an interrupt.	0
7	DISPLAY READY: This flag is set within 5 microseconds after a PR display transfer (load Y Position), and indicates the end of the display cycle. It is cleared during an NPR transfer (GO) and is set within 5 microseconds after the NPR block terminates.	1
8-11	SCALE: Determines the significance of memory data to be displayed during Mode 0 and 1 NPR transfers.	0011 (2^{10}-1 full scale)

764062 - X Position & Intensity (XPO)

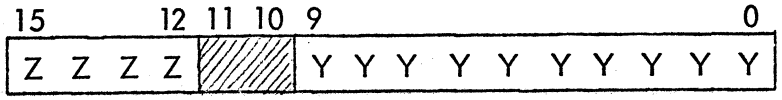


0 - 11 X Position Data
12 - 15 Intensity Data.

DATI transfers occur normally.
DATO transfers occur normaly.
DATOB Transfers occur as follows:

DATOB-764063	Loads only intensity information (Bits 12-15)
DATOB-764062	from an even memory address (word address); loads the entire 12 X Position bits (extended byte - bits 0-11)

764064 - Y Position and Intensity (YPO)



0 - 9 Y Position Data.
12 - 15 Intensity Data

DATI transfers occur normally.
DATO transfers occur normally.
DATOB transfers occur as follows:

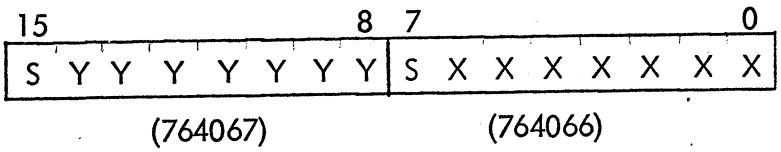
DATOB - 764065	Loads only intensity information (bits 12-15)
DATOB - 764064	from an even memory address (word address); loads the entire 10 Y Position bits (extended byte - bits 0-9).

Both DATO and DATOB 764064 load the Y Position register and then initiate one PR display cycle.

NOTE: DATI - Data transfer from slave to bus master.
DATO - Word transfer from bus master to slave.
DATOB - Byte transfer from bus master to slave.

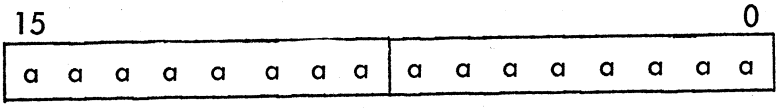
Refer to DEC PDP-11 UNIBUS INTERFACE MANUAL for additional information.

764066 – X,Y Step (X Step) (Y Step) (Step)



0 – 7 X Step Data (7 data bits + sign).
8 – 15 Y Step Data (7 data bits + sign).

Current Memory Address Registers



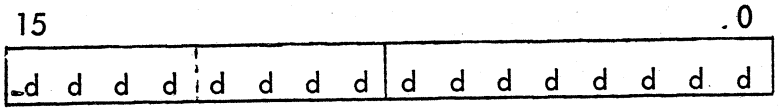
764070 (CMA1)

0 – 15 CMA1 Address information loaded with the initial address of the list of word or byte portions of the 24 data bits transferred during NPR Mode 0 transfers.

764072 (CMA2)

0 – 15 CMA2 address information loaded with the initial address of the list of word or byte portions of the 24 data bits transferred during NPR Mode 0 transfers.

764074 – Word Count (WDCNT)



0 – 15 Word Count Data. Loaded with the negative value of the number of points to be displayed. Decremented by each NPR display cycle. Halts NPR display when equal to zero. When WDCNT = 0 and an NPR transfer is initiated, 65,536 NPR points are attempted (See CSR time-out note).

Sample NPR Set-up and Go

```
START:  BIS   #20, DSPCSR
        MOV   SRC, YPO
        MOV   SRC, XPO
        MOV   SRC, STEP
        MOV   SRC, CMA1
       (MOV   SRC, CMA2)
        CLR   WDCNT
        SUB   SRC, WDCNT
        MOV   SRC, DSPCSR

        CONTINUE
```

Enables Intensity Control

Where bits 12-15 of the source are zeroes (not used in Mode 3).

Where bits 12-15 are set to the desired intensity level if a constant intensity display is desired.

Sets desired X and Y autoincrement (not used in Mode 3).

Sets CMA1 to initial address of data list.

MODE 0 Only - Sets CMA2 to initial address of byte data list.

Sets negative value of number of data points into WDCNT.

Where source bit 0 is set; bit 4 is set for intensity data from memory, cleared for constant intensity; all other bits reflect desired NPR conditions.

4.2.8 Live Time Clock

The TP-5470 Live Time Clock system consists of from one to eight independently gated clocks which generate timing flags at a program-controlled rate. The system interfaces directly with the DEC PDP-11 computer, utilizing the Unibus for data, address and control timing signals. This system operates either under continuous program control, or via the PDP-11 bus interrupt system.

4.2.8.1 Block Diagram Description

The basic element of the live time clock system is a gated clock which divides 100 KHz timing pulses by a program-selected ratio. The master clock in position 7 contains a crystal oscillator which generates the 100 KHz signal to be distributed to all of the 8 possible clocks. The slave clocks are identical to the master, with the exception that they do not contain an internal oscillator. Slave clocks must be added in mumerical sequence from 0 through 7; and for each clock added, 2 wire-wrapped jumpers must be removed to enable the clock flag function.

Clock	Remove Jumpers	
0	Standard	
1	A2A1 - A2E1	E4U1 - E4P1
2	A2E1 - A2D1	E4P1 - E4R2
3	A2D1 - A2M1	E4R2 - E4R1
4	A2M1 - A2L1	E4R1 - E4N2
5	A2L1 - A2R1	E4N2 - E4M2
6	A2R1 - A2T1	E4M2 - E4V2
7	Master Clock	

(Refer also to Schematic 114-000110-000)

When the Enable/Reset input is low, the clock does not count; and all of the divider circuits are cleared to the zero state. Thus, whenever a clock is enabled by applying a logic "one" to this input, the count always begins from zero.

The "External Gate" input generates the "live time" function. When this input is low, the clock accumulates counts normally. When the input goes to the high state (logic one) indicating "busy" or "dead time", the clock ceases to count but retains the existing count. When the input goes low again, the clock resumes counting where it left off.

The clock circuitry divides the incoming 100 KHz timing pulses by 100, 1,000, 10,000, and 100,000 simultaneously. The Program-Controlled Divider circuitry selects one of these division rates and applies the output signal to the flag flip-flop. Every time the selected number of counts is reached, the flip-flop changes state. Generally, as soon as a clock flag is set, this condition is sensed, the program utilizes the time information and then clears the clock flag. During this time, if the clock is properly gated, it continues to run without interruption, since clearing or setting the clock flag has no effect on the counting circuitry.

The clocks are individually enabled by setting corresponding bits of the Clock Enable Register with a program data transfer. Clearing bits in this register disables and resets the respective clocks.

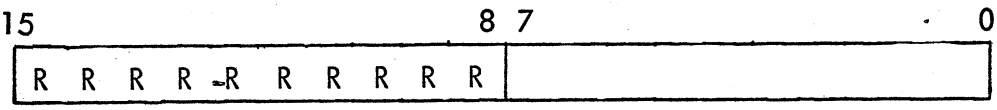
The division ratios for all clocks is set by the two-bit Clock Rate Select portion of the Command Register. Four ratios are available which generate flags after an accumulated time of 1 ms, 10 ms, .1 sec., or 1 sec.

The Command Register Interrupt Enable bit enables any true clock flag to generate a PDP-11 interrupt at priority level 5 through vector address 300. The interrupt service routine generally reads the clock flags, manipulates the time information, and then clears the flags it has processed.

The Address Selector gates data to and from the Unibus when Clock input or output functions are requested. The Interrupt Control circuitry processes interrupt requests to the Unibus by generating appropriate bus control signals.

4.2.8.2 Address Codes

4.2.8.2.1 764120 - Flag & Select Register (LTCSEL)



0 - 7 ENABLE/DISABLE CLOCKS: When set, each bit enables the corresponding clock (0-7) to begin counting a 100 KHz timing signal from the initial or zero state. Each cleared bit disables the corresponding clock and resets it to the initial or zero state.

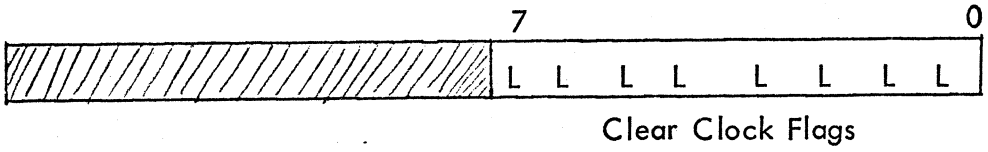
Initialize: Disables all clocks

NOTE: Each clock has an additional external gating input for a "device busy" signal. This input is used to generate the device "live time" function since an enabled clock only advances the count, while this input is at a logic 0 level. When this input is at a logic 1 level, the clock holds at the existing count.

8 - 15 READ CLOCK FLAGS: This is a read only function which reads the current status of all clock flags into the corresponding bit position of the byte. Each flag changes state after a predetermined number of 100 KHz timing pulses have been counted.

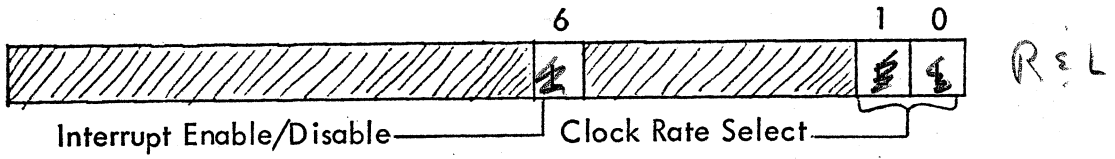
Initialize: Clears all flags

4.2.8.2.2 764122 - Clear Flags (LTC CLR)



0 - 7 CLEAR CLOCK FLAGS: This is a load only function which clears those clock flags corresponding to the bits which are set. Neither the counting operation nor the clock count are affected.

4.2.8.2.3 764124 - Command & Status Register (LTC CSR)



0 - 1 CLOCK RATE SELECT: Selects the rate at which the clock flag is changed.

Code:		Rate:	Time:
	00	1 KHz	1 ms
	01	100 KHz	10 ms
	10	10 Hz	100 ms
	11	1 Hz	1 Sec.

6 INTERRUPT ENABLE/DISABLE: Vector 300; priority 5

When this bit is set, any clock flag set will generate an interrupt through vector address 300.

Initialize: Clears all 3 bits.

NOTE: L designates Load Only bit. Read attempt results in "0" as data.
R designates Read Only bit. Load attempt is ignored.

4.2.8.3 Sample Program

This program uses clock 7 to establish a 40 Hz refresh rate for a CRT display. Being a real time application, clock 7 "External Gate" must be at a logic 0.

```
RFRESH   MOV  #100, LTCCSR      (Enable interrupt; set 1 ms clock rate)
         MOV  #200, LTCSEL      (Enable clock 7)
         CONTINUE (or WAIT FOR INTERRUPT)
```

INTERRUPT SERVICE ROUTINE:

```
CLKINT   MOV  LTCSEL, SAVE      (Move flags to SAVE)
         MOVB SAVE+1, LTCCLR    (Clear processed flags)
         BPL  OTHER             (OTHER routine processes clocks other than 7)
         INC  CLOK 7            (Increment time cell)
         CMP  #31, CLOK 7       (Compare 25 ms to clock 7 time)
         BNE  RETURN            (If not 25 ms, wait for next clock)
         CLR  CLOK 7            (At 25 ms, reset time cell)
         JSR  DISPLAY           (Perform refresh)
RETURN   BITB #177,SAVE+1       (Look for other clock flags)
         BNE  OTHER
         RTI                    (Return from interrupt)
```

As long as Clock 7 runs, the Display subroutine will be executed every 25 ms (40 Hz).

4.2.9 Light Pen Assembly

The Light Pen Assembly consists of three basic units:

The light pen barrel and fiber optics
The photodetector and pulse-shaper
The computer interface

The pen barrel is machined from aluminum and fitted with an actuator and write switch. The actuator is made from soft plastic so as not to scratch the glass or plastic face plate of the display scope. A rugged plastic fiber light guide extends from the back of the pen barrel and is connected at the other end to the light cover of the light detector. This detector is an RCA 931A photomultiplier operating at 1 mA from a 1 KV regulated DC supply. The output of the photomultiplier is amplified by an operational amplifier and shaped to provide a logic level pulse to the computer interface. The computer interface is usually a Display Scope Control.

4.2.9.1 Principles of Operation

The light pen will operate with a variety of display scopes, including a 5-inch laboratory type oscilloscope. The use of larger scopes such as the Hewlett-Packard 1300A Display will provide the user with more gratifying control over the computer.

When the pen is aimed at a spot being displayed on the oscilloscope screen, light is collected by the fiber optics light guide and is transmitted to the photomultiplier. The light is converted to an electrical signal by the photomultiplier and amplified. This signal is then fed to an amplifier containing a μ710 comparator and an emitter follower. The input to the amplifier has a differentiation time constant of about 1 μsec, and this is sensitive only to pulses from the photomultiplier with short rise times. The purpose of the differentiation is to accept the fast rise light signal emitted by the spots displayed on the oscilloscope and reject slower varying light sources such as fluorescent lights and light fluctuations caused by pen motion in brightly lighted rooms. The output of the operational amplifier is clamped at -3 volts* to provide a suitable logic signal for the computer interface. In order to use the light pen facility, appropriate programs are loaded into the computer.

When the pen is aimed at a spot on the display oscilloscope, it will receive a "hit" each time the spot is displayed. As described above, this will result in a -3 volt pulse being presented to the Display Control, thence to the light-pen-strobe gate, which will set the L.P. Flag flip-flop.

When the pen is placed against the screen of the display tube, the actuator in the tip of the pen depresses and throws the switch in the pen barrel from the normally closed to the open position. This switch is wired directly to the

* or 0 v for a positive logic system.

interface so that the switch position can be sensed and is normally used to signal the computer that the user of the pen desires to "write" on the screen. If the pen is pressed against the display screen, the pen switch will be in the open position and a gate on the interface card will pull to -3 volts. Upon issuing DPSPD, the computer will skip the following instruction.

4.2.9.3 Maintenance

In the light pen fails to operate properly, make the following checks before performing detailed checks of the various components:

1. See that the computer program is operating properly.
2. Make sure that the adjustment of the sensitivity control is adequate for the oscilloscope intensity level.
3. Check for dirt obstructing entry of light into front of pen barrel.
4. Make sure that 110 volts AC are being supplied to the high voltage power supply and that the fuse is good.
5. Check connecting electrical cable between pen and power supply chassis.
6. Check connecting cable between power supply chassis and computer interface.

If the above checks do not reveal the trouble, perform the following checks:

1. If pen does not work at all:

   a. Check output of power supply using voltmeter. Output should be 1000 volts. Note that the voltage is negative with respect to ground. Use caution when making a measurement, since the supply can deliver enough current to provide a resounding shock when measured across output terminals of supply.

   b. With all cables connected and the computer on, check the amplifier supply voltages on the light pen chassis. Pin A should be at +12 volts DC and pin B should be at -12 volts.

   c. Loosen the fiber optics barrel from the photomultiplier light cover using an Allen wrench and remove the barrel. Aim the pen barrelat a light source and make sure that at least 12 fibers appear brightly lighted at the opposite end. Poorly illuminated fiber ends indicate dirt in pen tip or damaged fibers. Upon reinserting the barrel into the photomultiplier light cover, push it in firmly so that contact is made with envelope of the photomultiplier and tighten the set screw with an Allen wrench.

2. If no trouble has yet been found, detailed checks should be made on the electronics to isolate the failure.

   a. Generate a spot near the center of the screen using the program written for your particular computer and interface.

   b. Adjust the intensity to produce a relatively bright spot.

   c. Position the pen over the spot and firmly attach it to an appropriate support. The barrel of the pen should be perpendicular to the display screen.

   d. With an oscilloscope equipped with a high impedance probe, look at the signal on pin 10 of the photomultiplier socket (see drawing number 26012). USE EXTREME CAUTION, SINCE THERE ARE 1,000 VOLTS ON THE ADJACENT PIN!! The signal at this point should be a negative going pulse a few microseconds long with an amplitude between .25 and 5 volts. This same signal should appear differentiated on pin F of the amplifier socket. Adjust the position of the light pen or use the centering controls on the scope to give maximum signal.

   e. If the photomultiplier signal appears satisfactorily, move the probe to pin D* of the amplifier socket. The signal on this pin should be .2 to 10 microseconds wide and should go from ground to -3 volts. If no signal appears, refer to the installation section for adjustment instructions.

   f. If a satisfactory signal appears at output of the amplifier, put the scope probe on the corresponding pin of the Display Scope Control. The signal at this pin should be identical to that found at pin D on the amplifier socket.

   g. If the signal is satisfactory at this pin, the trouble is in either the interface, the computer, or the computer program.

3. If the optical signal is all right but the switch does not work:

   a. Disconnect miniature coaxial connector which connects pen write switch to chassis, and with an ohmmeter set on low resistance scale, measure the resistance between the center pin and outside of the pen connector. The meter should read a short circuit with the actuator in the normal position and an open circuit with the actuator depressed.

   b. If this check indicates a satisfactory operation, replace connector and repeat test with probe at the display scope control. If this test fails, the trouble is in the connecting wires between the coaxial connector and the control.

* Or pin S for positive logic interfaces.

4.2.10 Functional Control Panel

The TP-5000 Functional Control Panel consists of 3 sections—the PDP-11 computer interface, the control panel logic, and the panel of switches and indicators. This manual will describe each of these sections separately.

4.2.10.1 PDP-11 Interface

Summary:

FCPCSØ	764Ø5Ø	Functional Control Panel Control/Status register for even numbered panels.
FCPCS1	764Ø52	Functional Control Panel Control/Status register for odd numbered panels.
FCPSEL	764Ø54	Functional Control Panel switch groun SELect register.
FCPDAT	764Ø56	Functional Control Panel DATa register.
FCPVØ	ØØØ31Ø	Functional Control Panel interrupt Vector address for even numbered panels.
FCPV1	ØØØ314	Functional Control Panel interrupt Vector address for odd numbered panels.

The PDP-11 interface to the TR-5000 FCP consists of two cards, a TP-41 address decoder and interrupt processor, and a TP-43 interface card.

The TP-41 card is logically identical to DEC's M105 address decoder and DEC's M782 interrupt control card combined. It plugs into slots E and F of the small peripheral space in the PDP-11 or a DD11 small peripheral block. The FCP address and interrupt vectors are determined only from this card. If desired, the above DEC cards can be substituted for the TP-41. A complete description of this card can be found in the Tennecomp logic card manual. The DEC cards are described in the PDP-11 Unibus interface manual, publication number DEC-11-HIAB-D.

The TP-43 card completes the interface to the PDP-11. This card contains interface logic to buffer the control panel data bus with the Unibus, strobe logic to generate data out strobe and switch group select strobes and data enable input strobe, and interrupt logic. For the detailed description of this card, refer to print number 114-000101.

The interface to the 8 Control Panel BUS lines (labeled CPBUSØ thru CPBUS7) and the 8 PDP-11 data lines (labeled LDØØ thru LDØ7) consists of IC's numbered 1 thru 10. Data is gated to the control panel by a single-shot (IC 12)

which is triggered by an output command and select 4 or 6 (SEL4 or SEL6). This single-shot holds the data for about 600 ns. by holding slave sync inhibit (LSSINH) low. The data is strobed into the proper register in the control panel by the trailing edge of this pulse. Strobes produced by this pulse are SWGSEL (SWitch Group SELect) for address 4 (SEL4), and LAMPSL (LAMP SeLect or data output to the control panel) for address 6 (SEL6).

The data-in strobe is generated when the IN (input) line and SEL6 (select 6) line both are true. This enables the PDOB (Put Data On the Bus) line which gates the selected switch group to the control panel bus. A single-shot (IC11) is triggered by this signal which holds SSINH (Slave Sync INHibit) low for about 600 ns. to give the bus lines time to settle.

Two interrupts are used in this interface. Interrupt A is enabled by bit 6 of select 0 address; interrupt B, by bit 6 of select 2 address. When a control panel has an interrupt pending, the appropriate line is held low (PBINTA for even-numbered panels—panels 0, 2, 4, etc.; PBINTB for odd-numbered panels). This line is connected to INTA or INTB of the interrupt control card and will cause an interrupt if the appropriate enable line is high. The status of the interrupt can be read on bit 7 of SEL0 and SEL2 for even and odd panels.

Interrupt level is selected by jumpers on this card. Levels 4 thru 7 are possible. Level 4 is shown on print 114-000101.

This interface card can drive any combination of up to 256 groups of 8 lights or other outputs and up to 256 groups of 8 switch contacts or other inputs. In normal operation, there will be a certain number of panels (up to 16) which are selected by bits 4 thru 7 of address 764054, each of which contains up to 16 groups of 8 contacts or lamps, including one status word for interrupt processing. Such an arrangement is described next.

4.2.10.2 Control Panel Interface

The Control Panel Interface consists of two DEC blocks with 15 single-height logic cards. A card location chart is found on print number 130-000100. The logic diagram is on print number 114-000100. This interface is designed for 8 lamps and 16 groups of 8 switch contacts or inputs, including one group for the 8 lamps, and special logic for contact bounce elimination and interrupt control for 8 pushbuttons. There is also one status word.

Sheet 1 contains the logic for switch group selection and lamp register and drivers. Data comes in on the bi-directional data bus (CPBUSn) to the two registers and is strobed to the proper register by the appropriate strobe. Data is strobed to the select register by SWGSEA. When the address of the lamps (012) is loaded

in the select register (board A5), gate B6 at the top of the page is enabled. If a lamp strobe (LAMPSA) should now occur, data on the bus would be strobed into the lamp register. The lamp register is connected directly to the lamp drivers; therefore, whatever is in this register will be displayed on the lamps. The lamp register is also connected to switch group input number 012. Thus, the lamps may be read as well as controlled by the computer. The 4 most significant bits of the select register are gated by gate B5 to produce THUNIT (this unit selected). This signal enables the lamp register (when selected) and all input gates.

The two connectors, pushbutton logic, and data input enable logic are on sheet 2. Lines from the computer come in on the connector at A7 and are buffered and connected to the connector at A8. The 8 CPBUSn lines are not buffered, but are connected directly between connectors. The pushbutton logic consists of 8 buffers, an 8-input AND gate, and a flip-flop used to eliminate contact bounce at the interrupt circuit. When a button is pressed, the flip-flop at B5 is set (B5D2 goes true) and B6E1 goes to ground. This enables bit 7 of word 0 to be true. This bit is reset when the pushbuttons are read or when all buttons are released. The output of this gate is "ORed" with the interrupt line from other panels which are connected in series with this one. When more than 2 panels are used, the programmer must interrogate the status of each panel (odd or even only, as appropriate) to determine which has caused the interrupt. He must then read the pushbuttons to clear the interrupt for that panel so that other panels may interrupt. Note that only one panel in the interrupt string may interrupt at any one time—that is, if a button is depressed, the interrupt line goes low. As this is an "OR" line, other panels with buttons depressed will not be recognized until this interrupt line returns high; thus the need for the interrupt clear flip-flop at B6. This flip-flop is set when B6N1 goes low as a result of reading the pushbuttons and is reset when all buttons are released.

The two interrupt lines at connectors A7 and A8 are rotated so that every other panel is connected to each line.

The data in strobe (PDOB) is "ANDed" with the "this unit" (THUNIT) line to produce the input (to the computer) strobe PDOBA which enables the 8 input gates on sheets 3 and 4. Both of these sheets are almost identical; sheet 3 for bits 0 thru 3, and sheet 4 for bits 4 thru 7. Cards A1 thru A4 and B1 thru B4 are 16-input multiplexers. An open collector NAND gate is also on 3 of the cards to be used for driving the Control Panel Data Bus. The multiplexers accept a low true signal from each of the switch contacts and 4 decode lines from the switch select register. These decode lines select one of 16 input gates to be enabled to the output, where it is then gated with PDOBA to the control panel bus. There are 16 possible 8-bit words. Table 1 is a list of all bits assigned in this configuration.

TABLE 1

Control Panel Switch Bit Assignments

Switch Group Number (octal)	BIT NO. Ø	1	2	3	4	5	6	7	
ØØ	Ø	Ø	Ø	Ø	Ø	Ø	Ø	status	
Ø1	SWØ	SW1	SW2	SW3	SW4	SW5	SW6	SW7	Toggle Switches
Ø2	Ø-1	Ø-2	Ø-4	Ø-8	1-1	1-2	1-4	1-8	Rotary Switches Ø & 1
Ø3	2-1	2-2	2-4	2-8	3-1	3-2	3-4	3-8	Rotary Switches 2 & 3
Ø4	1-1	1-2	1-4	1-8	Ø	Ø	Ø	Ø	Thumbwheel 1
Ø5	3-1	3-2	3-4	3-8	2-1	2-2	2-4	2-8	Thumbwheels 2 & 3
Ø6	5-1	5-2	5-4	5-8	4-1	4-2	4-4	4-8	Thumbwheels 4 & 5
Ø7	7-1	7-2	7-4	7-8	Ø	Ø	Ø	Ø	Thumbwheel 7
1Ø	9-1	9-2	9-4	9-8	8-1	8-2	8-4	8-8	Thumbwheels 8 & 9
11	11-1	11-2	11-4	11-8	1Ø-1	1Ø-2	1Ø-4	1Ø-8	Thumbwheels 10 & 11
12	LØ	L1	L2	L3	L4	L5	L6	L7*	Lamps
13	PBØ	PB1	PB2	PB3	PB4	PB5	PB6	PB7	Pushbuttons
14 thru 17	0	0	0	0	0	0	0	0	Not Used

* Lamp 7 is not present in this configuration, but it can be set and read by the computer.

4.2.10.3 Panel

Figure 4.2.10-1 is a view of the front of the panel. It contains the following switches and indicators:

8 Toggle switches
4 Rotary switches
10 Decades of Thumbwheel switches
8 Pushbutton switches
7 Indicator lamps.

The toggles and pushbutton switches are simply on-off switches. When the toggle is in the up position or the pushbutton is depressed, a 1 can be read into the computer. The rotaries are 12-position binary coded switches with code 0000 at "9 o'clock" position and 1011 at "8 o'clock" position. The thumbwheels are 10-position BCD switches. Figure 4.2.10-1 indicates the switch number which corresponds to the bit position in table 1.

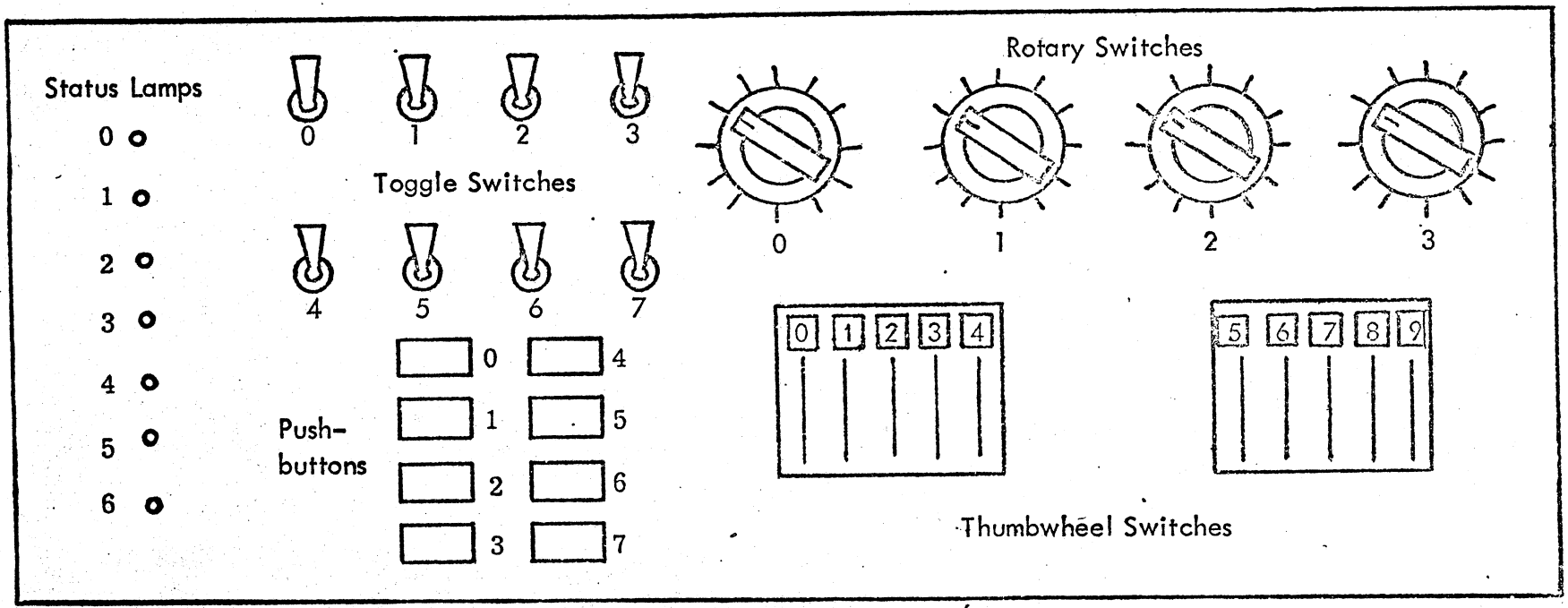
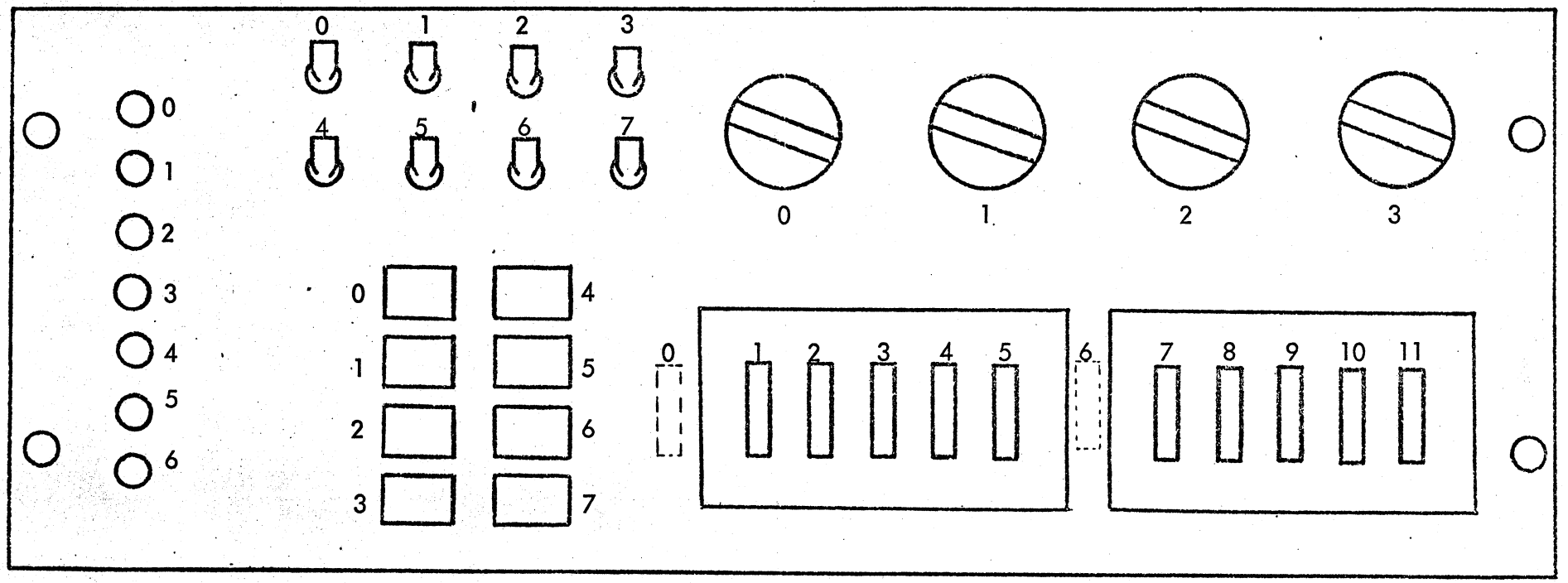


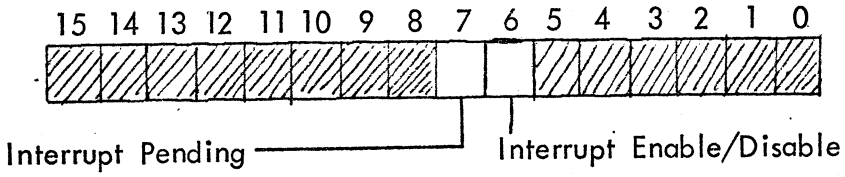
Figure 1. Functional Control Panel
Switch Arrangement



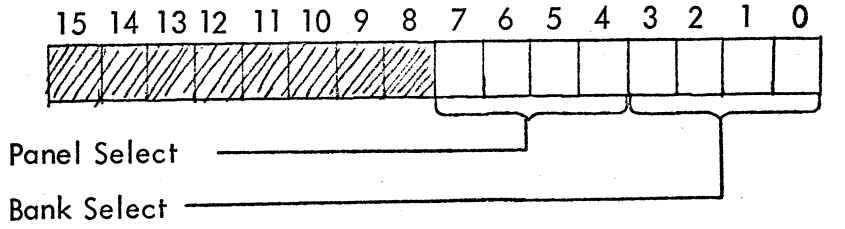
FUNCTIONAL CONTROL PANEL SWITCH ASSIGNMENTS

FUNCTIONAL CONTROL PANEL PROGRAMMING

FCPCSR (164050)

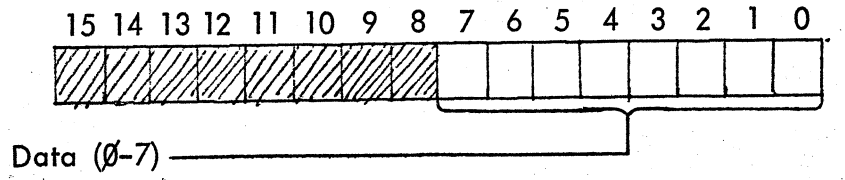


FCPSEL (164054)



Bank Select Ø	-	Interrupt Status
Bank Select 1	-	Toggle Switches
Bank Select 2	-	Rotary Switches Ø & 1
Bank Select 3	-	Rotary Switches 2 & 3
Bank Select 4	-	Thumbwheel 1
Bank Select 5	-	Thumbwheels 2 & 3
Bank Select 6	-	Thumbwheels 4 & 5
Bank Select 7	-	Thumbwheel 7
Bank Select 8	-	Thumbwheels 8 & 9
Bank Select 9	-	Thumbwheels 10 & 11
Bank Select 10	-	Lamps
Bank Select 11	-	Pushbuttons

FCPDAT (164056)



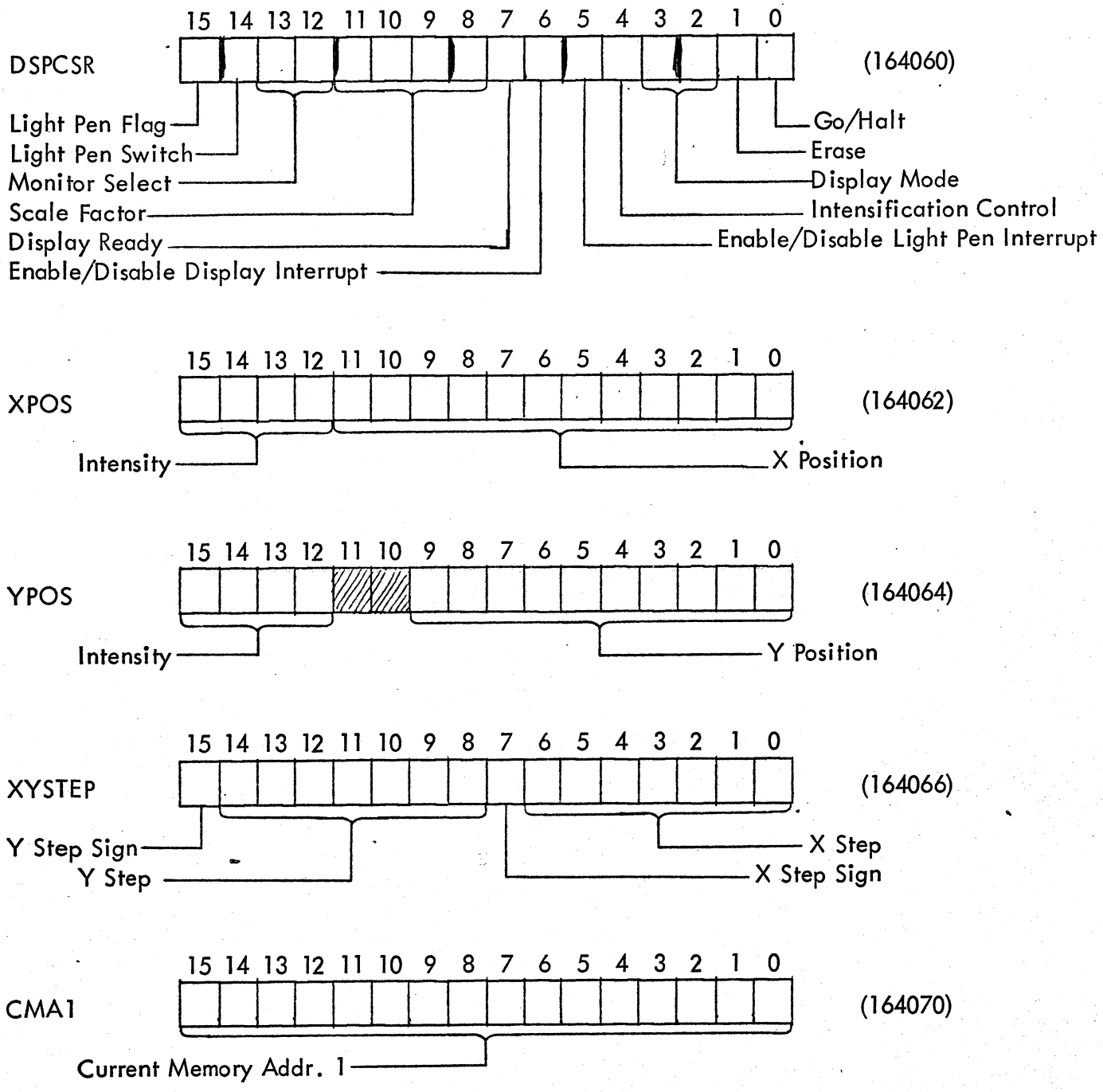
The data register reflects the following information when the associated bank is selected:

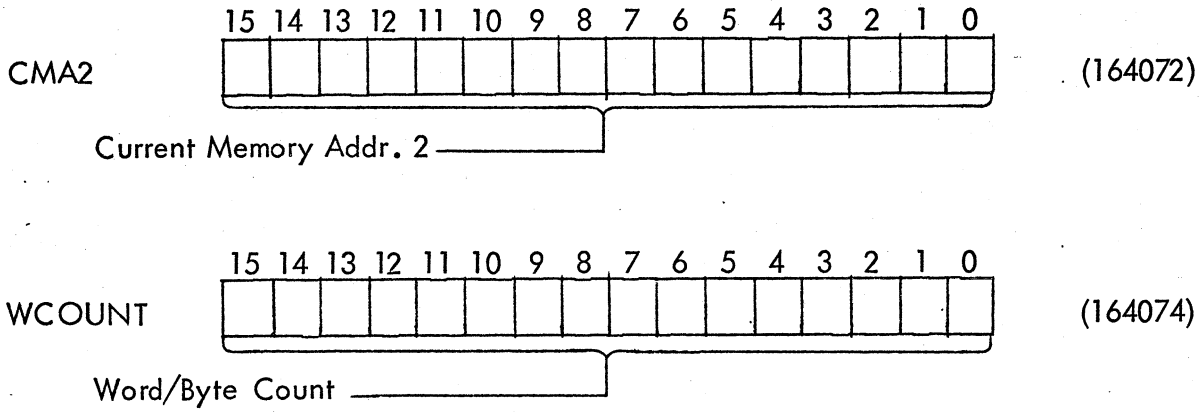
Bank #	Data
0	Bit 0 is interrupt status; 1-7 not used.
1	Bits 0-7 correspond to toggle switches 0-7.
2	Bits 0-3 → rotary 0; bits 4-7 → rotary 1
3	Bits 0-3 → rotary 2; bits 4-7 → rotary 3
4	Bits 4-7 → thumb 0*; bits 0-3 → thumb 1

Bank #	Data
5	Bits 4-7 → thumb 2; bits 0-3 → thumb 3
6	Bits 4-7 → thumb 4; bits 0-3 → thumb 5
7	Bits 4-7 → thumb 6*; bits 0-3 → thumb 7
8	Bits 4-7 → thumb 8; bits 0-3 → thumb 9
9	Bits 4-7 → thumb 10; bits 0-3 → thumb 11
10	Bits 0-6 correspond to lamps 0-6 (Read/Write)
11	Bits 0-7 correspond to pushbuttons 0-7

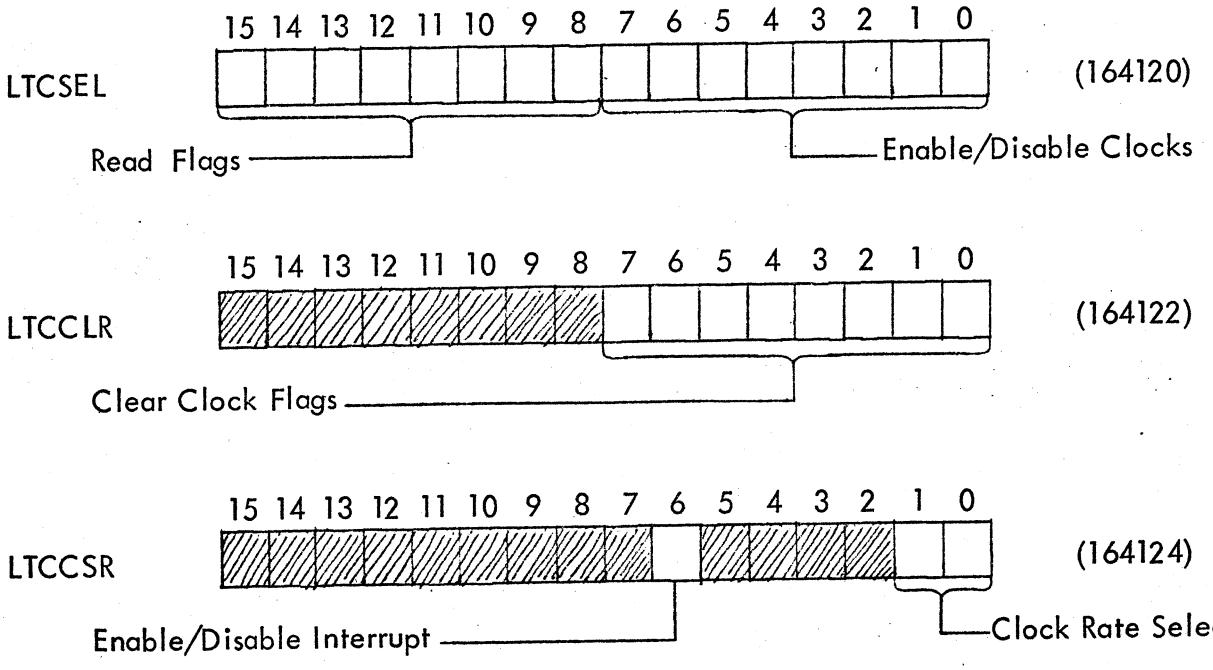
* Thumbwheel switches 0 & 6 available only on 12-digit panels.

TP-1420/11 DISPLAY CONTROL PROGRAMMING




CMA2
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
(164072)
Current Memory Addr. 2
WCOUNT
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
(164074)
Word/Byte Count

LIVE TIME CLOCKS PROGRAMMING

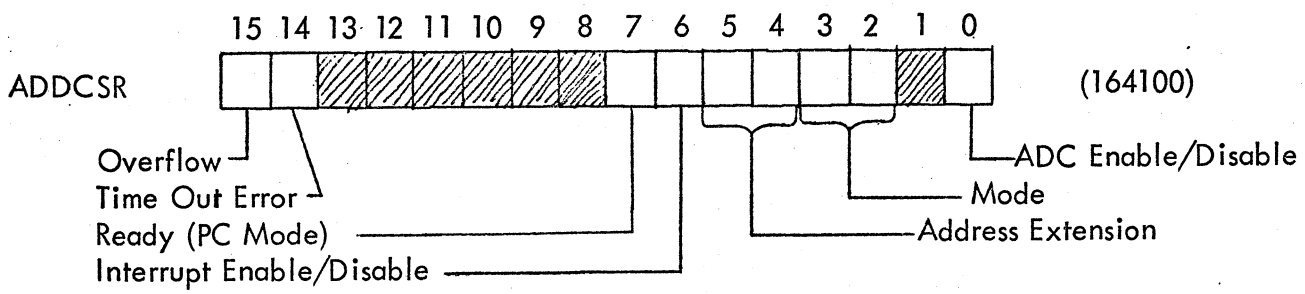


Clock rates are:

Bits 1 & 0	Rate	
00	1000 Hz	(1 ms)
01	100 Hz	(10 ms)
10	10 Hz	(.1 s)
11	1 Hz	(1 s)

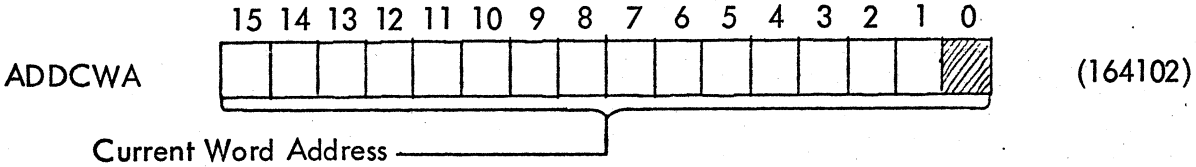
VECTOR = 300

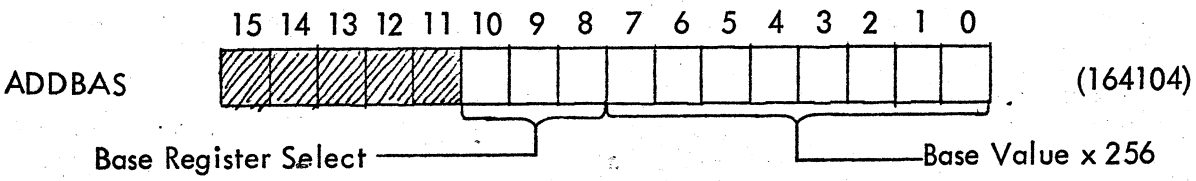
TP-1517/11/P ADC CONTROL (ADD-1) PROGRAMMING

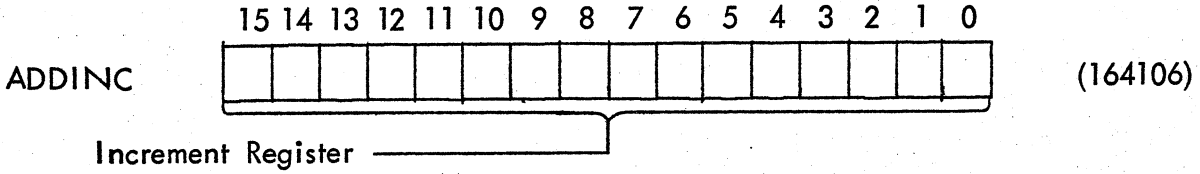


Modes:

00	Add-1 (NPR)
01	Add-1 (PC)
10	Multiscale
11	Not Used







TP-1517/11/P ADC CONTROL (LIST) PROGRAMMING