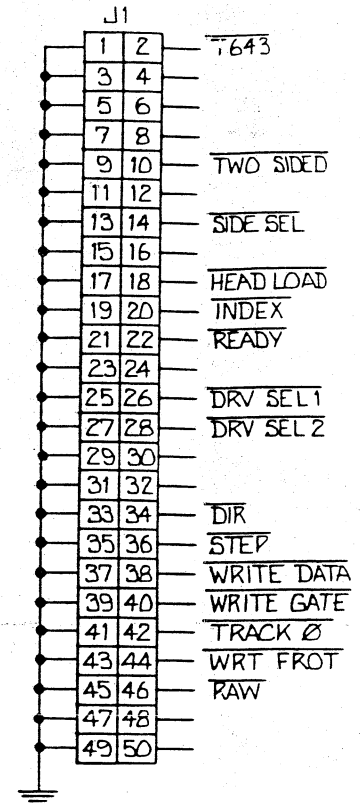
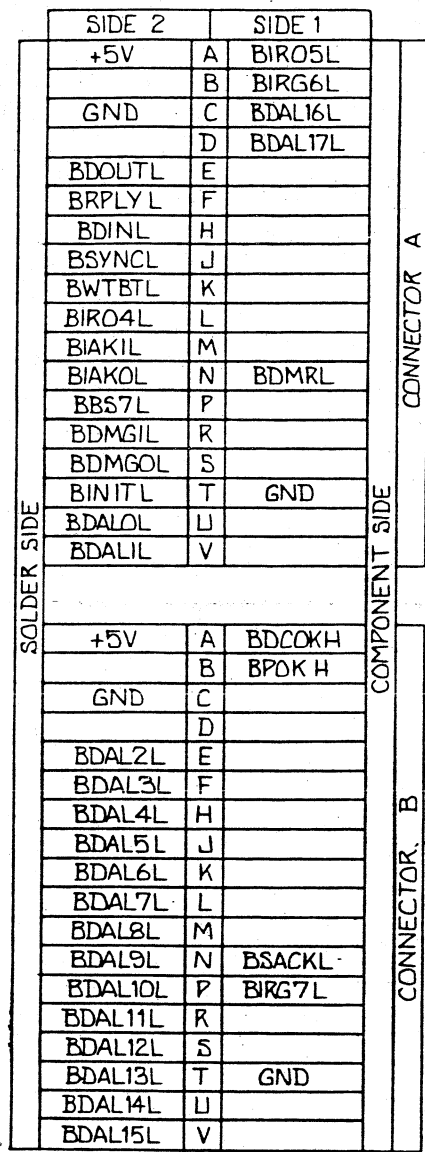


LAST REFERENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U71
CAPACITOR	C37
RESISTOR	R24
RESISTOR MODULE	RU2
TRANSISTOR	G4
DIODE	CR5
CONNECTOR	J1
OSCILLATOR	Y1

REF. DESIG.	GATES USED PER TOTAL	PART NUMBER
U12	NOT USED	SPARE
U29	2 / 4	74S32



ADDRESS	STANDARD	ALTERNATE
DEVICE	177170	177174
VECTOR	264	270

PRIORITY LEVEL CONFIGURATION

PRIORITY LEVEL	ASSERT LEVEL	MONITOR LEVEL	JUMPER											
			34/35	34/33	40/41	39/40	31/32	31/30	43/42	43/44	37/36	37/36		
4*	4	5,6	OUT	IN	OUT	IN	IN	OUT	OUT	IN	IN	OUT		
5	4,5	6	OUT	IN	OUT	IN	OUT	OUT	OUT	IN	OUT	IN		
6	4,6	7	IN	OUT	OUT	IN	OUT	IN	IN	OUT	IN	OUT		
7	4,6,7	NONE	IN	OUT	IN	OUT	OUT	IN	IN	OUT	OUT	IN		

* FACTORY PRESET

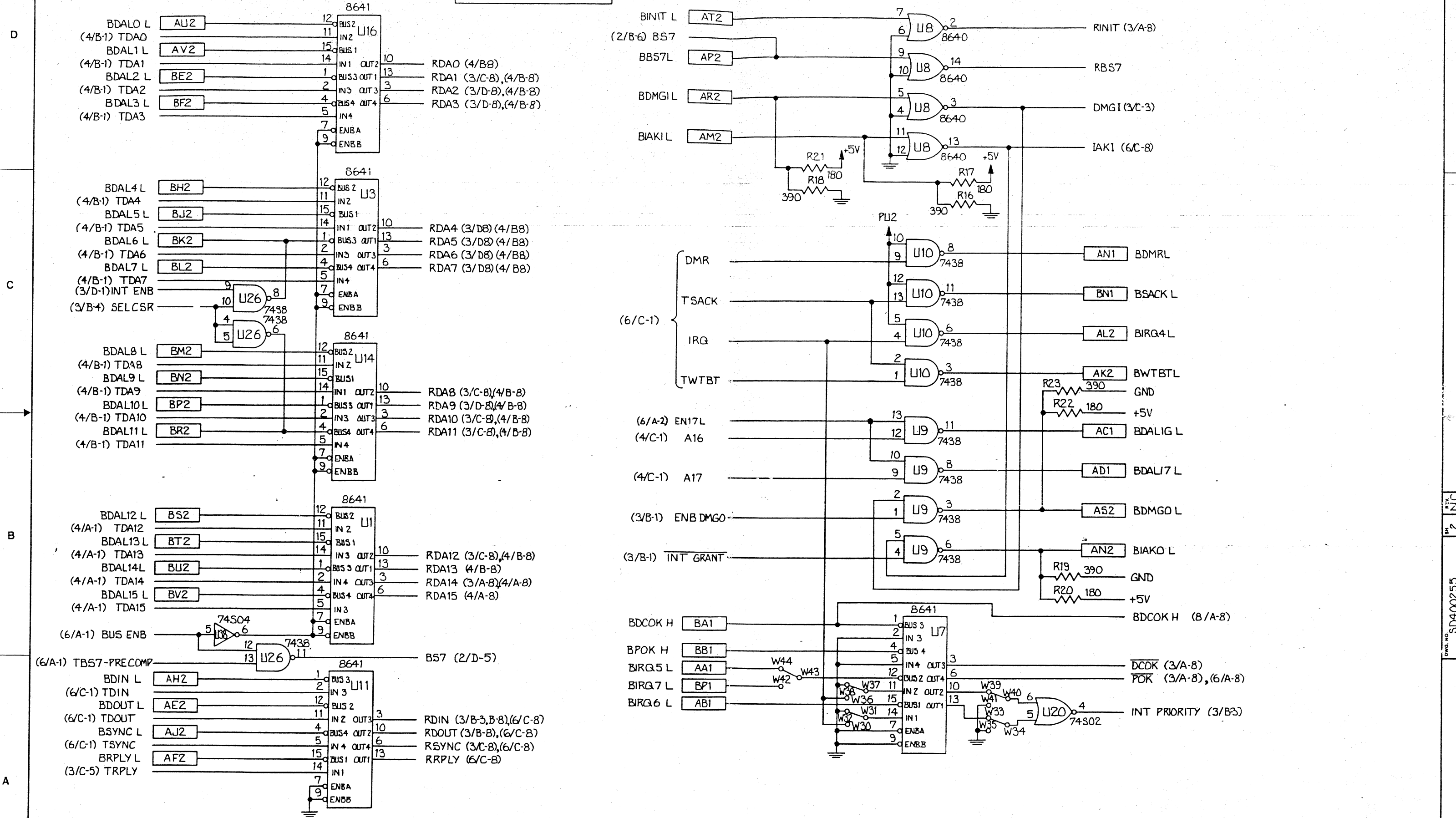
MISCELLANEOUS OPTIONS

OPTION	DRIVE SELECT		SIDE SELECT		WIRE CURRENT	BOOTSTRAP	WRITE PRECOMP	FACTORY TEST			DEVICE READY	22 BIT ADDRESS						
	3/2	1/2	6/7	6/5	6/8	9 / 10	26/25	26/27	18/19	18/17	15/16	13/14	20/21	11/12	47/49	49/48	45 / 46	
BOOTSTRAP ENABLED							IN	OUT										
BOOTSTRAP ** DISABLED							OUT	IN										
WRITE PRECOMP ** ENABLED									IN	OUT								
WRITE PRECOMP DISABLE									OUT	IN								
WRITE CURRENT CONTROL ENABLED						IN												
WRITE CURRENT ** CONTROL DISABLED						OUT												
SINGLE OR DOUBLE ** SIDED DRIVERS	OUT	IN	IN	OUT	OUT													
ONE DOUBLE SIDED DRIVE DRIVE 0 = SIDE 0 DRIVE 1 = SIDE 1	IN	IN	OUT	IN	OUT													
STANDARD READY															OUT	IN		
TRUE READY															IN	OUT		
ENABLE 22 BIT ADDRESSING																		OUT
DISABLE 22 BIT ADDRESSING																		IN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES : 1/64 .XX ± .020 °0'30 .XXX ± .010		THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO SIGMA INFORMATION SYSTEMS, INC. AND MAY NOT BE REPRODUCED OR USED FOR OTHER THAN MAINTENANCE PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM AN OFFICER OF THE ABOVE FIRM.			
MATERIAL	FINISH	DRAWN: <i>[Signature]</i> J2-29-82 CHECKED:	TITLE: SCHEMATIC DIAGRAM - SDC-RXV31, FLOPPY CONTROLLER		
NEXT ASSY.	USED ON	ENGINEER	APPROVED	APPROVED	APPROVED
APPLICATION	DO NOT SCALE DRAWING	SCALE NONE		WORK ORDER NO.	SHEET 1 OF 8

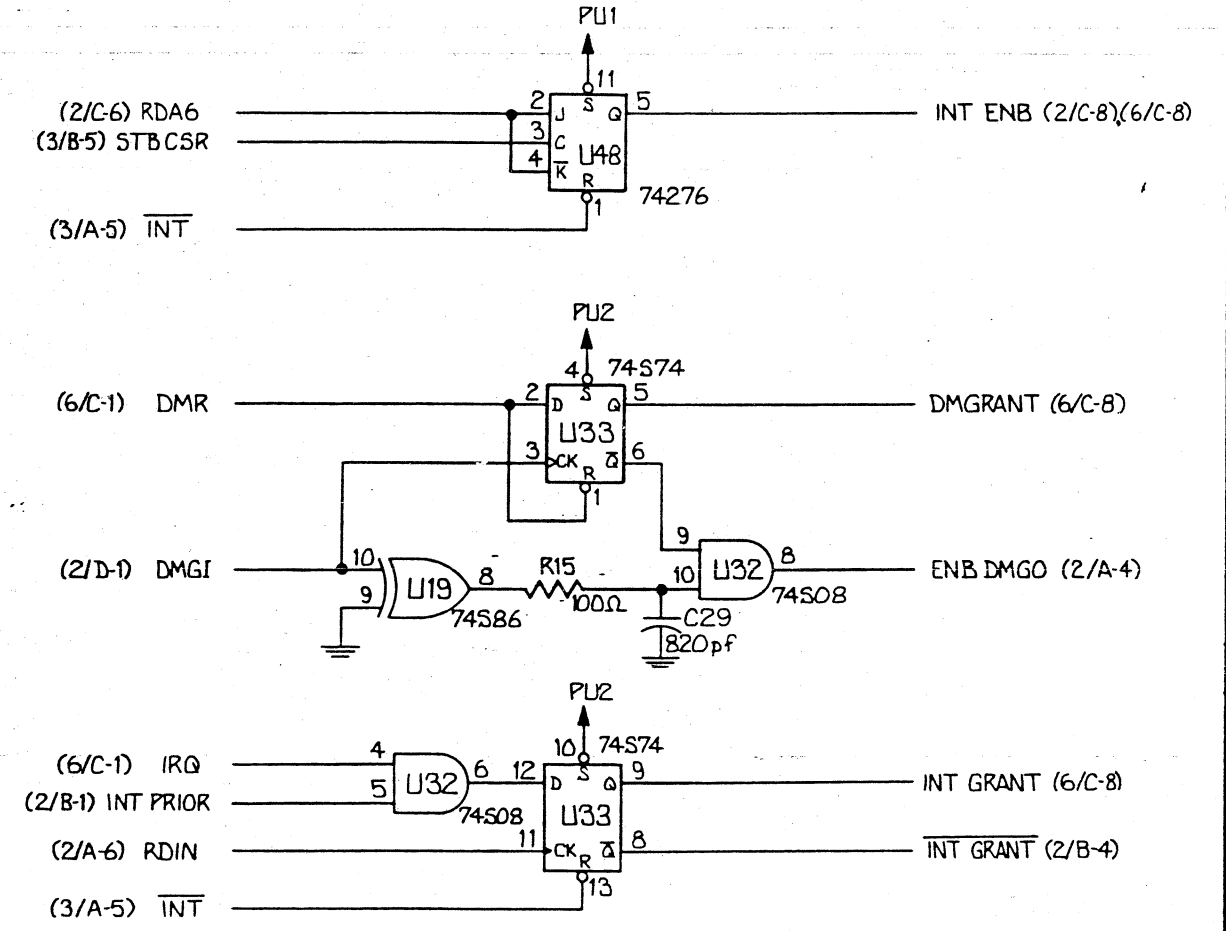
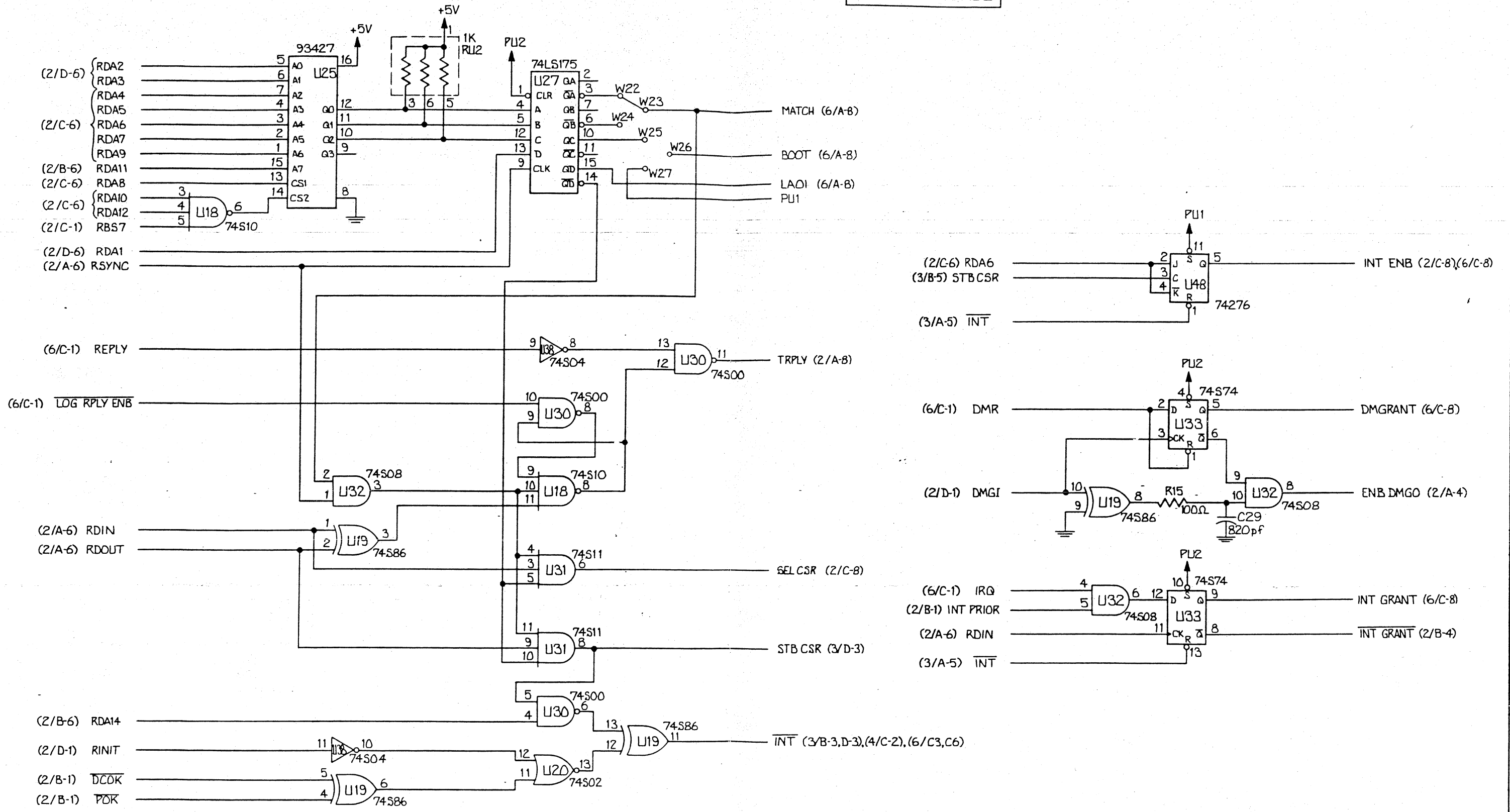
DWG NO SD400255

Q BUS INTERFACE



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

Q BUS CONTROL

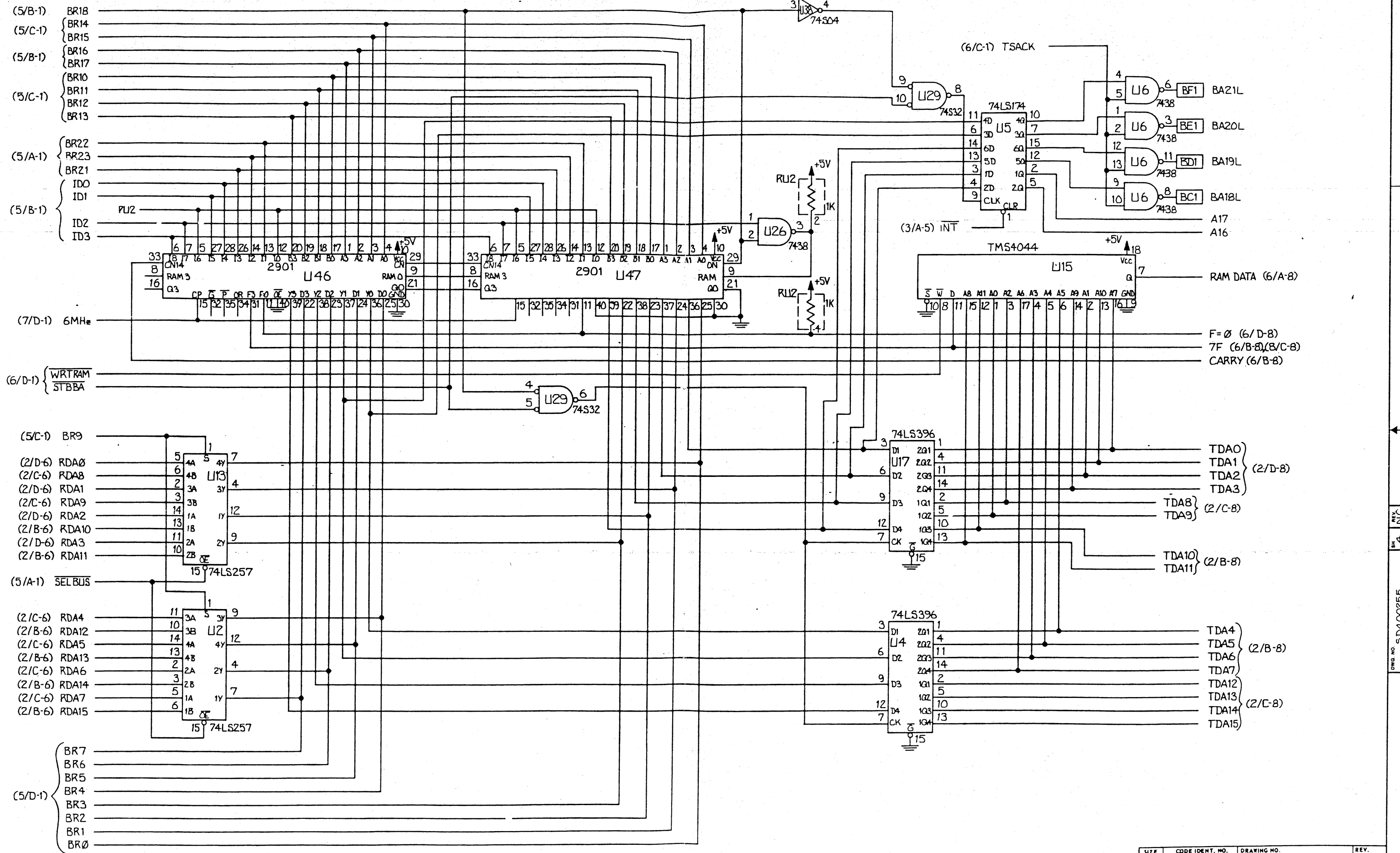


DRAWING NO. SD400255 REV. 3 NC

SIZE D	CODE IDENT. NO.	DRAWING NO. SD400255	REV. NC
SCALE NONE	WORK ORDER NO.	SHEET 3 OF 8	

MUP-8 BIT

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



D

D

C

C

B

B

A

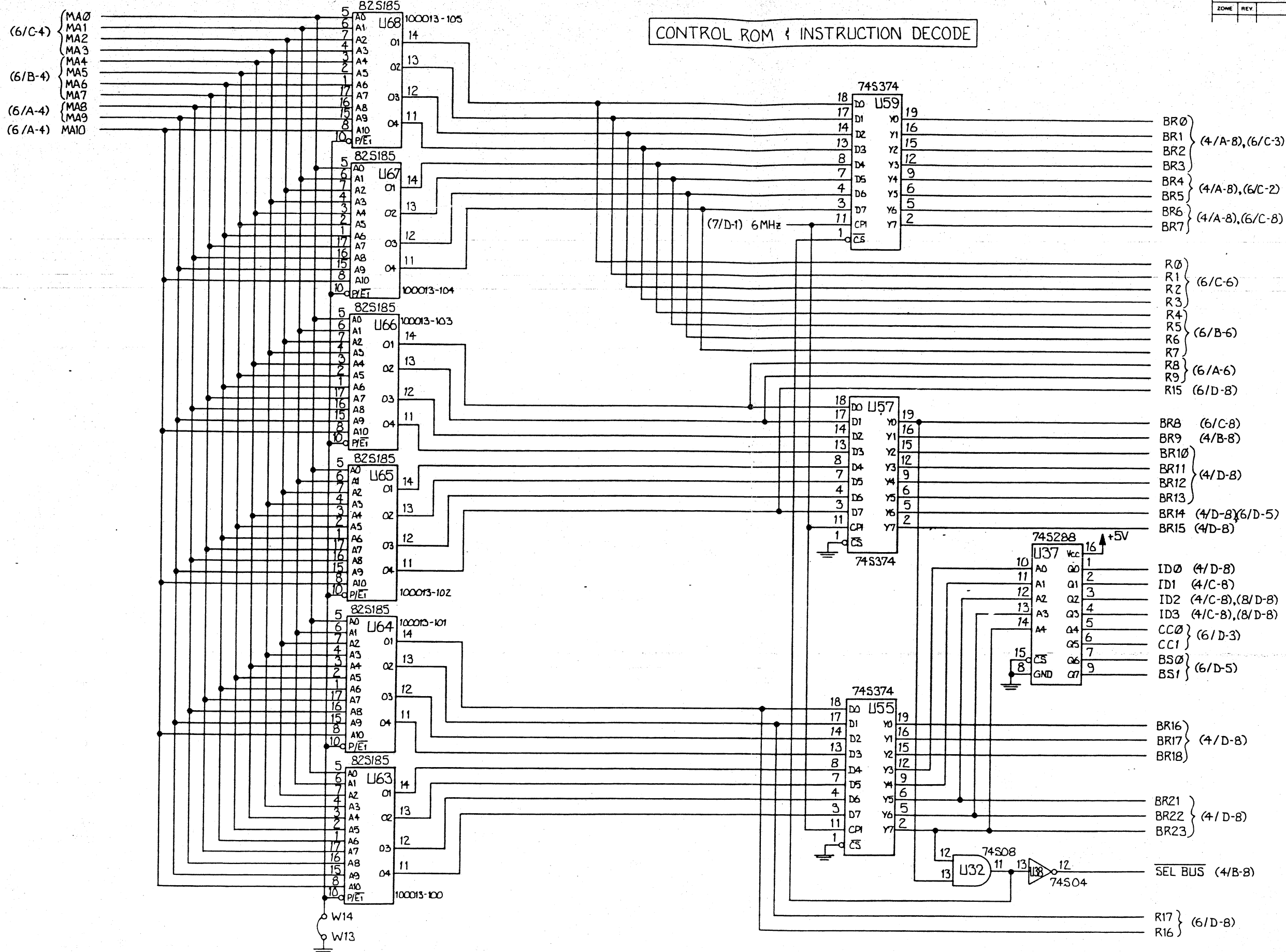
A

DWG. NO. 5D400255

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		5D400255	N.C
SCALE NONE		WORK ORDER NO.	SHEET 4 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

CONTROL ROM & INSTRUCTION DECODE



- BR0
- BR1 } (4/A-8), (6/C-3)
- BR2
- BR3
- BR4 } (4/A-8), (6/C-2)
- BR5
- BR6 } (4/A-8), (6/C-8)
- BR7

- R0
- R1 } (6/C-6)
- R2
- R3
- R4
- R5 } (6/B-6)
- R6
- R7
- R8 } (6/A-6)
- R9
- R15 } (6/D-8)

- BR8 } (6/C-8)
- BR9 } (4/B-8)
- BR10
- BR11 } (4/D-8)
- BR12
- BR13
- BR14 } (4/D-8), (6/D-5)
- BR15 } (4/D-8)

- ID0 } (4/D-8)
- ID1 } (4/C-8)
- ID2 } (4/C-8), (8/D-8)
- ID3 } (4/C-8), (8/D-8)
- CC0 } (6/D-3)
- CC1
- BS0 } (6/D-5)
- BS1

- BR16 } (4/D-8)
- BR17
- BR18

- BR21 } (4/D-8)
- BR22
- BR23

SEL BUS (4/B-8)

- R17 } (6/D-8)
- R16

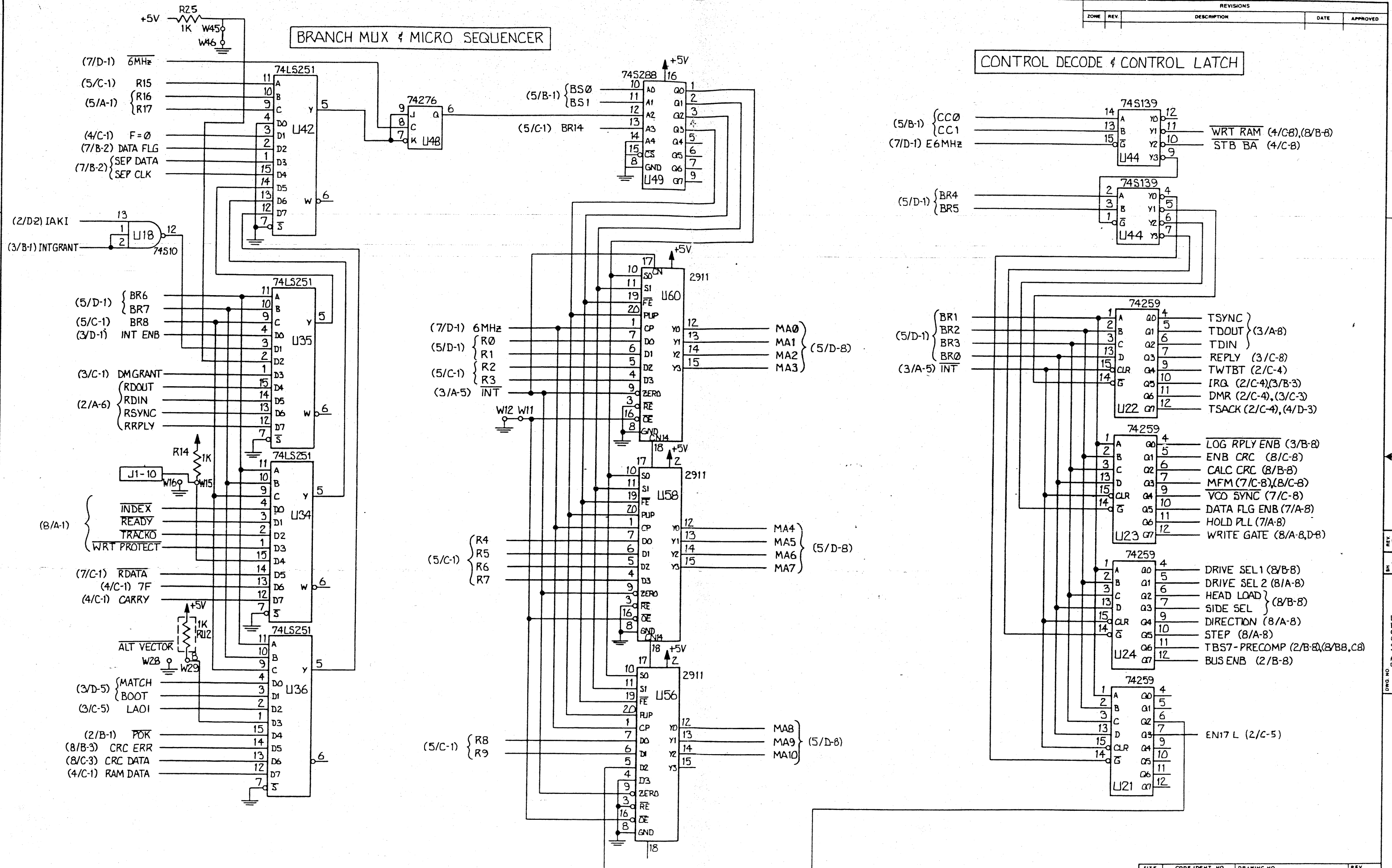
SIZE D	CODE IDENT. NO.	DRAWING NO. SD400255	REV. NC
SCALE NONE	WORK ORDER NO.	SHEET 5 OF 8	

DWG NO. SD400255 REV. 5 NC

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

BRANCH MUX & MICRO SEQUENCER

CONTROL DECODE & CONTROL LATCH



(7/D-1) 6MHz
 (5/C-1) R15
 (5/A-1) {R16, R17}
 (4/C-1) F=0
 (7/B-2) DATA FLG
 (7/B-2) {SEP DATA, SEP CLK}

(5/D-1) {BR6, BR7, BR8}
 (5/C-1) BR8
 (3/D-1) INT ENB
 (3/C-1) DMGRANT
 (2/A-6) {RDOUT, RDIN, RSYNC, RRPLY}

(B/A-1) {INDEX, READY, TRACKO, WRT PROTECT}

(7/C-1) RDATA
 (4/C-1) 7F
 (4/C-1) CARRY

ALT VECTOR
 (3/D-5) {MATCH, BOOT}
 (3/C-5) LAOI
 (2/B-1) POK
 (8/B-3) CRC ERR
 (8/C-3) CRC DATA
 (4/C-1) RAM DATA

(7/D-1) 6MHz
 (5/D-1) {R0, R1, R2, R3}
 (5/C-1) R3
 (3/A-5) INT

(5/C-1) {R4, R5, R6, R7}

(5/C-1) {R8, R9}

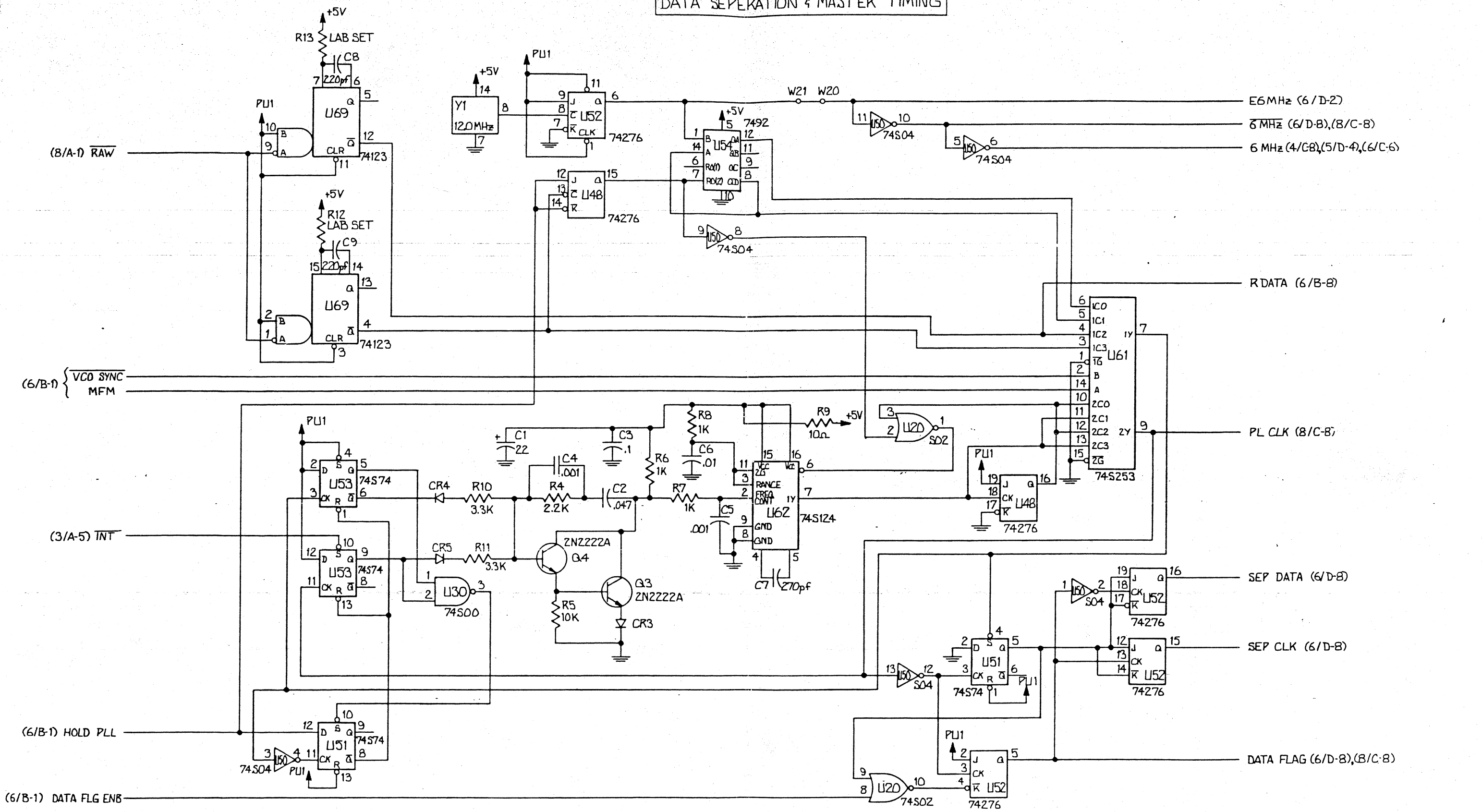
(5/B-1) {CC0, CC1}
 (7/D-1) E6MHz

(5/D-1) {BR4, BR5}

(5/D-1) {BR1, BR2, BR3, BR0}
 (3/A-5) INT

DATA SEPERATION 4 MASTER TIMING

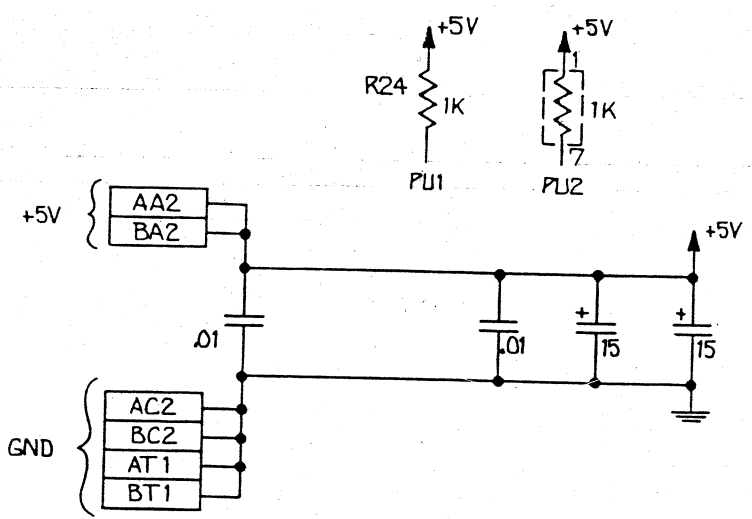
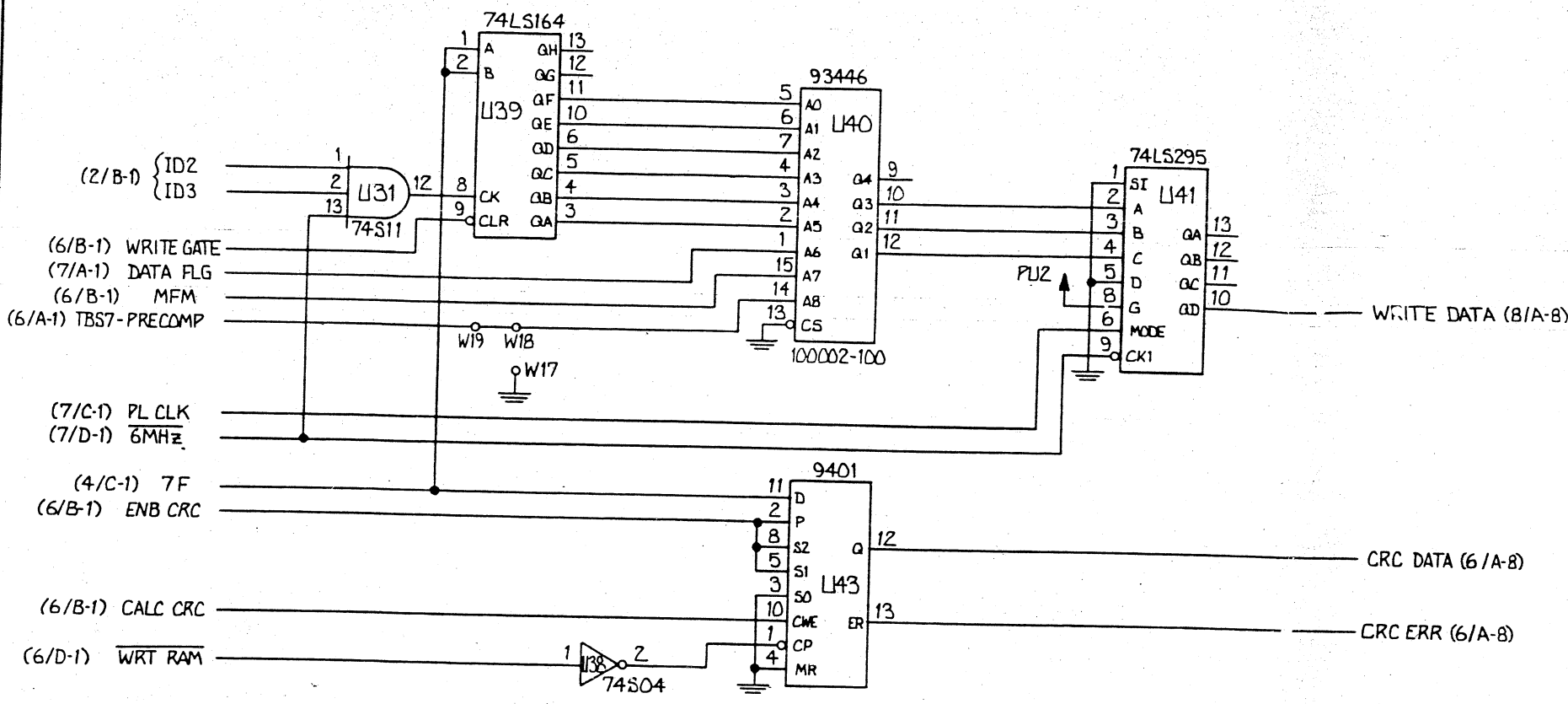
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



SIZE D	CODE IDENT. NO.	DRAWING NO. SD400255	REV. NC
SCALE NONE		WORK ORDER NO.	SHEET 7 OF 8

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

WRITE PRECOMP & CRC GENERATOR



DRIVE INTERFACE

