SCD - DLV11J

Serial Line Interface Manual

Sigma

SCD - DLV11J

Serial Line Interface Manual

Anaheim, California

June 1982 - Revision B

Contents

Tables

Figures

Section 1
General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and operate the SCD-DLV11J serial line interface manufactured by Sigma Information Systems, Anaheim, California.

The material is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the SCD-DLV11J and the specifications for the interface.

Section 2 - INSTALLATION. This section explains the procedures for equipment installation.

Section 3 - PROGRAMMING CONSIDERATIONS. This section conains address selection, register data bit functions, baud rate selection and interfacing.

1.2 GENERAL DESCRIPTION

The SCD-DLV11J is a 4-channel asynchronous serial line interface between the LSI-11 bus and standard I/O devices. The device receives parallel data from the LSI-11 bus, converts it to a serial word and transmits it to the peripheral device. The SCD-DLV11J also receives a serial data word and converts it to parallel data to be output to the LSI-11 bus.

There are two control status registers per channel: a receiver CSR (RSCR) and a transmitter CSR (XCSR). The CSRs maintain information on the status of the operation and contains bits which control the mode of operation. There are two data buffer registers per channel: a receiver (RBUF) and a transmitter (XBUF). The buffer registers buffer data to external devices.

The module has the ability to act as a polled or interrupting peripheral dictated by processor (software) commands. Channel 4 can be configured as a dedicated console device interface.

The SCD-DLV11J responds to any address in the upper 4K peripheral page (160000_8 to 177776_8). It operates in sixteen contiguous registers unless channel 4 is configured as the console device; in which case, twelve contiguous addresses are required, and channel 4 operates at 177560_8 through 177566_8.

All standard baud rates are supported. Each channel has independent baud rate switch selects. Device address and interrupts are also switch selectable per channel.

Each serial line can be jumper selected for compatibility with EIA RS232, RS422 or RS423.

1.3 FEATURES

+ 4-channel asynchronous serial line interface on single dual-wide module
+ Switch selectable addressing and vectors
+ Switch selectable baud rates from 150 to 38.4K
+ Compatible with DEC* operating systems and diagnostics for DLV11J
+ Two CSRs and two BUFs for each of the four channels
+ Data Word Format and interface type are individually jumper selectable for each of the four channels.
+ Responds to peripheral addresses in the upper 4K bank of memory.

*DEC and Q bus are registered trademarks of Digital Equipment Corp.

1.4 SPECIFICATIONS

Power Requirements:	+5VDC @ 1.55A, +12VDC @ 0.70A
Device Address:	Factory preset at 176500-526, Console 177560-566. Switch select alternates at 160000-177776.
Vector Select:	Factory preset at 300-324, Console 60-64. Switch select alternates at 000-776.
Baud Rate:	Each channel independently switch selectable 150, 300, 600, 1200, 4800, 9600, 19.2K and 38.4K baud.
Data Word Format	Each channel jumper selectable.
Data Bits:	5, 6, 7, 8
Parity Mode:	Odd, Even or None
Stop Bits:	1 or 2.
Interface Select:	RS232-C, RS422, RS423. Each chanel independently jumper selectable.
Master Reset:	UART Master Reset on DCOK L or INIT H jumper selectable.
Installation:	Plugs directly into any standard Q bus* slot, observing Q bus rules.
Dimensions:	Single dual-wide board 5.2"W x 8.9"H (13.2cmW x 22.8cmH).
Temperature:	
Operating:	$0^{o}C$ to $50^{o}C$
Storage:	$-40^{o}C$ to $85^{o}C$
Humidity:	10% to 90% noncondensing

Section 2
Installation

2.1 UNPACKING AND INSPECTION

The SCD-DLV11J is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SCD-DLV11J and visually inspect for physical damage. If any damage has occurred contact the factory immediately.

2.2 FACTORY CONFIGURATIONS

Ensure that switches and jumpers are properly selected by referring to the appropriate paragraphs in this section. Refer to Table 2-1 for factory configurations and to Figure 2-1 for switch and jumper locations.

CHANNEL	ADDRESS	REGISTER	VECTOR	REFERENCE
1	176500	RCSR1	300	2.3 (ADDRESS)
	176502	RBUF1		
	176504	XCSR1	304	
	176506	XBUF1		
2	176510	RCSR2	310	
	176512	RBUF2		
	176514	XCSR2	314	
	176516	SBUF2		
3	176520	RCSR3	320	
	176522	RBUF3		
	176524	XCSR3	324	
	176526	XBUF3		
4*	177560	RCSR4	60	2.4 (VECTOR)
	177562	RBUF4		
	177564	XCSR4	64	
	177566	XBUF4		
Baud Rate		9600		2.5
Line Parameters		8 Data bits No Parity 1 Stop bit		2.6
Interface		RS232-C		2.7
UART Operation		Reset on INIT		2.8
*Channel 4 as console device interface				

TABLE 2-1: FACTORY CONFIGURATIONS

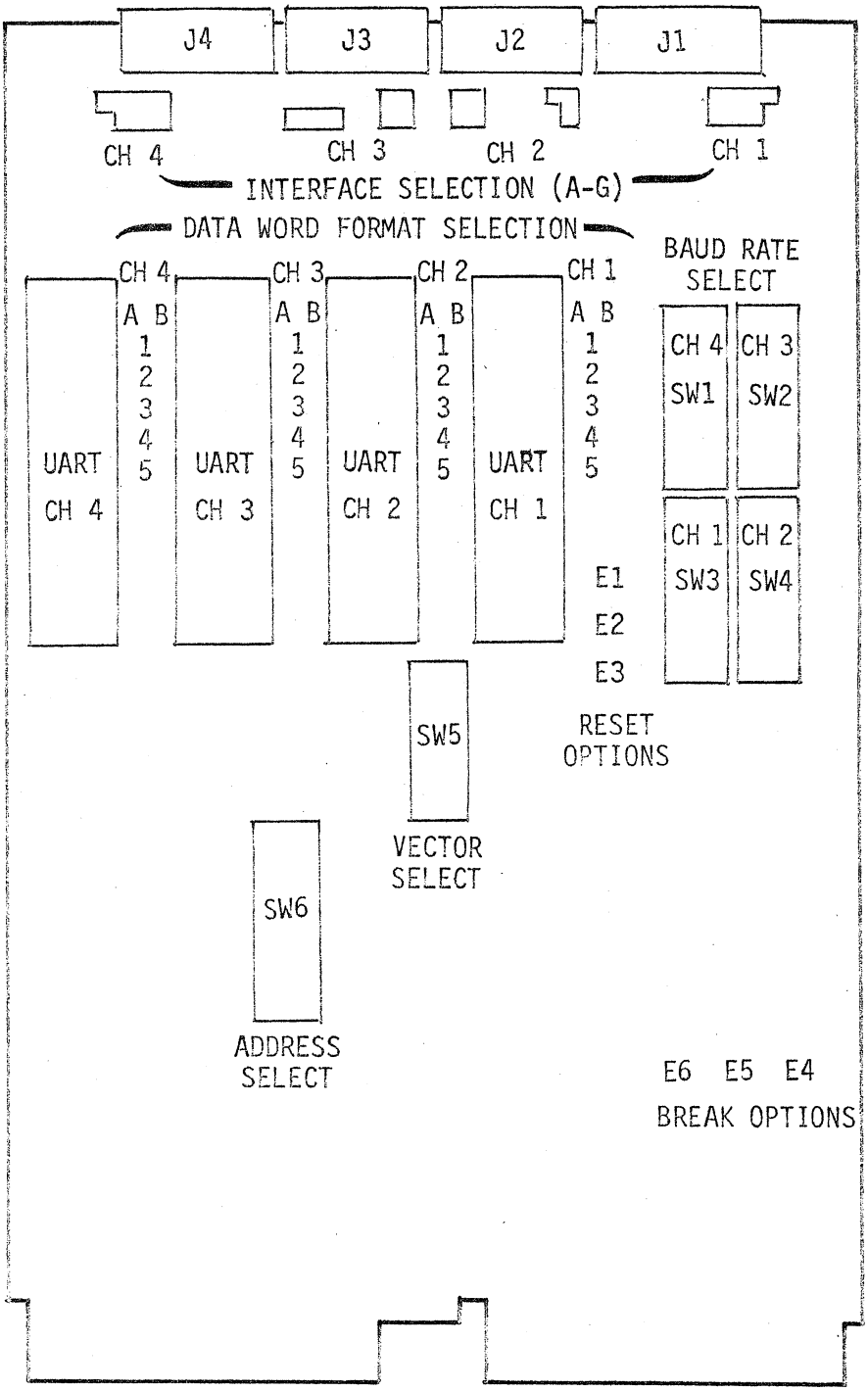


FIGURE 2-1: SWITCH AND JUMPER LOCATIONS

2.3 ADDRESS SELECTION

Address word bit assignments are shown below. Switch 6, positions 1 through 8 control addressing of individual address bits.

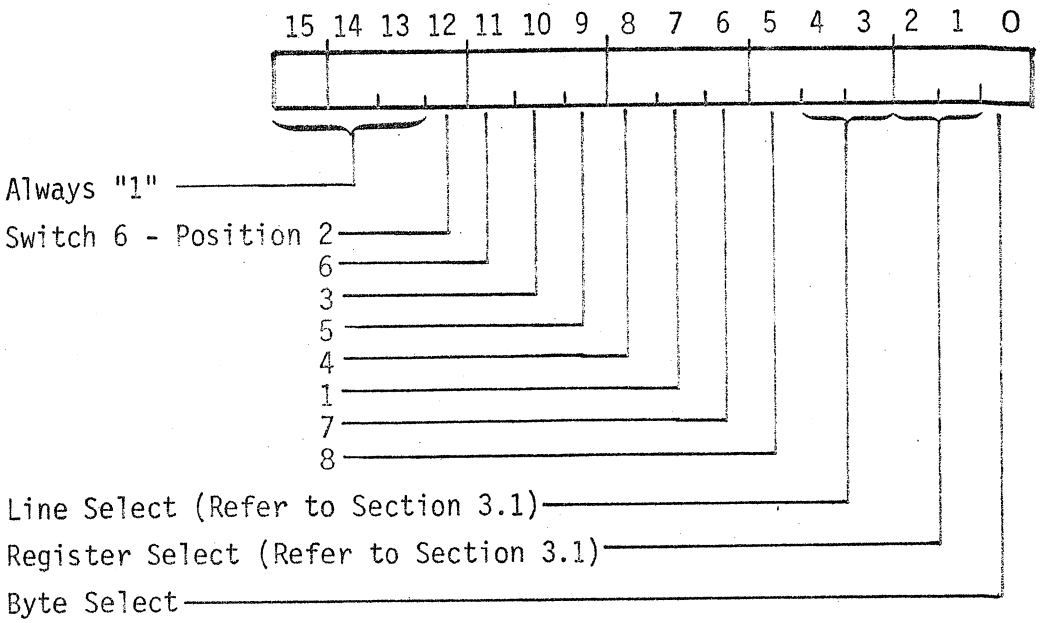


Table 2-2 shows switch settings for the most commonly used base address installations. Note that switch 6 (SW6) position 9 OFF enables channel 4 as the console port; SW6-9 ON disables channel 4 as the console port. For proper addressing, switch 5 (SW5) position 4 must always be ON.

BASE ADDRESS	SW6 POSITIONS							
	1	2	3	4	5	6	7	8
176500	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
176540	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
176600	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
176640	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF

TABLE 2-2: SAMPLE ADDRESS SWITCH SELECTIONS

2.4 VECTOR SELECTION

Two interrupt vectors are provided for each of the four SLU channels for a total of eight vectors. The procedure for configuring the vectors is similar to that used for configuring the base device register address; the configured base vector is the channel 1 relocations in memory (Program Counter address and Processor Status Word). Hence, sequential vectors appear in increments of four.

The module is factory configured with interrupt vector base of 300. It is also configured for channel 4 operation as the console device; thus, channel 4 automatically has interrupt vectors of 60 and 64.

Interrupt priority within the SCD-DLV11J is structured as shown in Table 2-3.

INTERRUPT PRIORITY	REQUESTING FUNCTION
1 (highest)	Channel 1, Receiver
2	Channel 2, Receiver
3	Channel 3, Receiver
4	Channel 4, Receiver
5	Channel 1, Transmitter
6	Channel 2, Transmitter
7	Channel 3, Transmitter
8 (lowest)	Channel 4, Transmitter

TABLE 2-3: INTERRUPT PRIORITIES

Switch 5 (SW5) sets the module base vector as shown in Table 2-4.

BASE VECTOR	SW5 POSITIONS 4*	5	6	7	8
300	ON	OFF	OFF	ON	ON
340	ON	OFF	OFF	ON	OFF
400	ON	ON	ON	OFF	ON
440	ON	ON	ON	OFF	OFF
500	ON	ON	OFF	OFF	ON
540	ON	ON	OFF	OFF	OFF

*Always On.

TABLE 2-4: VECTOR SELECTION

2.5 BAUD RATE SELECTION

Baud rates for each of the four channels on the SCD-DLV11J are set individually by switch 1 through switch 4 (SW1-SW4) The respective channels/switches are defined in Table 2-5.

CHANNEL	SWITCH
1	SW3
2	SW4
3	SW2
4	SW1

TABLE 2-5: BAUD RATE SWITCH/CHANNEL

Baud rates are determined by setting the desired position of SW1 through SW4 ON as shown in Table 2-6 below.

SWITCH SW1-SW4 POSITION	BAUD RATE
1	External
2	19.2K
3	38.4K
4	1200
5	2400
6	4800
7*	9600
8	600
9	300
10	150
*Factory configuration. Position 7 ON for 9600 baud.	

TABLE 2-6: BAUD RATE SELECTION

2.6 DATA WORD FORMAT

The data word format for each of the channels on the SCD-DLV11J is individually jumper selectable. The number of data bits, the number of stop bits, and the parity mode are determined as shown in Table 2-7 below.

JUMPER	FUNCTION	DESCRIPTION
A5 to B5	PARITY ENABLE	In = Parity Enable, Out = Parity Disable*
A1 to B1	PARITY TYPE	In = Odd Parity, Out = Even Parity (Parity must be enabled)
A4 to B4*	STOP BITS	In = 1 Stop Bit,* Out = 2 Stop Bits
A2 to B2 A3 to B3	DATA BITS	A2 to B2 / A3 to B3 / Length IN / IN / 5 Bits OUT / IN / 6 Bits IN / OUT / 7 Bits OUT / OUT / 8 Bits*
*Factory configuration: no parity, 1 stop bit, 8 data bits,		

TABLE 2-7: LINE PARAMETER FACTORY JUMPER CONFIGURATIONS

2.7 SERIAL INTERFACE SELECTION

The SCD-DLV11J interfaces with standard EIA RS232C, RS423 and RS422 devices. The serial interface in configured on a per line basis; i.e., there are four sets of A, B, C, D, E, F, G jumpers corresponding to the four channels. Table 2-8 defines the interface selection.

JUMPERS RS 232-C*	JUMPERS RS 422	SIGNAL
E to F	F to G	XMT DATA+
B to D	B to C	XMT DATA-
*Factory Configuration		

TABLE 2-8: SERIAL INTERFACE SELECTION

NOTE: For RS 422 operation, install four 100 ohm resistors in R1 bank location.

2.8 UART OPERATION

When the BREAK key on the console is pressed, the UART detects a framing error. The processor response to the error is jumper selectable. The option of UART Master Reset on DCOKL or INITH, is also jumper selectable. Jumper locations for both functions are defined in Table 2-9 below.

JUMPER	FUNCTION
E1 to E2	Reset on BDCOK
E2 to E3*	Reset on BINIT
E4 to E5	Assert HALT on BREAK
E5 to E6	Boot on BREAK
*Factory Configuration	

TABLE 2-9: UART JUMPER CONFIGURATIONS

NOTE: If channel 4 is not used as the console device interface, ensure that no jumper exists between E4-E5-E6 or a framing error will cause the processor to halt to reboot.

2.9 INTERFACE CONNECTOR

The serial interface connector (J1, J2, J3 or J4) is shown in Figure 2-2 and the associated pin assignments are defined in Table 2-10.

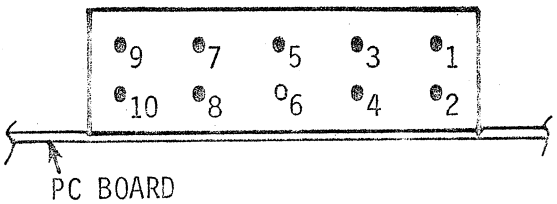


FIGURE 2-2: I/O CONNECTOR

I/O CONNECTOR PIN NUMBER	SIGNAL
1	CLK
2	GND
3	XMT DATA +
4	XMT DATA -
5	GND
6	KEY
7	RCV DATA -
8	RCV DATA +
9	GND
10	+12VDC

TABLE 2-10: I/O PIN ASSIGNMENTS

2.10 CABLES

Cables to mate with the 2 x 5 pin SCD-DLV11J connector are available from Sigma Information Systems. The standard cable is compatible with the DEC VT100.

When building a cable for the SCD-DLV11J, consider the following:

A) The receivers have differential inputs. For RS-232C or RS-423, RECEIVE DATA - (Pin 7 on 2 x 5 pin connector) must be tied to signal ground (Pins 2, 5, or 9) in order to maintain proper EIA levels. RS-422 is balanced and uses both RECEIVE DATA + and RECEIVE DATA -.

B) To directly connect to a local EIA RS-232C terminal, it is necessary to use a Null Modem. To build the Null Modem into the cable, switch RECEIVE DATA (Pin 2) with TRANSMITTED DATA (Pin 3) on the RS-232C connector.

C) To mate to the SCD-DLV11J connector block, the following parts are required:

CABLE CONNECTOR	AMP P/N 87456-9
CLIP CONTACTS	AMP P/N 87124-1
KEY PIN (Pin 6)	AMP P/N 87179-1

D) To mate to a VT100 or compatible terminal, the following parts are needed:

RS-232C CONNECTOR	AMP P/N 205207-1
CRIMP TERMINAL	AMP P/N 66504-4
STRAIN RELIEF COVER	AMP P/N 206472-1

Use 4-conductor cable, Alpha P/N 5004.

The cable wire list for a null modem cable switchable for interconnection from an SCD=DLV11J to a VT100 compatible terminal is illustrated in Figure 2-3 and defined in Table 2-11.

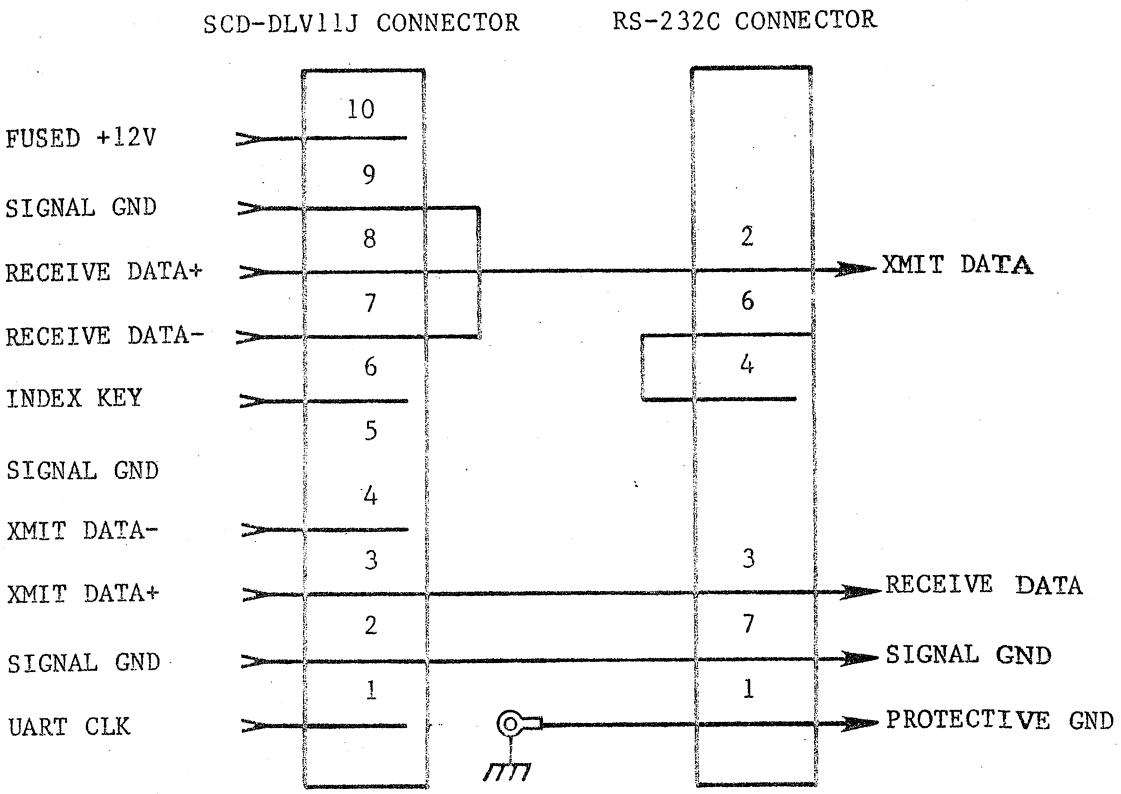


FIGURE 2-3: SCD-DLV11J/RS-232C CONNECTIONS

PIN NO.	SIGNAL
1	UART CLOCK IN OR OUT (16 x BAUD RATE, CMOS)
2	SIGNAL GND
3	TRANSMIT DATA +
4	TRANSMIT DATA -
5	SIGNAL GND
6	INDEX KEY - NO PIN
7	RECEIVE DATA -
8	RECEIVE DATA +
9	SIGNAL GND
10	FUSED +12VDC FOR 20mA DLV11KA

TABLE 2-11: SCD-DLV11J PIN CONNECTIONS

2.11 BUS SIGNALS

Bus signals and associated pin assignments are shown in Table 2-12.

CONNECTOR A		CONNECTOR B	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
AA1	Not Used	BA1	BDCOK H
AB1	Not Used	BB1	Not Used
AC1	Not Used	BC1	Not Used
AD1	Not Used	BD1	Not Used
AE1	Not Used	BE1	Not Used
AF1	Not Used	BF1	Not Used
AH1	Not Used	BH1	Not Used
AJ1	GND	BJ1	GND
AK1	Not Used	BK1	Not Used
AL1	Not Used	BL1	Not Used
AM1	GND	BM1	GND
AN1	Not Used	BN1	Not Used
AP1	BHALH	BP1	Not Used
AR1	Not Used	BR1	Not Used
AS1	Not Used	BS1	Not Used
AT1	GND	BT1	GND
AU1	Not Used	BU1	Not Used
AV1	Not Used	BV1	+5VDC
AA2	+5VDC	BA2	+5VDC
AB2	Not Used	BB2	Not Used
AC2	GND	BC2	GND
AD2	+12VDC	BD2	Not Used
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	Not Used	BK2	BDAL6 L
AL2	BIRQL	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDALO L	BU2	BDAL14 L
AV2	BDALI L	BV2	BDAL15 L

TABLE 2-12: BUS SIGNALS AND PIN ASSIGNMENTS

Section 3
Programming Information

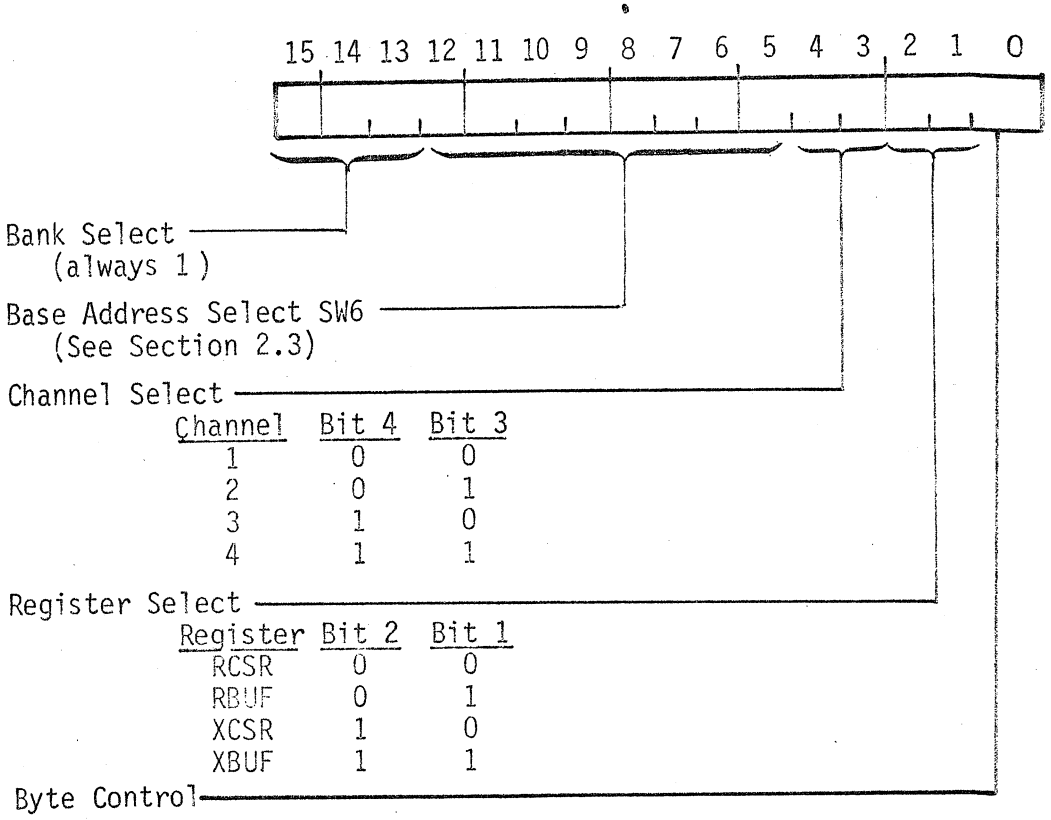
3.1 ADDRESS SELECTION

The SCD-DLV11J responds to any address in the upper 4K peripheral page. It is limited to blocks of 16 addresses which start at addresses with the last two digits of either 00 or 40. If channel 4 is used as the console device, 12 slot memory blocks starting at XXXX00 or XXXX40 can be used. Each channel has four device registers which can be individually addressed by the program. The device registers are:

RCSR	Receiver Control/Status Register
RBUF	Receiver Buffer
XCSR	Transmitter Control/Status Register
XBUF	Transmitter Buffer

If channel 4 is configured as the dedicated console interface, the associated device register addresses are 177560-177566.

The device address format is shown in Figure 3-1.



Channel	Bit 4	Bit 3
1	0	0
2	0	1
3	1	0
4	1	1

Register	Bit 2	Bit 1
RCSR	0	0
RBUF	0	1
XCSR	1	0
XBUF	1	1

FIGURE 3-1: DEVICE ADDRESS FORMAT

3.2 VECTOR FORMAT

Eight interrupt vectors are switch and PROM selected on the SCD-DLV11J. Each channel is capable of generating two interrupts, one from the receiver buffer, and one from the transmitter buffer. Vector addresses range from 000 to 776. The console device interrupt vectors are 60 and 64. If an interrupt acknowledge is granted, the vector address is placed on the data/address bus lines.

Although the SCD-DLV11J has eight separate interrupting registers, it is capable of handling only one interrupt at a time. Therefore, the interrupts are prioritized as shown in Table 2-10.

The format for the vector address is shown in Figure 3-2.

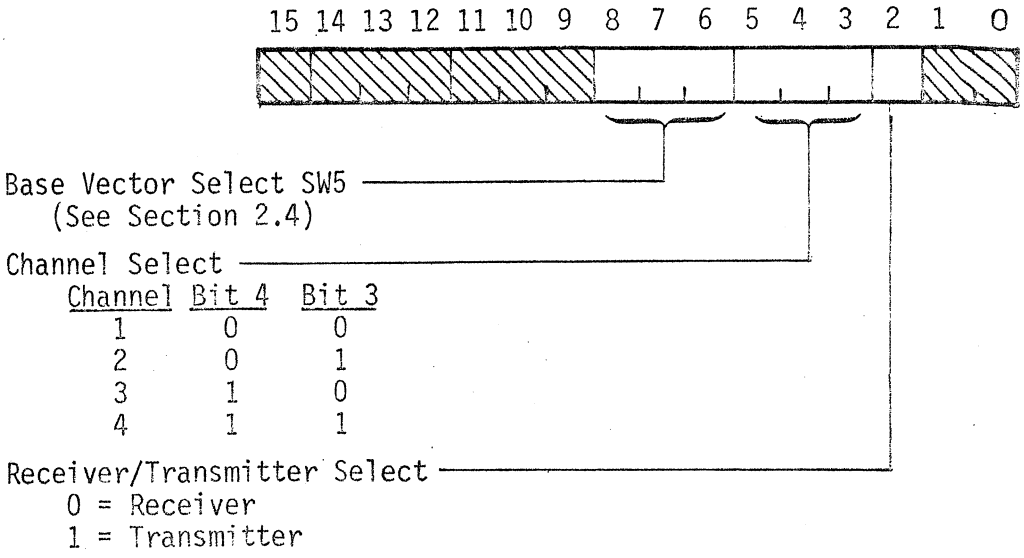


FIGURE 3-2: VECTOR ADDRESS FORMAT

3.3 REGISTER WORD FORMATS

The SCD-DLV11J has four word formats, one for each of the four channels.

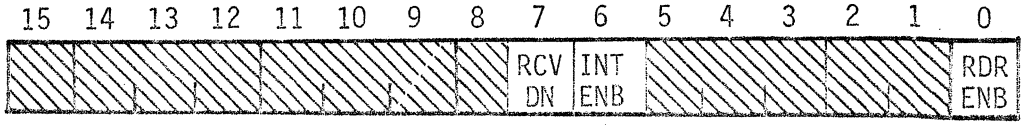


FIGURE 3-3: RECEIVER CONTROL/STATUS REGISTER

7 RCV DN — RECEIVER DONE. Read only. Set when an entire word has been received and is ready for transmission to the CPU. If INT ENB is set, setting RCV DN starts interrupt sequence.

6 INT ENB — RECEIVER INTERRUPT ENABLE. Read/Write. Set under program control. Enables RCV DN to initiate an interrupt sequence. Cleared by INIT or program control.

0 RDR ENB — READER ENABLE. Write only. Setting RDR ENB advances the paper tape reader on an LT-33 terminal one character. Setting RDR ENB also clears RCV DN. Read as zero.

NOTE: Current loop option is necessary for the operation of this bit

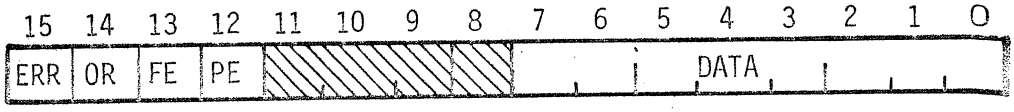


FIGURE 3-4: RECEIVER BUFFER REGISTER
(All bits are Read only.)

15	ERR	ERROR. Set whenever bits 14, 13 or 12 are set.
14	OR	OVERRUN. Set when previous character was not completely ready (RCSR bit 7 not cleared) prior to receiving a new character. Cleared by INIT. NOTE: One full character time is allowed betwen RCV DN (CSR bit 7) being set and the setting of the OR bit when back-to-back characters are being received.
13	FE	FRAMING ERROR. Set when no valid STOP bit is present for the character being received. Cleared by INIT.
12	PE	RECEIVER PARITY ERROR. Set when the received parity does not agree with the expected parity. Always zero if the device is configured for No Parity.
7-0	DATA	RECEIVED DATA BITS. Five to eight data bits in a right-justified format. Upper bits read zero when not enabled.

NOTE: All error bits remain valid until next character is received.

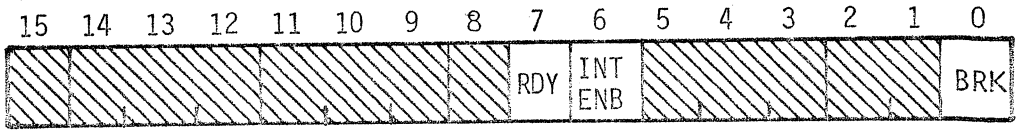


FIGURE 3-5: TRANSMITTER CONTROL/STATUS REGISTER

7	RDY	TRANSMITTER READY. Read only. Set when XBUF is ready to receive another character from CPU. RDY starts and interrupt sequence if INT ENB (bit 6) is set.
6	INT ENB	TRANSMITTER INTERRUPT ENABLE. Read/Write. Set under program control if an interrupt sequence should be started when RDY (bit 7) is set. Cleared by INIT or program control.
0	BRK	BREAK. Read/Write. Set or cleared under program control. When set, a continuous space level is transmitted. RDY (bit 7) and INT ENB (bit 6) are still operable, allowing software timing of BRK. When not set, character transmission can proceed in normal fashion. Cleared by INIT.

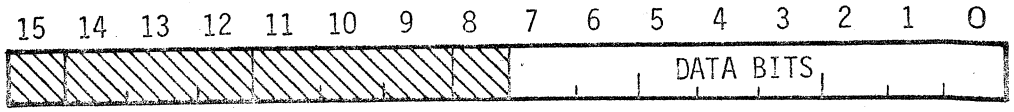


FIGURE 3-6: TRANSMITTER BUFFER

0-7	DATA BITS	TRANSMITTER DATA BITS. Write only. Contains five to eight right-justified data bits. Loaded under software control for serial transmission.

3.4 ASYNCHRONOUS TRANSMISSION FORMAT

In asynchronous transmission, for proper data recovery by the receiver, data characters are transmitted in the format shown in Figure 3-7.

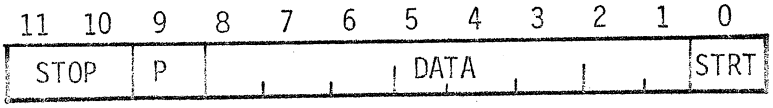


FIGURE 3-7: SERIAL DATA WORD FORMAT

11-10	STOP	STOP. Can be configured for either one or two STOP bits. When the first STOP bit is received, the UART shifts the data in parallel from the receiver shift register to a parallel holding register. All STRT, STOP and P bits are removed from the data. The receiver asserts RCV DN (RSCR bit 7), and all data and error bits become valid.
9	P	PARITY. Can be configured for odd, even, or no parity. If the device is configured for no parity, the STOP bits follow immediately after the DATA.
8-1	DATA	DATA BITS. Contain five to eight characters. Shifted by the UART so the least significant bit is in the lowest bit position in the register (right justified).
0	STRT	START. Detected by the UART as a mark-to-space transition, causing it to begin loading the character into the storage register.