USER'S GUIDE

FOR

VRG-Q

GRAPHICS AND ALPHANUMERIC INTERFACE

Peritek

THIS DOCUMENT CONTAINS THE FOLLOWING MANUALS:

VRG-Q

USERS MANUAL

HD46505 CRTC

USERS MANUAL

PCMSP

SUBROUTINE PACKAGE MANUAL

VRG-Q

USER'S MANUAL

Q-BUS

GRAPHICS + CHARACTER

VIDEO DISPLAY INTERFACE

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Chapter I
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information about the VIURAM VRG-Q raster scan video graphics interface for the Q-Bus, The information enables the user to install, select options, program and maintain the interface.

I.2 FUNCTIONAL DESCRIPTION

The VRG-Q VIURAM is a combined dot graphics and character video interface which connects any DEC LSI-11 series microcomputer to a standard video monitor.

The VIURAM contains two display memories; a 16K word graphics display memory, and a 1K word alphanumeric display memory (when the alphanumeric option is installed). In the graphics memory, each bit in each word corresponds to a pixel position on the video display. In the alphanumeric memory, each byte corresponds to a character block position on the display. When an ASCII character code is stored in the character memory, the character image appears on the display in the corresponding block position.

The VIURAM utilizes a unique buffered dual port memory so CPU activity does not cause interference on the display. This is done by interleaving the CPU access with video generator access to the memory.

Two modes of access to the VIURAM's memories have been provided. First, the VIURAM memories can be accessed on a line by line basis through a bank of 32 data registers located in the I/O page. Second, by setting an enabling bit in the VIURAM CSR register, the entire contents of each memory can be addressed directly in the 22-bit address space of the Q-Bus.

Several other features have been implemented in the VRG-Q: the graphics memory can be loaded automatically by the VIURAM with a particular bit pattern (preloaded into the first line of the alphanumeric display) in 30 msec, (useful for clearing the

memory); the video output can be blanked without changing the image stored in memory; the graphics display image can be complemented (reverse video) by setting a single bit. This also has no effect on the actual data stored in memory. The display can be scrolled, in multiples of 16 raster lines, under software control.

The character generator ROM is compatible with standard UVEPROMs such as the 2716. This means that the user can customize the alphanumeric character set. The standard character generator is a high resolution 7x11 dot matrix in an 8x16 character block. Display characters include the 96 character USASCII set plus 32 special symbols.

The characters can be displayed in positive video (white character on dark field) or reverse video (dark character on white field). An addressable character cursor is also provided.

The character and graphics serial data streams are Exclusive OR'd together, to improve legibility in mixed graphic/alphanumeric display. The video output to the monitor can be set up in either composite video/sync or separate video and horizontal and vertical syncs.

The VIURAM occupies one dual height slot (8" x 5") in any Q-Bus backplane and requires +5 and +12 volt power. It generates its own -5 volt power for the dynamic RAMs with an on-board charge pump circuit.

VIURAM is pronounced "view-ram" and stands for Video Interface Unit Random Access Memory. The VIURAM is available in two standard configurations:

Graphics Only: VRG-Q
Alphanumeric and Graphics: VRG-Q/A

I.3 DEVICE OPTIONS

Jumper selectable options provide the user with the ability to customize the VIURAM to work with his computer configuration, video monitor and display requirements.

Data Register Address - the base address of the raster line or character line addressing function can be set on a 32 word

boundary anywhere in the I/O page.

Control Register Address - The base address of the VIURAM control registers may be set on a 4 word boundary anywhere in the top 1K words of the I/O page (i.e., above address 774000).

Memory Address - the base address of the direct memory addressing function can be set on 16K word boundaries anywhere in the 22-bit address space of the Q-Bus Plus.

Direct Memory Addressing - a jumper option enables the direct memory addressing function so the control bit in the CSR can select between line addressing and direct addressing.

Video Output - the video output circuit can be configured to supply either composite video/sync or separate video, horizontal sync and vertical sync.

All VIURAM VRG-Q boards are set up in the following configuration unless specific arrangements are made at the time of ordering:

Data Register Base Address - 774000
Control Register Base Address - 774140
Direct Addressing Mode Disabled
Alphanumeric Option - not installed
Video Output - Separate Video, Horizontal and Vertical Sync

I.4 SPECIFICATIONS

Graphics Display: 512 x 512 x 1 interlaced display.

Character Display: 32 lines of 64 characters. Each character block is 16 raster lines by 8 dots wide. Reverse video display mode is selected on a character by character basis.

Video Output: Graphics and character signals are Exclusive OR'd together, then output as RS170 composite video/sync or as separate TTL outputs.

Character Generator: 2716 EPROM with user definable character set of 128 characters. A standard 96 character USASCII set plus 32 special characters, (7x11 dot matrix, including descenders) is normally supplied.

CRT Controller: Programmable for 50/60 Hz operation. Also provides blinking character cursor and hardware scrolling functions.

Display Memories: Graphics and character memories are completely independent. Both memories are fully buffered so CPU access does not interfere with display. Graphics memory is 16K words (16 bits/word) dynamic RAM. Character memory is 1K words static RAM.

Memory Access: Both graphics and character memory are accessed through the same 16K word address space. The memories can be accessed through data registers in the I/O page or by direct addressing. Bits in the control register determine which access mode is active and whether character or graphics memory is being accessed.

Direct Addressing: Memory address can be set up on any 16K word boundary in the 22-bit address space of the Q-Bus.

Line Addressing: 32 data registers in the I/O page correspond to the 512 dots on a graphics line or the 64 characters on a character line. Bits in the control register determine which memory (graphics or character) and which line are being accessed.

Memory Disable: The memory select can be disabled under software control so multiple VRG's can share the same direct address space and/or data register address space.

Graphics Memory Clear: Screen clear mode allows graphics memory to be set to any desired value in 1/30 second without processor attention.

Display Blank: Display blank mode allows the video output to be blanked without affecting the contents of the display memories.

Display Complement: The graphics display image can be complemented without affecting the contents of the display

memory.

Module Size: Dual height card, 5.2" X 8.9".

Mounting Requirements: Plugs directly into any Q-Bus backplane.

Q-Bus Loading: One bus load.

Power Required: 2.5 amps at +5 volts, .6 amps at +12 volts

Monitor Interface: Separate TTL level Horizontal Sync, Vertical Sync and Video Outputs standard. EIA RS-170 composite video signal (1.4 volts P-P, sync negative) for driving into 75 ohm load optional.

Operating Environment: Temperature: zero degrees centigrade to 50 degrees centigrade, Relative Humidity: up to 90% (non-condensing).

Chapter II
INSTALLATION

II.1 INCOMING INSPECTION

Unpack the VIURAM and visually inspect the board to see if any damage occurred in shipping. If there has been any physical damage to the board, do not attempt to use it. File a claim with the carrier at once and contact Peritek Corporation for information regarding repair or replacement.

II.2 INITIAL TESTING

If the board passes physical inspection, then it should be given a power on test. This test will verify that the video generation circuitry and computer interface are working properly. It should be completed before any of the jumper options are changed.

Equipment required for the test is a video monitor and an LSI-11 with floppy disk drive and the RT11 operating system.

The VRG-Q is setup to respond to the following addresses in the I/O page:

Control Registers:	774140 - 774146
Data Registers:	774000 - 774076

Before installing the VRG-Q in your backplane be sure there are no other devices which respond to these addresses.

Plug the VRG-Q into your backplane, power up in halt mode and use micro-ODT to verify that the control registers can be read. Note that the data registers cannot be read until the initialization program is run.

Boot up RT11 and initialize the VRG-Q by executing the program VRGINT from the VRG-Q software diskette. Then, execute VRGTST to test the graphics memory. This program runs for several minutes before announcing "RAM IS OK". If RAM is faulty an error message will come out much sooner.

If the parallel character memory option is installed then PCMTST can be executed to verify that the character memory is also functioning properly.

If these procedures execute without problems then it is time to connect a monitor to the VRG-Q and try to generate a display. The board is set up for use with a monitor having direct drive (TTL level) inputs. Make the appropriate connections to your monitor (see Section II.5) and power it up.

-----WARNING-----

When the VRG-Q powers up, the CRT controller chip is held in a reset state. It remains reset until the VGO bit (octal 40) in the CSR is set. The CRT controller must be initialized before the VGO bit is set otherwise damage to the monitor may result.

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VRGINT is the only program provided by Peritek which will set VGO and it does so only after initializing the CRT controller. All other Peritek-supplied software will exit if VGO is not set. The user is advised to adhere to this convention when writing programs for the VRG-Q.

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Once the monitor is connected run VRGINT, if necessary, then run VRGSAV according to the following dialogue:

```
.RUN VRGSAV
#Enter 'S' to save 'R' to restore image
#R
Enter file name for restore
*TP1
```

The program will now read image file TP1.IMG into memory and transfer it to the VRG-Q. Adjust the brightness, contrast and

hold controls on the monitor to get a good image. Adjust horizontal and vertical drives to get a square image centered on the monitor. At this point it may become necessary to adjust the timing parameters in VRGINT to get the best picture (see Section IV.5).

If any problems are encountered in these procedures, please contact Peritek Corporation for assistance.

II.3 OPTION SELECTION

A standard board is assumed. (See Section I.3). The following instructions tell how to modify the VRG-Q to a non-standard configuration. Only rosin-core solder and a low wattage soldering iron (<40 watts) should be used in make the changes.

II.3a MEMORY AND REGISTER ADDRESSES

There are three separately addressable functions (control registers, data registers, memory) on the VRG-Q.

Each of the three memory and register functions has a row of wire-wrap pins associated with it. The wire-wrap pins correspond to reference inputs on the address comparator chips. Each function has a default address which is fixed on the board at the time of manufacture with wire-wrap jumpers connected in a chain from the square pad at the end of each row to some of the pins in that row. A change in the address necessitates removal of this chain of jumpers and the installation of a new chain which defines the new address. Each pin represents one bit in the address.

II.3a1 DIRECT ADDRESSING JUMPER CHANGES (Refer to Figure II.3.1)

The backplane may have to be wired for 22-bit addressing before direct addressing can be used. See the application note on how to implement 22-bit addressing in Section V.2.

The direct addressing option is hard-wire disabled by jumper H. The jumper must be removed to permit the option to work, since it overrides the DMAEN bit.

The direct address is determined by a set of jumpers which determines which 32K word field the VIURAM will reside in and another pair of jumpers which determine if the 16K word VRG memory will be in the bottom half or the top half of that field.

The default field address is set to field 0 (00000000 to 00177777) and must be set to some other field before use. Install a jumper wire chain between the address bit pins to be decoded as "ones" and the square pad at the end of the jumper row hole.

Jumper Hole Number	Bus Address Bit Equivalent	Default Value	Default Jumper Installed
1	19	0	N
2	18	0	N
3	20	0	N
4	17	0	N
5	21	0	N
6	16	0	N
7	Ground	-	N

The graphics memory can be placed in the upper or lower 16K word block of its selected 32K field. The default is in the high block. To change the position, cut the trace (on the component side of the board) between JP1-1 and JP1-2.

Jumper Hole Number	Bus Address Bit	Default Value	Default Jumper Installed
JP1-1	15	N/C	N
JP1-2	Input	C	Y
JP1-3	15	C	Y

The VIURAM should not be installed in the lowest field of memory, nor should it be installed at an address where it will overlap the I/O page (top half of field 3 if 18-bit addressing is being used, top half of field 63 if 22-bit addressing is being used).

II.3a2 DATA REGISTERS (Refer to Figure II.3.2)

The data register base address can be placed anywhere in the I/O page between 760000 and 777700 on a 32 word boundary. The default address is 774000. To change the address, remove the jumper chain and install a new chain which defines the new address. A connection to ground is made for the corresponding bit to be low.

Jumper Hole Number	Bus Address Bit	Default Value	Default Jumper Installed
1	9	0	Y
2	12	1	N
3	8	0	Y
4	11	1	N
5	7	0	Y
6	10	0	Y
7	6	0	Y
8	Ground	-	Y

II.3a3 CONTROL REGISTERS (Refer to Figure II.3.3)

The control register base address can be placed anywhere in the I/O page between 774000 and 777770 on 4 word boundaries. The default address is 774140. To change the address, remove the jumper chain and install a new chain which defines the new address. A connection to ground is made for the corresponding bit to be low.

Jumper Hole Number	Bus Address Bit	Default Value	Default Jumper Installed
1	6	1	N
2	10	0	Y
3	7	0	Y
4	3	0	Y
5	9	0	Y
6	4	0	Y
7	8	0	Y
8	5	1	N
9	Ground	-	Y

II.3b VIDEO OUTPUT (Refer to Figure II.3.4)

The video output can be set up either as composite video/sync or as separate vertical sync, horizontal sync and video. The default mode is the separated signals.

Connection	Function	Mode
H5 to H1	Horizontal Sync to Driver	Separate
H7 to H8	Horizontal Driver to Output Pin	Separate
H9 to H10	Horizontal Sync = High Active Signal. No Jumper for Low Active Signal	Separate
H3 to H4	Vertical Sync = High Active Signal. No Jumper for Low Active Signal	Separate
H5 to H3	Horizontal Sync XOR'd with Vertical Sync	Composite
H2 to H1	XOR'd Signal to Sync Driver	Composite
H7 to H6	Sync Driver to Video Output	Composite

NOTE: All four jumpers in the separate mode must be removed before installation of the composite mode jumpers.

II.4 EPROM PROGRAMMING INFORMATION

The EPROM pinout convention followed in the VIURAM is at variance with standard INTEL labelling. The following chart is

supplied to clarify those differences. The VIURAM conventions must be followed lest exciting but incorrect results occur. True data and address levels are used in programming the EPROM. A one bit corresponds to a pixel turned on, a zero bit represents a pixel turned off. CROMDATA0 is the leftmost pixel in a character. RA0-3 are the raster line address lines with 0 selecting the top line of the character block down to 15 at the bottom. VA0-6 are the character select address lines.

Pin Number	VIURAM Name	2316/2716
1	VD3	A7
2	VD2	A6
3	VD1	A5
4	VD0	A4
5	RA3	A3
6	RA2	A2
7	RA1	A1
8	RA0	A0
9	CROMDATA7 (MSB)	O0 (LSB)
10	CROMDATA6	O1
11	CROMDATA5	O2
12	GROUND	VSS
13	CROMDATA4	O3
14	CROMDATA3	O4
15	CROMDATA2	O5
16	CROMDATA1	O6
17	CROMDATA0 (LSB)	O7 (MSB)
18	GROUND	CE
19	VD6	AID
20	GROUND	OE
21	+5	Vpp
22	VD5	A9
23	VD4	A8
24	+5	VCC

II.5 CONNECTIONS TO THE VIURAM

Two connector options are provided on the VIURAM. One is a coaxial connector for composite video; the other (standard) is a header for separated video/sync signals and composite video.

COMPOSITE VIDEO CONNECTOR J1

J1 is a miniature coaxial connector, which supplies an EIA RS-170 composite video-sync signal. The connector part number AMP #50084-1. The mating connector parts are AMP #201143-1 (or 201143-6) pin, 32866 ferrule, and 45638-2 crimping tool.

The connector and/or cable is available by special order from Peritek Corporation.

VIDEO I/O CONNECTOR J2

J2 is a ten pin header, with connections to the video output.

Pin	Signal Name
1	TTL HORIZONTAL SYNC
3	TTL VERTICAL SYNC
5	TTL VIDEO
7	GROUND
9	COMPOSITE VIDEO/SYNC
2,4,6,8,10	GROUND

Mating connector is 3M #3473-3000.

The TTL video and TTL horizontal sync signals are driven by 74S136 open collector gates and pulled up by 220 ohm resistors. The TTL vertical sync signal is driven by a 7486 totem-pole gate. Jumper options allow the sync signals to be made high or low active.

JUMPER H

PIN		FUNCTION
7	-	GROUND
6	-	• 16
5	-	• 21
4	-	• 17
3	-	• 20
2	-	• 18
1	-	• 19

DIRECT ADDRESSING

TO ENABLE, CUT JUMPER H. TO SET ADDRESS, INSTALL JUMPERS FROM THOSE PINS WHICH MUST DECODE AS ONES IN THE ADDRESS TO GROUND. DO NOT USE FIELD 0 OR FIELD 63.

JP1

BANK SELECT

TO SELECT THE LOW 16K, INSTALL JUMPER BETWEEN JP1-2 AND JP1-1. TO SELECT THE HIGH 16K, INSTALL JUMPER BETWEEN JP1-2 AND JP1-3 (STANDARD)

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DRAWN BY: KAD

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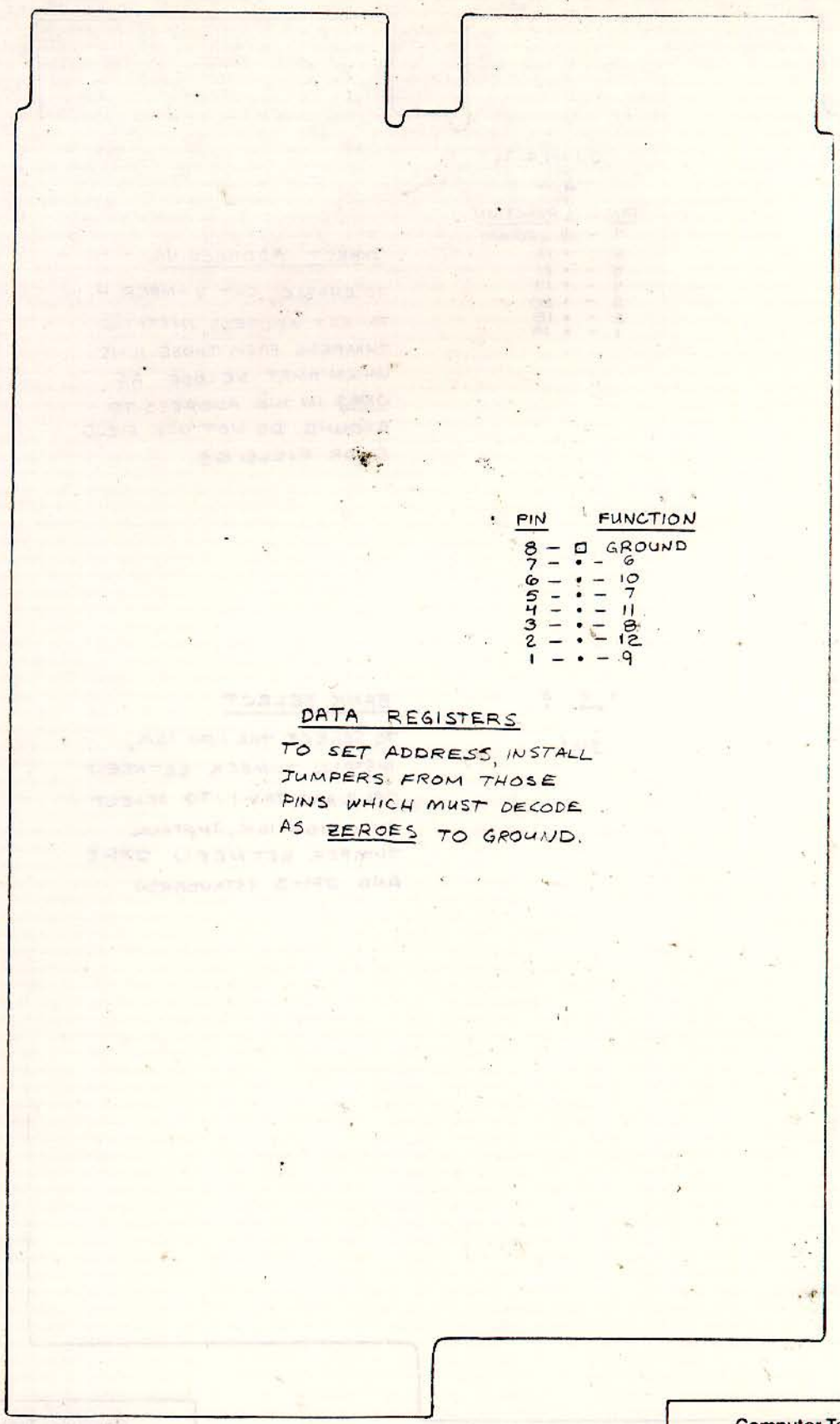
DATE: 3-31-81

REVISED:

TITLE: VRG-Q DIRECT ADDRESSING JUMPERS

DRAWING NUMBER: FIGURE 11.3.1



DATA REGISTERS

TO SET ADDRESS, INSTALL JUMPERS FROM THOSE PINS WHICH MUST DECODE AS ZEROES TO GROUND.

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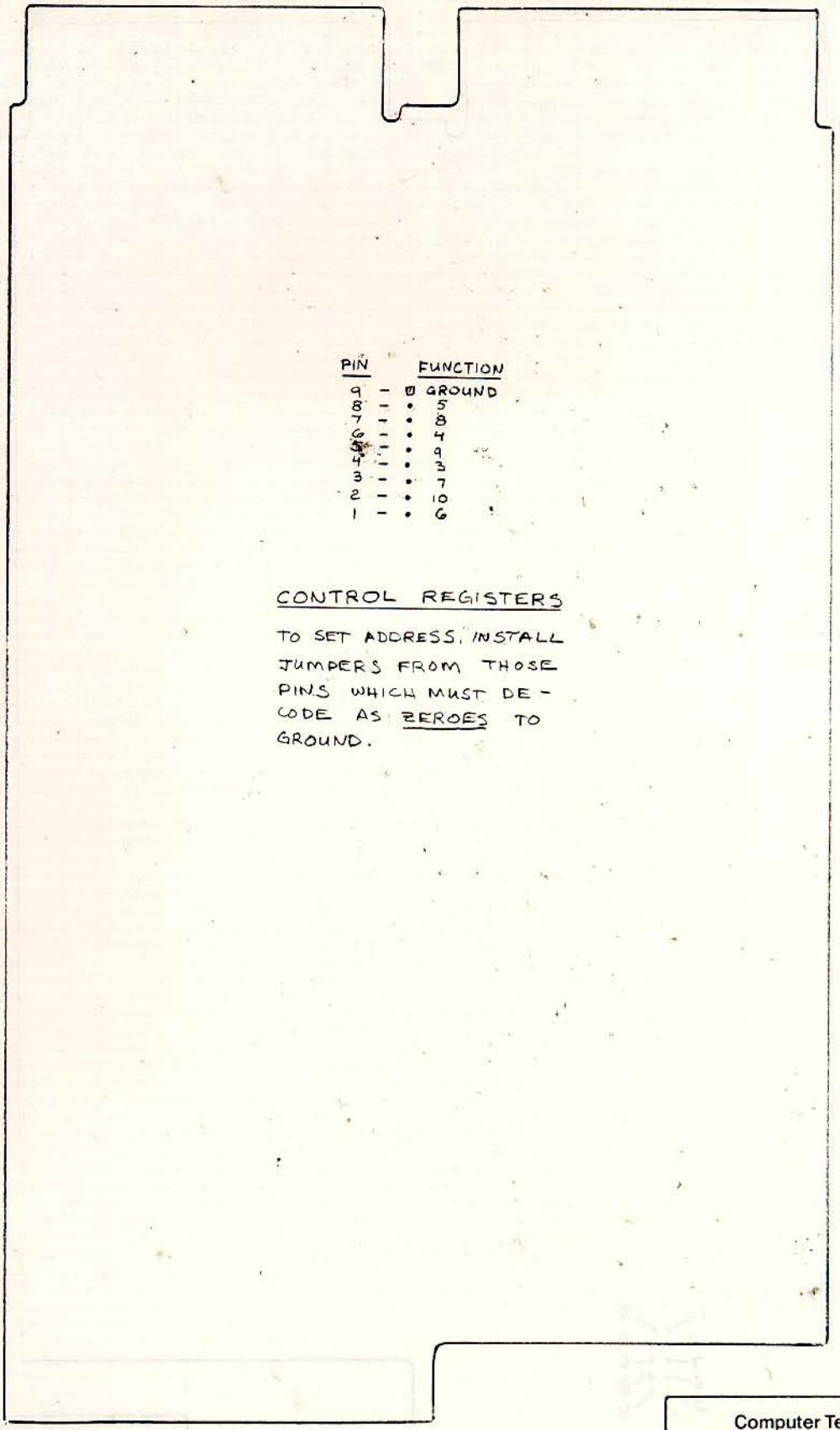
TITLE: VRG-Q DATA REGISTER ADDRESS JUMPERS

DRAWING NUMBER: FIGURE 11.3.2



CONTROL REGISTERS

TO SET ADDRESS, INSTALL JUMPERS FROM THOSE PINS WHICH MUST DECODE AS ZEROES TO GROUND.

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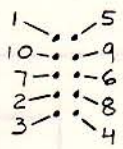
TITLE: VRG-Q CONTROL REGISTER ADDRESS JUMPERS

DRAWING NUMBER: FIGURE 11.3.3



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Peritek corporation

DRAWN BY:

SCALE:

DATE: 7-15-81

REVISED:

TITLE: VRG-Q VIDEO OUTPUT JUMPERS -REV 2 BOARDS

DRAWING NUMBER: FIGURE 11.3.4

Chapter III
THEORY OF OPERATION

III.1 INTRODUCTION

The basis of the VIURAM design is a synchronous timing scheme which permits access to the on-board memory, registers and CRT controller chip by the CPU without interference in the video display. Processor accesses are interleaved with the loading of a display data buffer, so the processor can communicate with the VIURAM while display information is read from the buffer. Since there are two memories (graphics and alphanumeric) the buffer must hold data from both. The buffer supplies ASCII character codes which are decoded by the character generator, serialized and manipulated by the display mode logic as required. In addition, the buffer supplies the (graphics) bit data which is serialized and also fed into the display mode logic. This video signal, together with the sync signals, drives the video display monitor. The video timing is generated by the HITACHI HD46505 programmable CRT controller chip (CRTC). The bus interface timing is synchronized to the CRTC to make the interleaved access scheme possible.

The following discussion describes the operation of a VIURAM equipped with both alphanumeric (CRAM) and graphics (GRAM) memory. Refer to the block diagram (Figure III.1) and the timing diagram (Figure III.2) as necessary.

III.2 MASTER CLOCK

The master clock on the VIURAM is a 20 MHz crystal controlled oscillator. This frequency is divided down by a 4 bit counter to supply the basic timing signals which control the VIURAM. These include the dot clock, buffer clocks, CRTC clock and the display data shift register load pulses. Two full cycles of the clock counter (1.6 us) defines the basic display/processor cycle time of the VIURAM.

III.3 Q-BUS INTERFACE AND TIMING

The Q-Bus is an asynchronous bus, consisting of a 16 bit bidirectional multiplexed address/data bus, 6 extended address lines and 5 primary control lines. Refer to the DEC LSI-11 Microcomputer Processor Handbook for detailed information concerning operation of the Q-Bus.

The VIURAM buffers the address/data lines with latching bidirectional bus transceivers, which store the address on the bus at the leading edge of SYNC. At the onset of processor portion (C1) of the VIURAM timing cycle, the bus transceivers are gated onto the VIURAM's internal data bus. Two eight bit address comparators compare the data on the bus with their reference inputs, which are set by user installed jumpers. An additional bus comparator examines the extended address lines directly. The comparators' outputs are OR'd together, along with the VRON (memory response enable bit) and the result is latched about 125 ns after the onset of C1. When a comparison is detected, SYNCGRNT is set and the VIURAM begins a processor access cycle. If no comparison is made, the VIURAM just does an extra dynamic RAM refresh cycle. False comparisons by the decoding logic are prevented by entering the comparator enable mode only when SYNC*(DIN+DOUT)=1. Furthermore, if this function is true but about to go false at the onset of C1, it will inhibit the SYNCGRNT flipflop when it does go false and this will happen before the SYNCGRNT flipflop is clocked.

When SYNCGRNT is set, the CRAM/GRAM memory address multiplexers are switched over to the processor address inputs, and certain data lines and the state of the control register address comparator are latched. With this information and in conjunction with the CRAM and DMAEN bits, the VIURAM can determine which of the four devices, CRAM, GRAM, CRTC or a control register is being accessed. Although the timing differs somewhat between devices, a general overview will be given here; timing details will be covered in the sections devoted to each device.

At the beginning of SYNCGRNT, the VIURAM timing will go into a read, write or write byte mode, depending on the Q-Bus signals DIN, DOUT and WTBT. When DIN is set, the CPU is requesting data from the VIURAM; the timing waits about 100 ns after SYNCGRNT to ensure sufficient address setup time and then enables the selected device. Data is asserted on the internal data bus some

50-400 ns after assertion of the device chip select line(s), depending on the access time of the device. SYNCGRNT is terminated 500 ns after it begins. On its trailing edge, the data is latched by the bidirectional bus transceivers and asserted on the Q-Bus, and BRPLY is set. The data is held on the Q-Bus until the CPU gets around to responding, which is some arbitrary time after BRPLY is asserted. Once it responds, it removes DIN and clears OUTSEL, which removes data from the Q-Bus. During this transaction time, the VIURAM continues on its way, loading new data into the display buffer. It doesn't have to wait for the CPU, since the data is latched, and the timing logic for the CPU transaction is independent of the refresh operation.

In the event that DOUT was set, the VIURAM is required to accept data from the CPU. At the onset of SYNCGRNT, the bus transceivers are allowed to continue driving the internal data bus, but are strobed again to pass through the data on the Q-Bus side which is to be written into the VIURAM. The selected device also has its write enable turned on at this point. About 100 ns after SYNCGRNT goes true, the selected device has its chip enable line(s) turned on and the data is strobed into the device. The GRAM does this on the leading edge of the chip enable, the control registers use a clock pulse in the middle of the write cycle, and the CRTC and CRAM strobe data in on the trailing edge of chip select. Chip select is terminated as before by SYNCGRNT going false. At this point OUTSEL is set, but only BRPLY is asserted, not the data bus, since no data was required by the CPU. The VIURAM proceeds from this point just as it did in the Data-In Cycle except that DOUT going away clears OUTSEL. The Write Byte mode works identically to the write mode except that WTBT controls whether the top or bottom byte of the selected device gets written. This operation is only significant for CRAM and GRAM. A byte write into the CRTC or control registers results in the entire word being written.

III.4 CONTROL REGISTERS

The control register's 4 word address space includes not only the control register but also the CRTC registers. This section only covers the former; see Section III.5 for the latter.

The VIURAM control register is a multifunction device. It provides the various display and memory control bits, and also

the line address register. The line address register is a nine bit read/write register, which is used to select a 32 word block of memory in CRAM and the GRAM. Moreover, when the DMAEN bit is set, this register functions not as a programmed I/O register, but rather as a bus address register, and is used in conjunction with the direct addressing comparator to provide the VIURAM direct address mode. This is done using a synchronous counter for the register. The counter is used because it supplies both a read/write port to the internal data bus and a (static) output port to the control logic. The counter is loaded by setting its write enable and then giving it a clock pulse. The counter is given three clock pulses during C1. In programmed I/O mode, the write enable is set during the second and third clock pulses, which occur during the normal data out period. In the direct addressing mode, the write enable comes during the first clock pulse period, which occurs when address information is present on the data bus.

The other part of the control register operates independently of the line register, as far as programming is concerned, since it operates only in the programmed I/O mode. It uses read and write strobes which operate in the normal data in and out periods of C1. The bit functions are completely defined in Section IV.3.

III.5 VIDEO TIMING

The video timing is controlled by the CRTC. The CRTC must be initialized by the processor with a predetermined set of parameters for its internal register file. Once initialized, the CRTC generates the display refresh addresses (MA), the row addresses (RA) for the character generator, the programmable cursor function, blanking, horizontal sync and vertical sync.

The CRTC is similar to other LSI CRT controllers in that it is a character oriented device, and as such, several tricks must be used for it to function properly in a graphics application. Because it can address a maximum of 128 character lines, the Row Address lines must be used to expand the number of raster lines to more that 512 lines. If the mix of MA lines and RA lines from the CRTC is chosen properly, then the character display addressing falls out for free.

The programmability of the CRTC must be restricted to things like sync width and positioning for it to be used in a mixed line mode, because binary addressing of the memory must always be maintained. Since the graphics memory is formatted as a 512 x 512 array, thirty two row addresses in the dynamic RAM are selected every raster line time. The GRAM gets completely refreshed every 4 line times (252 us) or about 8 times more than required.

The VIURAM interface timing is synchronized to the CRTC's low order address line (MA0) to ensure that data for the display buffer is taken when the address lines are stable.

For detailed operation and programming of the CRTC, see Section IV.5 and the Appendix. Some important timing values are:

Dot rate	= 10 MHz
Dot time	= 100 ns
Character time	= 800 ns
Display line time	= 51.2 us
Full line time	= 62.4 us
Horizontal sync	= 3.2 us
Vertical sync	= 249.6 us
Frame time	= 16.95 ms
Display refresh	= 29.5 Hz
VIURAM CPU/Display cycle time	= 1.6 us

The CRTC operates in the interlaced mode, so a monitor with a long persistence phosphor is very desirable to minimize flicker. In addition, a monitor with separate sync (TTL level) inputs is recommended because the corner definition is better and it is more stable in interlace applications.

The CRTC controller is accessed as part of the control register address space, and uses the upper two word locations. Only the bottom byte of each word is used, and most registers are read or write only (see Appendix). The CRTC requires a chip enable time of about 450 ns, and although it strobes data on the trailing edge of the enable pulse, the address must be set up before enable is asserted.

III.6 GRAPHICS MEMORY

The graphics memory (GRAM) is a 16K by 16-bit dynamic random access memory, which provides the data for the 512 dot by 512 line graphics display. The memory uses 16 standard 16K x 1, 16 pin, 250 ns RAM chips. Since the general operation of the CPU access has already been described, this section will be concerned only with the display buffer period.

At the beginning of the display buffer load period (C2), the timing does a buffer load from the character memory. About 200 ns after C2 starts, it is the GRAM's turn, and RAS is asserted, loading the row address into the GRAM. About 40 ns later, the column addresses are switched to the address inputs by MEMTOP going high. About 50 ns after that, the column addresses are stored in to the GRAM. About 250 ns after RAS, the data outputs become valid, and about 420 ns after RAS the data is strobed into the data buffer. 200 ns are then given over the GRAM precharge period, during which RAS and CAS are held inactive. The GRAM is accessed during C1 in a manner similar to C2, but the access is not preceded by a CRAM access.

III.7 CHARACTER MEMORY

The character memory (CRAM) is a 1K by 16 bit static random access memory, which provides data for the 64 character by 32 line alphanumeric display. The memory uses 4 standard 1K x 4, 18 pin, 300 ns RAM chips. Refer to III.3 for the CPU cycle description.

The CRAM buffer load period actually starts when the C1 precharge period (for the GRAM) begins. The address multiplexers are switched over to the display refresh address (from the CRTC) and the CRAM access time is measured from this point. C2 begins 200 ns later, and the CRAMs are selected. About 150 ns after C2 begis the output data becomes valid, and is strobed into the display buffer about 50 ns later. The rest of the C2 is devoted to the GRAM buffer load.

III.8 DISPLAY DATA BUFFER

The display data buffer (DDB) is a 4 word by 16 bit register file, which is used to hold one word each of graphics and

alphanumeric data. The DDB has separate read and write control logic, which permits data to be written into one part of it while different data is being read from another part. Refer to the diagram in Figure III.2 during the following description.

Starting with C2, the DDB passes to its outputs the low byte of the data currently being loaded into it from CRAM. 200 ns later, at the onset of RAS, the data is loaded into the character generator address register. The data from the GRAM is then loaded into the DDB, and on the trailing edge of C2, the lower byte of this GRAM data is written into the graphics shift register and the data from the character generator is written into the alphanumeric shift register. Now, at the beginning of C1, the low byte data previously loaded into the shift registers is shifted out bit by bit and sent to the monitor. While this is happening, the outputs of the DDB are shifted so that they put out the top byte, first of the CRAM, and then the GRAM. Thus data saved from C2 is loaded into registers at the end of C1 and displayed during the next C2 so that new data can be loaded during this next C2.

III.9 DISPLAY MODES

The display mode register stores the state of composite blanking, cursor, and reverse video enable and is updated every character time. If composite blanking is set, then the video will be disabled and the output to the monitor will go to black level. The cursor indicates an address match between the CRTC refresh address and the CRTC internal cursor address register. Its presence is made known to the user by a blinking reversal of the character image in the cursor match position. Reverse video causes the selected character to become black on white background. Both cursor and reverse video apply only to the alphanumeric display. There are two additional programmed I/O functions: Graphics reverse video, which is used to reverse the entire graphics image, and screen blank which has the same effect as the composite blanking signal.

III.10 GRAPHICS DATA OUTPUT

The graphics data output is generated by loading the graphics data shift register with data from the display data buffer on the trailing edge of both C1 and C2. The data is then

shifted out of the shift register, bit by bit, 100 ns per bit, during the subsequent C2 or C1 cycle. The shift register output is gated through the reverse video logic and then Exclusive OR'd with the alphanumeric data.

III.11 CHARACTER DATA OUTPUT

The character data output is generated by loading the alphanumeric data shift register with data from the character generator on the trailing edge of both C1 and C2. The character generator address register holds the ASCII code data supplied to it through the DDB from the CRAM for the 600 ns period allocated for character generator decoding. Row address data supplied by the CRTC selects which raster line of the character is to be decoded. At the end of this decode period the alphanumeric shift register is loaded, coincident with the loading of the graphics shift register. The output is gated with the cursor and reverse video signals and then Exclusive OR'd with the graphics serial data.

III.12 VIDEO OUTPUT

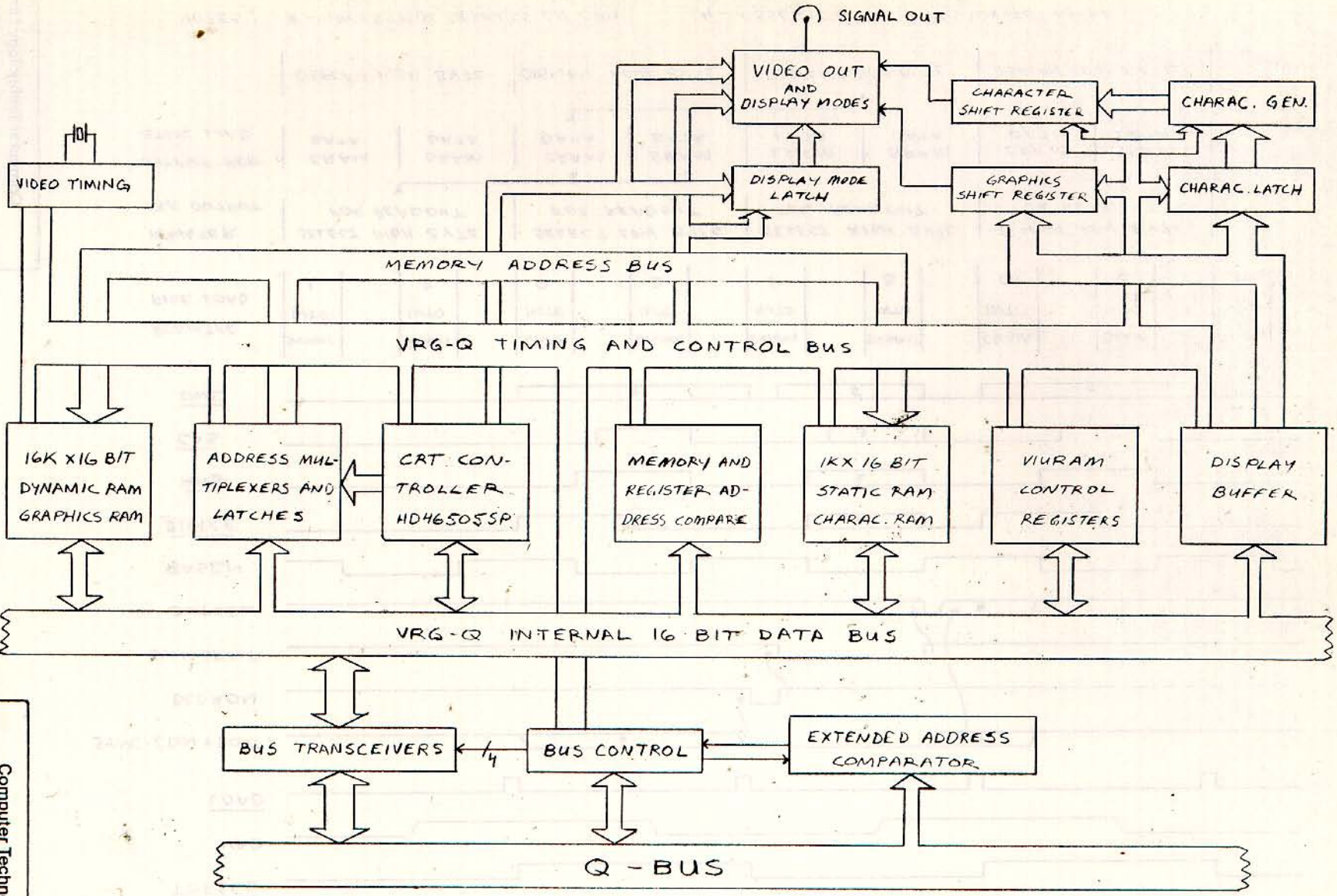
The video output circuit is the final link in the chain between the display memories and the video output connector. The Exclusive OR of the graphics and alphanumeric serial data streams is gated with the composite blanking and screen blank signals and then fed to the output synchronizer. The synchronizer clocks the data out at the dot clock speed, and by clocking the data just as it goes to the monitor, ensures that differences in propagation delay in the upstream logic have no effect on the framing of the video data. If this is not done, then overlap of blanking and video occurs which mainfests itself in very thin vertical lines on either side of the display.

The synchronized video is connected to an open collector driver, and thus to the video output connectors. Jumpers allow the video output to be mixed with composite sync or to have separate video, horizontal sync and vertical sync. In the composite mode, the video signal is about 0.8 volts above black level and sync is about 0.5 volts below black level. In the separated mode, all three signals are TTL level, either high or low active.

To ensure that the video signal is as clean as possible, the supply voltage to the video output circuit is generated by a 5 volt regulator working from the 12 volt supply. The regulator ensures a low impedance ripple free +5 volts no matter what kind of noise is on the normal +5 and +12 volt supply lines.

III.13 CHARGE PUMP

The GRAM uses standard 16K x 1 dynamic RAMs, which means that +5, +12 and -5 volts must be supplied. The backplane supplies +5 and +12, but the VIURAM must supply the -5. An INTERSIL ICL7660 is used to do this. This chip generates -5 from +5 with about 98% conversion efficiency with the load connected. Essentially, the ICL7660 generates the -5 by switching in a capacitor between +5 and ground, then disconnecting the capacitor and reconnecting it so that its positive terminal goes to ground and its negative terminal goes to the output of the circuit. The output voltage is smoothed by an additional capacitor and then distributed to the RAM chips. A reverse biased high speed diode is connected between the output and ground, so that if the output is accidentally made to go above ground (i.e., greater than 0 volts) the diode will clamp the output to ground. This is necessary to protect the RAMs which could otherwise be destroyed when the charge pump circuit fails.



TITLE: VRG-Q BLOCK DIAGRAM

Peritek corporation

Computer Technology Division

DRAWN BY: [illegible]

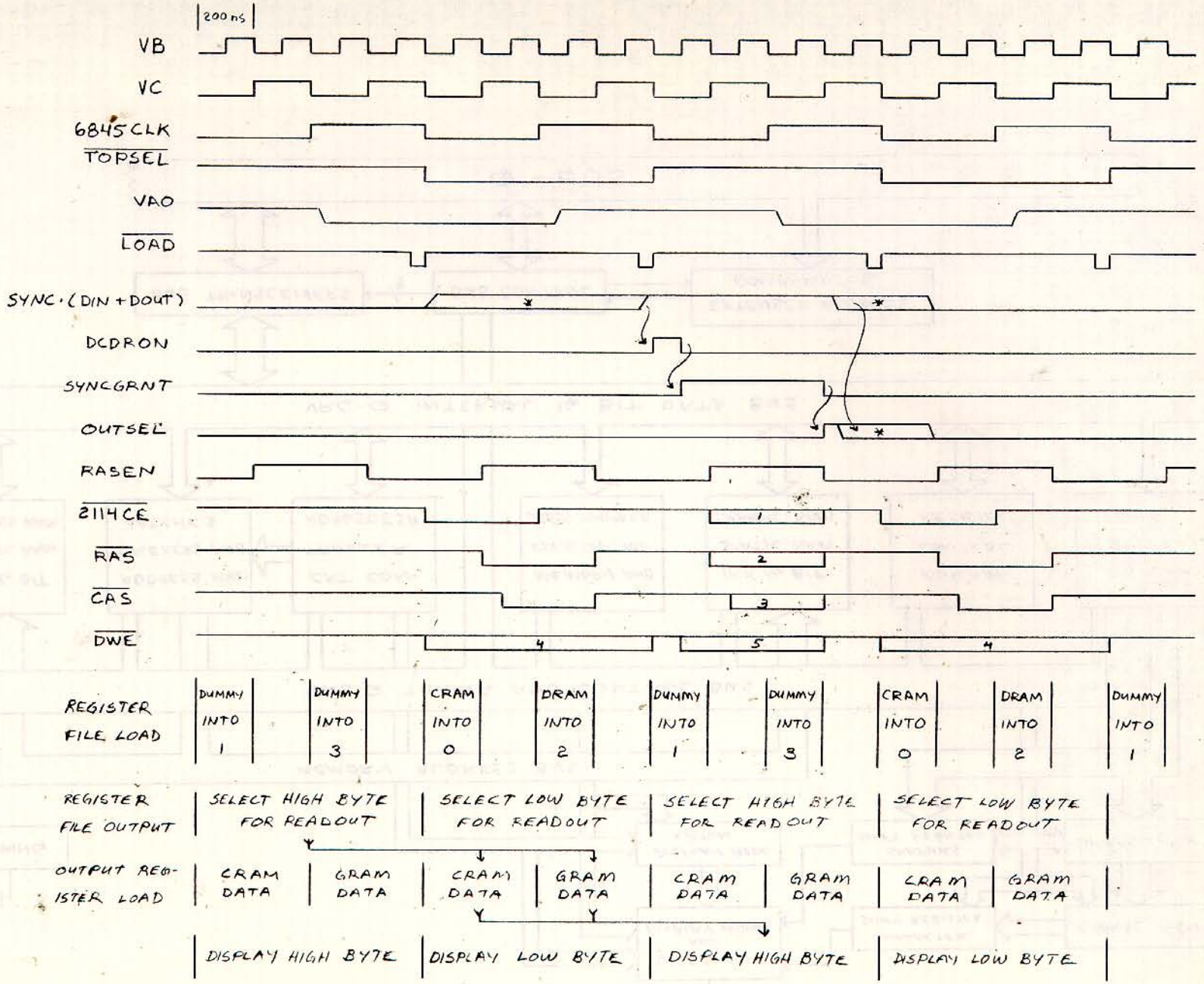
SCALE:

DATE: 4-1-81

REVISED:

DRAWING NUMBER: FIGURE III.1

TITLE: VRG-Q TIMING DIAGRAM



NOTES:
- * - UNCERTAIN, DEPENDS ON CPU
- 1 - ASSERTED IF CRAM ACCESS
- 2,3 - ASSERTED IF GRAM ACCESS
- 4 - ASSERTED IF AUTO-WRITE MODE
- 5 - ASSERTED IF WRITE INTO GRAM

Computer Technology Division

Peritek corporation

DRAWN BY: JRD

SCALE:

REVISED:

DATE: 4-1-81

DRAWING NUMBER: FIGURE III.2

Chapter IV
PROGRAMMING

IV.1 SUMMARY

Programming the VIURAM is very simple because the computer has immediate random access to every bit position and every character position on the display. The display changes as soon as the information in the graphics or alphanumeric memories changes. There is no waiting for character transmission to an external device, so no output queue or interrupt servicing are necessary.

The VIURAM is actually four different devices: a graphics video memory, an alphanumeric video memory, a control register, and the CRTC, which contains two registers. Furthermore, the video memories can be accessed directly or on a line by line basis.

The graphics video memory contains 256K bits which represent the status of all the pixels in the graphics image. The alphanumeric video memory contains 2K bytes which represent the characters which are displayed in parallel with the graphics image.

The control register controls the addressing mode of the memories, the line select for line addressing mode, and various display output control functions.

The CRTC controls the video display timing. It must be initialized after power up or reset to generate the display and to refresh the dynamic RAM's. The CRTC also is used to specify the starting address in memory of the display field (scrolling) and the nature and location of the character cursor.

Peritek Corporation offers a wide variety of software to support the VRG-Q. A number of utility and test programs are provided free of charge to first time purchasers of the VRG-Q. These programs are described in Section IV.6. Other software is also available. Contact Peritek for additional information.

IV.2 MEMORY ADDRESSING

The graphics memory is 16K words x 16 bits per word. Each bit in graphics memory corresponds to one pixel position on the display. When a bit is set (=1) the corresponding pixel is on, when the bit is clear (=0) the pixel is off. Each line of 512 pixels corresponds to 32 words in the graphics memory. Within that 32 word line, word 0 bit 0 corresponds to the leftmost pixel, word 0 bit 1 is the next pixel to the right and so forth, with bit 15 of word 31 representing the rightmost pixel on the line. When using direct addressing, bytes 0-63 represent the top line of the display, 64-127 are the second line, etc. When using line addressing a nine bit line address (in the control register) selects which of the 512 lines is being accessed. Line address 0 is at the top of the display.

The alphanumeric memory is 1K words x 2 bytes per word. Each byte in the alphanumeric memory represents one character block (8 pixels by 16 raster lines) on the display. The low order 7 bits of the byte act as an address into the EPROM character generator and select one 8 x 16 character pattern to be displayed in the corresponding character block for that byte. Standard 7-bit ASCII is used with the character generator provided when the alphanumeric option is ordered. The high order bit in each byte determines whether the character will appear in normal (white character on dark field) or reverse video. If the high order bit is set (=1) the character will display in reverse video.

The character display format is 32 lines with 64 characters per line. Each line corresponds to 64 bytes (32 words) of memory with byte 0 being the leftmost character and byte 63 the rightmost character on the line.

When using direct addressing, bytes 0-63 represent the top line of the display, bytes 64-127 the second line, ..., and bytes 1984-2047 the bottom line. Higher order address bits are "don't care" bits when the alphanumeric memory is selected.

When using line addressing, the low order 5 bits of the 9-bit line address, select which of the 32 character lines is being accessed. Line address 0 is at the top of the display. The high order 4 bits of the line address are "don't care" bits.

IV.3 VRG-Q CONTROL REGISTER

The VRG-Q responds to four device registers. They are:

774140 - Line Address and Display Control Register
774142 - Not used
774144 - CRTC Address Register
774146 - CRTC Data Buffer

The following table defines the VIURAM control register bits.

VRG-Q CONTROL REGISTER BIT ASSIGNMENTS

Mnemonic	Bit	R/W	Function
SCRNBLK	15	Y	Blanks the video display. Does not change any memory data. Cleared by BINIT.
LA8-LA0	14-6	Y	Line address register. Cleared by BINIT.
VGO	5	Y	Enables the CRTC when set. Cleared by BINIT which consequently resets the CRTC.
VRON	4	Y	Enables bus response to addresses in the display memory address range. Cleared by BINIT.
CRAM	3	Y	Enables the CRAM to be addressed in place of the GRAM. Cleared by BINIT.
MEMLOAD	2	Y	Loads a pattern stored in the first 64 bytes of CRAM into every line of the graphics memory as the display image is scanned. Cleared by BINIT.
RVEN	1	Y	Reverses the image of the graphics display. The white becomes black and the black becomes white. Cleared by BINIT.
DMAEN	0	Y	Enables direct addressing of the display memories in 22-bit Q-Bus Plus address space. Disables programmed control of the LAx bits. Cleared by BINIT.

Mnemonic	Function
SCRNBLK	Blanks the video display by turning off the video output signal. Horizontal and vertical sync are still produced.
LA8-LA0	Line address register. Line 0 is at the top of screen, line 777 at the bottom. Only bits LA0-LA4 are significant when addressing CRAM.
VGO	Enable CRTC. This bit must be set to generate a display and to refresh the dynamic RAM's. It should only be set after the video timing parameters have been initialized.
VRON	Enables the VRG-Q memory response for the data registers (when using line addressing) and main memory (when using direct memory access).
CRAM	Causes CRAM to respond to VRG-Q memory accesses (either line or direct) in place of GRAM.
MEMLOAD	Loads each byte in each line of GRAM with the data in the corresponding byte of line 0 (top line) of CRAM. Data in CRAM line 0 must be set up, then set this bit and wait at least 34 msec (wait for third clock tick if using a line time clock). Reset this bit before attempting to output to the VRG-Q again. This function is useful for setting GRAM to all zeroes or all ones (or some other pattern) without requiring CPU cycles.
RVEN	Complements the graphics image. For a graphics-only display, the state of a pixel is determined from the state of the corresponding bit in graphics memory (GBIT) according to the equation: Pixel = GBIT XOR RVEN If alphanumeric memory is present, then the state of a pixel is also affected by the state of the corresponding bit from the character generator (CGBIT) and bit 7 of the character (CBIT7) for the character block the pixel is in: Pixel = (GBIT XOR RVEN) XOR (CGBIT XOR CBIT7)

DMAEN Disables line addressing mode. If direct addressing has been implemented in the hardware (see Sections II.3 and V.2), then this bit enables the memory response to the direct addresses. Must be cleared before line addressing can be used again.

IV.4 CRTC REGISTERS

The CRTC has 18 internal registers. These internal registers are accessed indirectly through two external registers. One external register serves as an address into the internal register array, the second external register is a data buffer through which the selected internal register can be read or written. The two external registers are directly addressed as VRG-Q device registers. They are:

CRTC Address Register Bit Assignments

Mnemonic	Bit	R/W	Function
AR4-AR0	4-0	W only	CRTC Register File Select. Data loaded into this location functions as an address into the CRTC parameter register file. The data in that register is available in the CRTCBUF. Not cleared by BINIT.
------	15-5	---	Not used.

CRTC Data Buffer Bit Assignments

Mnemonic	Bit	R/W	Function
D7-D0	7-0	R/W	CRTC Data Buffer. The register selected by CRTCAR is accessed through this location. See Appendix for specific bit assignments as a function of this register. Most registers are read only or write only. Not cleared by BINIT.

The first ten CRTC internal registers (R0-R9) control the video timing and are explained in the next section. The

remaining eight registers have other functions as follows:

Register Pair	Function
R10-R11	Character cursor size and mode
R12-R13	Display starting address
R14-R15	Character cursor location
R16-R17	Not used in the VRG-Q

The character cursor is a hardware generated reverse video cursor which can be positioned at any of the 2048 character locations of the VRG-Q. The size of the cursor can range from a single scan line to all the scan lines in the full character block. Any sequence of contiguous scan lines can be selected for the cursor. Keep in mind that scan line 0 is at the top of the character block and scan line 15 is at the bottom. Load R10 with the starting scan line number and load R11 with the ending scan line. Typical values would be 0, 15 for a full block cursor and 15,15 for a single line at the bottom of the character block. bits 5 and 6 in R10 control the cursor mode as follows:

Bit 6	Bit 5	Cursor Mode
0	0	Cursor On
0	1	Cursor Off
1	0	Blink @ 4 Hz
1	1	Blink @ 2 Hz

Registers R14 and R15 control the location of the cursor on the screen. R15 is the low 8 bits of the address and R14 is the high six bits. Load a value from 0 to 2047 into these registers to position the cursor on the corresponding character block.

Registers R12 and R13 contol the address in memory at which the display starts. These registers can be used to effect scrolling of the display by one character line (16 raster lines) at a time. R13 is the low byte of the address and R14 is the high six bits. Normally the display starting address is zero. Increment the address by 64 to scroll up one line. This moves the previous top line to the bottom of the screen. The character and graphics memories always scroll together.

IV.5 VIDEO TIMING INITIALIZATION

the HD46505 controller (CRTC) in the VIURAM must be programmed to generate the proper video timing for the hardware configuration used and the display format used. Since the display format has been predetermined to be 512x512, many of the initialization parameters should not be changed from those recommended by Peritek Corporation. Certain parameters can still be adjusted by the user to suit the requirements of the monitor, in particular parameter 2 (horizontal sync position), parameter 3 (vertical and horizontal sync widths) and parameter 7 (vertical sync position).

This section explains how to calculate the timing parameters and how to initialize the CRTC. For further information, read the CRTC data sheet in the Appendix.

IV.5a HORIZONTAL TIMING

The horizontal timing parameters are a function of the monitor scan rate and the time it requires for horizontal retrace, the frequency of the VIURAM's video clock and the number displayed pixels per line. A typical monitor has a scan rate or 15,750 Hz $\pm$ 500 Hz, and requires about 11 microseconds for horizontal retrace. The standard video clock is 10.00 MHz. Although the line format is 512 pixels, the CRTC is programmed in terms of 8 bit character times and must be set up to display 64 characters/line. The only way to get 512 displayed lines on a standard monitor (in 30 Hz refresh) is to run it at the high end of its horizontal scan rate, or near 16250 Hz. The following calculations show how to obtain the horizontal parameters.

Monitor Scan Rate = 16250 Hz

Monitor Scan Period $= \frac{1}{16250 \text{ Hz}} = 61.5 \text{ ms}$

Character Times $= \frac{8 \text{ pixels/character}}{10 \text{ MHz}} = 800 \text{ ns}$

Total Character Times per Line $= \frac{61.5 \text{ ms}}{800 \text{ ns}} = 76.875$

This figure of 76.875 character times per line is a nominal value which must be rounded to an even number. Choosing 78 character times per scan line gives 78*.800 = 62.4 usec/line which is equivalent to a scan frequency of 16025 Hz, well within tolerance. It gives (78-64)*.800 = 11.2 usec for retrace, which should be adequate. The sync position and sync widths are chosen on the basis of specifications supplied by the monitor manufacturer, (and perhaps by some experimentation) to find values which give a centered and stable display. With 14 character times available for the retrace interval, a sync period of 5 character times with a "front porch" delay of 5 character times (and therefore a "back porch" of 4 character times) gives a good looking display on many monitors. Changing the horizontal sync position and/or width parameters may be required in some cases. Contact Peritek Corporation in the event that problems arise in obtaining a satisfactory display.

30 Hz Horizontal Parameters (U.S.)

Register File Number	Name	Value	How Calculated
0	Horizontal Total	77.	78.-1
1	Horizontal Displayed	64.	Given
2	Horizontal Sync Position	69.	64.+5
3	Horizontal Sync Width	5.*	Monitor Spec

* Plus vertical sync width calculated below.

When 25 Hz refresh (European) is desired, the parameters should be changed slightly to take advantage of the looser timing requirements which result from the additional raster lines obtained in the 25 Hz mode.

25 Hz Horizontal Parameters (European)

Register File Number	Name	Value	How Calculated
0	Horizontal Total	79.	80.-1
1	Horizontal Displayed	64.	Given
2	Horizontal Sync Position	69.	64.+5
3	Horizontal Sync Width	6.*	Monitor Spec

*Plus vertical sync width calculated below.

Horizontal scan rate is 15625 Hz or 64 ms.

IV.5b VERTICAL TIMING

The vertical timing parameters are a function of the actual horizontal scan rate, power line frequency, number of displayed raster lines, interlace mode and vertical retrace time. it is important that the frame refresh rate be close to the power line frequency to prevent "swimming" of the display.

The CRTC is programmed in terms of character lines, with 16 raster lines per character line. To obtain 512 displayed lines means 32 character lines. The display will be operated in interlaced mode and 60 Hz power line frequency.

Full Screen Refresh Rate = 30 Hz = $\frac{\text{Frame Rate}}{2}$

Horizontal Scan Rate = 16025 Hz

Scan Lines/Frame = $\frac{16025 \text{ Hz}}{30}$ = 535

Scan Lines/Character Line = 16

Total Character Lines = $\frac{535}{16}$ = 33.4375 = 33

Vertical Total Adjust = 535 - (16 * 33) = 7

Vertical Retrace Time = $\frac{(535 - 512)}{2}$ * 62.4 = .7176 ms

720 ms may be insufficient for the vertical blanking interval in some cases, so some "padding" of the vertical total adjust may be required. The vertical sync width should be close to 200 ms. It is programmed in scan line times so 200/62.4 = 3 scan lines. This value must be multiplied by 16 to shift it into the left 4 bits of parameter 3.

30 Hz Vertical Parameters (U.S.)

Register File Number	Name	Value	How Calculated
3	Vertical Sync Width	48*	16*3
4	Vertical Total	32	33-1
5	Vertical Total Adjust	7	535-(16*3)
6	Vertical Displayed	32	Given
7	Vertical Sync Position	32	Given
9	Scan Lines/Character Line	14	16-2

* Plus horizontal sync width calculated above.

The parameters for 50 Hz power line frequenc are a little different.

Full Screen Refresh Rate = 25 Hz = $\frac{\text{Frame Rate}}{2}$

Horizontal Scan Rate = 15625 Hz

Scan Lines/Frame = $\frac{15625}{25}$ = 625

Scan Lines/Character Line = 16

Total Character Lines = $\frac{625}{16}$ = 39.0625 = 39

Vertical Total Adjust = 625-(16*39) = 1

Vertical Retrace Time = $\frac{(625-512)}{2}$ * 64 = 3.616 ms

25 Hz Vertical Parameters (European)

Register File Number	Name	Value	How Calculated
3	Vertical Sync Width	48*	16*3
4	Vertical Total	38	39-1
5	Vertical Total Adjust	1	625-(16*39)
6	Vertical Displayed	32	Given
7	Vertical Sync Position	34	Empirical
9	Scan Lines/Character Line	14	16-2

* Plus horizontal sync width calculated above.

IV.5c MISCELLANEOUS PARAMETERS

Several other parameters must be set up. Each will be explained and a suggested value given.

Parameter 8 - Mode Control. This parameter controls the interlace mode and the display enable and cursor enable delay times. The display and cursor enable delay times are related to the manner in which characters are read from display memory and how long it takes to get them through the VRG logic. The two bit value for each is thus determined by the hardware design. Similarly, since the VRG is operated in full interlace mode, there is no choice in it's selection. This parameter 8 should be loaded with the value 83.

Parameters 10-11 - Cursor start and end. These parameters control the height of the hardware addressable cursor. To obtain a full block blinking cursor, parameter 10 should be loaded with 140 and parameter 11 with 14. To disable the cursor, load 40 into parameter 10.

Parameters 12-13 - Display start (H and L bytes). These parameters control the starting address in display memory. They are normally loaded with zero, but may be changed to scroll the display.

Parameters 14-15 - Cursor Position (H and L bytes). These parameters control the position of the hardware addressable cursor. A value of 0 places the cursor in the upper left-hand

corner of the display.

IV.6 SOFTWARE DOCUMENTATION

Four programs are provided on floppy diskette to first time users of the VRG-Q. These programs are used to initialize and test the operation of the VRG-Q.

The programs execute under the RT11 operating system. They are:

VRGINT	Initialize VRG-Q
VRGTST	Test graphics memory
PCMTST	Test parallel character memory
VRGSAV	Save and restore image to/from disk file

IV.6a VRGINT DOCUMENTATION

Purpose: To initialize the CRT controller chip used in the VRG-Q.

Operation: This program is executed by giving the monitor command:

```
.RUN VRGINT
```

It is recommended that this command be included in the user's startup command file.

VRGINT exits gracefully if no VRG-Q is installed.

Messages: None

Assemble: .MACRO VRGCND+VRGINT/OBJ

Link: .LINK VRGINT

Source Mods: The VRGCND file must be modified to reflect changes in device register location if the board addressing is changed.

The table of timing parameters may have to be changed to accommodate different monitors. See Section IV.5 for information

on how to determine the proper values for these parameters.

IV.6b VRGTST DOCUMENTATION

Purpose: To test the dynamic RAM's used in the VRG-Q graphics image memory.

Operation: The VRG-Q must be initialized prior to running this program. This program is executed by giving the monitor command:

```
.RUN VRGTST
```

Messages:

```
*** WARNING *** VRG NOT INITIALIZED --- EXIT
RAM DIAGNOSTIC FOR VRG-Q -- GRAPHICS MEMORY
RAM IS OK

     OR DATA              AND DATA
0000000000001000     0000000000001000
   OR ADDRESS           AND ADDRESS
011111111111110      000000Q000000000
```

Error Detection: The program makes several passes through memory using different data patterns. It uses an effective algorithm for detecting pattern sensitive RAM failures. It also will detect open or short circuited data and address lines as well as cross-connected data and address lines.

When an error occurs the bad data bit(s) are OR'd into a word (initially all zeroes) and AND'd into another word (initially all ones). The 14-bit word address is formed and is OR'd and AND'd in a similar manner. Testing continues until the entire memory has been checked with the current pattern. If any errors have been detected testing is terminated and the error message is displayed on the console device.

The example error message shown above indicates that bit 3 (and only bit 3) was bad, and that it was bad at a wide variety of addresses (possibly at all addresses).

Patches: The following locations may be patched by the user

to adapt the program to his needs.

Location	Value	Function
1000	174140	VRG CSR address
1002	174000	VRG data register base address
1004	2210	Delay counter (4 msec on 11/23)- used to test memory refresh function
1006	2	Pattern repetitions each cycle
1010	4	Number of complete cycles to execute

IV.6c PCMTST DOCUMENTATION

Purpose: To test the static RAM's used in the VRG-Q parallel character memory.

Operation: The VRG-Q must be initialized prior to running this program. This program is executed by giving the monitor command:

```
.RUN PCMTST
```

Messages:

```
*** WARNING *** VRG NOT INITIALIZED --- EXIT
RAM DIAGNOSTIC FOR VRG-Q -- GRAPHICS MEMORY
RAM IS OK

     OR DATA              AND DATA
0000000000001000    0000000000001000
   OR ADDRESS           AND ADDRESS
0000011111111110    0000000000000000
```

Error Detection: The program makes several passes through memory using different data patterns. It uses an effective algorithm for detecting pattern sensitive RAM failures. It also will detect open or short circuited data and address lines as well as cross-connected data and address lines.

When an error occurs the bad data bit(s) are OR'd into a word (initially all zeroes) and AND'd into another word (initially all ones). The 10-bit word address is formed and is OR'd and AND'd in a similar manner. Testing continues until the entire memory has been checked with the current pattern. If any

errors have been detected testing is terminated and the error message is displayed on the console device.

The example error message shown above indicates that bit 3 (and only bit 3) was bad, and that it was bad at a wide variety of addresses (possibly at all addresses).

Patches: Two locations may be patched by the user to adapt the program to his needs.

Location	Value	Function
1000	174140	VRG CSR address
1002	174000	VRG data register base address

IV.6d VRGSAV DOCUMENTATION

Purpose: To save to a disk file and restore from a disk file the image in the VRG-Q memory.

Operator Input: Interactive program. Types a prompting message on console device. In response operator should enter 'R' to restore image from disk file or 'S' to save image to a disk file. Operator then enters file name in standard RT11 format (i.e., name.ext). Default extension is 'IMG'. Use control/C to exit.

File Format: Binary file. No identifying information in file.

Error Messages:

Warning VRG not Initialized -- Exit
CSI Error - Retry
No file entered - Abort
Bad device name - Retry
File not found - Retry (Input file only)
Can't open file - Retry (Output file only)
Input error on file
Output error on file
Close error

Assemble: MACRO VRGCND+VRGSAV/OBJ Link: LINK VRGSAV

Chapter V
APPLICATION NOTES

V.1 MONITOR SELECTION

The VRG-Q can be used with a wide variety of monitors but for the highest quality display, a good quality monitor must be used. High quality monitors are available from Motorola, Ball, Hitachi and other manufacturers. Features to look for in a monitor are:

TTL level inputs
Horizontal drive (width) control
High resolution
High bandwidth
Good corner focus
Horizontal blanking interval <12 usec.
Horizontal scan rate, 15.75 KHz
Long persistence phosphor (e.g., P39, P41)

Monitors with composite video input can also be used but TTL input is preferred for highest quality display.

TTL input monitors have one drawback which can be serious. The horizontal drive transistor can burn out if the horizontal sync frequency is not correct. Unfortunately the CRTC chip, when uninitialized, typically generates a horizontal frequency which can destroy a horizontal drive transistor in a few seconds. Therefore it is very important that the CRTC be initialized before it is enabled.

V.2 22-BIT ADDRESSING

System based on the LSI-11/2 CPU do not have the ability to address more than 65K bytes of memory and therefore should not use the VRG in direct addressing mode.

The LSI-11/23 CPU with the memory management option and circuit revision C or newer has the ability to address up to 4 megabytes of memory. However, many backplanes in use today only have 18 address lines bussed.

To use direct addressing with the VRG all 22 address lines must be bussed. The following procedure explains how to modify a standard DEC Q-Bus backplane to bus the extra address lines.

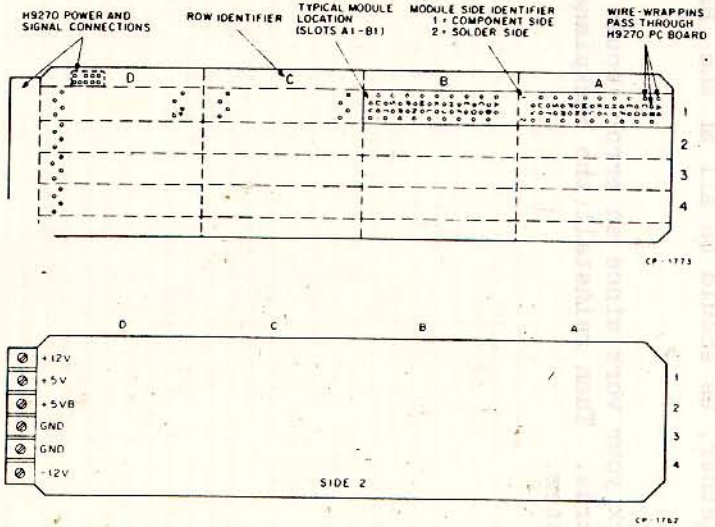
Turn off computer power, remove all boards from the computer and remove the backplane from the cabinet. Position the backplane so the wire-wrap pins are facing you. Orient the backplane so slot 1 is at the top.

Starting on the second group of wire-wrap pins (the "B" connector) count over three pins, to pin BC1. Install a wire-wrap jumper from slot one, BC1, to slot two, BC1. Install a jumper from slot 2, BC1, to slot three, BC1, and so on, to the last slot. Repeat this procedure for pins BD1, BE1, and BF1. If the backplane is a quad or hex-width unit, count over two more groups of pins (to the "D" connector) and repeat the procedure. Then wire-wrap a jumper from slot one BC1 to slot one DC1, slot one BD1 to slot one DD1, slot one BE1 to slot one DE1, and slot one BF1 to slot one DF1. Now, all of the BC1 (and DC1) pins should be bussed together, as should be all of the BD1's, BE1's and BF1's.

Be sure to check your work since an error could result in damage to the boards. Then reinstall the backplane and boards and power up the system.

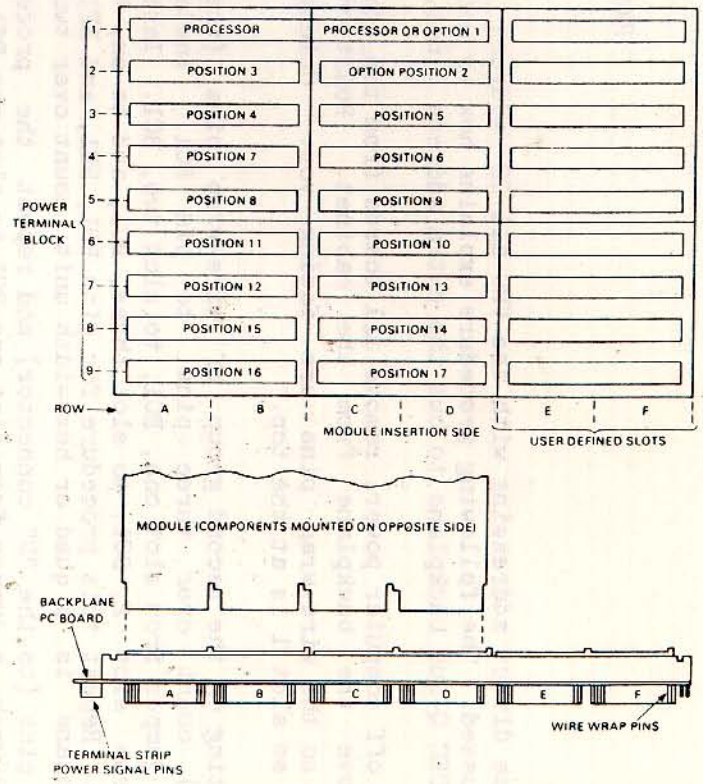
TITLE: VRG-Q BACKPLANE DIAGRAMS

H9270



H9270 Backplane Terminal Block (Pin Side View Shown)

DDV11-B



Computer Technology Division

Peritek corporation

DRAWN BY: VRD

SCALE:

REVISED:

DATE: 4-1-81

DRAWING NUMBER: FIGURE V.1

Chapter VI
MAINTENANCE

The VRG-Q requires no regular service, but if it is used in a particularly dirty environment, periodic dusting with dry compressed air is recommended.

Because of the heat generated by normal operation of the VRG-Q and other boards in the system, forced crossflow ventilation is required.

If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

NOTE: Failure to supply forced air cooling to the VRG-Q constitutes misuse of the board. Therefore, any failure of the VRG-Q due to overheating will not be covered by the warranty.

Chapter VII
WARRANTY

The VRG-Q is warranted to be free from defects in material or manufacture for a period of six months from date of shipment from factory. Peritek Corporation's obligation under this warranty is limited to replacing or repairing (at its option) any VRG-Q that is returned to the factory within this warranty period and is found by Peritek Corporation to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage.

All warranty repair work will be done at the Peritek Corporation factory. Before returning a module the customer must first request a Return Authorization Code from the factory.

This warranty is made in lieu of all other warranties expressed or implied.

Chapter VIII
SERVICE

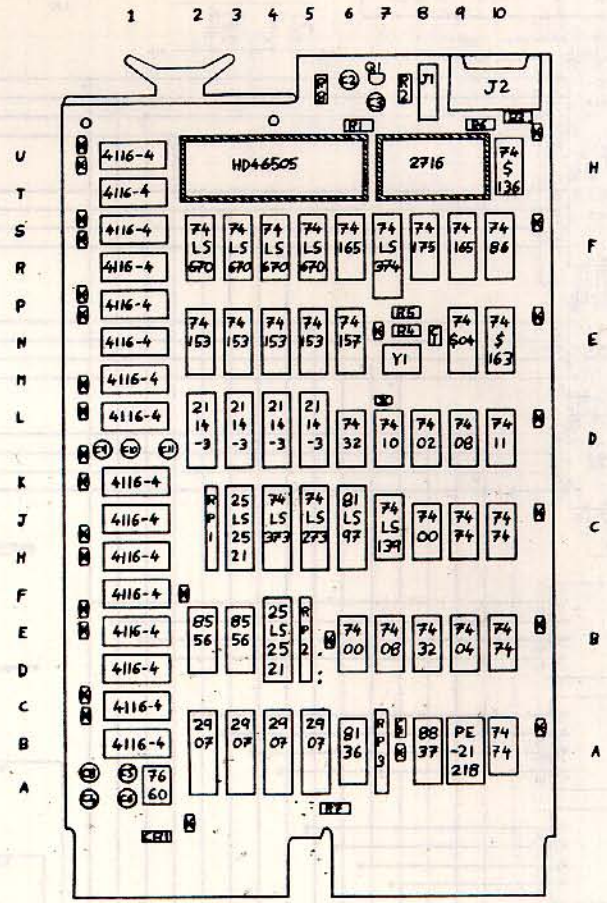
Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs to VRG-Q boards. If extensive repairs are required, Peritek Corporation will request a purchase order number for estimated time and materials charge. If replacement is required, a purchase order number will also be required.

Before returning a module to Peritek Corporation, the customer must first request a Return Authorization Code from the factory. The Return Authorization Code must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

All repair work will be done at the Peritek Corporation factory in Oakland, California, unless otherwise designated by Peritek Corporation. Customer should prepay shipping charges to the factory. Peritek Corporation will prepay return shipping charges to the customer.

Repair work is normally done within ten working days from receipt of module.

ITEM	QUANT	DESCRIPTION		VENDOR	LOCATION
1	2	7400	QUAD 2 INPUT NAND	TI, SIG, NAT	B6, C8
2	1	7402	QUAD 2 INPUT NOR	"	D8
3	1	7404	HEX INVERTER	"	B9
4	1	74S04	HEX INVERTER	"	E9
5	2	7408	QUAD 2 INPUT AND	"	B7, D9
6	1	7410	TRIPLE 3 INPUT NAND	"	D7
7	1	7411	TRIPLE 3 INPUT AND	"	D10
8	2	7432	QUAD 2 INPUT OR	"	B8, D6
9	3	7474	DUAL D FLIPFLOP	"	B10, C9, C10
10	1	74S86	QUAD 2 INPUT XOR	"	F10
11	1	74S136	QUAD 2 INPUT XOR	"	H10
12	1	74LS139	DUAL 2-TO-4 DECODER	"	C7
13	4	74153	DUAL 4-TO-1 SELECTOR	"	E2-5
14	1	74157	QUAD 2-TO-1 SELECTOR	"	E6
15	1	74S163	4 BIT BINARY COUNTER	"	E10
16	2	74165	8 BIT SHIFT REGISTER	"	F6, F9
17	1	74175	QUAD D FLIPFLOP	"	F8
18	1	74LS273	OCTAL D FLIPFLOP	"	C5
19	1	74LS373	TRISTATE OCTAL D LATCH	"	C4
20	1	74LS374	TRISTATE OCTAL D FLIPFLOP	"	F7
21	4	74LS670	TRISTATE 4 BY 4 REGISTER FILE	"	F2-5
22	4	2114-3	1024×4 STATIC RAM	NAT	D2-5
23	1	PE-21218	150 nS DELAY LINE	PULSE ENG.	A9
24	2	AM25LS2521	8 BIT COMPARATOR		B4, C3
25	1	2716	2K×8 EPROM	MOT	H7-9
26	4	AM2907	4 BIT BUS TRANCEIVER	AMD	A2-5
27	16	MCM4116AC25	16KX1 DYNAMIC RAM	MOSTEK	B1 THRU D1
28	1	HD46505SP	CRT CONTROLLER	HITACHI	H2-6
29	1	7660	-5 VOLT CHARGE PUMP	INTERSIL	A1
30	1	8136	6 BIT O.C. COMPARATOR		A6
31	1	81LS97	TRISTATE OCTAL BUFFER	NAT	C6
32	2	8656	TRISTATE PROGRAMMABLE BINARY COUNTER	"	B2, B3
33	1	8837	HEX RECEIVER	SIG, NAT	A8
34	1	78L05	5 VOLT REGULATOR	NAT	Q1
35	1	1N6263	DIODE	FAIR	CR1
36	2		39 Ω RESISTOR	ALLEN-BRADLEY	R3, R8
37	1		180 Ω "	"	R2
38	1		220 Ω "	"	R7
39	2		470 Ω "	"	R4, R5
40	1		10 KΩ "	"	R6
41	1		11 KΩ "	"	R1
42	3	4310R-101-122	10×1.2 KΩ " NETWORK	BOURNS	RP1, RP2, RP3
43	29	HC25U104DB05C4	.1 μFD CAPACITOR	SPRAGUE	*
44	2	CK05BX102K	.001 μFD "	AVX	C1, C7
45	7	D106X0016CA1	10 μFD, 16 V TANT "	NEMCO	C4-C6, C8-C11
46	2		2.2 μFD, 35 V " "	"	C2, C3
47	1	20.000	20 MHZ. CRYSTAL	NYMPH	Y1
48	1	DIL640P11	40 PIN LP ST SOCKET	CA	H2-6
49	1	DIL624P11	24 PIN LP ST SOCKET	"	H7-9
50	1	50084-1	COAX CONNECTOR	AMP	J1
51	1	3491-1002	10 PIN HEADER	3M	J2
52	1	SP2	CARD HANDLE	PHILLIPS	CPI
53	1	VRG-QIIPC	PC BOARD	CT	



* = .1 μFD CAPACITOR

▣ = DIP SOCKET

• = WIREWRAP PIN

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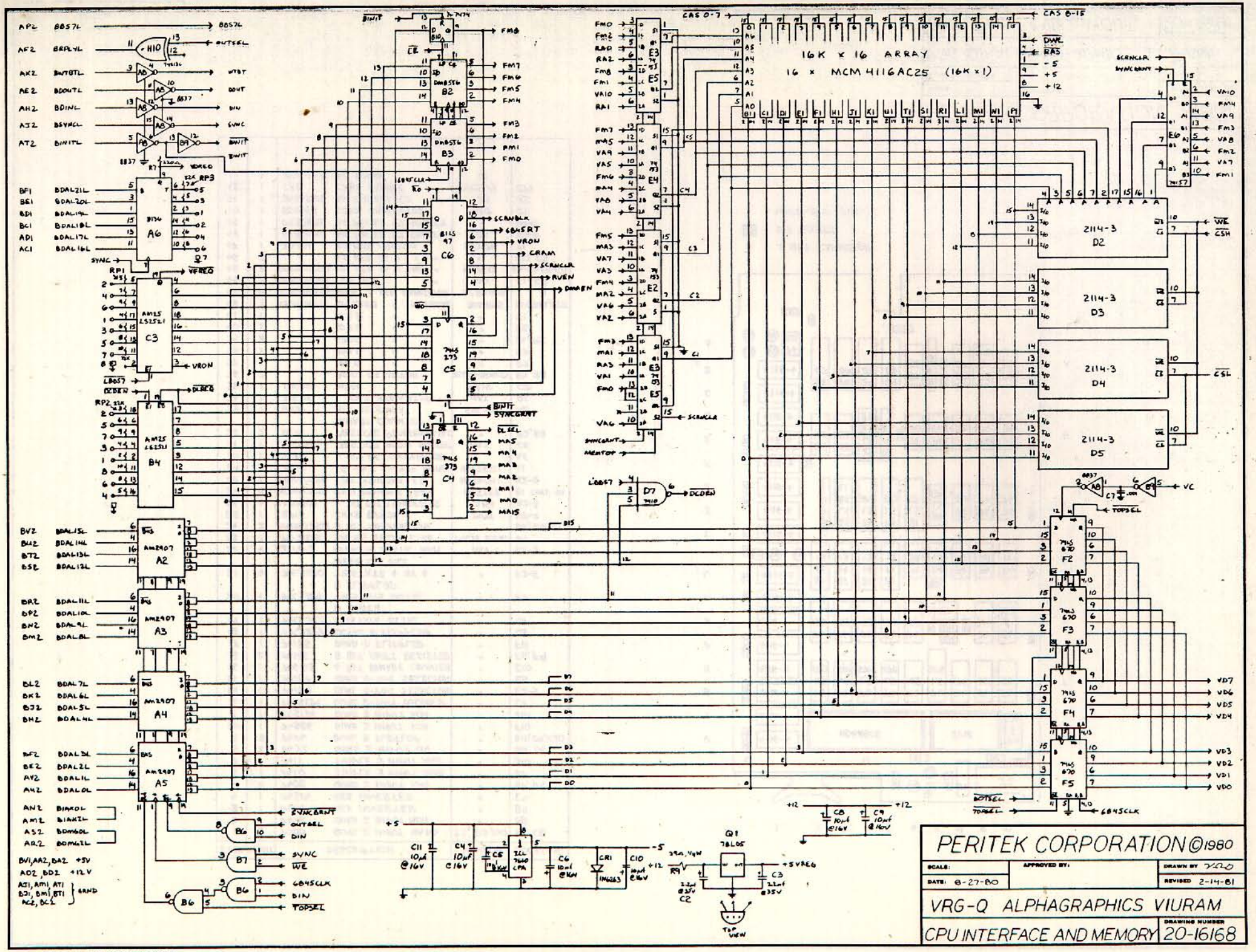
VRG-QII ALPHAGRAPHICS VIURAM

PARTS LIST AND LAYOUT — DRAWING NUMBER 20-16191


16K x 16 ARRAY
16 x MCM4116AC25 (16K x 1)
CAS 0-7
CAS 8-15
2114-3 D2
2114-3 D3
2114-3 D4
2114-3 D5
A6
C3
B4
A2
A3
A4
A5
B6
B7
C4
C5
C6
F2
F3
F4
F5
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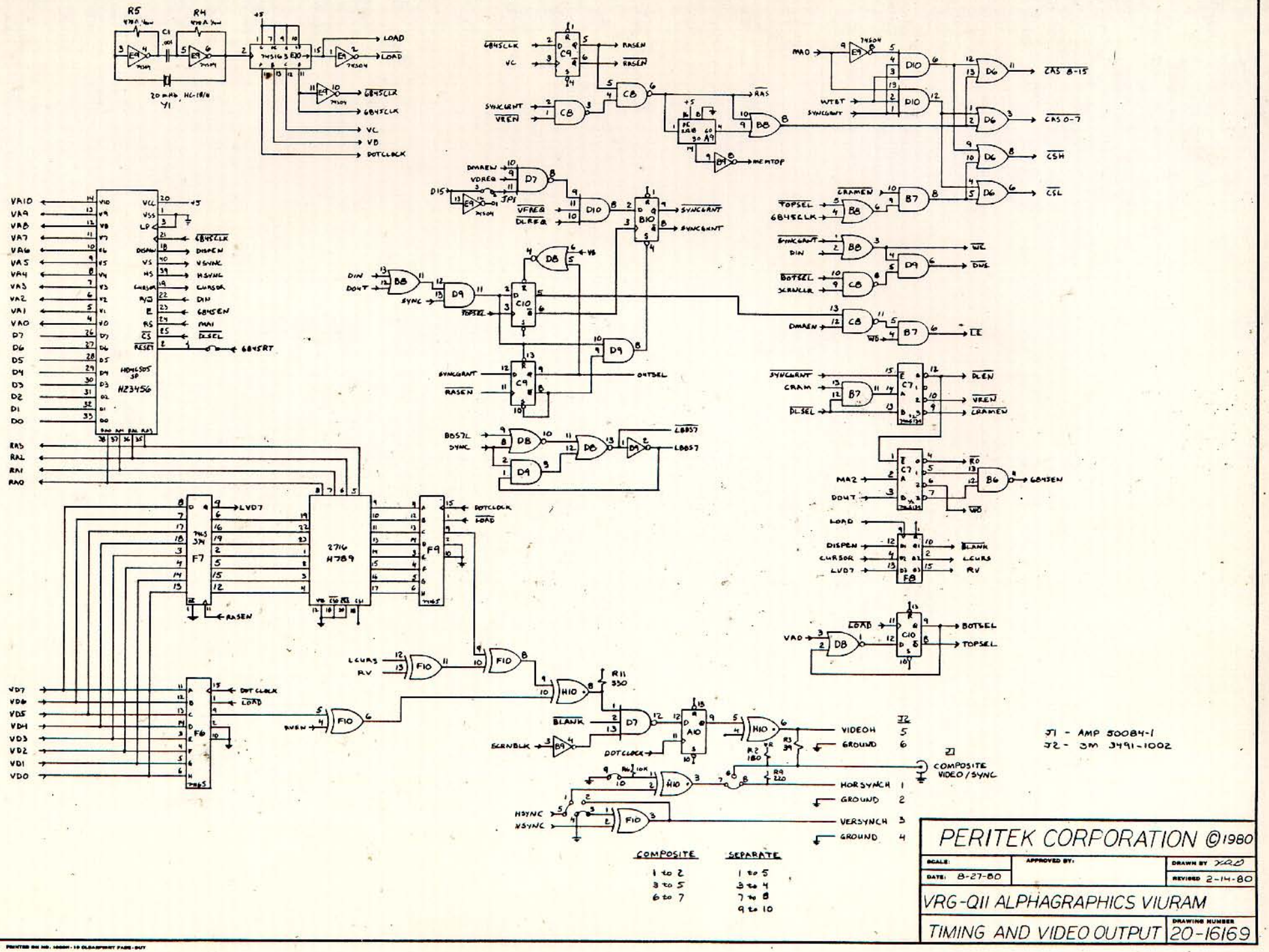
DATE: 8-27-80
REVISED 2-14-81
VRG-Q ALPHAGRAPHICS VIURAM
CPU INTERFACE AND MEMORY
DRAWING NUMBER 20-16168


RS
RH
20 mHz HC-18/U
Y1
LOAD
LOAD
6845CLK
6845CLK
VC
VD
DOTCLOCK
RASEN
RASEN
SYNCGRNT
VREN
RAS
MEMTOP
MA0
WTBT
SYNCGRNT
CAS 8-15
CAS 0-7
CSH
CSL
CRAMEN
TOPSEL
6845CLK
DMAREN
VDREQ
DISP
JP1
VFREQ
DLREQ
SYNCGRNT
SYNCGRNT
DIN
DOUT
SYNC
TOPSEL
DMAREN
WE
DWE
BOTSEL
SCRNCLR
LE
SYNCGRNT
RASEN
OUTSEL
SYNCGRNT
CRAM
DLSEL
DLEN
VREN
CRAMEN
BBS7L
SYNC
LBBS7
LBBS7
MA2
DOUT
RO
6845EN
WD
LOAD
DISPEN
CURSOR
LVD7
BLANK
LCURS
RV
FB
VA0
LOAD
BOTSEL
TOPSEL
VA10
VA9
VA8
VA7
VA6
VA5
VA4
VA3
VA2
VA1
VA0
D7
D6
D5
D4
D3
D2
D1
D0
HZ3456
6845CLK
DISPEN
VSYNC
HSYNC
CURSOR
DIN
6845EN
RAI
DSEL
RESET
6845RT
RA3
RA2
RA1
RA0
LVD7
F7
RASEN
2716
H789
F9
DOTCLOCK
LOAD
VD7
VD6
VD5
VD4
VD3
VD2
VD1
VD0
F6
DOT CLOCK
LOAD
LCURS
RV
F10
F10
H10
R11
330
BLANK
SCRNBLK
DOTCLOCK
A10
H10
VIDEOH
GROUND
R2
180
R3
39
COMPOSITE
VIDEO/SYNC
R9
220
HORSYNCH
GROUND
HSYNC
VSYNC
VERSYNCH
GROUND
J2
5
6
J1
1
2
3
4
J1 - AMP 50084-1
J2 - 3M 3491-1002
COMPOSITE
1 to 2
3 to 5
6 to 7
SEPARATE
1 to 5
3 to 4
7 to 8
9 to 10
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REVISED 2-14-80
VRG-QII ALPHAGRAPHICS VIURAM
TIMING AND VIDEO OUTPUT
DRAWING NUMBER
20-16169

HD46505 (CRTC)

CRT Controller

Peritek corporation

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SCALE:	
DATE:	REVISED:
DRAWING NUMBER:	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	-0.3	–	0.8	Vdc
Input Leakage Current		I_{in}	–	1.0	2.5	μAdc
Three-State (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	-10	2.0	10	μAdc
Output High Voltage (I_{load} = -205 μA) (I_{load} = -100 μA)	 D0-D7 Other Outputs	V_{OH}	 2.4 2.4	 – –	 – –	Vdc
Output Low Voltage (I_{load} = 1.6 mA)		V_{OL}	–	–	0.4	Vdc
Power Dissipation		P_D	–	600	–	mW
Input Capacitance	 D0-D7 All others	C_{in}	 – –	 – –	 12.5 10	pF
Output Capacitance	All Outputs	C_{out}	–	–	10	pF
Minimum Clock Pulse Width, Low		P_{WCL}	160	–	–	ns
Minimum Clock Pulse Width, High		P_{WCH}	200	–	–	ns
Clock Frequency		f_c	–	–	2.5	MHz
Rise and Fall Time for Clock Input		t_{cr}, t_{cf}	–	–	20	ns
Memory Address Delay Time		t_{MAD}	–	–	160	ns
Raster Address Delay Time		t_{RAD}	–	–	160	ns
Display Timing Delay Time		t_{DTD}	–	–	300	ns
Horizontal Sync Delay Time		t_{HSD}	–	–	300	ns
Vertical Sync Delay Time		t_{VSD}	–	–	300	ns
Cursor Display Timing Delay Time		t_{CDD}	–	–	300	ns
Light Pen Strobe Minimum Pulse Width		PW_{LPH}	100	–	–	ns
Light Pen Strobe Disable Time		t_{LPD1}	–	–	120	ns
		t_{LPD2}	–	–	0	ns

Note: The light pen strobe must fall to low level before VSYNC pulse rises.

BUS TIMING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
READ/WRITE				
Enable Cycle Time	t_{cycE}	1.0	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	μs
Setup Time, $\overline{CS}$ and RS valid to enable positive transition	t_{AS}	160	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time (Read) (write)	t_H	10 10	– –	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	–	25	ns
Data Setup Time	t_{DSW}	195	–	ns
Data Access Time	t_{ACC}	–	480	ns

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	-0.3 to +7.0	Vdc
Input Voltage	V_{in}*	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*With respect to V_{SS} (Gnd).

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PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) – The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal Register File and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation. A high level on a data pin is a logical "1."

Enable (E) – The Enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

Chip Select ($\overline{CS}$) – The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC when low to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) – The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active low ("0").

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and Display Enable signals.

Vertical Sync (V SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable – This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active Display Area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the Refresh RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Refresh Memory Addresses (MA0-MA13) – These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs drive a TTL load and 30pF. A high level on MA0-MA13 is a logical "1."

Raster Addresses (RA0-RA4) – These 5 outputs from the internal Raster Counter address the Character ROM for the row of a character. These outputs drive a TTL load and 30pF. A high level (on RA0-RA4) is a logical "1."

OTHER PINS

Cursor – This TTL compatible output indicates Cursor Display to external Video Processing Logic. Active high signal.

Clock (CLK) – The CLK TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTR) – This high impedance TTL/MOS compatible input latches the current Refresh Addresses in the Register File. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd

$\overline{RES}$ – The $\overline{RES}$ input is used to Reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into following status:

(A) All the counters in CRTC are cleared and the device stops the display operation.
(B) All the outputs go down to low level.
(C) Control registers in CRTC are not affected and remain unchanged.

This signal is different from other M6800 family in the following functions:

(A) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(B) After $\overline{RES}$ has gone down to low level, output signals of MA0-MA13 and RA0-RA4, synchronizing with CLK low level, goes down to low level. (At least 1 cycle CLK signal is necessary for reset.)
(C) The CRTC starts the Display operation immediately after the release of $\overline{RES}$ signal.

TABLE 1 – CRTC Operating Mode

$\overline{RES}$	LPSTB	OPERATING MODE
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

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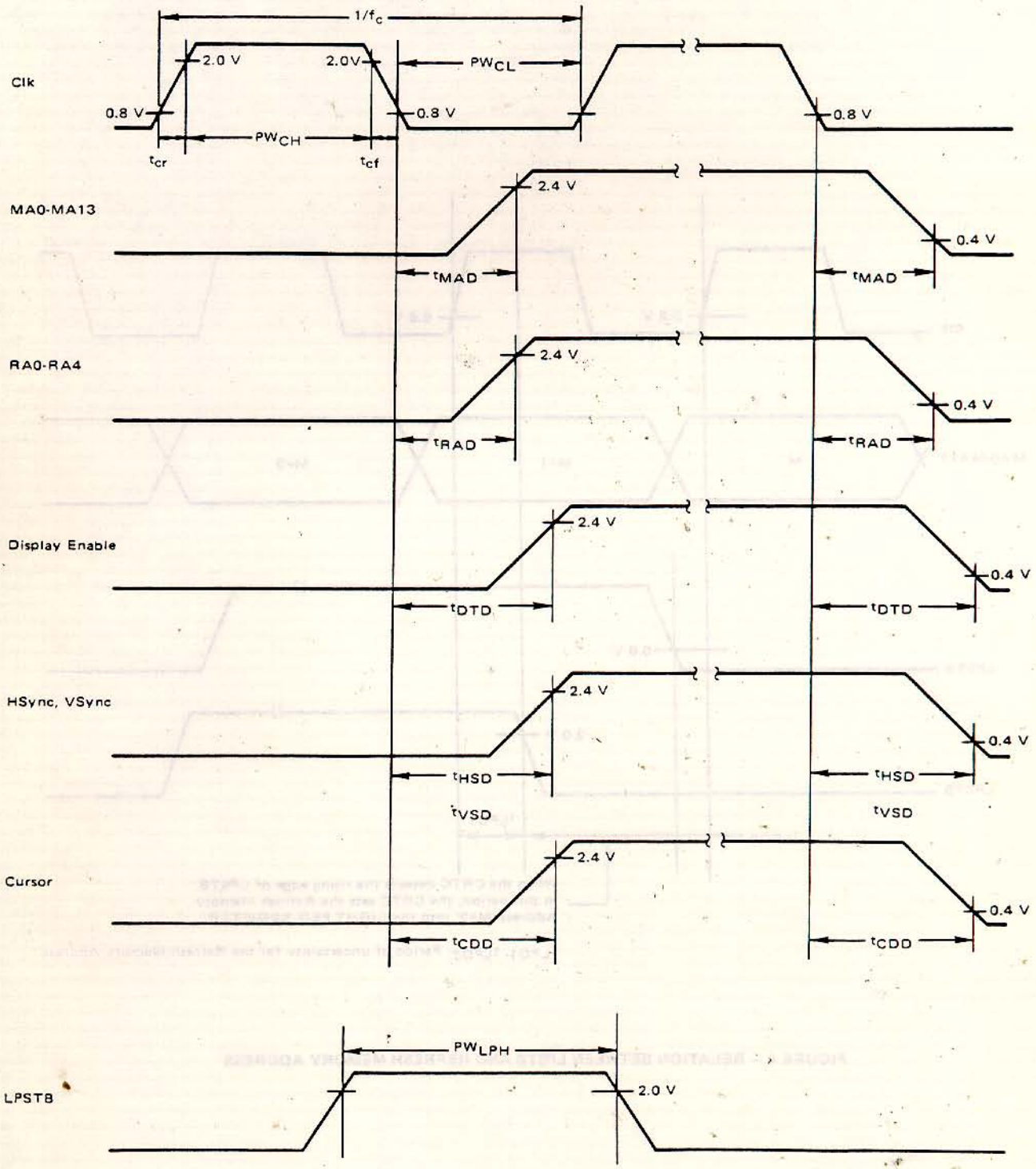

FIGURE 3 – CRTC TIMING CHART

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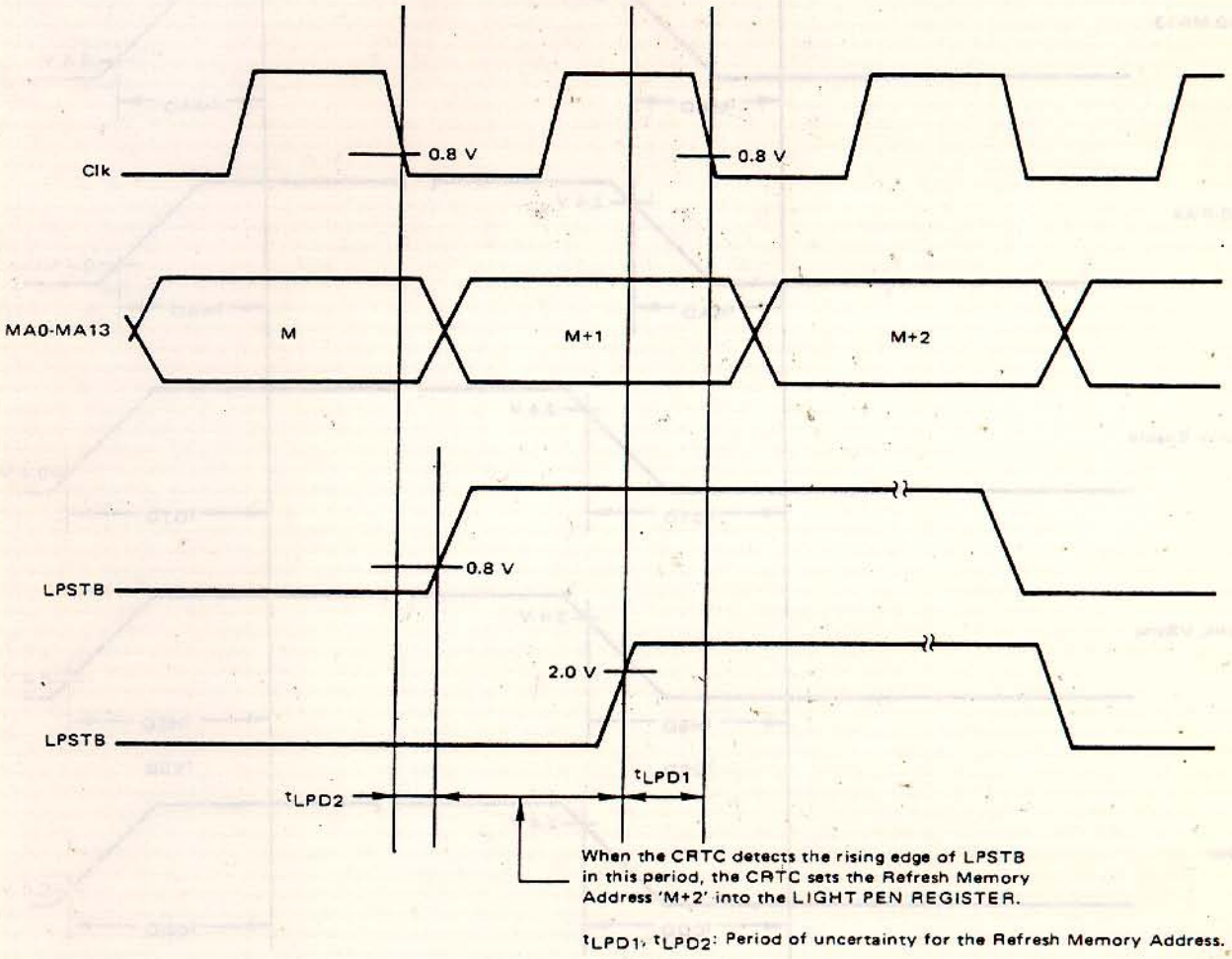

FIGURE 4 – RELATION BETWEEN LPSTB AND REFRESH MEMORY ADDRESS

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● FEATURES

The HD46505 (CRTC) is a peripheral chip of HMCS6800 Microcomputer LSI families. It is designed in order to provide a simple and effective means of interfacing the raster scan CRT display to MPU bus. Its primary function is to generate the proper refresh address and video timings according to display format.

HD46505 is applicable to wide range of raster scan displays.

It is optimized for hardware/software balance in order to achieve integration of complex CRT interface functions and to maintain flexibility.

Applications include intelligent CRT terminals, information display systems and video games.

- Programmable Screen and Character Format.
- Line Buffer-less Refreshing
- 14 Bits Refresh Memory Address
- Programmable Interface or Non-Interface Scan
- Cursor Control Function
- Programmable Cursor Format and its Blink
- Light Pen Detection Function
- Limited or Full Graphic Display Capability
- Character by Character Video Control (Color, Blink, Inverse, etc.)
- Hardware Scrolling and Paging Functions
- No DMA Required, Refresh Memory is Time-multiplexed Between CRTC and MPU
- Directly Interfaceable to MPU Bus
- Single +5V Power Supply
- Directly TTL Compatible—All Inputs and Outputs
- N Channel E/D MOS Technology
- 40 Pin DIL Package

CRTC DESCRIPTION

As shown in Figure 1, the primary function of the CRTC is to generate refresh addresses (MA0-MA13), row selects (RA0-RA4), and video monitor timing (HSYNC, VSYNC) and Display Enable. Other functions include an internal cursor register which generates a Cursor output when its contents compare to the current Refresh Address. A light-pen strobe input signal allows capture of Refresh Address in an internal light pen register.

All timing in the CRTC is derived from the Clk input. In alphanumeric terminals, this signal is the character rate. Character rate is divided down from video rate by external High Speed Timing when the video frequency is greater than 3 MHz. Shift Register, Latch, and MUX Control signals are also provided by external High Speed Timing.

The processor communicates with the CRTC through a buffered 8-bit Data Bus by reading/writing into the 18-register file of the CRTC.

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For

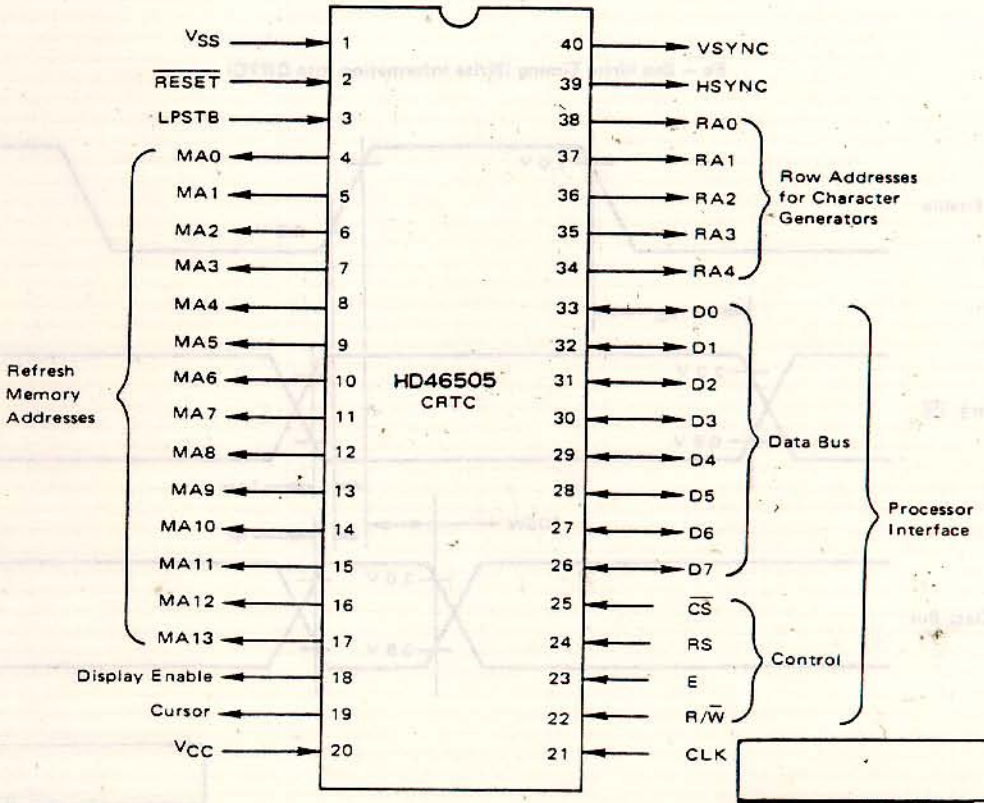

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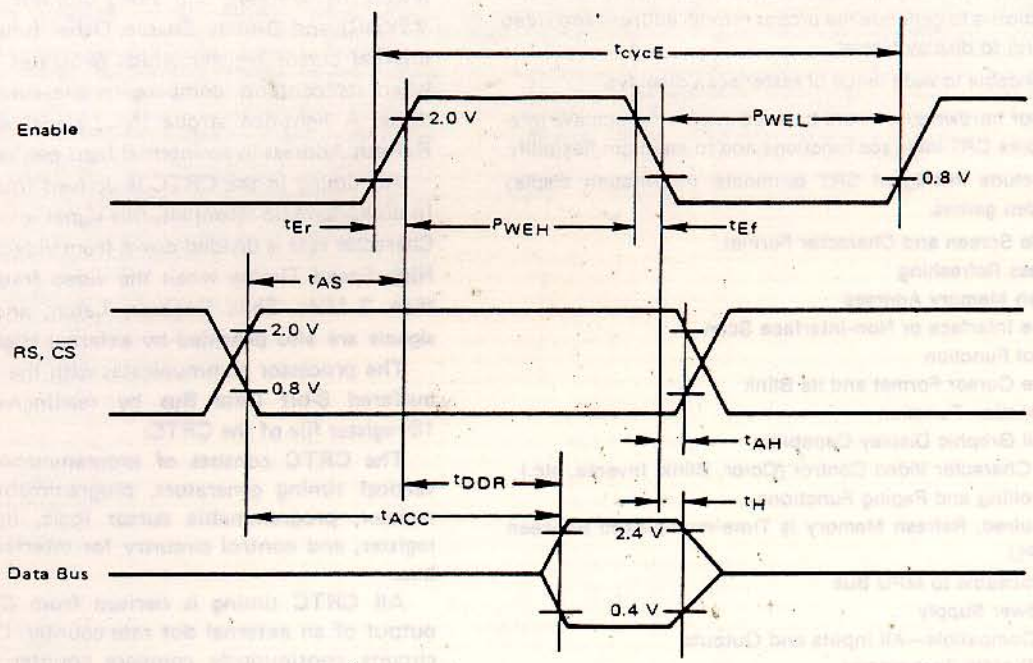
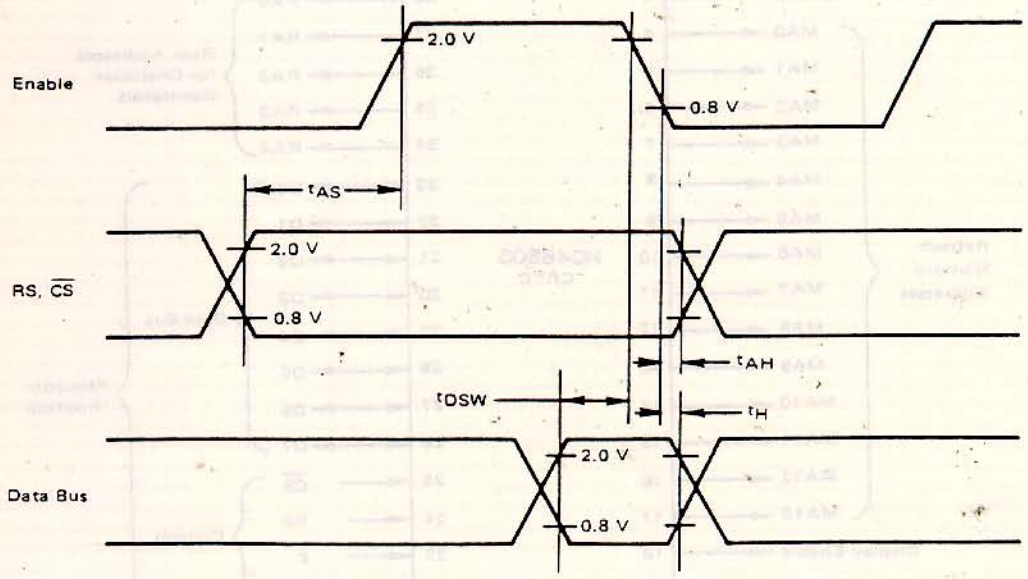
FIGURE 5 – BUS TIMING CHART

5a – Bus Read Timing (Read Information From CRTC)



5b – Bus Write Timing (Write Information Into CRTC)



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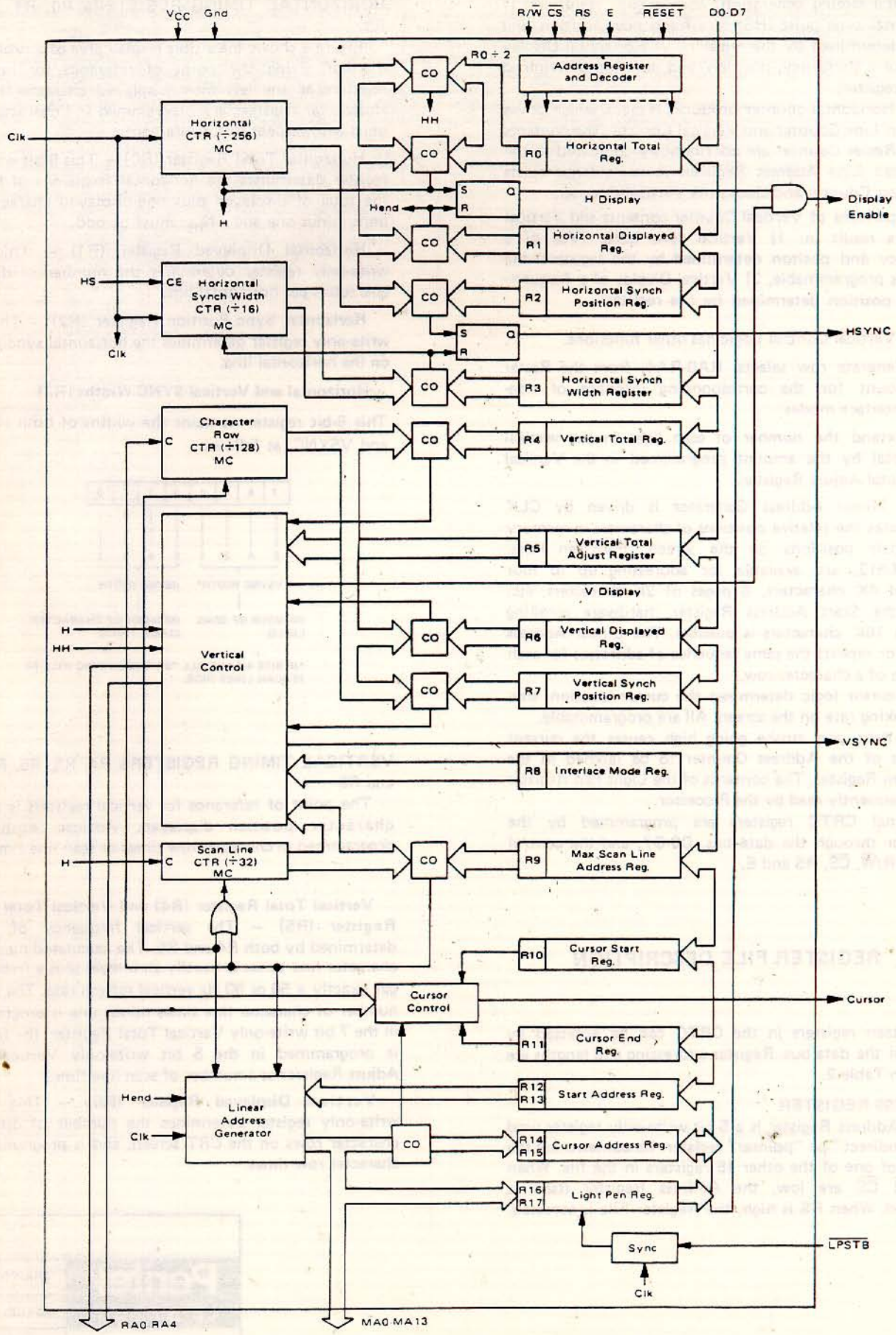


FIGURE 1 CRTC FUNCTIONAL BLOCK DIAGRAM

horizontal timing generation, comparisons result in: 1) Horizontal sync pulse (HS) of a frequency, position, and width determined by the registers, 2) Horizontal Display Signal of a frequency, position, and duration determined by the registers.

The Horizontal counter produces H clock which drives the Scan Line Counter and Vertical Control. The contents of the Raster Counter are continuously compared to the Max Scan Line Address Register. A coincidence resets the Raster Counter and clocks the Vertical Counter.

Comparisons of Vertical Counter contents and Vertical Registers result in: 1) Vertical sync pulse (VS) of a frequency and positon determined by the registers—the width is programmable, 2) Vertical Display of a frequency and position determined by the registers.

The Vertical Control Logic has other functions.

1. Generate row selects, RA0-RA4, from the Raster Count for the corresponding interlace or non-interlace modes.
2. Extend the number of scan lines in the vertical total by the amount programmed in the Vertical Total Adjust Register.

The Linear Address Generator is driven by CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA0-MA13, are available for addressing up to four pages of 4K characters, 8 pages of 2K characters, etc. Using the Start Address Register, hardware scrolling through 16K characters is possible. The Linear Address Generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blinking rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the Address Counter to be latched in the Light Pen Register. The contents of the Light Pen Register are subsequently read by the Processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals—R/$\overline{W}$, $\overline{CS}$, RS and E.

REGISTER FILE DESCRIPTION

Nineteen registers in the CRTC can be accessed by means of the data bus. Register addressing and lengths are shown in Table 2.

ADDRESS REGISTER

The Address Register is a 5 bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the Register File is accessed.

HORIZONTAL TIMING REGISTERS R0, R1, R2, and R3

Figure 9 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in "character time" units with respect to the reference.

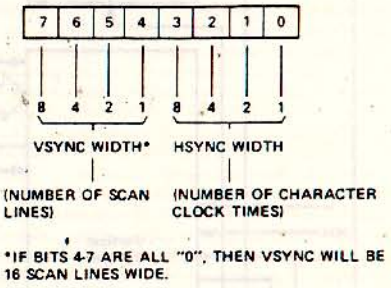
Horizontal Total Register (R0) — This 8 bit write-only register determines the horizontal frequency of HS. It is the total of displayed plus non-displayed character time units minus one and N_{ht} must be odd.

Horizontal Displayed Register (R1) — This 8 bit write-only register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2) — This 8 bit write-only register determines the horizontal sync postiion on the horizontal line.

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

VERTICAL TIMING REGISTERS R4, R5, R6, R7, R8, and R9

The point of reference for vertical registers is the top character position displayed. Vertical registers are programmed in character row times or scan line times.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) — The vertical frequency of VS is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7 bit write-only Vertical Total Register; the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6) — This 7 bit write-only register determines the number of displayed character rows on the CRT screen, and is programmed in character row times.

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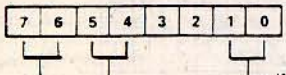
Vertical Sync Position (R7) — This 7 bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur.

Display Mode Register (R8) — This 6 bit write-only register is used to select the operating modes of the CRTC and is outlined, as follows:



INTERLACE MODE CONTROL

BIT		OPERATION
1	0	
X	0	Non-Interlace
0	1	Interlace SYNC Raster Scan
1	1	Interlace SYNC and Video Raster Scan

DISPLAY ENABLE SKEW

BIT		OPERATION
5	4	
0	0	no delay
0	1	delay Display Enable 1 character time
1	0	delay Display Enable 2 character times
1	1	— — — —

CURSOR SKEW

BIT		OPERATION
7	6	
0	0	no delay
0	1	delay Cursor 1 character time
1	0	delay Cursor 2 character times
1	1	— — — —

Maximum Scan Line Address Register (R9) — This 5 bit write-only register determines the number of scan lines per character row including spacing. The programmed value is a max address and is one less than the number of scan lines.

OTHER REGISTERS

Cursor Start Register (R10) — This 7 bit write-only register controls the cursor format (see Figure 10). Bit 5 is the blink timing control. When bit 5 is low, the blink frequency is 1/16 of the vertical field rate, and when bit 5 is high, the blink frequency is 1/32 of the vertical field rate. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower 5 bits.

Cursor End Register (R11) — This 5 bit write-only register sets the cursor end scan line.

Start Address Register (H & L) (R12, R13) — Start Address Register is a 14 bit read/write register which determines the first address put out as a refresh address after vertical blanking. It consists of an 8 bit lower register, and a 6 bit higher register.

Cursor Register (H & L) (R14, R15) — This 14 bit read/write register stores the cursor location. This register consists of an 8 bit lower and 6 bit higher register.

Light Pen Register (H & L) (R16, R17) — This 14 bit read-only register is used to store the contents of the Address Register (H & L) when the LPSTB input pulses high. This register consists of an 8 bit lower and 6 bit higher register.

LIGHT PEN

The contents of the CRTC Address Counter are strobed into R16/R17 Light Pen Registers on the next high to low CLK transition after LPSTB goes high. In most systems, the light pen signal would also cause a processor interrupt routine to read R16/R17. Slow light pen response requires the processor software to modify the captured address read from R16/R17 by a calibration factor.

PROGRAMMING CONSIDERATIONS

Initialization — Registers R0-R15 must be initialized after power is turned on. The processor normally loads the CRTC registers sequentially from a firmware table. Henceforth, R0-R11 are not changed in most systems.

Hardware Scrolling — Registers R12/R13 contents determine which memory location is the first displayed character on the screen. Since the CRTC Linear Address Generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16K block or refresh memory. By centering the R12/R13 pointer in the middle of the available memory space, scrolling up or down is possible . . . by line, page, or character.

INTERNAL REGISTER DESCRIPTION

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X
0	0	X	X	X	X	X	X	Address Reg.	Reg. No.		√	X	X	X	4	3	2	1	0
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac.		√	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		√	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		√	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines/ # Char.		√	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row		√	X	6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		√	X	X	X	4	3	2	1	0
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		√	X	6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		√	X	6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control			√	7	6	5	4	X	X	1	0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines		√	X	X	X	4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√	X	B	P	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√	X	X	X	4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Addr (H)		√	√	X	X	5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Addr (L)		√	√	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√	X	X	5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√		X	X	5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		7	6	5	4	3	2	1	0

Overall Register Structure and Addressing

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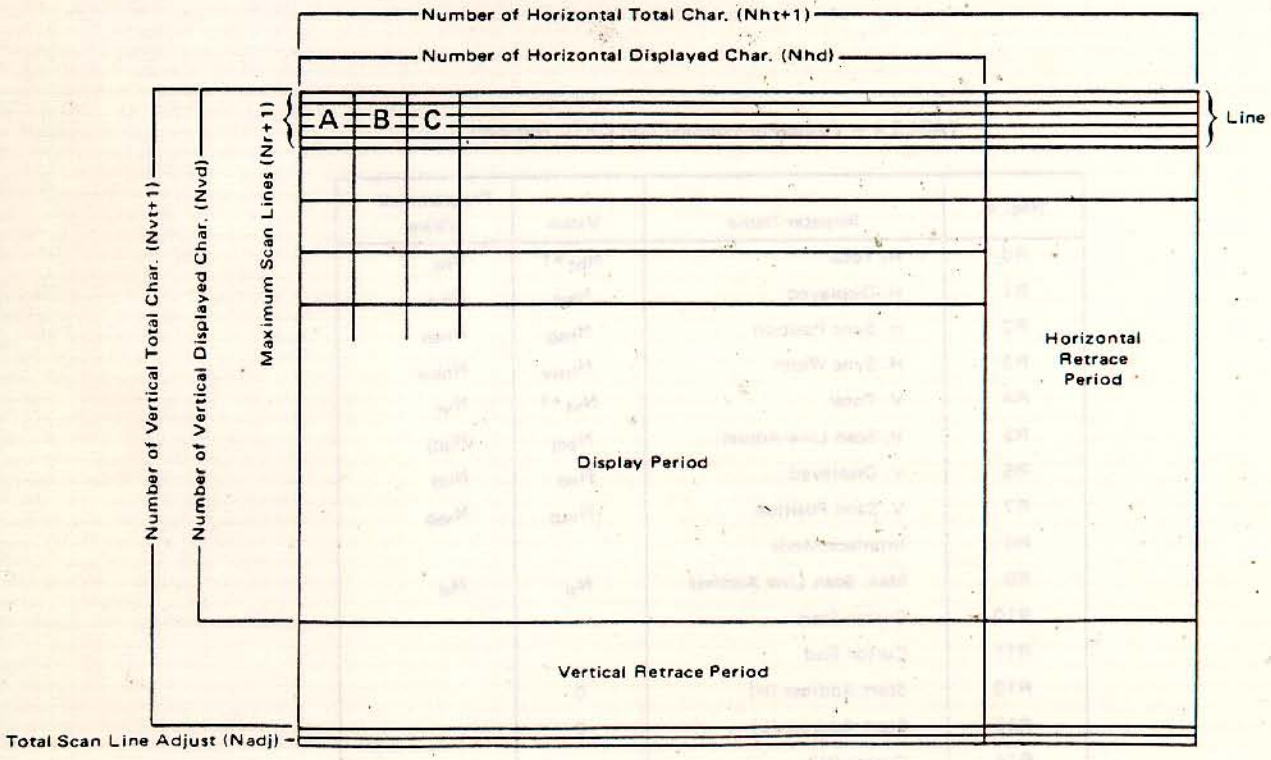
FIGURE 9 – ILLUSTRATION OF THE CRT SCREEN FORMAT



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OPERATION OF THE CRTC

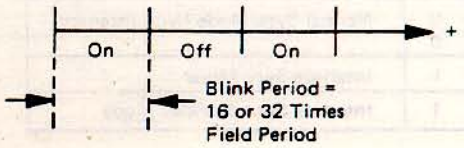
Timing Chart of the CRT Interface Signals — Timing charts of CRT interface signals are illustrated in this section with the aid of programmed example of the CRTC. When values listed in Table 4 are programmed into CRTC control registers, the device provides the outputs as shown in the Timing Diagrams (Figures 13 through 15). The screen format of this example is shown in Figure 9. Figure 16 is an illustration of the relation between Refresh Memory Address (MA0-MA13), Raster Address (RA0-RA4) and the position on the screen. In this example, the start address is assumed to be "0".

TABLE 4 — Values Programmed Into CRTC Registers

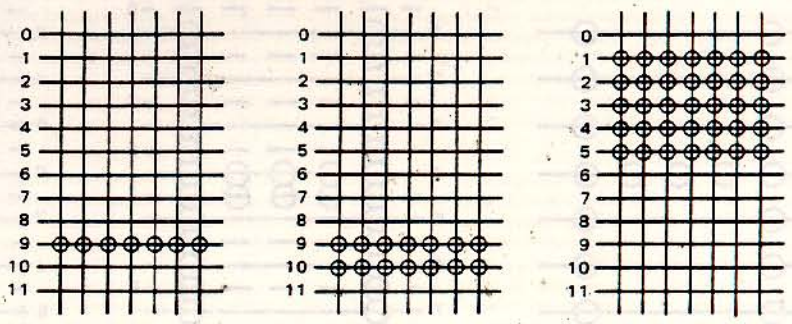
Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht}+1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt}+1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start		
R11	Cursor End		
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen (L)		

Cursor Start Register

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate



Example of Cursor Display Mode



Cursor Start Adr. = 9
Cursor End Adr. = 9

Cursor Start Adr. = 9
Cursor End Adr. = 10

Cursor Start Adr. = 1
Cursor End Adr. = 5

FIGURE 10 – CURSOR CONTROL

CURSOR

The Cursor Start and End Registers allow a cursor of up to 32 scan lines in height to be placed on any scan lines of the character block as shown in Figure 10. Using Bits 5 & 6 of the Cursor Start Register, the cursor is programmed with blink periods of 16 or 32 times the field period. Optional non-blink and non-display modes can also be selected. When an external 2X blink on characters is required, it may be necessary to perform cursor blink externally as well so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for blinking cursor and externally inverting the video signal with an exclusive-OR.

The cursor is positioned by changing the contents of registers R14 and R15. The cursor can be placed at any of 16K character positions, thus facilitating hardware paging and scrolling through memory without loss of the cursor's original position.

Interlace Mode Register

Bit 1	Bit 0	Mode
0 1	0 0	Normal Sync Mode (Non-Interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

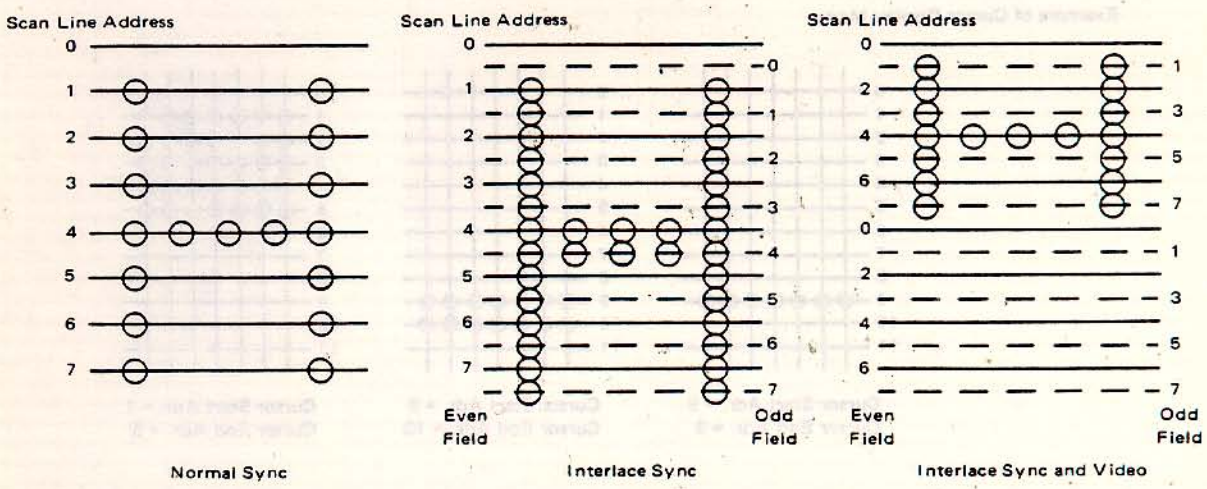
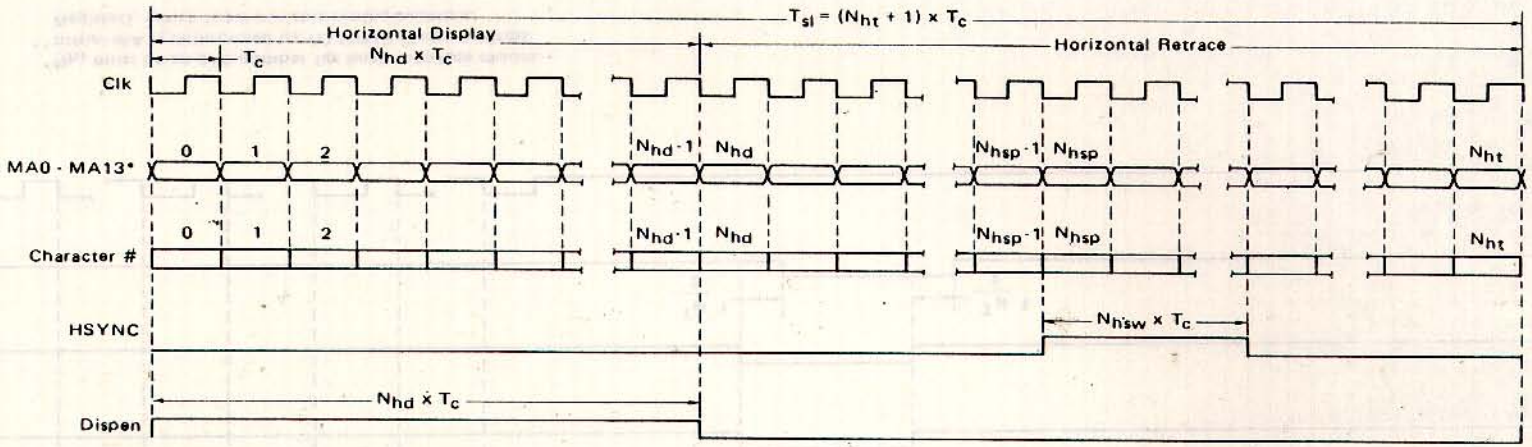


FIGURE 11 – INTERFACE CONTROL

INTERLACE/NON-INTERLACE DISPLAY MODES

An illustration of the 3 raster scan modes of operation is shown in Figure 11. Normal sync mode is non-interlace. In this mode, each scan line is refreshed at the vertical field rate (e.g., 50 or 60 Hz). Frame time is divided into even and odd alternating fields. The horizontal and vertical timing relationship results in the displacement of scan lines in the odd field with respect to the even field. When the same information is painted in both fields, the mode is called "Interlace Sync;" this is a useful mode for enhancing readability by filling in a character. When the even lines of a character are displayed in the even field and the odd lines in the odd field, the mode is called "Interlace Sync and Video." This last mode effectively doubles the character density on a monitor of a given bandwidth. The disadvantage of both interlace modes is an apparent flicker effect, which can be reduced by careful monitor design.



*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

FIGURE 13 – CRTC HORIZONTAL TIMING

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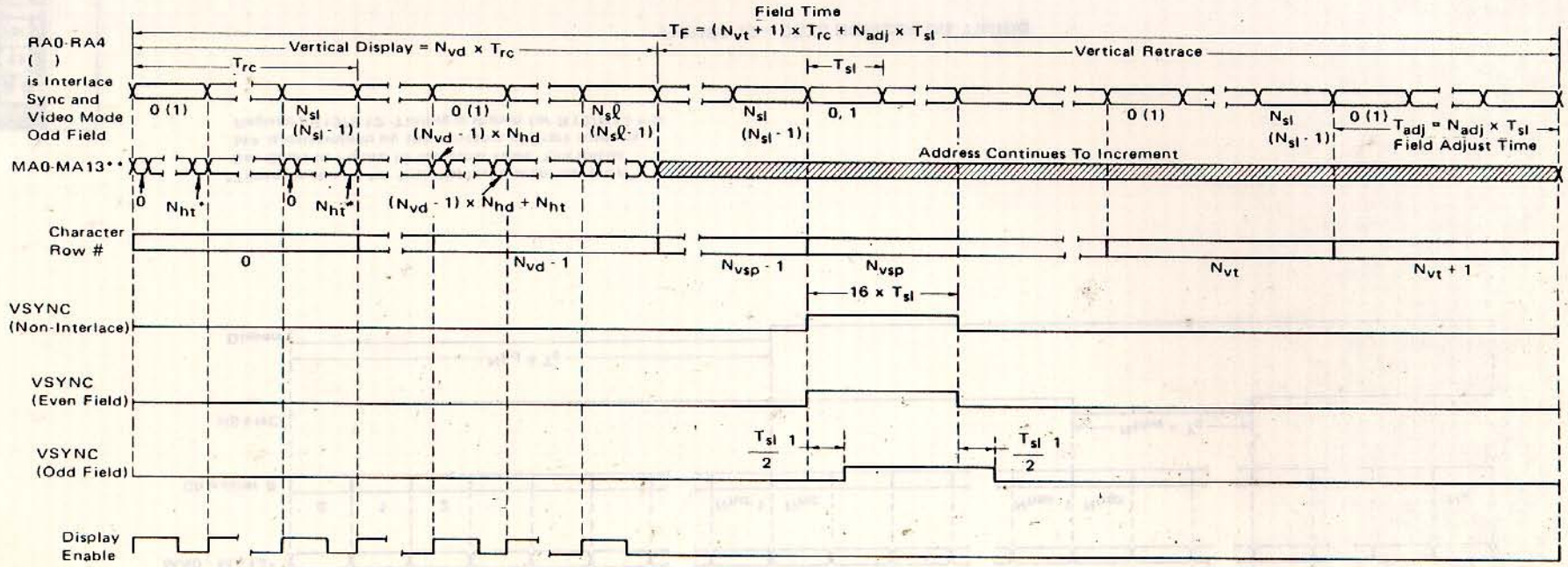

*N_{ht} must be an odd number for both interlace modes.
**Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example.

FIGURE 14 – CRTC VERTICAL TIMING

TITLE:

DRAWING NUMBER:

DATE:

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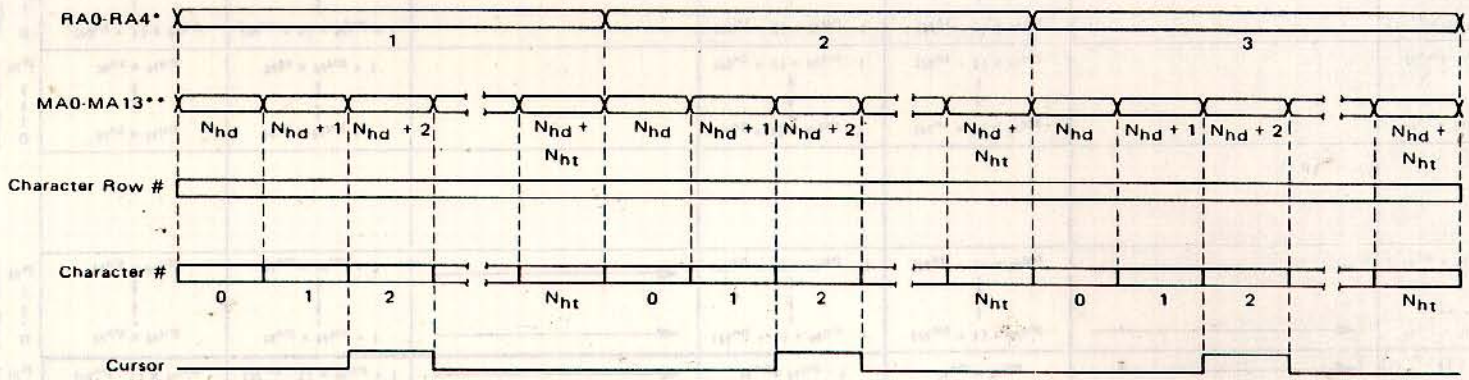

*Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:

Cursor Register = $N_{hd} + 2$
Cursor Start = 1
Cursor End = 3

** The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

FIGURE 15 – CURSOR TIMING

TITLE:

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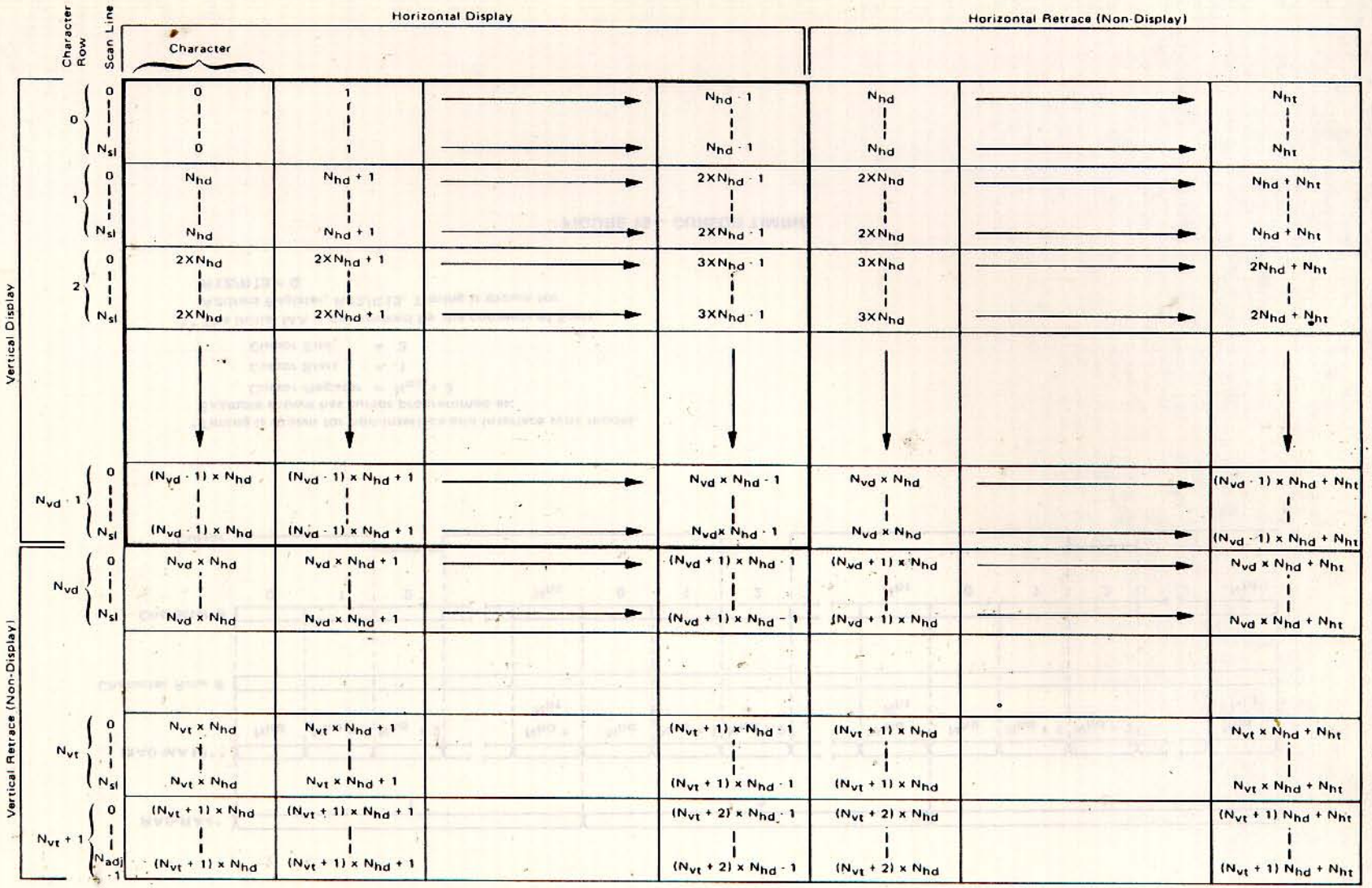

NOTE 1 The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace and Interlace Sync Modes are shown.

FIGURE 16 – REFRESH MEMORY ADDRESSING (MA0-MA13) STATE CHART

TITLE:

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DATE:

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SCALE:

DRAWN BY:

PCMSP

PARALLEL CHARACTER MEMORY SUBROUTINE PACKAGE

for the

VRG-Q Parallel Character Memory

by

PERITEK CORPORATION
5550 Redwood Road
Oakland, CA 94619
(415) 531-6500

Version 1.0 (RT)
Date: 28-MAY-82

TABLE OF CONTENTS

Chapter I
INTRODUCTION

I.1 PCMSP FEATURES

PCMSP is a set of subroutines which provides basic character functions on the VRG-Q's parallel character memory. PCMSP is provided in object file format for linking with the user's main program and is optionally available in source format.

PCMSP is coded in assembly language for maximum speed and minimum size. It requires approximately 520 words of storage.

PCMSP works entirely in the line/column coordinate system, with line numbers from 0 to 31 and column numbers from 0 to 63. Line 0, column 0 is in the upper left hand corner of the screen.

The functions provided by PCMSP include:

Position the character pointer (CP) to a location on the screen given in absolute coordinates or in coordinates relative to the previous location of the CP.

Display a visible cursor at the location of the CP.

Clear character memory or portions of it.

Select one of multiple VRG's.

Draw individual characters or strings of characters in the character memory, in either normal or reverse video modes.

Read current coordinates of CP.

Read an individual character value and its video mode.

Read an entire character line of VRG-Q parallel character memory.

PCMSP does not access the graphics memory. It uses only the parallel character memory. Characters displayed by PCMSP are determined by the EPROM character generator on the VRG-Q.

I.2 HARDWARE ENVIRONMENT

PCMSP is set up to work with a VRG-Q, with the parallel character memory option, at the standard addresses (see VRG-Q User's Manual). The standard initialization program (VRGINT) must be executed before PCMSP is used.

PCMSP will work with the VRG-Q on any LSI-11/2 or LSI-11/23 processor. The instruction set options (EIS,FIS,FPU) are not used. PCMSP can also be used with a VRG-Q connected to a Unibus PDP-11 processor through a bus converter. The processor must have the SOB and XOR instructions, so older PDP-11's (05,10,15,20) will not work.

I.3 SOFTWARE ENVIRONMENT

PCMSP is provided in object file format compatible with the RT-11 operating system. It is available as a MACRO-11 source file which is compatible with both RT-11 and RSX-11M.

PCMSP supports three different calling sequences. The sequences supported are:

1. FORTRAN IV / FORTRAN IV-Plus
2. BASIC-11
3. WHITESMITH'S C

Separate object file modules are supplied for each of these sequences.

PCMSP is compatible with major PDP-11/LSI-11 operating systems such as RT-11 (SJ,FB,XM), TSX-Plus, RSX-11S, and RSX-11M. Operating systems using memory management must allow the user to map to the I/O page, so PCMSP can access the VRG-Q.

I.4 NOMENCLATURE

The following terms have special meanings which the reader should be familiar with:

character cursor - A blinking or nonblinking solid box (user determined) or dashed line, which indicates the current location of the character pointer.

character pointer - Pointer into the character memory which indicates the starting point of a string, the base point for relative addressing, etc.

CP - Character Pointer

CRT controller address register - Address register on the CRT controller chip which is used to access the CRT controller data register lookup table.

CRT controller data register - Data register on the CRT controller chip, containing various parameters which are needed internally by the CRT controller chip.

reverse video - A mode on the graphics display in which black characters are output on a white field rather than the normal white character output on a black field.

VIURAM base address - The starting memory address for the graphics display.

VIURAM control register - The VRG-Q device register containing bit flags for screen blank, direct memory access, reverse video, line select, selection of character or graphics memory, etc.

I.5 RELATED SOFTWARE

GSP-1 and GSP-2 are subroutine packages which provide additional functions for the high level language programmer using the VRG-Q.

GSP-1 is a set of subroutines which provide basic functions on the VRG-Q using graphics memory. GSP-1 provides subroutines to plot vectors and points, to move the graphics pointer, to clear graphics memory, change the graphics cursor, set bits in

the VIURAM control register, plot characters on graphics memory, and read back values from data in graphics memory into buffers.

GSP-2 is a set of subroutines which provide basic and advanced functions on the VRG-Q using the graphics memory. GSP-2 contains all the functions of GSP-1 plus several additional capabilities. GSP-2 provides the user with the ability to generate circles, arcs, and polygons; to fill circles and rectangles with fill patterns to perform fast line scans and fills using fill patterns; to plot vectors with patterned lines; to magnify, independently in the X and Y directions, characters plotted on graphics memory; and to convert binary image data from graphics memory to Printronix format.

Chapter II
DISTRIBUTION KIT

II.1 MEDIA

PCMSP is distributed on RX01 compatible single density, single sided diskettes. RT-11 file format is used.

II.2 OBJECT CODE FILES

PCMSP is provided as object files for the three different subroutine calling sequences which are supported.

FILE	LANGUAGE COMPATABILITY
PCMSPF.OBJ	FORTRAN IV, FORTRAN IV-Plus
PCMSPB.OBJ	BASIC-11 (BSUBS.OBJ and BSCLI.MAC also provided)
PCMSPC.OBJ	Whitesmith's C

II.3 SOURCE CODE FILES

PCMSP source consists of three header files used to select the desired calling sequence, a header file which defines the VRG-Q register addresses, a file containing required macros, and a code file:

FILE	CONTENTS
VRGCND.MAC	VRG-Q definitions
FSEL.MAC	Header for FORTRAN calling sequence
CSEL.MAC	Header for C calling sequence
BSEL.MAC	Header for BASIC calling sequence
GSPMAC.MAC	Macro definitions for PCMSP
PCMSP.MAC	Code
BSUBS.MAC	Auxillary functions for BASIC-11 calling sequences
BSCLI.MAC	Link table for BASIC-11 interpreter

The RT-11 monitor commands used to create the object files from these sources are as follows:

```
MACRO/OBJ:PCMSPF    GSPMAC+VRGCND+FSEL+PCMSP

MACRO/OBJ:PCMSPC    GSPMAC+VRGCND+CSEL+PCMSP

MACRO/OBJ:PCMSPB    GSPMAC+VRGCND+BSEL+PCMSP

MACRO/OBJ:BSUBS     BSUBS

MACRO/OBJ:BSCLI     BSMAC+BSASM+BSCLI
```

Note that the VRGCND file should be modified if non-standard VRG-Q addresses are used.

Chapter III
INSTALLATION

III.1 LINKING PROCEDURES

The object file to be used should be copied to the user's 'DK:' device. Then the following command can be used to link PCMSP with a FORTRAN program named 'MAIN':

```
LINK   MAIN,PCMSPF
```

As an alternative, the object module PCMSPF can be merged into SYSLIB or another user library so it does not have to be explicitly named at link time.

Similar procedures can be followed for using PCMSP with the C language.

III.2 PATCHES

Certain key parameters in PCMSP are identified by global symbols so they can be easily located for patching. The symbols show up in the link map in the GSP PSECT. They are:

SYMBOL	DEFAULT VALUE	MEANING
CRSTRT	174000	VIURAM base address
VCCSRE	174140	VIURAM control register
CARLP	174144	CRT controller chip address register
CCBUF	174146	CRT controller chip data register

III.3 BASIC-11 INSTALLATION

A special version of BASIC must be generated to make use of the PCMSP. Generating a special version of BASIC is a simple process. It is well described in Chapter 4 of the "Basic-11 Installation Guide." The reader should familiarize himself with that chapter, paying special attention to the section on use of assembly language routines with BASIC.

The following steps must be taken to generate a special version of BASIC:

1. Edit the file BSCLI.MAC which is part of the PCMSP distribution kit. There are three parameters at the bottom of the first page of the file. They are:

   ```
   GSP1  = 0
   PCMSP = 0
   GSP2  = 0
   ```

   These parameters enable the linkage between BASIC-11 and the corresponding VRG software module. To include PCMSP linkage, change the line

   ```
   PCMSP = 0
   ```

   to read

   ```
   PCMSP = 1
   ```

   Do the same for GSP1 or GSP2 if either of those modules is to be included.

2. Assemble BSCLI with the two modules BSMAC and BSASM which are part of the BASIC-11 package. Use the following command:

   ```
   MACRO/OBJ:BSCLI   BSMAC+BSASM+BSCLI
   ```

3. Make sure that the object module just generated and the two object modules from the PCMSP distribution kit (BSUBS.OBJ and PCMSPB.OBJ) are on the device to be used for generating BASIC, which will also include the BASIC-11 distribution kit.

4. Follow the procedures for generating a new version of BASIC given in Chapter 4 of the Installation Guide. Be sure to include CALL support. The following modules must be included:

BSCLI,BSUBS,PCMSPB,BSCLLB.

Include GSP1 or GSP2 if either one is desired.

Chapter IV
PROGRAMMING

IV.1 INTRODUCTION

PCMSP consists of several routines which allow the high level language programmer to access the VRG-Q graphics board's parallel character memory without having to worry about either the hardware or the way the software accesses the hardware. This chapter describes the software interface to the PCMSP subroutines.

IV.2 PARAMETERS

All coordinate data passed to PCMSP refers to absolute screen locations in the range 0 - 31 in the vertical and 0 - 63 in the horizontal directions. Coordinates outside the range are clamped to the nearest valid value.

IV.2a Parameters in FORTRAN and C

PCMSP routines in FORTRAN and C do not use any floating point (real) values. All data passed from the main program to or from PCMSP is either integer or character data. Integer arrays and character strings are also used.

In all cases, the variables given are the following types:

```
(FORTRAN)                       (C)
INTEGER L,IC,DL,DIC,V,N,C       int l,ic,dl,dic,v,n,c;
INTEGER CARLP,CCBUF,CRSTRT      int carlp,ccbuf,crstrt;
INTEGER BUF(33),VCCSRE          int buf[33],vccsre;
DIMENSION STR(-)                char *str;
```

(STR is a character (byte) array in FORTRAN)
(STR and str must be null terminated ASCII strings)

IV.2b Parameters in BASIC

PCMSP routines use only integers and strings internally. However, for the convenience of the user, PCMSP will automatically convert scalar numeric parameters as required. Single and double precision floating point parameters may be used, as well as integers and nulls. If a null parameter is given as an input to PCMSP, its value is taken to be zero. Null parameters for returned values are properly handled, with no value being returned.

The following calls are all acceptable:

```
CMOVE(1%,1%)
CMOVE(L,C)
CMOVE(A%,C)
CMOVE(,)
```

Floating point values are truncated, of course.

Only scalar parameters may be used with PCMSP. No arrays are allowed.

IV.3 SUBROUTINES

There are five groups of subroutines which are included in this software package. The subroutines (showing the FORTRAN calling sequence) are listed below:

a) CHARACTER POINTER MOVEMENT
- CMOVE(L,IC)
- CMOVRL(DL,DIC)
- CPHOME
- CPLFT
- CPLR(N)
- CPUD(N)

b) CHARACTER I/O
- PCOUT(C,V)
- PCDSPL(STR,V)

c) CONTROL
- CCRS(N,L)
- CVRGSL(CRSTRT,VCCSRE)

d) READBACK
- PCRD(L,IC)
- CHRVAL(C,V)
- CRDLN(L,BUF)

e) SCREEN
- PCLCLR(V)
- PCSCLR(V)
- PCBLNK(V)
- PCSCRL(N,V)

IV.3a Character Pointer (CP) Movement Functions

This section contains routines which move the CP around on the screen.

FORTRAN: CALL CMOVE (L,IC)
BASIC: CMOVE (L,IC)
C: cmove (l,ic)

Move the CP to line L, column IC.

FORTRAN: CALL CMOVRL (DL,DIC)
BASIC: CMOVRL (DL,DIC)
C: cmovrl (dl,dic)

Move the CP to line (old-L+DL), column (old-IC+DIC).

FORTRAN: CALL CPHOME
BASIC: CPHOME
C: cphome ()

Move the CP to line 0, column 0.

FORTRAN: CALL CPLFT
BASIC: CPLFT
C: cplft ()

Move the CP to column 0 on the current line.

FORTRAN: CALL CPLR (N)
BASIC: CPLR (N)
C: cplr (n)

Move the CP right N columns. If N is negative, move the CP left -N columns.

FORTRAN: CALL CPUD (N)
BASIC: CPUD (N)
C: cpud (n)

Move the CP down N lines. If N is negative, move the CP up -N lines.

IV.3b Character I/O Functions

The routine in this section display characters in the character memory at the location of the CP. They advance the CP when finished.

The second argument, V, enables the user to decide whether normal or reverse video is desired. It can have any of four

values as described below:

V	MODE
0	Normal video
1	Reverse video
2	Video mode remains unchanged

FORTRAN: CALL PCOUT (C,V)
BASIC: PCOUT (C,V)
C: pcout (c,v)

Display character with ASCII value C at the location of the CP and then advance the CP.

FORTRAN: CALL PCDSPL (STR,V)
BASIC: PCDSPL (A$,V)
C: pcdspl (str,v)

Display the null terminated string of ASCII characters, STR, at the location of the CP and advance the CP to the next character position after the string. If the string goes to the right margin on the screen, the CP is left at the right margin.

IV.3c Control Functions

The routines in this section affect various internal flags and registers. They do not affect the CP.

FORTRAN: CALL CCRS (N,L)
BASIC: CCRS (N,L)
C: ccrs (n,l)

Set character cursor pattern to N as shown below:

N = 0	CURSOR OFF
N = 1	NON-BLINKING CURSOR ON
N = 2	SLOW BLINKING CURSOR ON
N = 3	FAST BLINKING CURSOR ON

L corresponds to the number of raster lines in the cursor. It always starts at the bottom raster line of the character

block, and can range in size from 1 to 16 lines (L = 0 and L = 15 respectively).

If an argument is negative, the value for that variable remains unchanged.

FORTRAN: CALL CVRGSL (CRSTRT,VCCSRE)
BASIC: CVRGSL (CRSTRT,VCCSRE)
C: cvrgsl (crstrt,vccsre)

This subroutine is used in systems with multiple VIURAMs which are being operated by the same main program. It selects, for use by the other PCMSP routines, the VRG-Q with data register base address (CRSTRT) and control register address (VCCSRE). All subsequent PCMSP functions will be executed on this VRG-Q. If the VIURAM's have data registers at the same address, be sure to disable the character and graphics memories on the old unit before selecting the new unit. If any argument is zero, the old value for that variable is not changed.

The VIURAM data register base address corresponds to the global variable CRSTRT.

The VIURAM control register corresponds to the global variable VCCSRE.

This subroutine also modifies the CRT controller chip address register (global variable CARLP) and the CRT controller chip data register (global variable CCBUF) when VCCSRE is changed.

IV.3d Character Readback Functions

The routines in this section do not alter the display, but, instead, return information to the calling routine. No routines affect the CP.

```
FORTRAN:  CALL PCRD (L,IC)
BASIC:    PCRD (L,IC)
C:        pcrd (&l,&ic)
```

Returns the current line number of the CP in L, and the current column number of the CP in IC.

```
FORTRAN:  CALL CHRVAL (C,V)
BASIC:    CHRVAL (C,V)
C:        chrval (&c,&v)
```

Returns the 7-bit ASCII value of the character at the CP in C and whether or not it is reverse video in V. If the character is in reverse video, a 1 is returned, otherwise, a 0 is returned.

```
FORTRAN:  CALL CRDLN (L,BUF)
BASIC:    CRDLN (L,A$)
C:        crdln (l,&buf)
```

Return the binary value of the characters on line L in the area defined by BUF. BUF must be at least 65 bytes in size. Illegal values of L (less than zero or greater than 31 (decimal)) are ignored, and BUF remains unchanged. The CP remains in the old location. BUF is null terminated in C and FORTRAN.

IV.3e Screen Functions

The routines in this section are used to modify a large section the screen. They do not affect the CP.

The functions PCLCLR, PCSCLR, and PCBLNK all take an argument, describing how blanking should be done as far as normal / reverse video mode is concerned.

V	MODE (blank all character spaces and)
0	Normal blanking (make all spaces normal video)
1	Reverse blanking (make all spaces reverse video)
2	Blanking (leave video bits as are)

```
FORTRAN:  CALL PCLCLR (V)
BASIC:    PCLCLR (V)
C:        pclclr (v)
```

Clear the character line which the CP is on from the CP to the end of the line.

```
FORTRAN:  CALL PCSCLR (V)
BASIC:    PCSCLR (V)
C:        pcsclr (v)
```

Clear the character memory from the CP to the bottom of the page.

```
FORTRAN:  CALL PCBLNK (V)
BASIC:    PCBLNK (V)
C:        pcblnk (v)
```

Clear the entire character memory.

```
FORTRAN:  CALL PCSCRL (N,V)
BASIC:    PCSCRL (N,V)
C:        pcscrl (n,v)
```

Scroll the character memory abs(N) lines. If N is positive, scroll up, if N is negative, scroll down. Vacated lines are blanked.

Fill the new lines as follows:

V	FILL MODE
0	Normal video
1	Reverse video

IV.4 CHARACTER CURSOR

The character cursor is a box of a variable number of raster lines (initially 16) of 8 pixels width which can be turned off or on by the programmer calling the CCRS function. If turned on in non-blinking mode, the cursor appears as the complement of what is currently in the character memory at the location of the CP. If the cursor blinks, it is either showing the actual character (and video mode) at the CP, or its complement (it alternates between the two). Use of this routine also allows the programmer to select the type of cursor desired, be it a box, underline, overscore, etc.

IV.5 RETURN VALUES

There are no routines which return function values. In languages such as C which expect functions to return a value, the value is unspecified.

IV.6 ERROR MESSAGES

The PCMSP does not generate any error messages or error returns in C and FORTRAN. In BASIC, the following error messages may occur:

```
STK OFLOW IN VG S/W
ARGUMENT ERROR
STRING ERROR IN VG S/W
```