MMS1132

ADD-IN MEMORY
ARRAY BOARD

Motorola, Inc.

MOTOROLA INC.

MMS1132(0)
68ASD13330W
ADDENDUM #2

MMS1132

ADD-IN MEMORY ARRAY BOARD

The following changes and corrections should be made to the manual.

1) On page 2-6, the paragraph should read:

   There are three types of jumpers on the MMS1132 array board. Jumpers E1 and E2 are zero ohm resistors which are soldered onto the board in the factory. Jumpers E3 through E31 are normally "mini-jump" shorting plugs; however, the wafer posts could be wire wrapped instead. The last jumper is a staple jumper used for systems without memory management (see item k in section 2.3.2).

2) On page 2-17, add the following entry to section 2.3.2:

   k) Q-Bus Compatible Staple Jumper

      This jumper is used to disable address lines BDAL 18 through BDAL 21. To select this option remove the 7485 comparator chip located at U38 and insert the gold staple jumper from pin 6 to pin 11. In addition, make sure mini jumper E4 is removed.

MOTOROLA INC.

MMS1132(0)
68ASD13330W
ADDENDUM #1

MMS1132

ADD-IN MEMORY ARRAY BOARD

The following information is included to supplement the jumper installation of the MMS1132 manual. All MMS1132 memory array boards are shipped with various jumpers installed according to the following table.

TABLE A. JUMPER IDENTIFICATION

Board Version	Battery Back-up	RAM Type	Memory Size (Words)	Parity	BBS7	Refresh
N3032	E2	MCM66331L20: E8,E11	28K: E21,E22,E24,E25	E27	E28	E30
P3032	E2	MCM66331L20: E8,E11	28K: E21,E22,E24,E25	E26	E28	E30
N3064	E2	MCM6665L20: E7,E9	64K: E20,E21,E22,E23,E24,E25	E27	E28	E30
P3064	E2	MCM6665L20: E7,E9	64K: E20,E21,E22,E23,E24,E25	E26	E28	E30
N3065	E2	MCM66331L20: E8,E11	64K: E20,E21,E22,E23,E24,E25	E27	E28	E30
P3065	E2	MCM66331L20: E8,E11	64K: E20,E21,E22,E23,E24,E25	E26	E28	E30
N3128	E2	MCM6665L20: E7,E9	124K: E19,E20,E21,E22,E24,E25	E27	E28	E30
P3128	E2	MCM6665L20: E7,E9	124K: E19,E20,E21,E22,E24,E25	E26	E28	E30

MMS1132(O)
68ASD13330W

MMS1132

ADD-IN MEMORY ARRAY BOARD

USER'S MANUAL

First Edition

Printed in U.S.A.

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SPECIFICATIONS

Storage Capacity:	128K Words
Word Length:	16 Bits
Read Access Time:	225 nanoseconds (Nom)
Write Access Time:	175 nanoseconds (Nom)
Read Cycle Time:	525 nanoseconds (Nom)
Write Cycle Time:	525 nanoseconds (Nom)
Refresh Latency Time:	525 nanoseconds (Max)
Mode(s) of Operation:	Write (Word or Byte) Read Read/Modify/Write Refresh
Input/Output:	120 ohm Terminated Bus
Temperature:	0°C to 50°C (Operating) -40°C to 80°C (Non-operating)
Relative Humidity:	5 to 90% without condensation
Input Power:	+5 Vdc at 2.48A max, 1.2A typ (32K) +5 Vdc at 2.62A max, 1.23A typ (64K/128K)
Dimensions:	8.43 in (214.12 mm) wide by 5.19 in (131.75 mm) high by 0.056 in (1.42 mm) thick. Requires 0.5 in (12.7 mm) width connector slot.

Effective Capacity is Switch Selectable at any 1K Word Increment

Addressing is Switch Selectable to Start on Any 1K Word Boundary From 0 to 127K

Refresh Implemented Internal to the Board (Transparent to the System). On-Board Jumpers Permit Synchronization of Refresh if Desired.

Jumper Selectable Battery Backup Provisions Allow Use of Separate Power Source

Optional Parity and On-board Parity Controller

LSI-11 (Q-Bus and Q-Bus Plus)* Interface Compatible

* Trademarks of Digital Equipment Corporation

CHAPTER 1

GENERAL INFORMATION

1.1 DESCRIPTION

The MMS1132 is a high density add-in memory array board. The array board is intended for use in Digital Equipment Corporation's LSI-11*, LSI-11/2*, and LSI-11/23* processors as well as PDP-11V03* computer systems.

The MMS1132 utilizes 32K or 64K x 1 RAM devices and provides up to 128K words by 18 bits of memory storage on a single dual height module. The array also provides for battery back-up of stored data.

The power and signal pin-outs are compatible with any LSI-11 "Q" Bus Plus* board slot. The MMS1132 presents one standard bus load to the LSI-11 "Q" Bus Plus* independent of options or jumper selections.

The MMS1132 memory array board is implemented on one standard "Dual-height" printed circuit board. It requires only one single (1/2 inch) width connector slot.

* LSI, PDP, and "Q" Bus Plus are trademarks of Digital Equipment Corporation.

1.2 MODELS

The MMS1132 memory array board is produced in 8 variations. Table 1-1 lists the model designations, the memory capacity, the type of dynamic RAM used, number of memory devices used, and parity option.

TABLE 1-1. MODEL DESIGNATIONS

Device Number	Capacity In 16 Bit Word	Parity	Number of RAMS	RAM Type
MMS1132	Basic Assembly			
MMS1132N3032	32K	No	16	32K x 1
MMS1132P3032	32K	Yes	18	32K x 1
MMS1132N3064	64K	No	16	64K x 1
MMS1132P3064	64K	Yes	18	64K x 1
MMS1132N3065	64K	No	32	32K x 1
MMS1132P3065	64K	Yes	36	32K x 1
MMS1132N3128	128K	No	32	64K x 1
MMS1132P3128	128K	Yes	36	64K x 1

K = 1024, 1 word = 16 bits (2 bytes)

1.3 DC POWER REQUIREMENTS

Table 1-2 shows the power requirements for the single voltage supply required.

TABLE 1-2. POWER REQUIREMENTS

Model (MMS1132-)	Battery Back-Up (1)		Standby (2)		Active (3)		Unit (dc)
	Typ	Max	Typ	Max	Typ	Max	
N3032	430	825	920	1750	1040	2160	mA
P3032	435	840	1065	2025	1195	2480	mA
N3064	475	940	960	1750	1080	2160	mA
P3064	500	975	1100	2025	1230	2480	mA
N3065	430	825	920	1870	1040	2280	mA
P3065	435	840	1065	2160	1195	2620	mA
N3128	475	940	960	1870	1080	2280	mA
P3128	500	975	1100	2160	1230	2620	mA

NOTES:

(1) Battery back-up indicates +5 VBBU supplied through edge pin AV1 only and the board configured for battery back-up operation.

(2) Standby indicates power applied but no accesses taking place.

(3) Active indicates power applied and accesses occurring at the maximum allowed frequency.

CHAPTER 2

INSTALLATION

2.1 PRE-INSTALLATION

Prior to installation, check the following:

a) Adequate power supply for all units.

b) Prior placement for individual units.

c) Adequate equipment for checkout.

1) Multimeter

2) Oscilloscope

2.2 PREPARATION FOR USE

2.2.1 Handling

> CAUTION
>
> Turn power off before removing or installing a part or board.
>
> SPECIAL HANDLING REQUIRED
>
> Store board in special conductive bag. Do not touch circuitry while handling. Static discharge may damage components. If shipment of board is necessary, pack board in conductive (non-static) plastic bag and place in original carton for protection.

The circuit board must be kept in a unit or in a conductive plastic bag and transferred without touching the circuitry. Generally, it is required that the unit, the board, and installing or repairing personnel all be at the same (ground) potential. An installed and connected unit will have its case at ground potential and board changing may be accomplished. If the unit is on a bench or is not installed, a common ground

connection between installing and/or repairing personnel and the unit should be made.

In handling of unmounted chips, care should be taken to avoid differences in voltage potential. A conductive carrier, or a carrier having a conductive overlay should be used.

2.2.2 Precautions

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to high static electrical charges.

To avoid possible damage to the devices during handling, testing, or actual operation, use the following procedures:

a) The leads of devices should be in contact with a conductive material, except when being tested or in actual operation, to avoid build-up of static charge.

b) Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.

c) Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.

d) Signals should not be applied to the inputs while the device power supply is off.

2.3 MOUNTING

2.3.1 Pin Assigmments

Edge connector pin identification is shown in Figure 2-1 and pin assignments are listed in Table 2-1. The MMS1132 utilizes gold plated edge connectors. The identification system is based on the LSI-11 bus. The LSI-11 bus is based on the use of a dual-height board that plugs into a 2-slot bus connector. Each slot contains 36 pins (18 on the component side and 18 on the solder side).

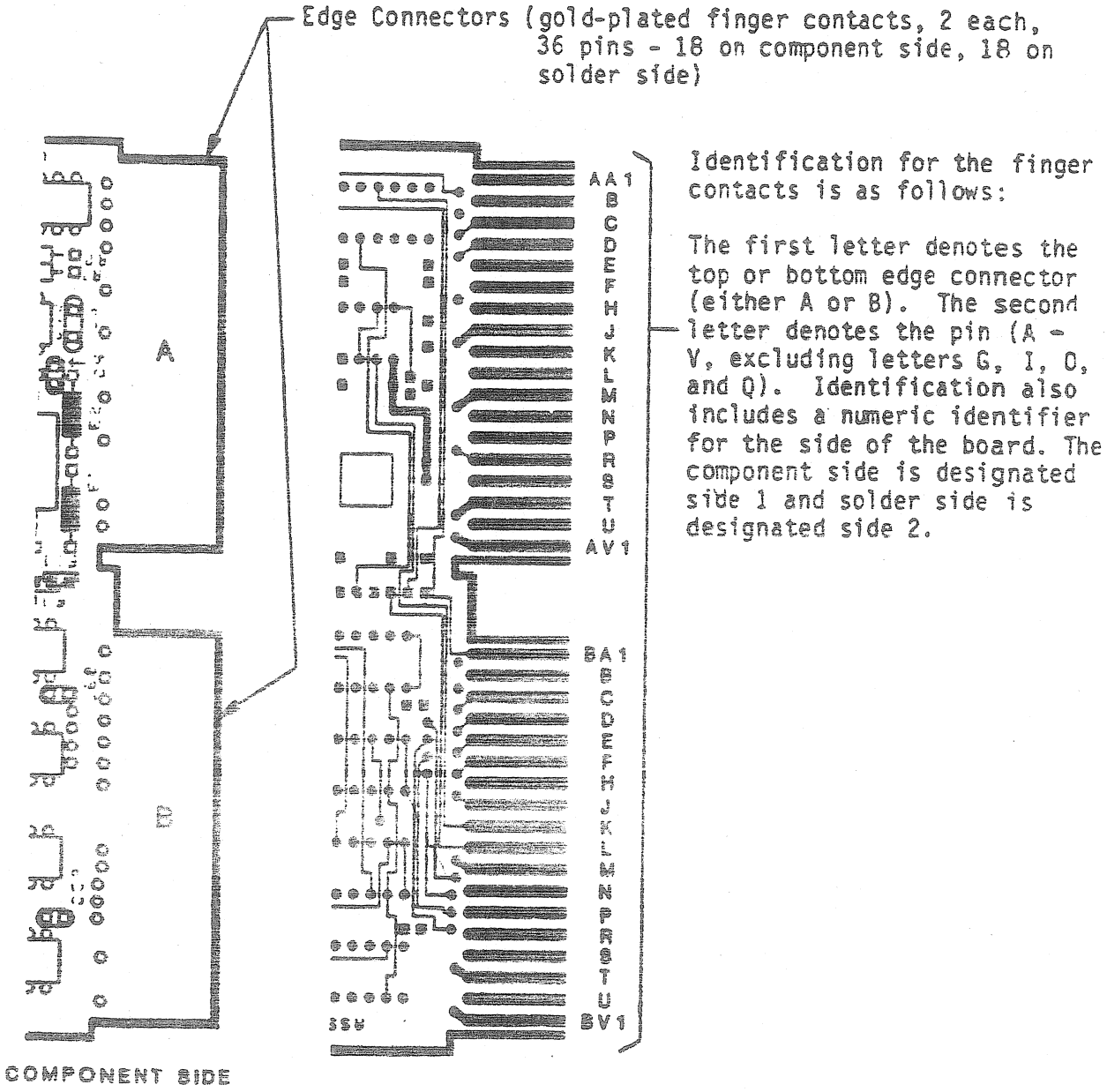


FIGURE 2-1. EDGE CONNECTOR IDENTIFICATION

TABLE 2-1. BUS PIN ASSIGNMENTS

Connector A			
Component Side (1)		Solder Side (2)	
Pin	Signal	Pin	Signal
AA1	---	AA2	+5 V
AB1	---	AB2	---
AC1	BDAL16 L	AC2	GND
AD1	BDAL17 L	AD2	---
AE1	---	AE2	BDOUT L
AF1	---	AF2	BRPLY L
AH1	---	AH2	BDIN L
AJ1	GND	AJ2	BSYNC L
AK1	---	AK2	BWTBT L
AL1	---	AL2	---
AM1	GND	AM2	Hard Wired on Memory Board
AN1	---	AN2	
AP1	---	AP2	BBS7 L
AR1	BREF L	AR2	Hard Wired on Memory Board
AS1	---	AS2	
AT1	GND	AT2	---
AU1	---	AU2	BDALØØ L
AV1	+5 VBBU	AV2	BDALØ1 L

Signals left blank (---) are not connected.

TABLE 2-1. BUS PIN ASSIGNMENTS (cont'd)

Connector B			
Component Side (1)		Solder Side (2)	
Pin	Signal	Pin	Signal
BA1	BDCOK H	BA2	+5 V
BB1	---	BB2	---
BC1	MMUDAL18 L	BC2	GND
BD1	MMUDAL19 L	BD2	---
BE1	MMUDAL20 L	BE2	BDALØ2 L
BF1	MMUDAL21 L	BF2	BDALØ3 L
BH1	---	BH2	BDALØ4 L
BJ1	GND	BJ2	BDALØ5 L
BK1	INT REF**	BK2	BDALØ6 L
BL1	EXT REF IN**	BL2	BDALØ7 L
BM1	GND	BM2	BDALØ8 L
BN1	---	BN2	BDALØ9 L
BP1	---	BP2	BDAL10 L
BR1	---	BR2	BDAL11 L
BS1	---	BS2	BDAL12 L
BT1	GND	BT2	BDAL13 L
BU1	---	BU2	BDAL14 L
BV1	+5 V	BV2	BDAL15 L

Signals left blank (---) are not connected.

**The internal refresh oscillator at BK1 is normally jumped to BL1 on the backplane. Jumper options allow for an external refresh oscillator to be connected through BL1.

2.3.2 Jumper Configuration

There are two types of jumpers on the MMS1132. Jumpers E1 and E2 are zero ohm resistors which are soldered onto the board. Jumpers E3 through E31 are normally "mini-jump" shorting plugs; however, the wafer posts could be wire wrapped instead. Figure 2-2 illustrates the jumper locations.

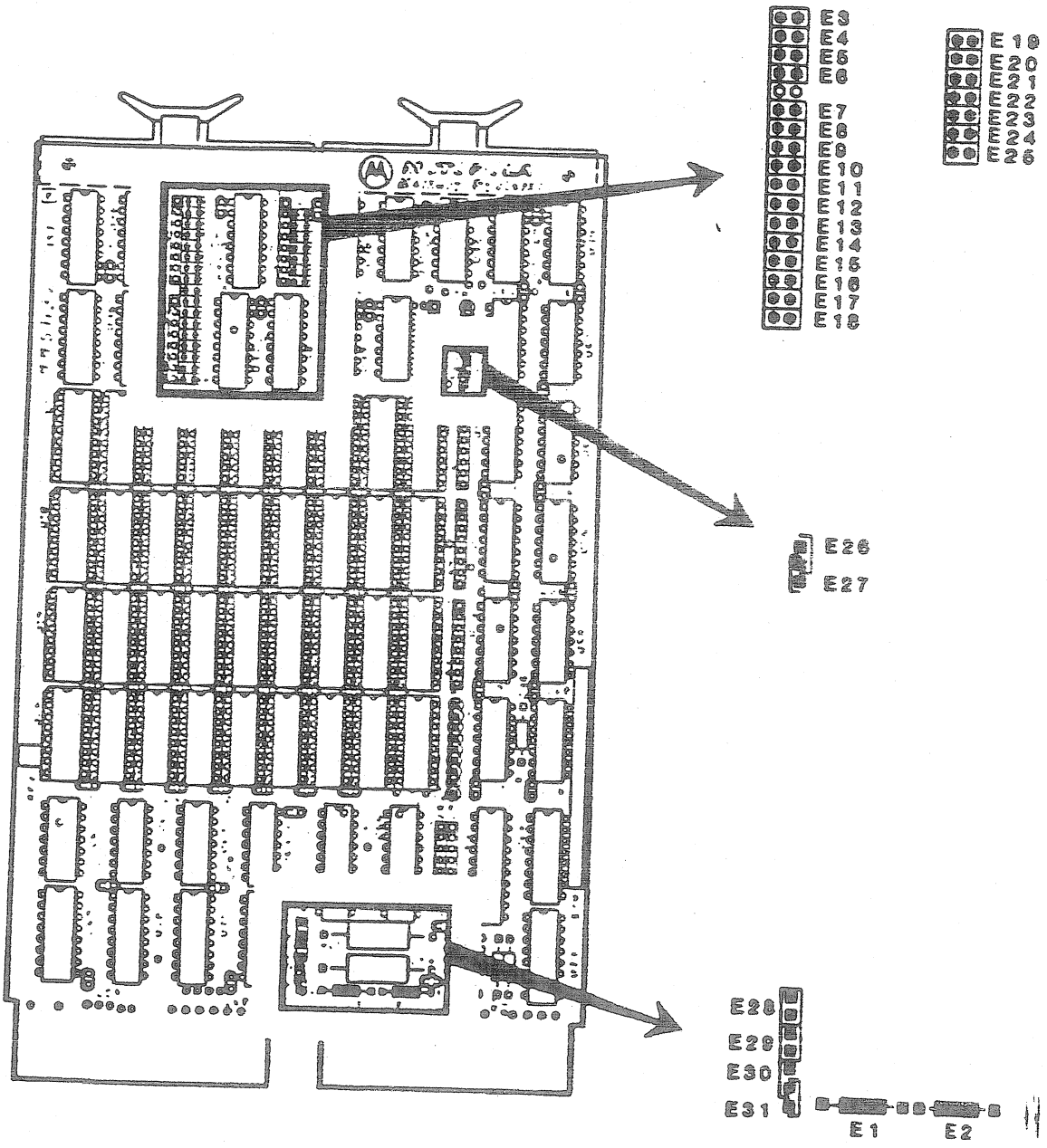


FIGURE 2-2. JUMPER LOCATIONS

a) Jumpers E1, E2

These two jumpers are associated with the +5 volts battery power distribution. In the non-battery back-up configuration (normal), E2 connects +5 volts from bus pins AA2, BA2, and BV1 to the +5 VBBU network on the MMS1132.

In the battery back-up configuration, E1 connects +5 volts from bus pin AV1 to the +5 VBBU network on the MMS1132.

b) Jumpers E3, E4, E5, E6

These four jumpers are used in LSI-11/23 systems that support extended memory management. In these systems memory space is extended to sixteen 128K word pages. Jumpers E3 thru E6 are used to establish which of these pages the MMS1132 will appear in. On some early revision CPU's the four MMU address lines were high true instead of low true. In these cases, the presence and absence of jumpers is opposite of that for low true MMU address lines. Refer to Table 2-2.

TABLE 2-2. EXTENDED MEMORY JUMPER CONFIGURATION

E3	E4	E5	E6	Page	Memory Address (Octal)
X	X	X	X	0	00000000 - 00777777
X	X	X	-	1	01000000 - 01777777
X	X	-	X	2	02000000 - 02777777
X	X	-	-	3	03000000 - 03777777
X	-	X	X	4	04000000 - 04777777
X	-	X	-	5	05000000 - 05777777
X	-	-	X	6	06000000 - 06777777
X	-	-	-	7	07000000 - 07777777
-	X	X	X	8	10000000 - 10777777
-	X	X	-	9	11000000 - 11777777
-	X	-	X	10	12000000 - 12777777
-	X	-	-	11	13000000 - 13777777
-	-	X	X	12	14000000 - 14777777
-	-	X	-	13	15000000 - 15777777
-	-	-	X	14	16000000 - 16777777
-	-	-	-	15	17000000 - 17777777

Normal (Low True MMU Bus Lines):
X = Jumper Present, - = Jumper Removed
Early CPU's (High True MMU Bus Lines):
- = Jumper Present, X = Jumper Removed

c) Jumpers E7, E8

These two jumpers are used to configure the MMS1132 to work with 64K or 32K x 1 RAM devices. When using 64K RAMs E7 routes translated address bit TA17 H to the row select logic. When using 32K RAMs E8 routes translated address bit TA16 H to the row select logic (refer to Table 2-3).

TABLE 2-3. RAM TYPE CONFIGURATION

RAM Type	E7	E8	E9	E10	E11
MCM6665L20	X	-	X	-	-
MCM66330L20	-	X	-	X	-
MCM66331L20	-	X	-	-	X

X = Jumper Installed
- = Jumper Absent

d) Jumpers E9, E10, E11

These three jumpers are used to configure the MMS1132 to work with 64K RAMs or either type of 32K partial RAMs (high half good or low half good).

e) Jumpers E12, E13, E14, E15, E16, E17, E18

These seven jumpers are used to establish the starting address of the MMS1132 within a 128K word page. Note that all memory on an MMS1132 exists on a single 128K word page. If the sum of the start address plus the size is greater than 128K, then the board will only select from the start address to the end of the page. The board will not extend into the low address space of the next page nor wrap around to the low address space of the current page. Refer to Table 2-4.

TABLE 2-4. STARTING ADDRESS JUMPER CONFIGURATION

E12	E13	E14	E15	E16	E17	E18	Starting Address (In Words)
-	-	-	-	-	-	-	0K
-	-	-	-	-	-	X	1K
-	-	-	-	-	X	-	2K
-	-	-	-	-	X	X	3K
-	-	-	-	X	-	-	4K
-	-	-	-	X	-	X	5K
-	-	-	-	X	X	-	6K
-	-	-	-	X	X	X	7K
-	-	-	X	-	-	-	8K
-	-	-	X	-	-	X	9K
-	-	-	X	-	X	-	10K
-	-	-	X	-	X	X	11K
-	-	-	X	X	-	-	12K
-	-	-	X	X	-	X	13K
-	-	-	X	X	X	-	14K
-	-	-	X	X	X	X	15K
-	-	X	-	-	-	-	16K
-	-	X	-	-	-	X	17K
-	-	X	-	-	X	-	18K
-	-	X	-	-	X	X	19K
-	-	X	-	X	-	-	20K
-	-	X	-	X	-	X	21K
-	-	X	-	X	X	-	22K
-	-	X	-	X	X	X	23K
-	-	X	X	-	-	-	24K
-	-	X	X	-	-	X	25K
-	-	X	X	-	X	-	26K
-	-	X	X	-	X	X	27K
-	-	X	X	X	-	-	28K
-	-	X	X	X	-	X	29K
-	-	X	X	X	X	-	30K
-	-	X	X	X	X	X	31K

TABLE 2-4. STARTING ADDRESS JUMPER CONFIGURATION (cont'd)

E12	E13	E14	E15	E16	E17	E18	Starting Address (In Words)
-	X	-	-	-	-	-	32K
-	X	-	-	-	-	X	33K
-	X	-	-	-	X	-	34K
-	X	-	-	-	X	X	35K
-	X	-	-	X	-	-	36K
-	X	-	-	X	-	X	37K
-	X	-	-	X	X	-	38K
-	X	-	-	X	X	X	39K
-	X	-	X	-	-	-	40K
-	X	-	X	-	-	X	41K
-	X	-	X	-	X	-	42K
-	X	-	X	-	X	X	43K
-	X	-	X	X	-	-	44K
-	X	-	X	X	-	X	45K
-	X	-	X	X	X	-	46K
-	X	-	X	X	X	X	47K
-	X	X	-	-	-	-	48K
-	X	X	-	-	-	X	49K
-	X	X	-	-	X	-	50K
-	X	X	-	-	X	X	51K
-	X	X	-	X	-	-	52K
-	X	X	-	X	-	X	53K
-	X	X	-	X	X	-	54K
-	X	X	-	X	X	X	55K
-	X	X	X	-	-	-	56K
-	X	X	X	-	-	X	57K
-	X	X	X	-	X	-	58K
-	X	X	X	-	X	X	59K
-	X	X	X	X	-	-	60K
-	X	X	X	X	-	X	61K
-	X	X	X	X	X	-	62K
-	X	X	X	X	X	X	63K

TABLE 2-4. STARTING ADDRESS JUMPER CONFIGURATION (cont'd)

E12	E13	E14	E15	E16	E17	E18	Starting Address (In Words)
X	-	-	-	-	-	-	64K
X	-	-	-	-	-	X	65K
X	-	-	-	-	X	-	66K
X	-	-	-	-	X	X	67K
X	-	-	-	X	-	-	68K
X	-	-	-	X	-	X	69K
X	-	-	-	X	X	-	70K
X	-	-	-	X	X	X	71K
X	-	-	X	-	-	-	72K
X	-	-	X	-	-	X	73K
X	-	-	X	-	X	-	74K
X	-	-	X	-	X	X	75K
X	-	-	X	X	-	-	76K
X	-	-	X	X	-	X	77K
X	-	-	X	X	X	-	78K
X	-	-	X	X	X	X	79K
X	-	X	-	-	-	-	80K
X	-	X	-	-	-	X	81K
X	-	X	-	-	X	-	82K
X	-	X	-	-	X	X	83K
X	-	X	-	X	-	-	84K
X	-	X	-	X	-	X	85K
X	-	X	-	X	X	-	86K
X	-	X	-	X	X	X	87K
X	-	X	X	-	-	-	88K
X	-	X	X	-	-	X	89K
X	-	X	X	-	X	-	90K
X	-	X	X	-	X	X	91K
X	-	X	X	X	-	-	92K
X	-	X	X	X	-	X	93K
X	-	X	X	X	X	-	94K
X	-	X	X	X	X	X	95K

TABLE 2-4. STARTING ADDRESS JUMPER CONFIGURATION (cont'd)

E12	E13	E14	E15	E16	E17	E18	Starting Address (In Words)
X	X	-	-	-	-	-	96K
X	X	-	-	-	-	X	97K
X	X	-	-	-	X	-	98K
X	X	-	-	-	X	X	99K
X	X	-	-	X	-	-	100K
X	X	-	-	X	-	X	101K
X	X	-	-	X	X	-	102K
X	X	-	-	X	X	X	103K
X	X	-	X	-	-	-	104K
X	X	-	X	-	-	X	105K
X	X	-	X	-	X	-	106K
X	X	-	X	-	X	X	107K
X	X	-	X	X	-	-	108K
X	X	-	X	X	-	X	109K
X	X	-	X	X	X	-	110K
X	X	-	X	X	X	X	111K
X	X	X	-	-	-	-	112K
X	X	X	-	-	-	X	113K
X	X	X	-	-	X	-	114K
X	X	X	-	-	X	X	115K
X	X	X	-	X	-	-	116K
X	X	X	-	X	-	X	117K
X	X	X	-	X	X	-	118K
X	X	X	-	X	X	X	119K
X	X	X	X	-	-	-	120K
X	X	X	X	-	-	X	121K
X	X	X	X	-	X	-	122K
X	X	X	X	-	X	X	123K
X	X	X	X	X	-	-	124K
X	X	X	X	X	-	X	125K
X	X	X	X	X	X	-	126K
X	X	X	X	X	X	X	127K

f) Jumpers E19, E20, E21, E22, E23, E24, E25

These seven jumpers establish the size of the memory space of the MMS1132 board. (1K - 128K words). See Table 2-5.

TABLE 2-5. MEMORY SIZE JUMPER CONFIGURATION

E19	E20	E21	E22	E23	E24	E25	Size (In Words)
-	-	-	-	-	-	-	1K
-	-	-	-	-	-	X	2K
-	-	-	-	-	X	-	3K
-	-	-	-	-	X	X	4K
-	-	-	-	X	-	-	5K
-	-	-	-	X	-	X	6K
-	-	-	-	X	X	-	7K
-	-	-	-	X	X	X	8K
-	-	-	X	-	-	-	9K
-	-	-	X	-	-	X	10K
-	-	-	X	-	X	-	11K
-	-	-	X	-	X	X	12K
-	-	-	X	X	-	-	13K
-	-	-	X	X	-	X	14K
-	-	-	X	X	X	-	15K
-	-	-	X	X	X	X	16K
-	-	X	-	-	-	-	17K
-	-	X	-	-	-	X	18K
-	-	X	-	-	X	-	19K
-	-	X	-	-	X	X	20K
-	-	X	-	X	-	-	21K
-	-	X	-	X	-	X	22K
-	-	X	-	X	X	-	23K
-	-	X	-	X	X	X	24K
-	-	X	X	-	-	-	25K
-	-	X	X	-	-	X	26K
-	-	X	X	-	X	-	27K
-	-	X	X	-	X	X	28K
-	-	X	X	X	-	-	29K
-	-	X	X	X	-	X	30K
-	-	X	X	X	X	-	31K
-	-	X	X	X	X	X	32K

TABLE 2-5. MEMORY SIZE JUMPER CONFIGURATION (cont'd)

E19	E20	E21	E22	E23	E24	E25	Size (In Words)
-	X	-	-	-	-	-	33K
-	X	-	-	-	-	X	34K
-	X	-	-	-	X	-	35K
-	X	-	-	-	X	X	36K
-	X	-	-	X	-	-	37K
-	X	-	-	X	-	X	38K
-	X	-	-	X	X	-	39K
-	X	-	-	X	X	X	40K
-	X	-	X	-	-	-	41K
-	X	-	X	-	-	X	42K
-	X	-	X	-	X	-	43K
-	X	-	X	-	X	X	44K
-	X	-	X	X	-	-	45K
-	X	-	X	X	-	X	46K
-	X	-	X	X	X	-	47K
-	X	-	X	X	X	X	48K
-	X	X	-	-	-	-	49K
-	X	X	-	-	-	X	50K
-	X	X	-	-	X	-	51K
-	X	X	-	-	X	X	52K
-	X	X	-	X	-	-	53K
-	X	X	-	X	-	X	54K
-	X	X	-	X	X	-	55K
-	X	X	-	X	X	X	56K
-	X	X	X	-	-	-	57K
-	X	X	X	-	-	X	58K
-	X	X	X	-	X	-	59K
-	X	X	X	-	X	X	60K
-	X	X	X	X	-	-	61K
-	X	X	X	X	-	X	63K
-	X	X	X	X	X	-	63K
-	X	X	X	X	X	X	64K

TABLE 2-5. MEMORY SIZE JUMPER CONFIGURATION (cont'd)

E19	E20	E21	E22	E23	E24	E25	Size (In Words)
X	-	-	-	-	-	-	65K
X	-	-	-	-	-	X	66K
X	-	-	-	-	X	-	67K
X	-	-	-	-	X	X	68K
X	-	-	-	X	-	-	69K
X	-	-	-	X	-	X	70K
X	-	-	-	X	X	-	71K
X	-	-	-	X	X	X	72K
X	-	-	X	-	-	-	73K
X	-	-	X	-	-	X	74K
X	-	-	X	-	X	-	75K
X	-	-	X	-	X	X	76K
X	-	-	X	X	-	-	77K
X	-	-	X	X	-	X	78K
X	-	-	X	X	X	-	79K
X	-	-	X	X	X	X	80K
X	-	X	-	-	-	-	81K
X	-	X	-	-	-	X	82K
X	-	X	-	-	X	-	83K
X	-	X	-	-	X	X	84K
X	-	X	-	X	-	-	85K
X	-	X	-	X	-	X	86K
X	-	X	-	X	X	-	87K
X	-	X	-	X	X	X	88K
X	-	X	X	-	-	-	89K
X	-	X	X	-	-	X	90K
X	-	X	X	-	X	-	91K
X	-	X	X	-	X	X	92K
X	-	X	X	X	-	-	93K
X	-	X	X	X	-	X	94K
X	-	X	X	X	X	-	95K
X	-	X	X	X	X	X	96K

TABLE 2-5. MEMORY SIZE JUMPER CONFIGURATION (cont'd)

E19	E20	E21	E22	E23	E24	E25	Size (In Words)
X	X	-	-	-	-	-	97K
X	X	-	-	-	-	X	98K
X	X	-	-	-	X	-	99K
X	X	-	-	-	X	X	100K
X	X	-	-	X	-	-	101K
X	X	-	-	X	-	X	102K
X	X	-	-	X	X	-	103K
X	X	-	-	X	X	X	104K
X	X	-	X	-	-	-	105K
X	X	-	X	-	-	X	106K
X	X	-	X	-	X	-	107K
X	X	-	X	-	X	X	108K
X	X	-	X	X	-	-	109K
X	X	-	X	X	-	X	110K
X	X	-	X	X	X	-	111K
X	X	-	X	X	X	X	112K
X	X	X	-	-	-	-	113K
X	X	X	-	-	-	X	114K
X	X	X	-	-	X	-	115K
X	X	X	-	-	X	X	116K
X	X	X	-	X	-	-	117K
X	X	X	-	X	-	X	118K
X	X	X	-	X	X	-	119K
X	X	X	-	X	X	X	120K
X	X	X	X	-	-	-	121K
X	X	X	X	-	-	X	122K
X	X	X	X	-	X	-	123K
X	X	X	X	-	X	X	124K
X	X	X	X	X	-	-	125K
X	X	X	X	X	-	X	126K
X	X	X	X	X	X	-	127K
X	X	X	X	X	X	X	128K

g) Jumpers E26, E27

These two jumpers are used to configure the parity option of the MMS1132. If E26 is installed then the output of the parity checking circuit will assert BDAL16 L if a parity error is detected during a read operation. If E27 is installed instead of E26, then parity is disabled and BDAL17 L will never be asserted by the MMS1132. Jumpers E26 and E27 should not be installed at the same time.

h) Jumper E28

This jumper is used to enable BBS7 L to override selection of the MMS1132. If E28 is not present, assertion of BBS7 L has no effect on the MMS1132.

i) Jumper E29

This jumper is used to enable a special form of refresh in conjunction with BREF L. When E29 is installed, both E3Ø and E31 should be removed. When E29 is installed BREF L may be used for synchronous refresh. The master would assert BREF L while BSYNC L was not asserted. The MMS1132 will perform a refresh cycle.

j) Jumpers E30, E31

These two jumpers are associated with the refresh circuitry. The board is normally built with E3Ø installed and E31 not installed. The normal refresh configuration is a jumper between BK1 and BL1 on the backplane. The internal asynchronous refresh oscillator is routed from BK1 through the backplane jumper to BL1, then through E3Ø to the refresh circuitry.

To synchronize refresh from one source to several boards, bus pin BL1 and tie it to the refresh oscillator source. The backplane jumpers must be removed from BK1-BL1.

If E31 is installed instead of E3Ø then no backplane jumper is required.

2.3.3 Operation

To use the MMS1132 Add-In Memory Array Board, after jumpers are installed, turn off system/backplane power and carefully insert the board into its proper slot. Turn on power.

CHAPTER 3

THEORY OF OPERATION

3.1 CONFIGURATIONS

There are two configurations of operation for the MMS1132, normal and battery backup. The board is shipped in the normal configuration (see Chapter 2). Jumpers may be changed to allow the board to work in the battery back-up configuration.

The power distribution within the MMS1132 board is partitioned in such a manner that the circuitry necessary for maintaining data can optionally be obtained from the pin assigned as +5 V BBU. This option can be implemented via jumpers E1 and E2. The board is normally shipped with jumper E2 installed and jumper E1 not installed (non battery back-up). To reconfigure for battery back-up, install jumper E1 and remove jumper E2.

For battery back-up, an uninterrupted power source must be connected (+5 volts battery to pin AV1).

3.2 ADDRESSING

The MMS1132 has jumpers to allow flexible configuration of the MMS1132 in address space. Addressing circuitry is also affected by two bus signals (BBS7 and BREFL).

Bus signal BBS7 (Bus Block Select 7) is an indicator that the CPU is making an I/O reference so the memory should be inhibited. In systems with more than 32K words of address space, it is sometimes desirable to defeat this inhibit so that all memory on the MMS1132 can be used. Jumper E28 is used for this option (see Chapter 2 on jumper configuration for details).

BREFL is a bus signal indicating that a CPU generated refresh cycle should be performed. The MMS1132 inhibits its board select and generates a refresh cycle in response to this signal. In systems using this type of refresh, the other type of refresh should be disabled by removing jumpers E30 and E31. The BREF L feature is enabled by installing jumper E29. Refer to Chapter 2 on jumper configuration for details.

Jumpers E19 through E25 are used to set the board size from 1K to 128K words. Jumpers E3 through E6 are used in LSI-11/23 systems with extended memory management. In these systems, jumpers E3 through E6 are used to configure the MMS1132 to reside in one of the 16-128K word pages. Jumpers E12 through E18 are used to set the starting address of the MMS1132 (ØK to 127K). Note that all memory on an MMS1132 must reside in the same 128K word page (i.e., if an MMS1132 is configured to start at 127K and its 'size' is set to 32K, it will actually only exist to the next 128K boundary and will not 'wraparound' or extend into the next 128K page).

3.3 BLOCK DIAGRAM

Refer to Figure 3-1.

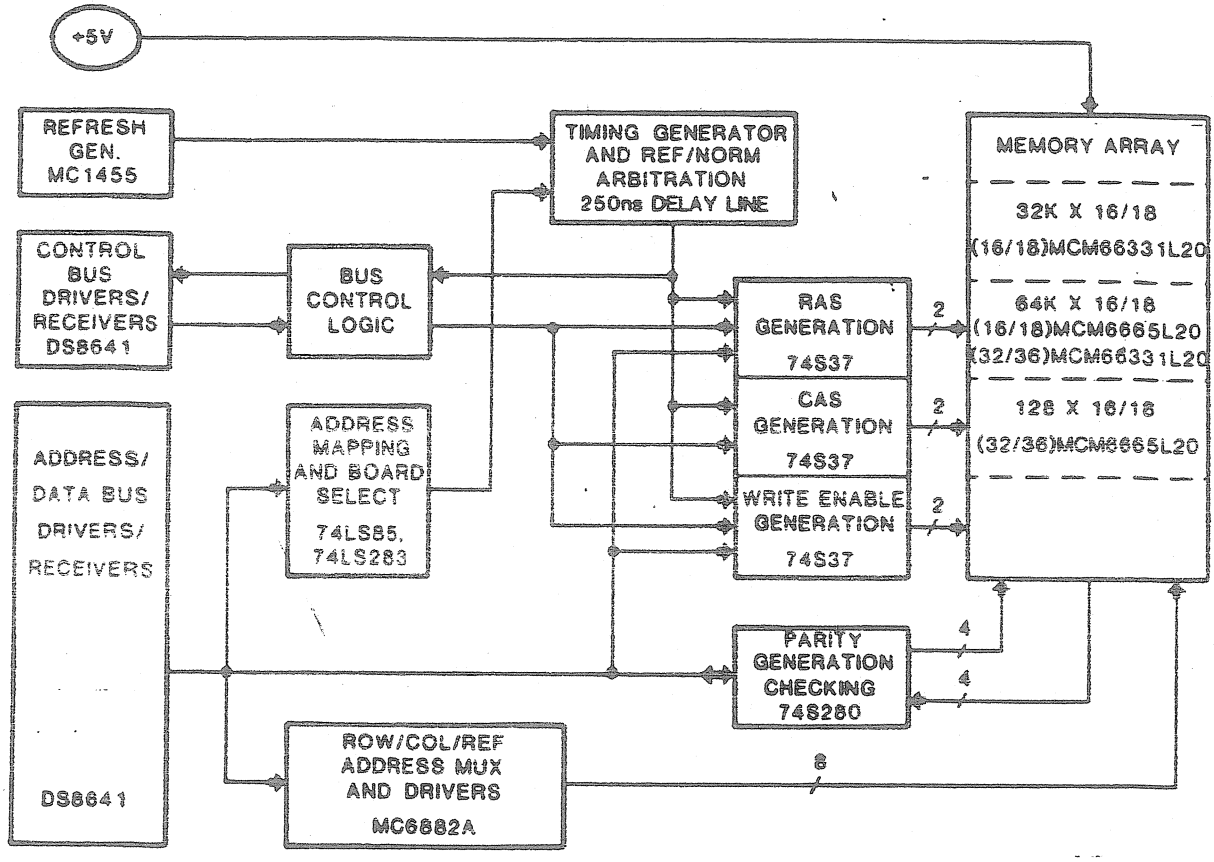


FIGURE 3-1. BLOCK DIAGRAM

3.4 MEMORY ARRAY

The memory array on the MMS1132 consists of a 36 device array. Figure 3-2 illustrates the memory array layout. On the non-parity versions, there are no parts inserted for U1, U10, U19, or U28. On versions with only one row of RAMs, no parts are inserted for U10 through U18 or U28 through U36.

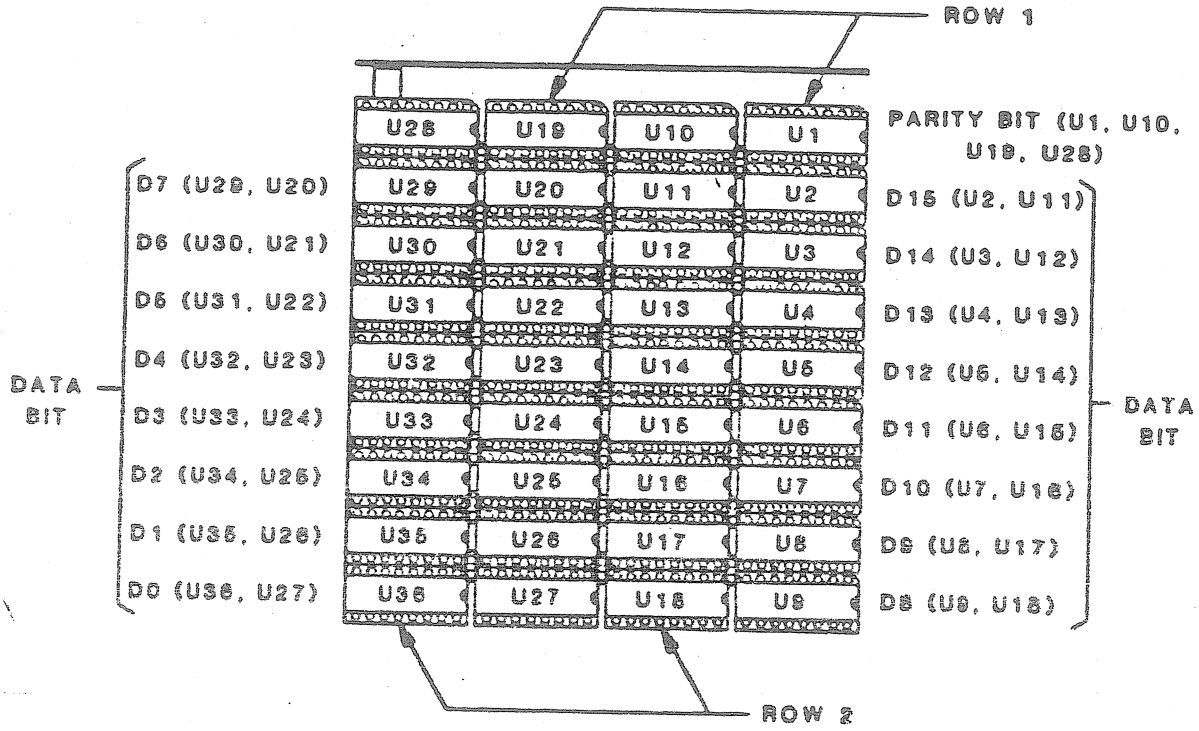


FIGURE 3-2. MEMORY ARRAY

3.5 INPUT/OUTPUT SIGNALS

The following table describes the various control and response signals of the MMS1132 array board.

TABLE 3-1. SIGNAL DESCRIPTIONS

Signal	Type	Description
BSYNC L	Input	This signal (when asserted low) indicates that the Master (CPU) has initiated a bus cycle. Depending upon the addressing jumper configuration, the cycle may or may not be intended for a particular MMS1132.
BWTBT L	Input	This signal is used to tell whether a cycle is a read or write cycle and if it is a write cycle, whether it is a byte or word write. If BWTBT L is not asserted at the falling edge of BSYNC L, then the cycle is a read cycle. If the cycle is a write cycle and BWTBT L is asserted low while BDOUT L is asserted low, then it is a byte write.
BBS7 L	Input	This signal is asserted low by the Master whenever an access is made to any address in block 7 (octal x7xxxx, where x = don't care). This is usually an I/O access so the MMS1132 should be deselected; however if jumper E28 is removed, then the board may select anyway.
BREF L	Input	This signal is used on some early versions of CPUs to perform memory refresh. Refer to E29 in Chapter 2 for a detailed explanation.
BRPLY L	Output	This signal is asserted low by the Slave (MMS1132) to indicate that write data has been taken or read data is available on the bus (BDAL00 through BDAL15).
BDCOK H	Input	This signal is asserted high on the bus when the system dc voltages are valid and stable.
BDIN L	Input	This signal is asserted low by the Master to indicate that the Slave (MMS1132) may place read data on the bus (BDAL00 through BDAL15).
BDOUT L	Input	This signal is asserted low by the Master to indicate that write data is valid and available on the bus (BDAL00 through BDAL15).

TABLE 3-1. SIGNAL DESCRIPTIONS (cont'd)

Signal	Type	Description
BDAL00-17	Input/ Output	These multi-function address/data lines are bi-directional and time multiplexed. During the first part of a bus cycle, they carry address information from the Master to the Slave (MMS1132). During the last portion of the cycle, they carry data to (write) or from (read) the Slave (MMS1132).
EXTREF IN	Input	This pin can be used to synchronize refresh between multiple memory boards in a system. See jumpers E30 and E31 in Chapter 2 for details. Normally refresh is performed by an on-board oscillator and EXTREF IN is not used.
MMUDAL18 L - MMUDAL21 L	Input	These four signals are used on LSI-11/23 CPUs with extended memory management. The lines behave as high order address bits. On some early versions of CPUs, these lines were high true instead of low true so addressing jumpers should be applied differently. The MMS1132 will operate with either polarity.

3.6 TIMING

Table 3-2 contains all the relevant timing parameters for the modes of operations for the MMS1132.

The following notes apply to all timing parameters (consistent with the specifications of the LSI-11 "Q" Bus Plus):

1) All Timing is measured on the memory side of the Bus transceivers.

2) Memory is not busy (i.e., assuming that no refresh cycle is in progress at the time of cycle initiation).

3) All access times are measured from the leading edge of SYNC H to the leading edge of RPLY H, and assume the minimum specified delay from SYNC H to DIN H (25 ns) and from SYNC H to DOUT H (50 ns).

4) The read modify write cycle assumes that the delay from RPLY H to DOUT H is 350 ns.

5) Cycle time is defined as the shortest time between recognition of successive SYNC H signals.

TABLE 3-2. MMS1132 TIMING

Parameter	Symbol	Typical	Worst Case	Unit
Write	t_{WA}	175	225	ns
Read	t_{RA}	225	275	ns
Read Modify Write	t_{RW}	575	---	ns
Cycle	t_{CY}	525	550	ns

3.6.1 MODES OF OPERATION

a. Normal Read

Refer to Figure 3-3, read cycle timing diagram. The read bus cycle is divided into two parts, address portion and data portion. During the address portion, a bus master transfers a memory address to the MMS1132 on signal lines BDAL0 L through BDAL17 L and MMUDAL18 L through MMUDAL21 L (22 lines total). This address is valid for a set-up time (75 ns) before and a hold time (25 ns) after the rising edge on the buffered signal SYNC H.

Also, during the addressing portion of the read cycle, the bus signal BWTBT L will be inactive and the state of the BBS7 L signal may override selection of the MMS1132 board if it is active and properly configured.

Determination of board select is made during the address set-up time and if selected, a read access time will be started with the activation of BSYNC L.

After the address portion of the cycle, the master activates the BDIN L bus signal which starts the data portion of the read cycle. When the read access time has timed and the DIN signal is present, the MMS1132 will activate the BRPLY H signal to indicate to the bus master that the requested data has been placed on the BDAL00 L through BDAL15 L bus pins.

The bus master then removes the BDIN L signal which causes the MMS1132 to remove the BRPLY L signal. The bus master then removes the BSYNC L signal which completes the read cycle.

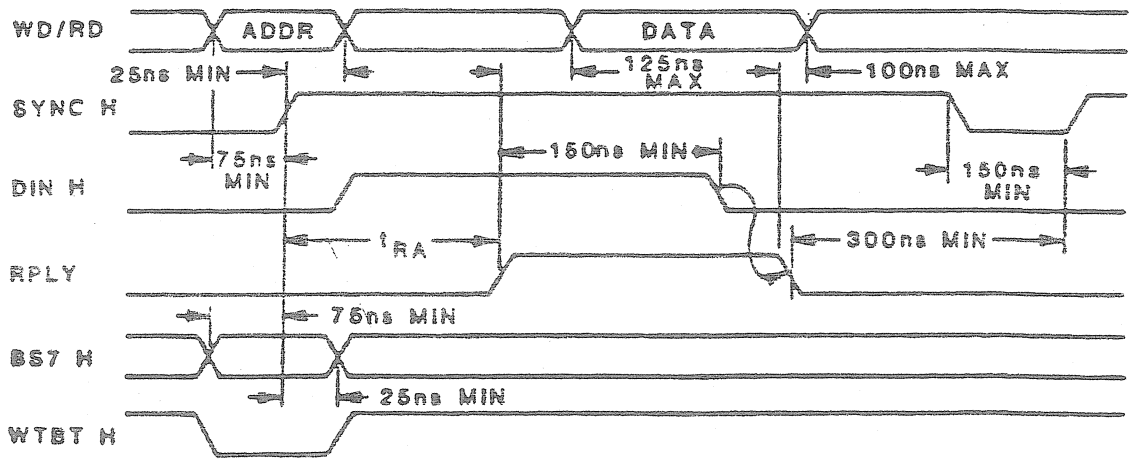
b. Normal Write

Refer to Figure 3-4, write cycle timing diagram. The write cycle is divided into two parts, address portion and data portion. The address portion is the same as described above for the read cycle except that the bus signal BWTBT L will be activated during the set-up and hold time.

Following the address portion of the write cycle the master activates the BDOUT L signal to start the data portion of the cycle. Data to to the MMS1132 is valid on bus lines BDAL00 L through BDAL15 L for 25 ns set-up time before BDOUT L is activated and for 25 ns hold time after BDOUT L is released.

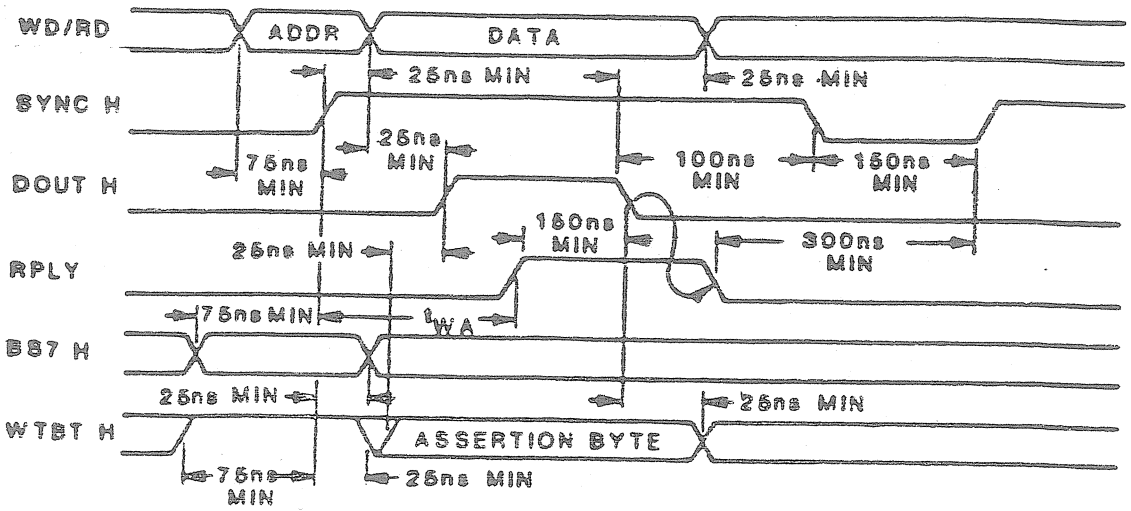
If the BWTBT L signal is asserted during the data portion of the cycle, then only one byte will be written instead of a 16 bit word. If BDAL16 L is asserted during the write operation then false parity is generated for diagnostic purposes.

Upon completion of the write operation the MMS1132 issues the BRPLY L signal, then the master releases BDOUT L, then the MMS1132 releases BRPLY L, and finally the master releases BSYNC L.



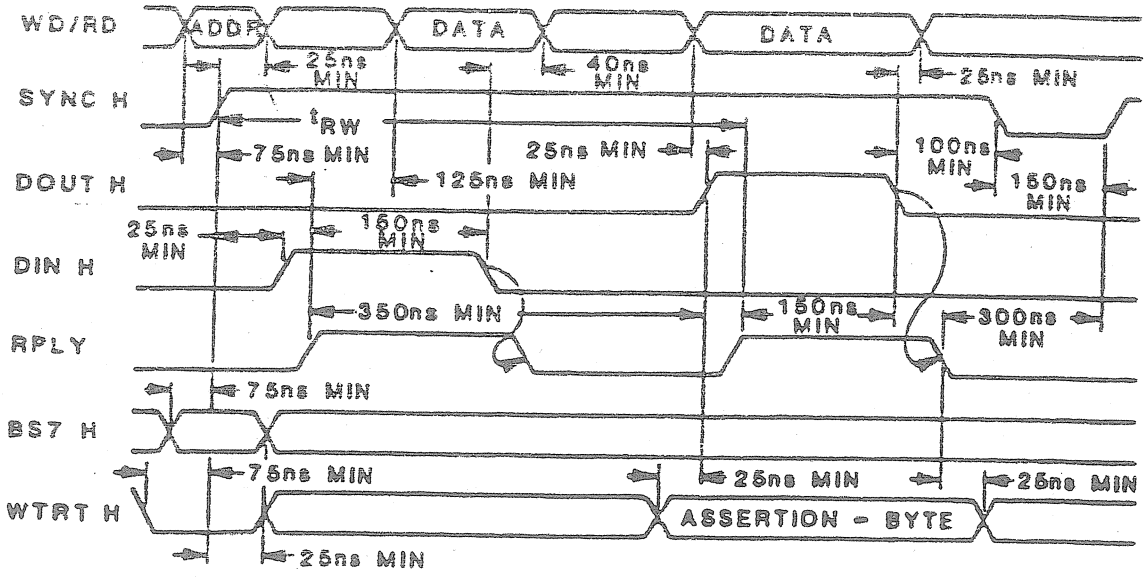
NOTE: All timing measured from inside bus transceivers.

FIGURE 3-3. READ CYCLE TIMING DIAGRAM



NOTE: All timing measured from inside bus transceivers.

FIGURE 3-4. WRITE CYCLE TIMING DIAGRAM



NOTE: All timing measured from inside bus transceivers.

FIGURE 3-5. READ/MODIFY/WRITE CYCLE TIMING DIAGRAM

c. Read-Modify-Write

Refer to Figure 3-5, read/modify/write cycle timing diagram.

The read/modify/write cycle is like a read cycle followed by a write cycle where BSYNC L remains asserted throughout the entire operation. The address is the same for the read and the write, however, the write may be a byte write while reads are always for full 16-bit words. The read/modify/write cycle is divided into three parts, the address portion, the read data portion, and the write data portion.

3.7 REFRESH LATENCY

The storage cells in the MMS1132 are implemented with dynamic MOS devices. The charge stored in each cell is automatically refreshed every 2 milliseconds. The latency induced to bus cycles concurrent with refresh cycles is no greater than the cycle time of the particular memory. A single refresh cycle is initiated approximately once every 16 microseconds.

CHAPTER 4

MAINTENANCE

4.1 TROUBLESHOOTING

For all troubleshooting, refer to the test point locations diagram, Figure 4-1, and the schematic diagram, Figure 4-2. The component location diagram is shown in Chapter 5.

Begin troubleshooting by checking the power supply voltage. Use caution when replacing defective parts. Improper handling and too much heat can destroy components.

4.2 TEST POINTS

Fifteen test points are included on the MMS1132 for convenience. Table 4-1 gives the test points and describes their function. Figure 4-1 illustrates the test point locations on the MMS1132.

TABLE 4-1. TEST POINT DESCRIPTION

Test Point	Description
TP1	Ground
TP2	Memory Address Drive MA1
TP3	Memory Address Drive MA5
TP4	Memory Address Drive MA4
TP5	Memory Address Drive MA3
TP6	Memory Address Drive MA6
TP7	Memory Address Drive MA2
TP8	Memory Address Drive MA0
TP9	Read Reply (Active High)
TP10	Bus Drive Enable (Active High)
TP11	Write Reply (Active High)
TP12	Memory RAS Enable
TP13	Memory CAS Enable
TP14	Ground
TP15	Timing Chain Input

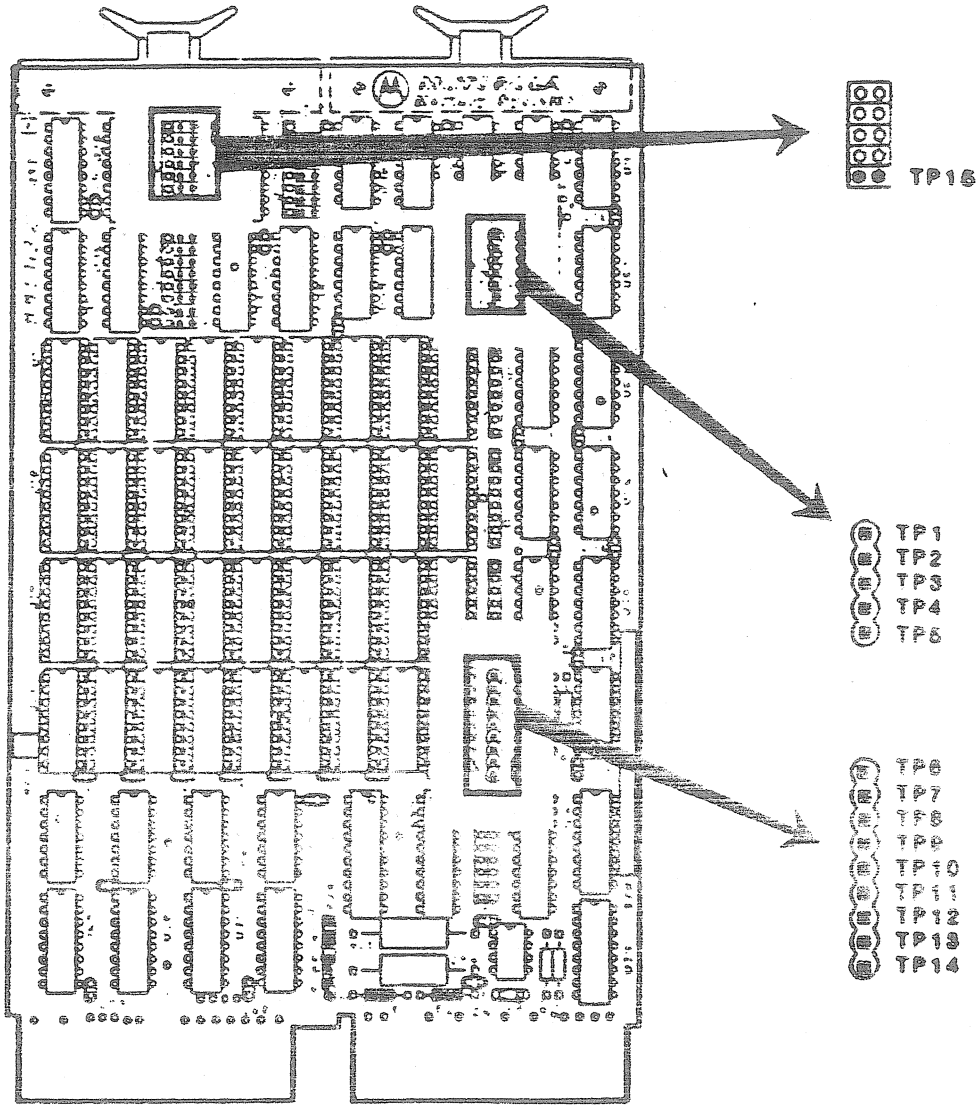


FIGURE 4-1. TEST POINT LOCATIONS

4.3 CIRCUIT DESCRIPTION

Refer to the schematic diagram, figure 4-2. Sheet 2 contains edge connector circuitry. The power connection requires a single 5-volt supply, applied through jumpers E1 and E2. Jumper E2 (normal) connects the +5 volts to the board battery network and E1 allows battery back-up configuration from bus pin AV1.

U40A and U49B concerns read reply. U49B pin 6 becomes active (high) when all inputs to U49B are low. The high becomes a low to U45 pins 4 and 12 for bus reply.

Write reply is developed in timing during a write cycle. When write reply is high to U45 pin 5, it also causes U45 pins 4 and 12 to go low for a bus reply signal.

U37, 69, 70, 71, and 72 buffer the multiplex data and address lines. During part of the cycle they carry address information, and in another part, carry data. U51C is a buffer enable for the board-to-bus direction when low, during a read cycle. U74 buffers the board main control signals and is only used as a receive buffer. U57C and D buffer the sync signal and delay it slightly.

Device U73 is the asynchronous refresh oscillator with an output to jumper E31 and the edge connector.

The parity circuits are U61, 62, 63, and 64. Parity generation occurs in U66 and 64 and parity checking in U61 and 63. Eight bits of data are used to generate a parity bit.

When doing a write cycle with the board configured for parity, if WA16 to pin 1 of U62 and 64 is active, it will force a parity error to be written into memory. The forced parity error is a test and verification feature.

When reading data from memory, the parity checking circuitry redevelops the parity bit including the stored parity. If the ODD output of U61 or 63 is low, a parity error will be generated through U51D. This parity error will be applied to jumper E26 if present, and to U37 for output to the bus.

Normal refresh occurs from U73 to bus pin BK1, through a backplane jumper to BL1 through E30 to U74, to U40E pin 11. A synchronous refresh uses the BREF L signal with E29 in place and E30 and 31 out.

The BDCOK H signal is low when the +5 volts dc input is missing, which will disable the board from performing any cycles.

Sheet 3 has address mapping devices U38, 46, and 47. U65, 66, and 67 form a 3-to-1 address multiplexer and driver. U59 is a refresh clock.

Device U38 compares the state of address lines WA18-21 to the state of address lines controlled by jumpers E3-6. A matching comparison gives a high output signal on U38 pin 6, and a low to U49A pin 1. All 5 inputs to U49A must be low to cause the board to be selected. The board select is true only at the rising edge of signal SYNCHB H.

Devices U46 and 47 are an adder combination for a starting address select signal.

Jumpers E12-18 provide conditions for comparison with address lines WD11-15 and WA16 and 17. When the comparison is in range, U46 pin 10 provides a high to U40B and thus a low to U49A pin 2.

The adder outputs of U46 and 47 also form signals TA11-17 (translated address) to U39 and 48. These signals are used with jumpers E19-25 to establish overall size of memory space.

Devices U50B and U52A are the two flip-flops that cause the start of a cycle. U50B is the refresh latch and U52A is the select latch. Since these signals are asynchronous to each other, arbitration logic is required. U51A, 51B, 43D, and 42C provide a high at U42C pin 8 (TP1). The high starts a signal through delay line U44 and clocks refresh/normal flip-flop U50A. The outputs of U50A determine whether a refresh or a normal cycle is to occur.

Signals RCY H and NCY H are not used before 50ns into the cycle, to establish stability. The delay line provides additional signals for proper relationships, and turns off after 250ns. At the end of a cycle, U41A pin 3 or U42A pin 3 will reset U50B or U52A (whichever was serviced).

A normal cycle begins with a RAS, 50ns after the delay line starts. This 50ns signal clocks U52B whose input is the normal cycle high (NCY H) signal from U50A pin 6. U50B outputs a high at pin 9 to U54B pin 5 and U54A pin 2.

The other input to U54B pin 4 is RAS1 enable, and to U54A pin 1 is RAS$\emptyset$ enable. Either RAS signal occurs from U55A through row select jumpers E7 and 8.

The U54B pin 6 output (for RAS1) is a high if U54B pin 4 is RAS1EN low. U53B pin 6 also is low (active) to the memory array since its input pin 4 is high through U54C and U54D for a normal cycle. RAS$\emptyset$ enable at U53D pin 11 occurs the same way if RAS$\emptyset$ is enabled from U55A. Both RAS$\emptyset$ and RAS1 cannot be enabled at the same time for a normal cycle, but are both on for a refresh cycle.

A refresh cycle makes U54C pin 8 low at 150ns into the cycle, making U54D pin 11 high. U54B pin 6 and U54A pin 3 are now both high since U52B pin 9 is low during refresh. Thus both RAS$\emptyset$ and RAS1 are enabled at the same time to the memory array.

CAS timing is controlled by flip-flop U56B which is clocked at 150ns into a cycle. A normal cycle will clock a high to U56B pin 9 and enable the memory array.

During a read cycle, the reply timing is controlled by U56A. A read cycle causes U43C pin 6 to be high, and at 200ns, both highs at U56A pins 2 and 3 will cause a low at read reply pin 6.

A write reply requires that the cycle has been underway for at least 150ns, to make U42D pin 12 high. Also DOUT H to U42D pin 13 must come from the bus. U42D pin 11 thus enables the write enable drivers U57A and B. U58A, B, and U40F determine how much of the word will be written.

WEL L (Write Enable Low) goes to the low order byte of all the memory words. WEH H (Write Enable High) goes to the high order byte of all the memory words. Normally, all 16 bits are written-to at the same time, except during the byte write cycle when the WTBT signal is activated. The low or high order byte will be enabled by U58A or U58B through the LAO H signal from U55B pin 9.

Control for address mutliplexing is through U41D, U58C, and U58D. With no signal in the delay line U44, U41D pin 11 and U58D pin 11 will both be high and U58C pin 8 low. This will select the row multiplexer U66. U66 inputs will then be transferred to the memory address lines XA$\emptyset$ through XA7 to become MA$\emptyset$-MA7.

During a normal cycle, when the 100ns tap of U44 is active, U58D pin 11 goes low. This turns off row driver U58C pin 8, turns on column driver U58D pin 11, and column multiplexer U65.

During a regular cycle (normal cycle), at 50ns RAS occurred, at 100ns the multiplexer switched from row to column address, and at 150ns the CAS occurred.

A refresh cycle will activate, at 50ns, the refresh low signal at U41D pin 11 to turn off the row address. Refresh driver U67 will be enabled to take addresses from the refresh counter U59. After the refresh cycle is ended, U67 is disabled and the refresh counter is incremented to the next state.

Sheet 4 shows the memory array, consisting of 36 devices arranged electrically as 2 rows of 18 devices (row $\emptyset$ and row 1). The write enable (WEL L) connects to the low order data bits of both rows. WEH L connects to all the high order data bits of both rows.

Device U1, 10, 19, and 26 are for parity circuits. Refer to figure 3-2 for the memory array layout.

FIGURE 4-2. SCHEMATIC DIAGRAM

Sheet 1: Index Page

Sheet 2: Schematic Diagram

Sheet 3: Schematic Diagram

Sheet 4: Schematic Diagram

NOTE: This is sheet 1 of Figure 4-2. The schematic diagram contains 3 sheets.

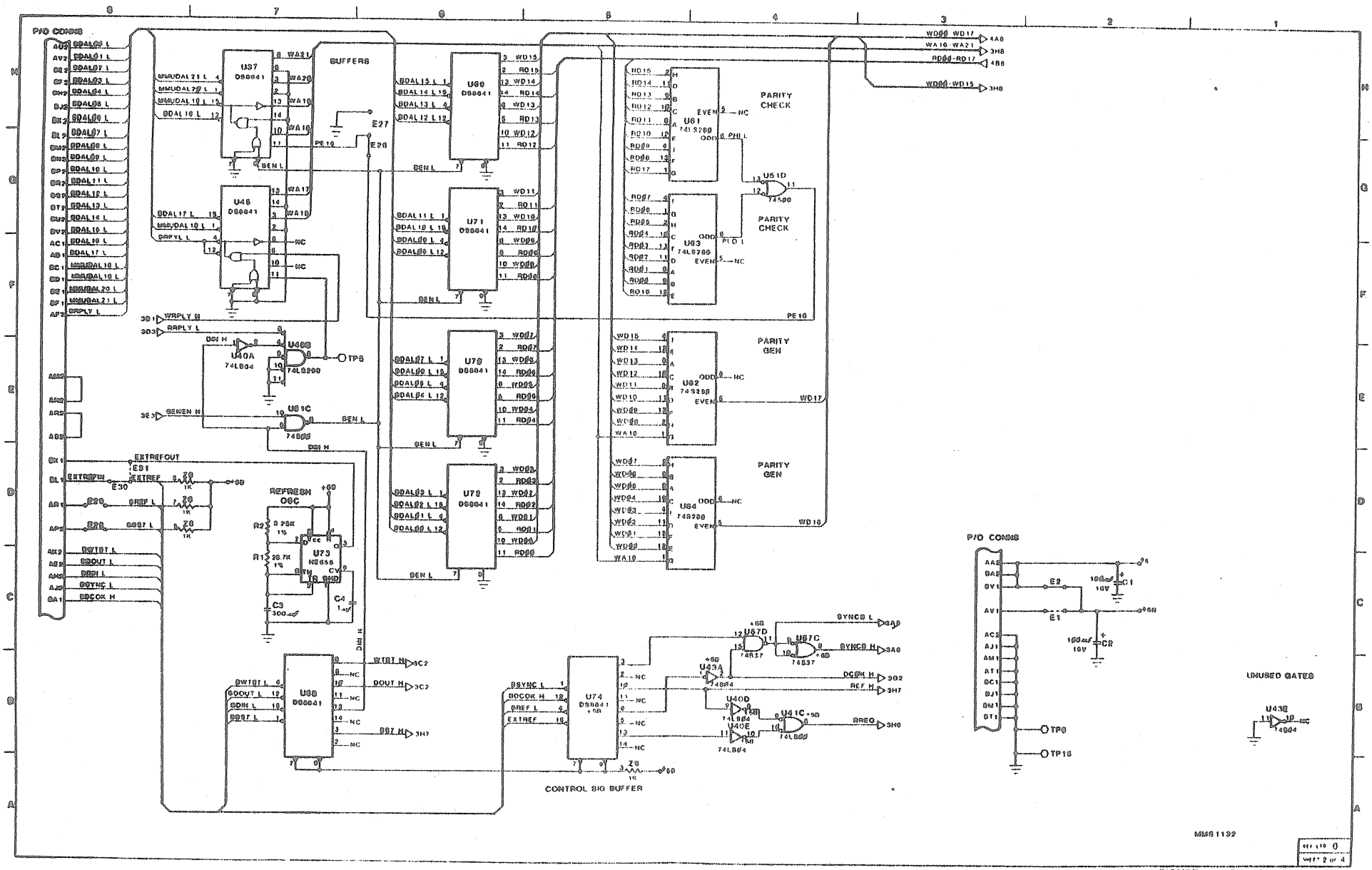


FIGURE 4-2 SCHEMATIC DIAGRAM
SHEET 2 OF 4 4-774-6

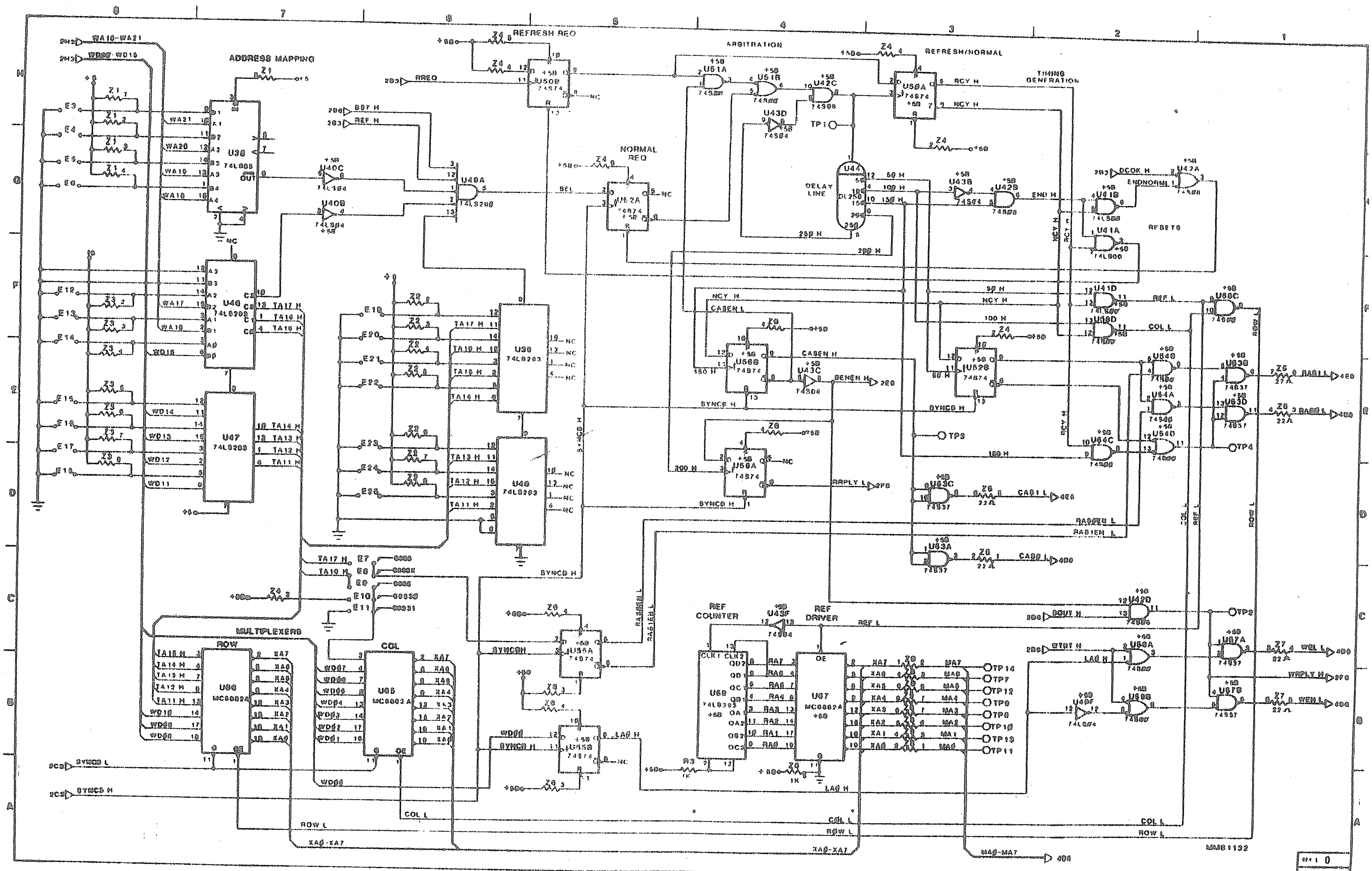


FIGURE 4-2 SCHEMATIC DIAGRAM
SHEET 3 OF 4 4-9/4-10

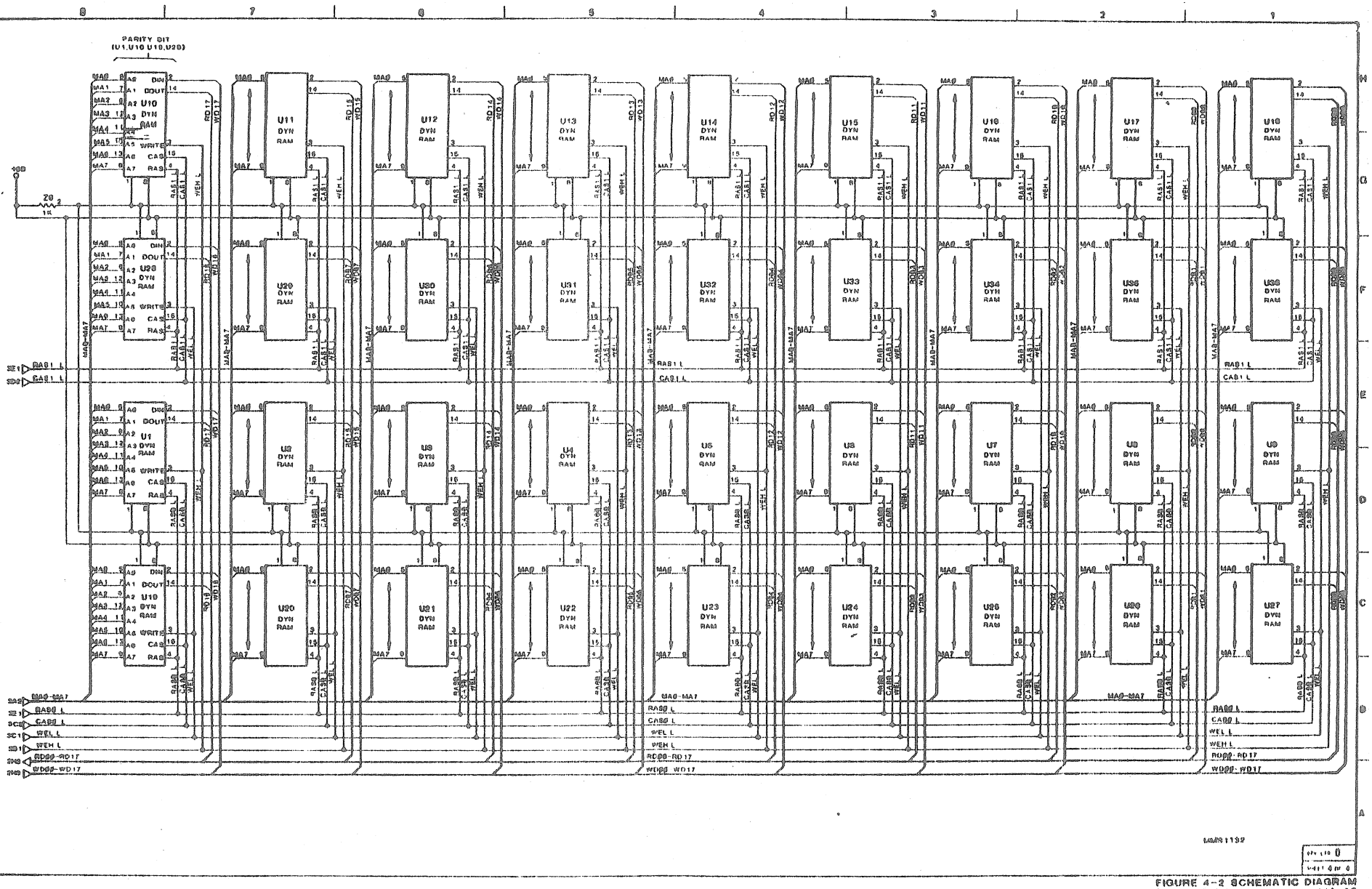


FIGURE 4-2 SCHEMATIC DIAGRAM
SHEET 4 OF 4 4-11/4-12

CHAPTER 5

PARTS LIST

5.1 GENERAL

This chapter consists of Figure 5-1, Board Outline and Component Layout, Table 5-1, which is a listing of parts contained in the MMS1132 Add-in Memory Array Board, and Table 5-2, Model Types and Special IC Quantities.

TABLE 5-1. MMS1132 PARTS LIST

Quan.	Description	Part Number	Reference Designation
1	PC Board, Basic	---	---
1	Integrated Circuit	74LS00	U41
3	Integrated Circuit	74S00	U51, 54, 58
1	Integrated Circuit	74S04	U43
1	Integrated Circuit	74LS04	U40
1	Integrated Circuit	74S08	U42
2	Integrated Circuit	74S37	U53, 57
4	Integrated Circuit	74S74	U50, 52, 55, 56
1	Integrated Circuit	74LS260	U49
4	Integrated Circuit	74LS283	U39, 46, 47, 48
1	Integrated Circuit	74LS393	U59
1	Integrated Circuit	74LS85	U38
3	Integrated Circuit	MC6882	U65, 66, 67
8	Integrated Circuit	DS8641	U37, 45, 68-72, 74
1	Integrated Circuit	NE555	U73
1	Integrated Circuit	Delay Line	U44
*36	Integrated Circuit	66331L20	U1-36*
*18	Integrated Circuit	6665L20	U1-9, U19-27*
* 2	Integrated Circuit	74S280	U62, 64*
* 2	Integrated Circuit	74LS280N	U61, 63*

* Varies per model type. Refer to Table 5-2.

TABLE 5-1. MMS1132 PARTS LIST (cont'd)

Quan.	Description	Part Number	Reference Designation
5	Resistor, SIP, 1K x 7		Z1-4, 6
2	Resistor, SIP, 33 x 4		Z8, 9
2	Resistor, SIP, 22 x 4		Z5, 7
1	Resistor, Zero ohm		E2
1	Resistor, 8.25K, 1/8W, 1%		R2
1	Resistor, 28.7K, 1/8W, 1%		R1
1	Resistor, 1K, 1/4W, 5%		R3
59	Capacitor, 0.1 uf mono		C4-62
1	Capacitor, 300 pf mica		C3
2	Capacitor, 100 uf, 16V		C1, 2
2	Card Puller		

TABLE 5-2. MODEL TYPES AND SPECIAL IC QUANTITIES

IC DEVICE AND REFERENCE DESIGNATION	MMS1132 MODEL TYPE							
	3032		3064		3065		3128	
	N	P	N	P	N	P	N	P
	device quantity							
MCM66331L20								
U2-9, 20-27	16							
U1-9, 19-27		18						
U2-9, 11-18, 20-27, 29-36					32			
U1-36						36		
MCM6665L20								
U2-9, 20-27			16					
U1-9, 19-27				18				
U2-9, 11-18, 20-27, 29-36							32	
U1-36								36
74S280								
U62, 64		2		2		2		2
74LS280N								
U61, 63		2		2		2		2

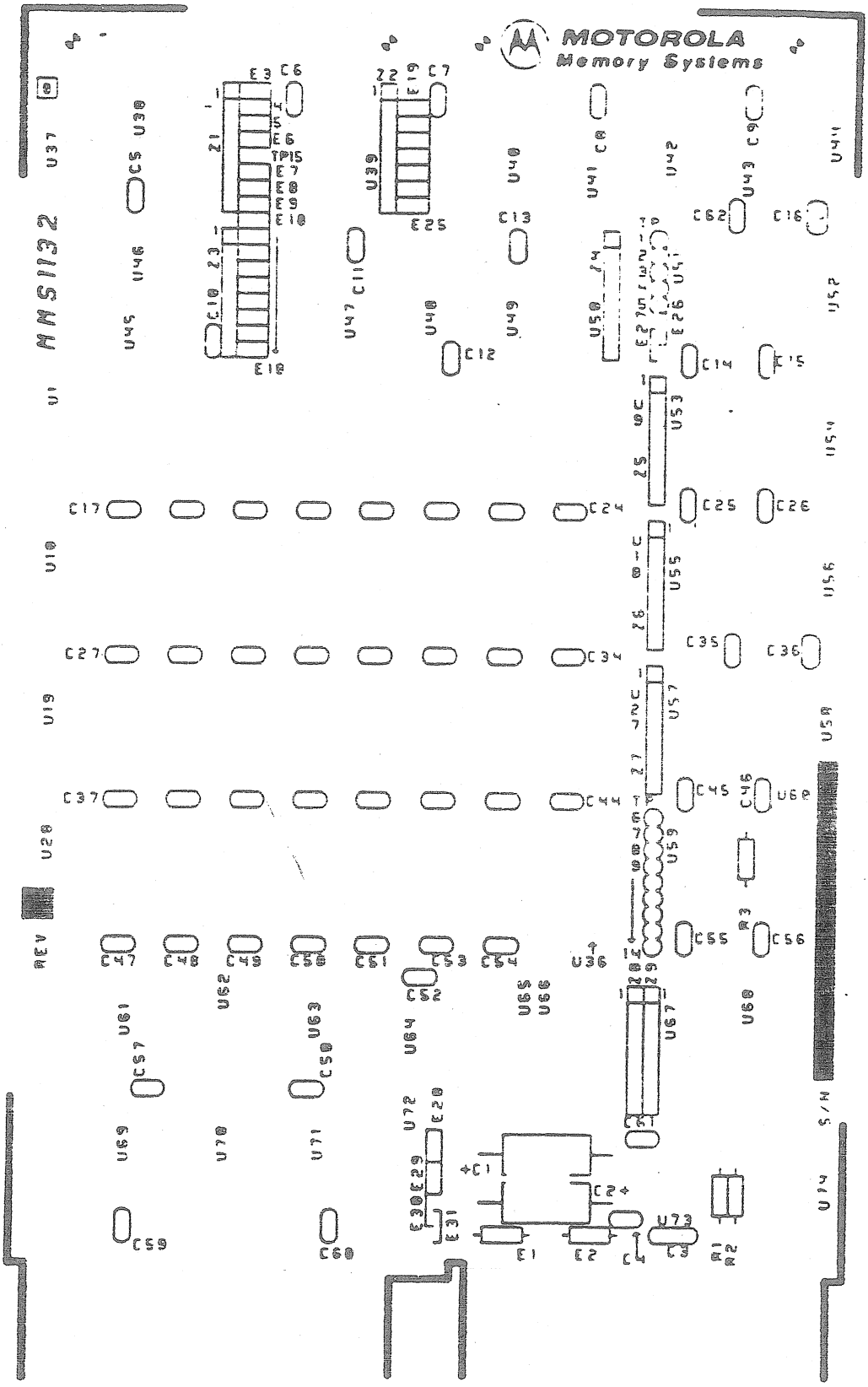


FIGURE 5-1. BOARD OUTLINE AND COMPONENT LAYOUT

APPENDIX 1

WARRANTY INFORMATION

Type M-FWS
FACTORY WARRANTY
SERVICE PLAN

The Factory Warranty Service plan sets forth the services available at Motorola Memory Systems for the repair of products and product subassemblies which fail during the warranty period. Motorola Memory Systems warrants all factory-supplied products in accordance with the Standard Warranty stated at the end of this service plan.

PLAN

Motorola Memory Systems provides complete factory support for its products and product subassemblies which fail during the warranty period.

Motorola factory authorization for a return must be obtained prior to returning any article to the factory. Upon authorization, the factory will issue a Customer Return Order Number which will be utilized for all correspondence regarding such a product being returned for service by Motorola Memory Systems.*

Any article returned to the factory must be properly packed and marked with a return address which includes the name and telephone number of the individual requesting the repair. The nature of the failure must be clearly identified.

If a subassembly is being returned, the serial number of the assembly from which the subassembly was removed must also be provided.

Within ten working days (plus shipping time) after receipt of the article, Motorola Memory Systems will either refund the purchase price, or repair or replace the article with a new or equivalent-to-new-performance article which has been subjected to appropriate tests, requalifying it to original specifications. See the STANDARD WARRANTY which governs all details of this plan.

CHARGES

Warranty repairs, as defined within the STANDARD WARRANTY, will be made at no charge to the customer for parts and labor. Articles returned to the factory should be shipped prepaid. They will be returned prepaid.

Repair, labor, and/or parts replacement made at the customer's request for failures not covered by warranty provisions will be invoiced to the customer at the then-current rates and conditions for Motorola Memory Systems' Factory Repair Service.

PARTS

The parts replaced will be new or equivalent to new in performance. Defective parts replaced become the property of Motorola Memory Systems.

MECHANICAL CONDITION

Factory repair is restricted to correcting article failure. Cosmetic refurbishment will not be performed.

STANDARD WARRANTY

The Seller warrants that the articles sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to the Seller's specifications, or as appropriate, to the Buyer's specifications which have been accepted in writing by the Seller. Seller's sole obligation hereunder shall be limited to either refunding the purchase price or repairing or replacing the articles for which written description of nonconformance hereunder is received within one year from date of initial shipment; provided a Customer Return Order Number is obtained* for return of nonconforming articles and; provided such articles are returned FOB Seller's plant or authorized repair center within thirty (30) days from expiration of said one year period. This warranty shall not apply to any products which Seller determines have, by Buyer or otherwise, been subjectd to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established therefore in the applicable specifications or otherwise have been subjected to mishandling, misuse, neglect, improper testing, repair, alteration or damage, assembly or processing that alters physical or electrical properties. Transportation charges for the return to the Buyer shall be paid by Motorola within the contiguous 48 United States and Canada. If Motorola determines that the products are not defective, Buyer shall pay Motorola all costs of handling and transportation. The warranty outside the contiguous 48 United States and Canada excludes all costs of shipping, customs clearance and related charges.

In no event will Seller be liable for any incidental or consequential damages. THIS WARRANTY EXTENDS TO BUYER ONLY AND NOT TO BUYER'S CUSTOMERS OR USERS OF BUYER'S PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED, OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS.

*Authorization and Customer Return Order Number are obtained by calling (512) 928-6000 X 4203, Motorola Memory Systems Warranty and Repair Service, 3501 Ed Bluestein Blvd., Austin, Texas 78721

Type M-FRS
FACTORY REPAIR
SERVICE PLAN

The Factory Repair Service plan sets forth the services available at Motorola Memory Systems for the repair of products and product subassemblies which are not under warranty.

PLAN

Motorola Memory Systems provides complete factory service for the repair and requalification of its products and product subassemblies.

Motorola factory authorization for a return must be obtained prior to returning any article to the factory. Upon authorization, the factory will issue a Customer Return Order Number which will be utilized for all correspondence regarding the product being serviced by Motorola Memory Systems*

Factory service requires a method for guaranteed payment for all repair and requalification services prior to any actual work performance.

Any article returned to the factory must be properly packed and marked with a return address which includes the name and telephone number of the individual requesting the repair. The nature of the failure must be clearly identified.

If a subassembly is being returned, the serial number of the assembly from which the subassembly was removed must also be provided.

Within ten working days (plus shipping time) after receipt of the article, Motorola Memory Systems will repair or replace the article with a new or equivalent-to-new-performance article which has been subjected to appropriate tests, requalifying it to original specifications.

CHARGES

Articles returned to the factory should be shipped prepaid. They will be returned prepaid. Repair, labor, and parts replaced will be invoiced to the customer at the then-current rates and conditions for Motorola Memory Systems' Factory Repair Service. A minimum factory service charge will be imposed for processing repair orders of small dollar value. Contact Motorola Memory Systems' Warranty and Repair Service for information regarding minimum factory service charges.

PARTS

The parts replaced will be new or equivalent to new in performance. Defective parts replaced become the property of Motorola Memory Systems.

MECHANICAL CONDITION

Factory repair is restricted to correcting article failure. Cosmetic refurbishment will not be performed.

WARRANTY

Motorola Memory Systems warrants only the repair and parts replaced for a period of ninety (90) days from date of return of repaired article to customer, provided factory authorization and a Customer Return Order Number is obtained* for the return of nonconformance of repair or parts replaced and; provided such repaired article is returned FOB Motorola Memory Systems' plant within thirty (30) days from expiration of said ninety (90) day period.

In no event will Seller be liable for any incidental or consequential damages. THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OR MERCHANTABILITY OR FITNESS.

*Authorization and Customer Return Order Number are obtained by calling (512) 928-6000 X 4203, Motorola Memory Systems, Warranty and Repair Service, 3501 Ed Bluestein Blvd., Austin, Texas 78721

APPENDIX 2

REQUEST FOR READER'S COMMENTS

REQUEST FOR READER'S COMMENTS

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2. Does the manual cover the information you expected or required? Please make suggestions for improvement.

3. What faults do you find with the manual?

4. Did you have any difficulty understanding descriptions or wording? Where?

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