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MLSI-512

MTX TV CRT CONTROLLER FAMILY

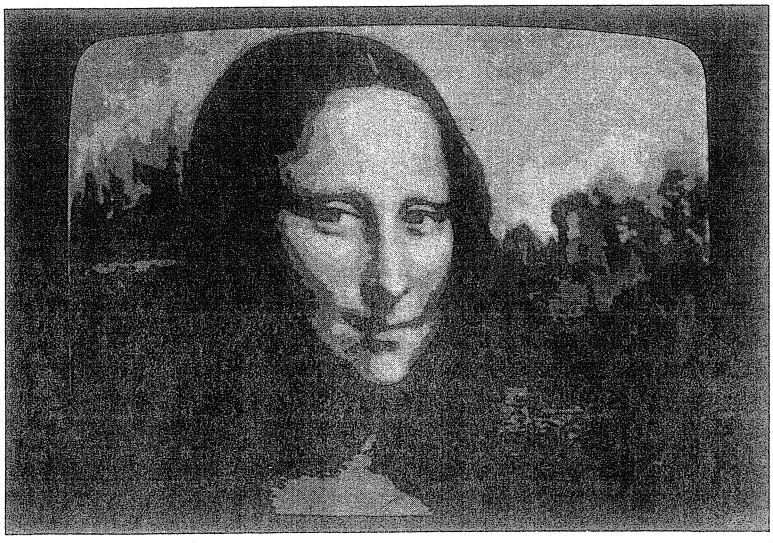
GRAPHIC DISPLAY

INTRODUCTION

The MTX-512 graphics family incorporates the revolutionary new concept of variable resolution graphics on a single controller card. The family of cards is designed to interface a mini or microcomputer to a TV type monitor and produce a graphics raster with selectable resolution. Any card in the MTX-512 family can be user programmed to produce a dot matrix of 256 X 256; 256 X 512; 512 X 512; or 256 X 1024 points. The family consists of a series of cards which are plug compatible with industry standard buses. These include the DEC PDP-11, LSI-11 and Intel SBC-80 buses. All cards in the family can be readily interfaced to other mini/microcomputers. Stand alone controllers can be configured by combining MTX-512 series cards and Intel or DEC card cages.

FEATURES:

- Resolutions of 256 X 256; 256 X 512; 512 X 512; 256 X 1024 points.
- Multiple cards stackable for color/grey scale applications.
- Single command image memory erase.
- Image memory can be read back.
- Vertical scroll built into hardware.
- Can be used as intelligent stand alone graphic controller.
- American/European TV standard operation field programmable.
- Compatible 24 line X 80 character display available.
- Can be synchronized to external sync generator.
- Powerful X-Y addressing technique.



BLOCK DIAGRAM

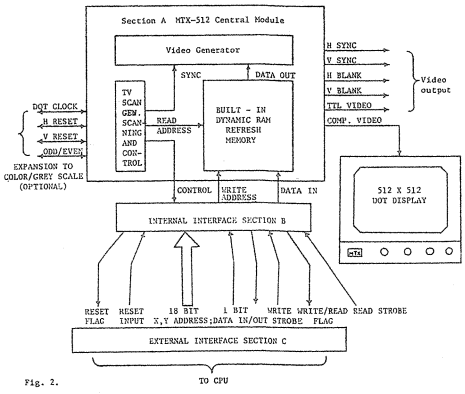


Fig. 2.

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1.0 MTX-512 FAMILY TECHNICAL SPECIFICATION

Nominal Resolution:	256 Vertical X 256 Horizontal; 256 X 512; 512 X 512; and 256 X 1024 factory or field programmable. Note that on American Standard card, the number of displayed lines is reduced. The actual resolutions displayed are 240 X 256; 240 X 512; 480 X 412; and 240 X 1024.
Write Time:	Dot write time 1.4 usec. max.
Erase:	Single instruction erases screen; 48 msec. max.
Scroll:	Built-in scroll register allows display to be shifted vertically with one line resolution.
Read/Write:	Image memory is fully read/write addressable.
Dimensions:	PC board $7\frac{3}{4}$ X $10\frac{1}{2}$ inches (MDC and MLSI), or 12 X $6\frac{1}{4}$ inches (MSBC)
Power:	+5V 800 mA, +15/12V 200 mA.
Outputs:	75 Ohm composite video, TTL video, horizontal and vertical sync and blank outputs, light pen.
TV Standard:	American or European standard available.
Synchronization:	Built-in crystal controlled TV scan generator, or external sync.
Color/Grey Scale:	Up to 24 bits/pixel (2^{24} different colors or grey scale levels/dot by using identical multiple boards).
Buses:	Digital Equipment PDP-11 (MDC); LSI (MLSI) or Intel SBC-80 (MSBC). 2480 test display also available on same buses.
Documentation:	A 24 page manual providing a complete functional description circuit schematics and other information is available separately for $10.00. Additional color/grey scale application note available on request.
Software:	A software package for 8080 based systems which features vector plot, alphanumeric generation and animation synchronization is available. A similar package using PDP-11 software will be available in the 4th quarter of '78.
Warranty:	90 days parts and labor.
Ordering:	Available directly from Matrox Electronic Systems Ltd., or its worldwide network of distributors. Specify options desired. Delivery 2-6 weeks.
Prices:	Quantity of One: 256 X 256 $ 895 256 X 512 $1095 512 X 512 $1395 256 X 1024 $1395

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3.0 FUNCTIONAL DESCRIPTION

3.1 Introduction

The MTX-512 family uses a number of memory locations or I/O ports for data transfers. Two basic I/O transfer formats are used for 8 and 16 bit processors respectively. In addition, the MTX-512 registers may be addressed either as memory locations or memory mapped I/O. The MDC and MLSI cards are memory mapped. The MSBC card is addressed as a group of I/O ports. Note that any of the above cards could be adapted for memory or I/O mapping with almost any other computer. More detail on this is provided in Section 8.

Figure 3 gives the address maps for both types of cards. The exact locations for the registers will be determined by on board jumpers. More detail is provided in Section 10.3. For convenience, the I/O locations are numbered 0-7 (note odd addresses are skipped for DEC compatible cards. This is because AØ is used for byte addressing.)

3.2 X-Y Registers

The MTX-512 graphics family uses a simple yet powerful X-Y addressing scheme. Two directly addressable registers store the X-Y coordinates of a given dot. (see Fig 4 - TV Screen Addressing). This allows two computer memory locations to address up to 262,000 bits of refresh memory. The X register requires a maximum of 10 bits for a resolution of up to 1024 points. The Y register requires a maximum of 9 bits for a resolution of up to 512 points. The LSB of X is ignored for the 512 point resolution, and the 2 LSB of X are ignored for the 256 point horizontal resolution. This allows software written for the 1024 resolution to work with lower resolution cards. The least significant bits, which are unused in the coarser resolution displays, are effectively truncated. A similar principle applies to the Y register. Except that it starts at a 9 bit word length.

For 16 bit processors, locations 2 and 4 are reserved for the X and Y registers. These registers occupy 10 and 9 bits on the data bus respectively. The LSB are ignored for lower resolution modes in the manner described above.

For 8 bit processors, it is necessary to split the X and Y registers into 2 subregisters each. This is because of the 8 bit word length restrictions. The most significant 8 bits of X and Y are stored in locations 4 and 6 respectively. The least significant bits of X and Y are stored in locations 5 and 7. The least significant bits of X and Y are ignored in coarser resolution modes. Thus, only the most significant bytes of X and Y are used in the 256 X 256 resolution mode.

None of the X-Y registers described above can be read by the processor.

3.3 Data Register

After the dot address is loaded, the dot intensity is loaded by outputting data to location 0. In systems requiring color or grey scale identical multiple MTX-512 cards are used. Each card stores one image bit per pixel. The image bit on a given card can be assigned to any data bus bit. (See Section 10.6). Thus the output of each card can be assigned a different weigh weight or color (See Section 5). In a single card system, the image bit is normally assigned to data bit Ø, The resultant TV display is a black and white image with the intensity either on or off.

FIGURE 3 - ADDRESS MAPS

16 BIT PROCESSORS (PDP-11, LSI-11)

WRITE

LOC	Fcn	A17 ... AØ	D15 ... D9 8 ... DØ
0	DATA	1 1 1 1 1 X X X X X X X X X X 0 0 0	X - - - - - - - - - - X X X
2	X	1 1 1 1 1 X X X X X X X X X X 0 1 0	- - - X X X X X X X X X X
4	Y	1 1 1 1 1 X X X X X X X X X X 1 0 0	- - - - - X X X X X X X X X
6	SCROLL	1 1 1 1 1 X X X X X X X X X X 1 1 0	- - - - - - X X X X X X X X

READ

LOC			
0	DATA	1 1 1 1 1 X X X X X X X X X X 0 0 0	0 0 0 0 0 0 0 0 0 0 X X X
2		1 1 1 1 1 X X X X X X X X X X 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0
4		1 1 1 1 1 X X X X X X X X X X 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0
6	FLAGS	1 1 1 1 1 X X X X X X X X X X 1 1 0	0 0 0 0 0 X X X 0 0 0 0 0

8 BIT PROCESSORS, (SBC-80)

WRITE

LOC		A15 ... AØ	D7 ... DØ
0	DATA	X X . . . X X 0 0 0	X - - - - X X X
1	-	X X . . . X X 0 0 1	- - - - - - - -
2	SCROLL	X X . . . X X 0 1 0	X X X X X X X X
3	-	X X . . . X X 0 1 0	- - - - - - - -
4	XH	X X . . . X X 1 0 0	X X X X X X X X
5	XL	X X . . . X X 1 0 1	- - - - - - X X
6	YH	X X . . . X X 1 1 0	X X X X X X X X
7	YL	X X . . . X X 1 1 1	- - - - - - - X

READ

LOC			
0	DATA	X X . . . X X 0 0 0	0 0 0 0 0 X X X
1		X X . . . X X 0 0 1	0 0 0 0 0 0 0 0
2	FLAGS	X X . . . X X 0 1 0	0 0 0 0 0 X X X
3		X X . . . X X 0 1 1	0 0 0 0 0 0 0 0
4		X X . . . X X 1 0 0	0 0 0 0 0 0 0 0
5		X X . . . X X 1 0 1	0 0 0 0 0 0 0 0
6		X X . . . X X 1 1 0	0 0 0 0 0 0 0 0
7		X X . . . X X 1 1 1	0 0 0 0 0 0 0 0

X - Logical 0 or 1
0 - Logical 0
- - Don't Care

3.3 Data Register (continued)

By assigning cards to different data bits, and strapping all the cards with the same address, the intensity or color of a given dot can be loaded in a single instruction.

In addition, data bit 15 (for 16 bit cards) or 7 (for 8 bit cards) acts as a memory erase enable. If this bit is high during a write operation to location Ø, the entire refresh memory of all cards is set to the color specified in the lower data bits.

The intensity or color of the addressed dot can also be read from location Ø.

3.4 Scroll Register

The scroll register is accessed by writing data to location 6 (16 bits) or 2 (8 bits). Setting the scroll register to Ø causes line Y = Ø to be displayed at the top of the picture. Setting the scroll register to 1 causes the line Y = 1 to be displayed at the top of the picture in the 256 line mode. The line Y = 2 will be at the top of the 512 line mode. The following table provides more detail. The scroll register cannot be read by the processor.

SCROLL TABLE

SCROLL REGISTER	TOP LINE 256 MODE Y =	TOP LINE 512 MODE Y =
0	0	0
1	1	2
2	2	4
3	3	6
4	4	8

3.5 Flag Register

The flag register is read by accessing location 6 (16 bit) or location 2 (8 bit). The flag registers are defined as follows:

Flag register 16 bit card, location 6:
Data Bit 5 = Light pen input
Data Bit 6 = Vertical blank, 1 = blank, Ø = video
Data Bit 7 = Ready load, Ø = busy erasing, 1 = not busy

Flag register 8 bit card, Location 1
Data Bit Ø = Ready load, Ø = busy erasing, 1 = not busy
Data Bit 1 = Vertical blank, 1 = blank, Ø = video
Data Bit 2 = Light pen input

Note that an erase command requires a minimum of 33 ms and a maximum of 48 ms. During this time, the 512 card should not be accessed for any other operations. The ready load flag is provided for testing the erase busy condition. The vertical blank flag is provided to assist in animation synchronization. The light pen input flag is directly connected to socket V, Pin 10. It provides a convenient means of interfacing a light pin to the CPU.

4.0 PRINCIPLE OF OPERATION

4.1 Explanation of Block Diagram

The MTX-512 series cards all have the same architecture and share much of the same circuitry. The circuit is divided into sections A, B, and C. These are respectively the MTX-512 central module, the internal interface, and the external interface. (Fig 2.)

The heart of the design is the MTX-512 central module. This module contains the TV sync generator, video generator, and dynamic RAM refresh memory. The TV sync generator/refresh memory combination is designed for programmable resolution using 4K, 8K, and 16K dynamic RAM's. This is accomplished by using a programmable sync generator to scan the refreh memory. The 4K, 8K and 16K dynamics can be interchanged in the memory portion because they are essentially pin compatible. One inserts only as much memory as is actually scanned by the sync generator. The TV sync generator is also designed in such as way that it can act as a master or a slave.

The dot clock, horizontal reset, vertical reset and odd/even lines are three state bi-directional lines. The master card outputs control signals onto these lines permitting the slave cards to operate synchronously. This feature allows multiple cards to be combined for color/grey scale operation.

The MTX-512 central module and internal interface is common on all cards in the family. The MTX-512 is offered on a number of popular buses including the Digital Equipment PDP-11, LSI-11 and Intel SBC-80. The external interface is the only part of the design which is changed for different buses. The commonality of the MTX-512 central module greatly reduces the cost of this broad line of graphics products. The key to the commonality of the central module is the internal interface. This has been designed for maximum flexibility.

The MTX-512 central module (See Fig 5) is itself made of three main blocks: the TV sync generator and control circuity, dynamic RAM refresh memory and a video generator. The sync generator consists of a crystal oscillator (A45) and a divider chain (A1, 2, 3, 4, 5, 6). This divider chain produces all timing signals for the memory scanning as well as horizontal and vertical sync. The TV sync generator can be programmed for different resolution formats, and for the American or European TV standard.

The scanning circuitry consists of multiplexers A9, 10, 11, 12 which provide proper address signals for the dynamic RAM. RAS and CAS RAM refresh signals are generated by A42, 45. RAM read/write control is effected by A13, 14, 15, 55, 6, 8.

The cursor consists of X-Y registers which are loaded by the CPU. A4 and A7 are the X register, A5 and A8 are the Y registers.

Scrolling is controlled by register A3 and counters A1 and A2 in section B. The memory read bit is selected by A53 and A54.

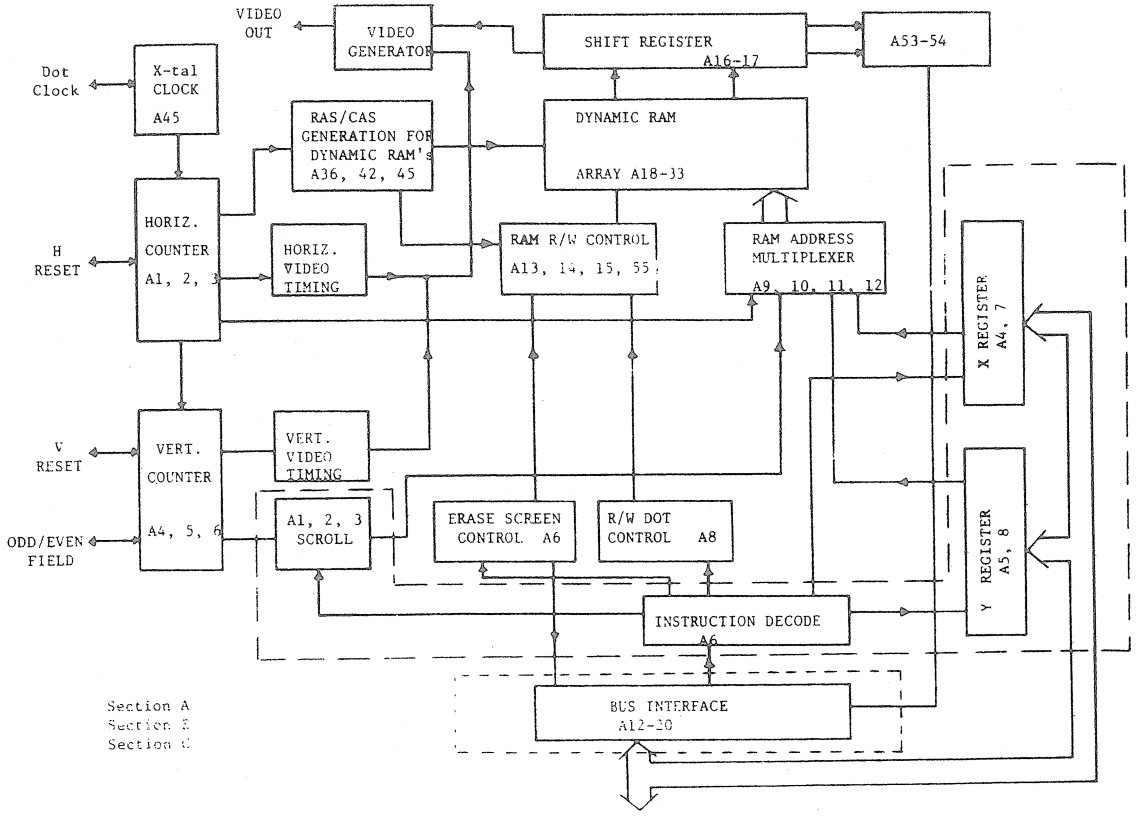
The refresh memory has 16 of the compatible 16 pin dynamic RAM's. (A13-33)

4.2 More on Variable Resolution

The variable resolution feature is made economically possible by the new generation of 16 pin dynamic RAM's. These memories are available in 4K, 8K, and 16K memory sizes in the same compatible 16 pin package. Unique circuit design techniques permit increasing resolution by simply plugging in higher density RAM's and changing programmable jumpers on the board. Thus the 256 X 256 version utilizes 16 4K dynamic RAM's; the 256 X 512 display uses 8K dynamics and the 512 X 512 and 256 X 1024 units employ 16K RAM's. The price of the MTX-512 family cards varies depending on the amount of resolution desired. This is because of the corresponding costs of dynamic RAM's.

The variable resolution feature of the MTX-512 family is facilitated through use of TV interlacing. Standard TV interlacing is produced when the lines of one field or scan fill in the spaces between the lines of the previous field. This can effectively double the resolution of the display in the vertical direction when compared to non-interlaced scans. Standard TV monitors utilize 262 lines per field or 525 lines per frame when interlaced. (This includes displayed lines plus retrace blanking.) The MTX-512 cards with 256 X 256 and 256 X 512 displays (actually 240 X 256 and 240 X 512 American; 256 X 256 and 256 X 512 European TV standard) are non-interlaced. The 512 X 512 display (actually 480 X 512 American; 512 X 512 European) uses standard vertical interlace to double the line resolution. The 256 X 1024 display (240 X 1024 American; 256 X 1024 European) utilizes a Matrox exclusive horizontal interlace technique. This permits doubling the horizontal resolution while at the same time using standard speed memories and logic. This unusual resolution (256 X 1024) is extremely useful in specialized applications such as plotting atomic spectra.

FIG. 5 DETAILED BLOCK DIAGRAM FOR MTX-512



5.0 COLOR/GREY SCALE EXPANSION

5.1 Introduction

The MTX-512 family of cards are designed in such as way that identical multiple boards can be stacked for color/grey scale systems. The sync generator on each card can act as a master or slave. A master card can control up to 23 slaves. In a system consisting of a master and a number of slaves, the video outputs of each card are synchronous. This allows the output to be combined by the user to form a customized color/grey scale system with up to 24 bits per pixel.

The photograph in Fig 1 was taken using three MTX-512 cards in a grey scale configuration. The picture was generated by feeding a TV camera output through a slow scan A/D converter. The three bit digitized output was fed to a three card MTX-512 system. The grey scale picture was produced by feeding the outputs of the three cards to a three bit D/A converter. The resulting picture has 8 discrete grey levels.

5.2 Imaging System Configuration

Fig 6 illustrates how to slave multiple MTX-512 cards for color/grey scale applications. The "V" socket contains all the signals required for expansion. A listing and description of these signals is provided below.

TABLE OF SIGNALS "V" SOCKETS

PIN	NAME (ABBREV.)	DESCRIPTION
1	Dot clock (DTC)	Bi-directional dot clock line.
2	Reset horizontal (HR)	Bi-directional horizontal reset
3	Reset vertical (VR)	Bi-directional vertical reset
4	Odd/even (O/E)	Bi-directional odd/even field
5	External Sync	External sync input to on board video encoder
6	+5V	+5V power 250 mA, Max.
7	Data out	TTL Video
8	Ground	
9	Alpha in	Alphanumeric input for 2480 add on
10	Light pen	Light pen input appears in flag register
11	Vertical blank (BV)	TTL vertical blank
12	Horizontal blank (BH)	TTL horizontal blank
13	Vertical sync (SV)	TTL vertical sync
14	Horizontal sync (SH)	TTL horizontal sync
15	Composite sync	TTL composite sync
16	Composite video (VDO)	Video output

The other key element is jumper W1 which controls whether a card acts as a master or as a slave. In a single card system, W1 is always inserted so that the card acts as a master. On slave cards in a multiple card system, W1 is deleted.

5.2 Imaging System Configuration (continued)

On the master card in a color/grey scale system, the following lines become outputs and are bused to other cards in the system.

Dot Clock
Reset Horizontal
Reset Vertical
Odd/Even Field

These lines act to fully synchronize the sync generators on slave cards with the master. The video outputs of every card are fully synchronous. This allows the user to combine the outputs in various ways to achieve the kind of display required. Feeding the TTL video outputs to a D/A converter will yield a grey scale imaging system. A color system can be obtained by feeding the same signals to a color encoder. More detail on this is provided in the Matrox color/grey scale application notes.

The image data bit for each card can be tied internally to any bit on the data bus. As was described in Section 3.3, this allows the color or intensity of a dot to be specified in a single command. A table for the image bit assignment is given in Section 10.6 More information is also provided in the Graphics Application Note.

Note also that the alpha input is always tied low via jumpers on the V socket when it is not used.

5.3 Combining the 2480 and 512

A compatible 2480 alphanumeric text display is available for most cards in the 512 series. The 512 card contains an alphanumeric input which accepts the TTL video output of the 2480. The result is a powerful display combining both graphics and alphanumerics without the overhead involved in generating alphanumerics using graphics techniques.

Figure 7 illustrates how the connection is accomplished. The 512 card acts as a master and the 2480 units acts as a slave. Multiple 512 type graphics cards can be slaved for additional color/grey scale capability.

5.4 External Sync

The Matrox 512 graphics cards can be synchronized from an external video source. This is useful in applications where the graphic output will be combined with other video signals. (e.g. broadcasting).

A simple external circuit consisting of six IC's is required for this function (see Fig 8). More detail on this circuit is provided in the Matrox color/grey scale application notes.

5.5 Software Rules

To write into the MTX-512 refresh memory, the CPU simply writes into location Ø. To read, the CPU executes a read cycle at location Ø. However

5.5 Software Rules (continued)

for multiple board systems, additional rules have to be observed when reading or writing into location Ø (data register).

Successive writes into location Ø are not recommended. For example, for single board systems:

```
* WRITE Ø              * WRITE (any instruction which writes into
  WRITE Ø                        memory)
```

is all right, however, for successive writes to multiple boards, it is recommended to insert a single nop or assure in the program that location Ø is not written into successively. Example, multiple board systems:

```
WRITE Ø
NOP
WRITE Ø
```

To read from location Ø for a single board, any read Ø instruction will work. Example:

```
* READ Ø              * READ = any read memory instruction
```

However, to read multiple boards at the same time, a double read has to be executed.

```
READ Ø
READ Ø
```

The requirement to not execute two subsequent writes and to execute two reads is only for multiple board systems where boards are synchronized.

The reason for this is master/slave synchronization of the video boards. Due to variations in delays on different boards for the same read/write operation (propagation of X,Y counters, propagation of address, etc) and the asynchronous nature of the CPU read/write request, some boards will go into read/wirte cycle sooner or later than the master board. These rules assure that the CPU gives enough time for all of the boards to execute the read/write cycle.

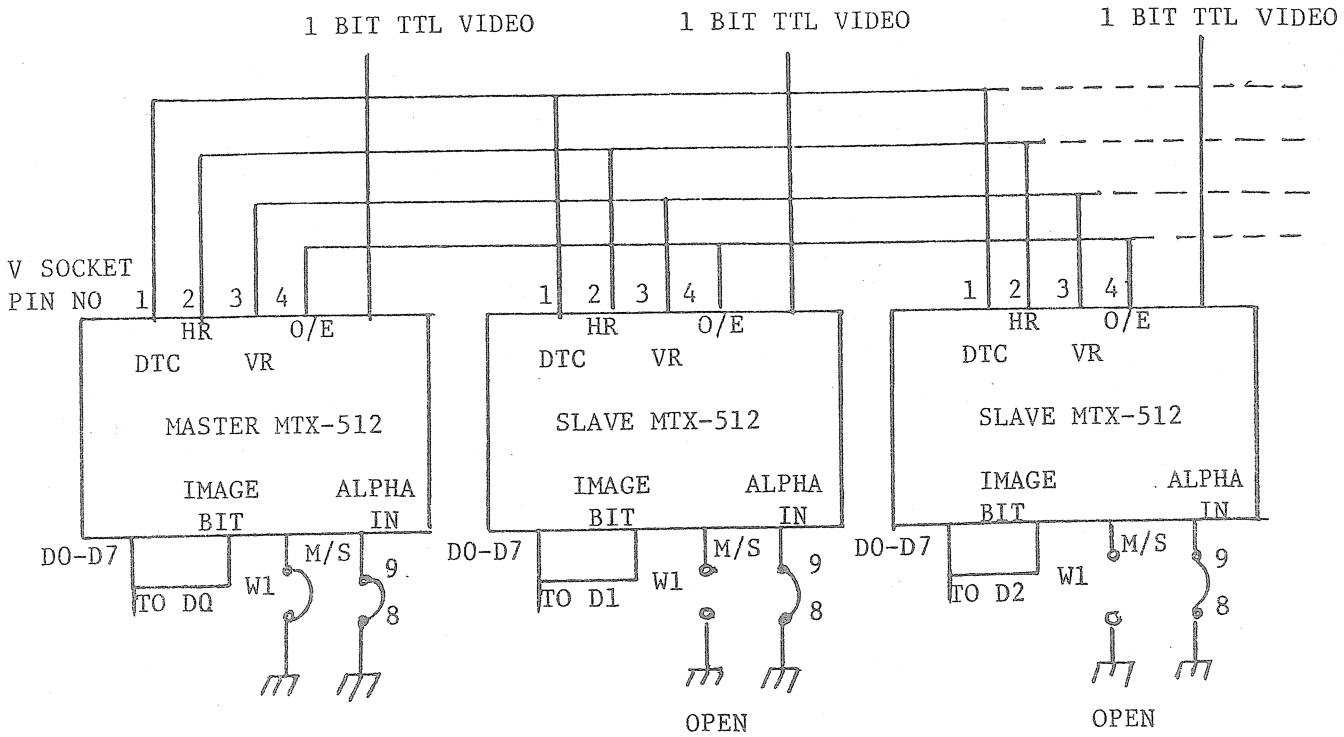
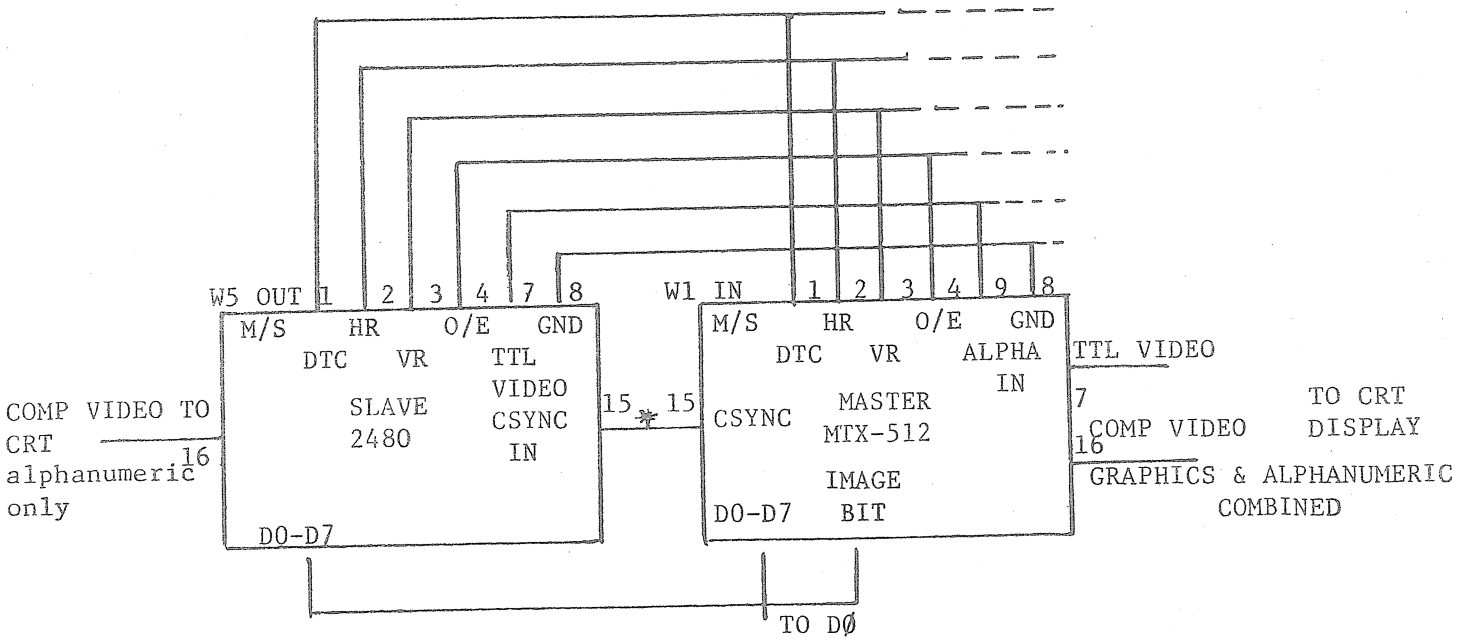
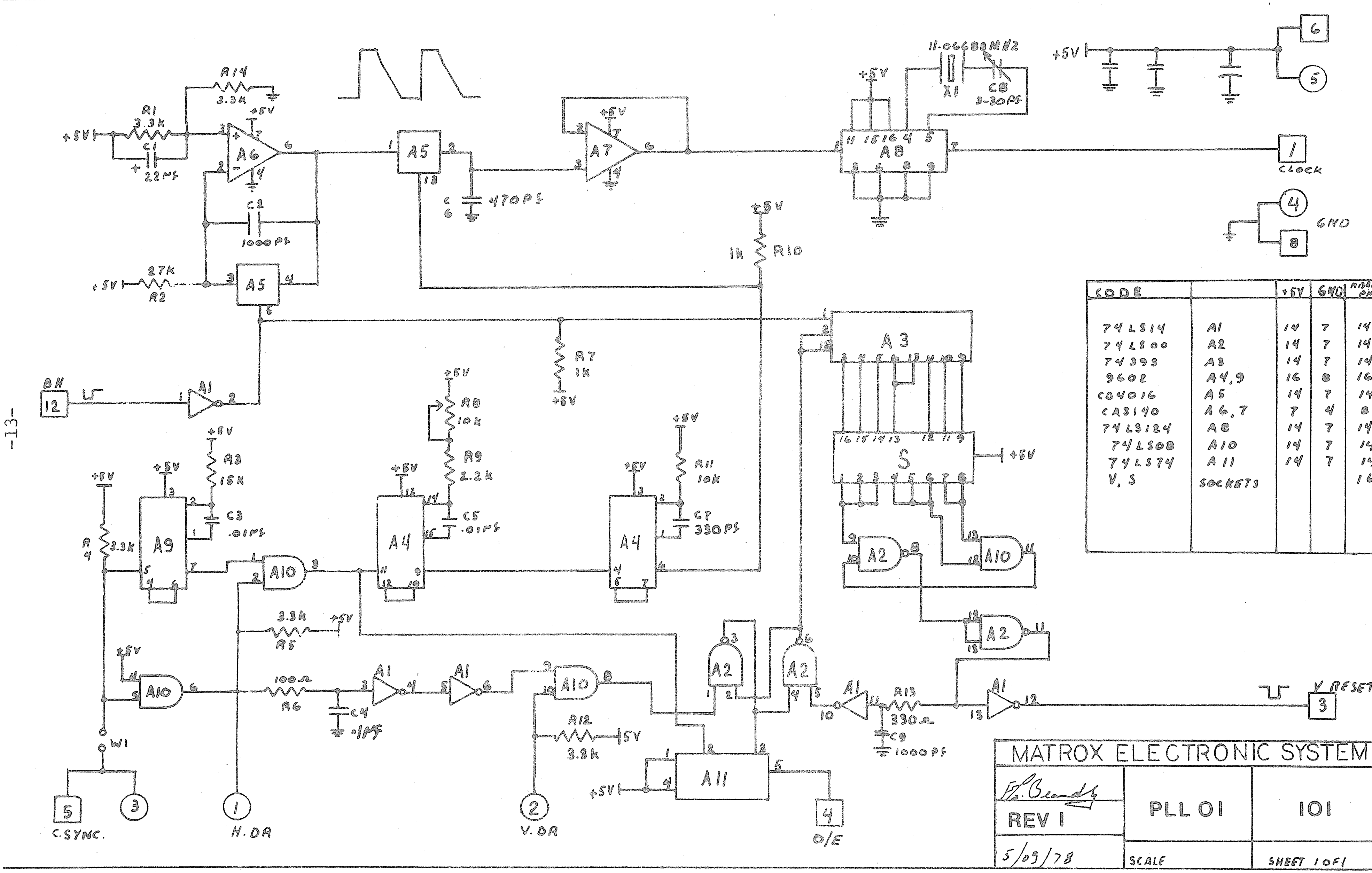


FIG 6 - SLAVING MULTIPLE MTX-512 CARDS FOR COLOR/GREY SCALE APPLICATIONS



* Needed only for separate alphanumeric output from 248Ø

FIG 7 - ADDING 2480 and MTX-512 OUTPUTS FOR A COMBINED ALPHANUMERIC/GRAPHIC DISPLAY



CODE		+5V	GND	[illegible]
74LS14	A1	14	7	14
74LS00	A2	14	7	14
74393	A3	14	7	14
9602	A4,9	16	8	16
CD4016	A5	14	7	14
CA3140	A6,7	7	4	8
74LS124	A8	14	7	14
74LS08	A10	14	7	14
74LS74	A11	14	7	14
V, S	SOCKETS			16

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6.0 RESOLUTION AND TV STANDARD SELECTION

The following table lists all jumpers required on programmable plugs P, R, J. These plugs are used to select either American or European standard operation and also the display resolution. Note (1) designates jumper in, and (0) designates jumper out.

TABLE OF JUMPERS

		AMERICAN STD				EUROPEAN STD			
		256 X 256	512 X 256	512 X 512	256 X 1024	256 X 256	512 X 256	512 X 512	256 X 1024
P	1	1	1	1	1	0	0	0	0
	2	1	1	1	1	0	0	0	0
	3	0	0	0	0	1	1	1	1
	4	0	0	0	0	1	1	1	1
	5	1	1	1	1	0	0	0	0
	6	0	0	0	0	0	0	0	0
	7	0	0	1	0	0	0	1	0
	8	0	0	0	0	0	0	0	0
R	1	0	0	0	0	0	0	0	0
	2	1	*	1	1	1	*	1	1
	3	0	0	0	1	0	0	0	1
	4	1	1	1	0	1	1	1	0
	5	0	1	1	1	0	1	1	1
	6	1	0	0	0	1	0	0	0
	7	0	1	1	1	0	1	1	1
	8	1	0	0	0	1	0	0	0
J	1	1	0	0	0	1	0	0	0
	2	0	1	0	0	0	1	0	0
	3	0	0	1	1	0	0	1	1
	4	0	1	1	1	0	1	1	1
	5	0	0	0	1	0	0	0	1
	6	0	0	1	0	0	0	1	0
	7	1	1	1	1	0	0	0	0
	8	0	0	0	0	1	1	1	1

NOTE: That any standard 16 pin dynamic RAM works in the MTX-512 family.

4K RAM's are used in the 256 X 512 mode.

16K RAM's are used in the 512 X 512 and 256 X 1024 mode.

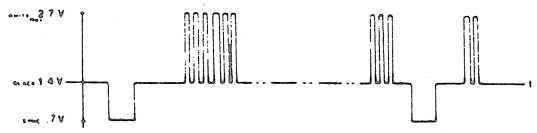
* Jumper in for 8K RAM's market A6L. out for A6H.

Max. Access time for 4K Dynamic RAMS is 1 usec.
Max. access time for 8K and 16K RAMS is 650 nsec.

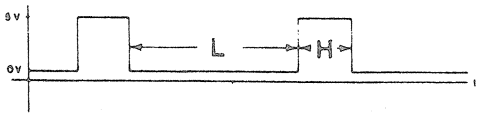
7.0 VIDEO SIGNALS

The following table gives timing information for the video signals which are present on socket V.

VIDEO SIGNALS



Composite video signal. Output impedance 75 Ohms.
Short circuit protection built in. Pin V - 16



Horizontal and Vertical Sync signals

SIGNAL	FREQ.	HIGH	LOW	STD.	V PIN NO.
SH Horizontal Sync	15.8 KHZ	5.67 us	57.6 us	AS	14
	15.8 KHZ	5.67 us	57.6 us	ES	
SV Vertical Sync	60.HZ	190 us	16.47 ms	AS	13
	50.2 HZ	190 us	19.73 ms	ES	
$\overline{BH}$ Blank Horizontal	15.8 KHZ	46 us	17.26 us	AS	12
	15.8 KHZ	46 us	17.26 us	ES	
$\overline{BV}$ Blank Vertical	60 HZ	15.3 ms	1.4 ms	AS	11
	50.2 HZ	16.2 ms	3.7 ms	ES	
DRC Dot Clock	11.06688 MHZ			AS	1
	11.06688 MHZ			ES	

8.0 INTERFACING TO OTHER COMPUTERS

8.1 Introduction

Although the MTX-512 family is available on a number of the industry standard buses, it is still possible to adapt any card in the family to interface to another processor. There are two basic methods of doing this.

8.2 Direct Interface

The first method is to interface the 512 card directly to the processor's bus. The address, data, and control bus of the 512 card must be matched to the cooresponding processor lines. Generally, except for polarity, the address and data buses can be directly connected. The polarity of the MDC, MLSI, and MSBC buses is negative true. The MSBC is available with a positive true bus as a special option. Matching the timing and polarities of control signals such as the read/write strobes requires some design effort.

8.3 Interface to I/O Port

The second method of interfacing a 512 card to another processor is through a standard parallel I/O port. The MDC cards are particularity suitable for this. Fig 9 indicates how this connection is made. Note that the MDC card has negative true logic on all input lines.

Data is transferred to the MDC via I/O lines P0 to P10. The MDC register location is addressed by P11 and P12. P13 true indicates a write operation from the I/O port to the MDC. P13 false indicates a read operation. The STB line should go true when all the above lines are valid. SSYN replies with a true when the MDC card has executed the command. STB then goes false followed by SSYN going false. (See timing diagram, Section 10.4)

8.4 Stand Alone Controller

The various cards in the MTX-512 family are designed to be plug-in compatible with a number of industry standard buses. Combining an MTX-512 card with a CPU and mainframe such as the Intel SBC-80 or DEC LSI-11 allows the user to configure a stand alone intelligent graphics controller. The large range of software and peripheral devices available for these units gives the designer complete freedom to customize his controller. A stand alone controller can be readily interfaced to any computer via parallel or serial ports.

9.0 MAINTENANCE AND WARRENTY

The MTX-512 is a fairly complex card and to understand its operation. requires extensive knowledge of TV scanning, synamic memories and hardware. The complete circuit and assembly schematics are supplied to allow a com-

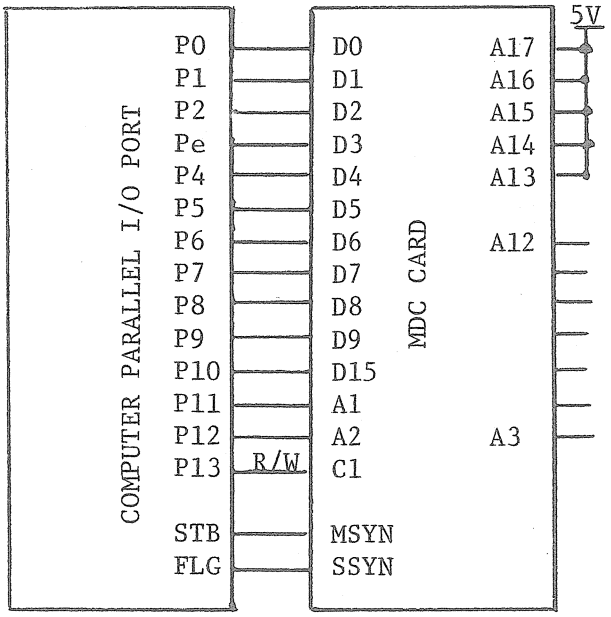


Fig. 9 - INTERFACING MDC CARD TO STANDARD PARALLEL I/O PORT

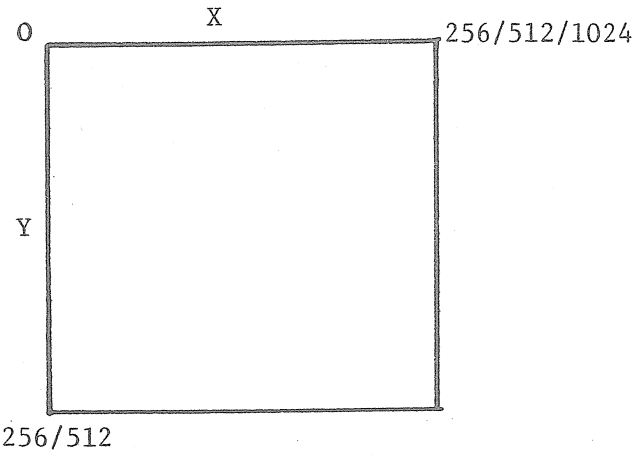


FIG 4 - TV SCREEN X-Y ADDRESSING

9.0 MAINTENANCE AND WARRANTY (continued)

petent user to troubleshoot the board if necessary. However, each board is fully tested, assembled and burned in for 48 hours before shipping to ensure reliability. In case of trouble, a warranty is provided.

Matrox products are warranted against defects in materials and workmanship for a period of three months from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damage.

Non-warranty repairs are billed at a minimum of $50 and according to time and materials required.

10.0 SCHEMATICS TABLES AND OTHER DATA

10.1 Pin Assignment

The following table gives the pin assignments for the MLSI card and a brief definition of the function of each connection.

MLSI CARD I/O SIGNAL SUMMARY

SIGNAL	PIN NO.	DEFINITIONS
BDAL 0	AU2	Data/address lines: the 16 address/data lines are used by the CPU to select the MLSI card. (A unique memory or device register). The master then receives or sends data on these bus lines. Address and data are multiplexed on these lines. Peripheral devices are normally assigned addresses in 28-32K range (160000-177777).
BDAL 1	AV2	
BDAL 2	BE2	
BDAL 3	BF2	
BDAL 4	BH2	
BDAL 5	BJ2	
BDAL 6	BK2	
BDAL 7	BL2	
BDAL 8	BM2	
BDAL 9	BN2	
BDAL 10	BP2	
BDAL 11	BR2	
BDAL 12	BS2	
BDAL 13	BT2	
BDAL 14	BU2	
BDAL 15	BV2	
BSYNC	AJ2	Bus Sync: a control signal asserted by the CPU to indicate that it has placed an address on the BDAL0-15 lines.
BBS7	AP2	Bank Slec
BBS7	AP2	Bank Select 7: The CPU asserts this signal when an address in 28-32K range is placed on the bus. This aignal enables address decoders on the MLSI-11 interface.

10.1 Pin Assignments (continued)

	SIGNAL	PIN NO.	DEFINITIONS
BDIN	BDIN	AH2	Bus Data In: This control signal is asserted by the CPU during a DATA INPUT or read cycle (DATI)
	BDOUT	AE2	Bus Data Out: This control signal is asserted by the CPU during a DATA OUTPUT or write cycle (DATO)
	BRPLY	AF2	Bus Reply: This control signal is asserted by the slave device in response to BDIN or BDOUT. This indicates that the slave has placed its data on the bus or that it has accepted data from the bus.
	BIAK	AM2, AN2 CM2, CN2	Interrupt acknowledge I/O lines are jumpered together to provide continuity for other devices used on the LSI-11 bus.
	BDMG	AR2, AS2 CR2, CS2	DMA I/O lines are jumpered together to provide continuity for other devices used on the LSI-11 bus.
	+12V	BD2	
	+5V	BA2	
	GND	BC2	

10.2 Timing Diagram

The timing diagrams for input/output operations to the MLSI card are given below. The following is a brief functional description of the MLSI-timing. Note that the MLSI-bus uses negative true logic.

DATI or Read Cycle

The CPU asserts the address on the address/data bus (BDAL1-12, and BBSY7). After a delay to allow the address information to settle, the bus sync (BSYNC) signal causes the address information to be latched for the complete duration of the input cycle. Once the address is latched on the MLSI interface, the CPU asserts the bus data in (BDIN) signal. The BDIN signal requests the interface to place data onto the bus. After a delay for access time, the MLSI-11 places valid data in the bus. (BDALØ-15) and then asserts BRPLY. The CPU then negates BDIN, The MLSI-11 removes data from the bus and negates BRPLY. The dropping of BRPLY ends the bus cycle cuasing BSYNC to negate from the CPU.

10.2 Timing Diagram (Continued)

DATO or Write Cycle

Similar to the read cycle, the CPU asserts the address (BDALØ-12, and BBS7) and the bus sync (BSYNC). After the address has been latched on the MLSI-11 interface, the CPU negates the address and asserts bus data out (BDOUT) The BDOUT signal enables the interface to receive data being sent to the BDAL bus from the CPU. When the interface has received the data, it acknowledges with a bus reply (BRPLY) signal. On receipt of BRPLY, the CPU negates the BDOUT. The MLSI-11 responds by negating BRPLY. The dropping of BRPLY ends the bus cycle causing the CPU to negate BSYNC.

Note that all bus outputs from the MLSI cards are open collector drivers. All inputs are high impedance receivers with TTL compatible levels. The bus utilizes negative true logic.

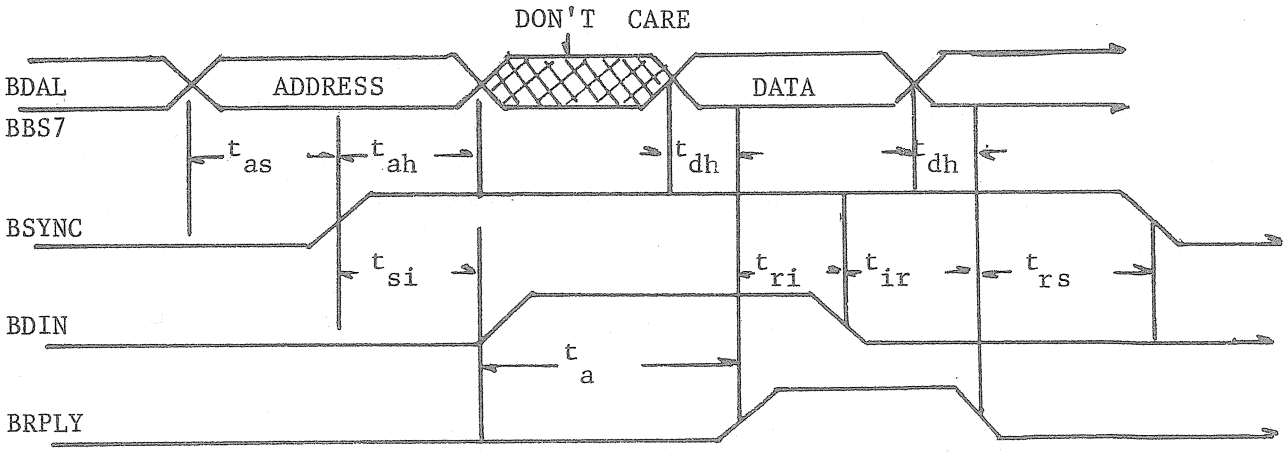


FIG 10 - DATA IN (READ) CYCLE TIMING

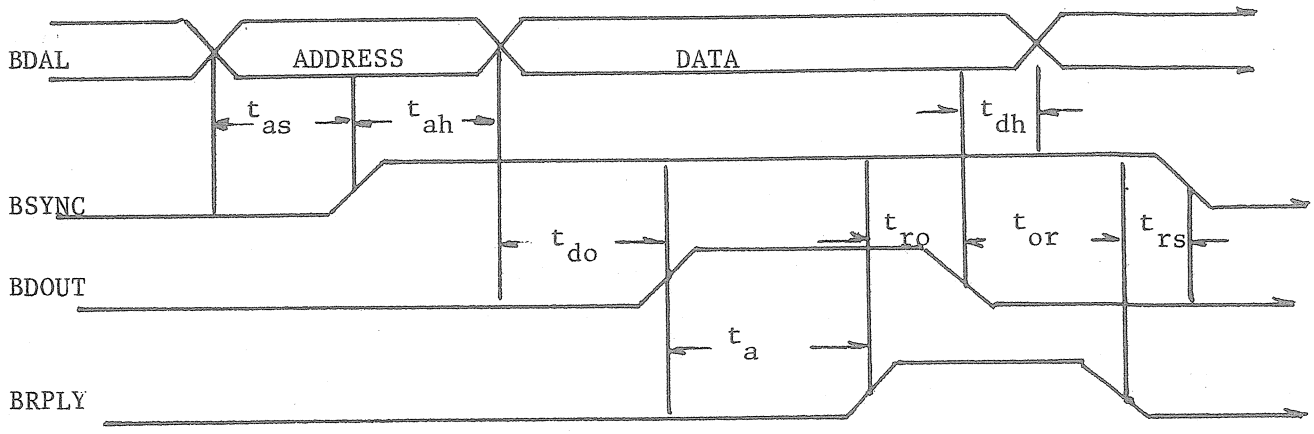


FIG 11 - DATA OUT (WRITE) CYCLE TIMING

10.2 Timing Diagram (continued)

READ CYCLE

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Address set-up	tas	75		ns
Address hold	tah	25		ns
Sync to DIN	tsi	50		ns
Access time	ta		1.4	usec
Reply to DIN	tri	150		ns
DIN to reply	tir	150		ns
Reply to sync	trs	50		ns
Data hold	tdh	150		ns

WRITE CYCLE

Address set-up	tas	75		ns
Address hold	tah	25		ns
Data to DOUT	tdo	25		ns
Access time	ta		1.4	usec
Reply to DOUT	tro	150		ns
DOUT to reply	tor	150		ns
Reply to sync	trs	50		ns
Data hold	tdh	25		ns

10.3 Address Jumpers

The following table is for the location of address jumpers. The jumpers permit the starting location of the MLSI registers to be positioned at the desired location in the CPU address space. A given address line will be decoded as 1 if the jumper is out and 0 if the jumper is in. Address lines A3-A12 are set by jumpers. The top address bits A13, 14, 15 are decoded by the CPU as signal BBS7.

BBS7			A12								A3		A0		
1	1	1	X	X	X	X	X	X	X	X	X	X	0	0	0

Note: AØ is ignored by the MLSI card (used for PDP-11 byte instructions.)
Example: The MLSI-512 is shipped with address jumpered to 160000 octal. (Y1 to Y8, Q7 and Q8 jumpers in).

TABLE OF JUMPER POSITION

ADDRESS LINE	JUMPER SOCKET LOCATION
A3	Y1-16
A4	Y2-15
A5	Y3-14
A6	Y4-13
A7	Y5-12
A8	Y6-11
A9	Y7-10
A10	Y8-9
A11	Q7-10
A12	Q8-9

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10.4 Image Bit Jumpers

As outlined in Section 3 and 5, the image memory bit can be assigned to different data bus bits. This feature simplifies software for color/grey scale imaging systems. The following table is for the assignment of the data bis. For expansion beyond the limits given below, consult the factory.

TABLE OF IMAGE BIT ASSIGNMENT JUMPERS

DATA BIT NUMBER	JUMPER SOCKET LOCATION
0	Q1-16
1	Q2-15
2	Q3-14
3	Q4-13
4	Q5-12
5	Q6-11

11.0 ORDERING INFORMATION

The Matrox 512 family of graphics cards are available in many bus standares, resolutions, and TV standards. The part number is designed to identify the options desired by the user. The prefix identifies the bus standard, the middle portion identifies the resolution, and the suffix identifies the TV standard.

PREFIX:

MDC : Digital Equipment PDP-11 Unibus compatible card.
MLSI: Digital Equipment LSI-11 compatible card.
MSBC: Intel SBC-80 or MDS-80 compatible card.

MIDDLE PORTION:

-256: 256 vertical X 256 horizontal point resolution.
-256-512: 256 vertical X 512 horizontal point resolution.
-512: 512 vertical X 512 horizontal point resolution.
-256-1024: 256 vertical X 1024 horizontal point resolution.

SUFFIX:

-AS: American Standard; -ES: European Standard

an example will illustrate the use of the part number: MLSI-256-512-AS

This card is plug compatible with the DEC LSI-11 bus, has 256 X 512 resolution, and operates with American TV standard monitors.

OTHER PRODUCTS AVAILABLE:

A very low cost 256 X 256 resolution graphics family is also available from Matrox. A compatible family of 24 line X 80 (or 40) character alphanumeric display cards is offered.

11.0 ORDERING INFORMATION (continued)

A complete software package for the MSBC-256 card operated in 256 X 256 resolution mode is available. The software package features point and vector plot, software selectable resolution, alphanumeric generation and animation synchronization. A similar software package for the MDC and MLSI cards will be available in the fourth quarter of '78.

The versatile MTX-512 family can be used in virtually any application where CRT graphics are required. The low cost of the family is a fraction of that of competing systems.

Typical application areas include process control systems, computer aided design, business and educational displays, displays for research applications. curve plotting, medical displays and image processing.

Matrox offers a complete line of alphanumeric and graphic display interfaces for micro and minicomputers. We have a product for almost any application.

12.0 MTX-512 RECOMMENDED MONITOR CHARACTERISTICS

1. MTX-512 series cards operated in 256 X 256 resolution mode can be used with any standard TV monitor.
2. MTX-512 series cards operated in 256 X 512 resolution mode require a monitor with 10 mHz bandwidth for best results. A standard P4 phosphor is acceptable.
3. MTX-512 series cards operated in 512 X 512 resolution mode require a monitor with a 10 mHz bandwidth for best results. A P39 or other high persistance phosphor is recommended to avoid flicker. (512 X 512 resolution uses an interlaced picture, with 30 Hz or 25 Hz refresh rate). Flicker is most noticeable when displaying drawings or graphs with fine lines. Color or grey scale images with larger area features exhibit much less flicker. Satisfactory results can be obtained using standard phosphors when displaying color/grey scale images.
4. MTX-512 series cards operated in 256 X 1024 resolution mode requires a monitor with a 15 mHz bandwidth and 1000 line resolution for best results. A P39 or other high persistance phosphor is recommended to avoid flicker. (See Point 3).

Suitable monitors may be obtained from the following companies:

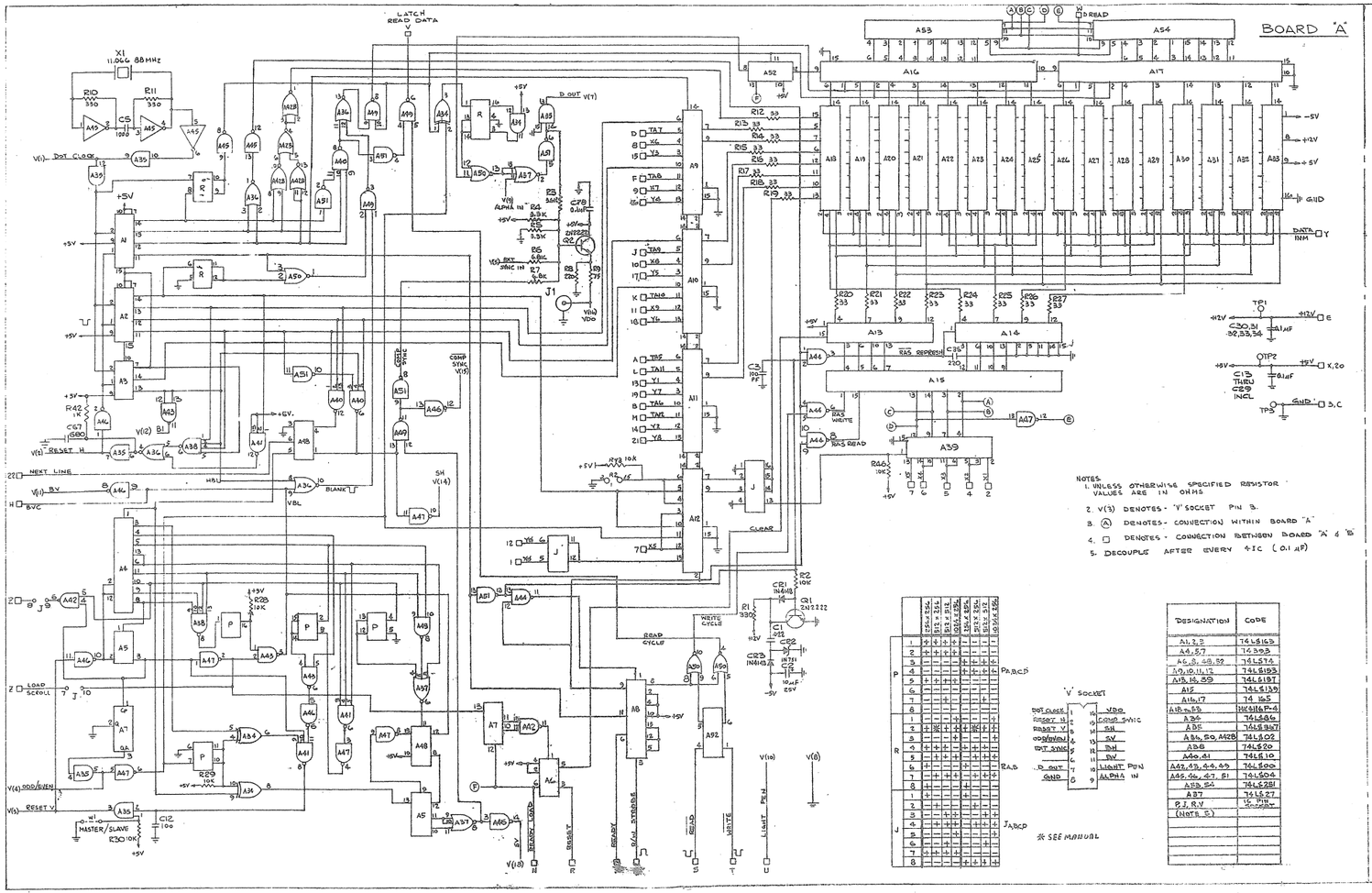
1. Electrohome Limited
   Kitchener, Ontario, Canada
   N2G 4J6
   (519) 744-7111

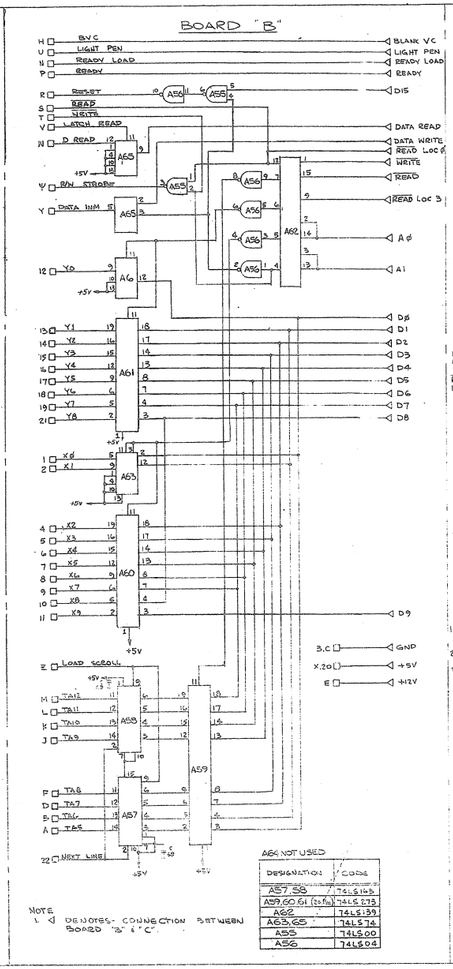
2. Ball Brothers Research Corp.,
   St. Paul. Minnesota 55113
   (612) 622-1742

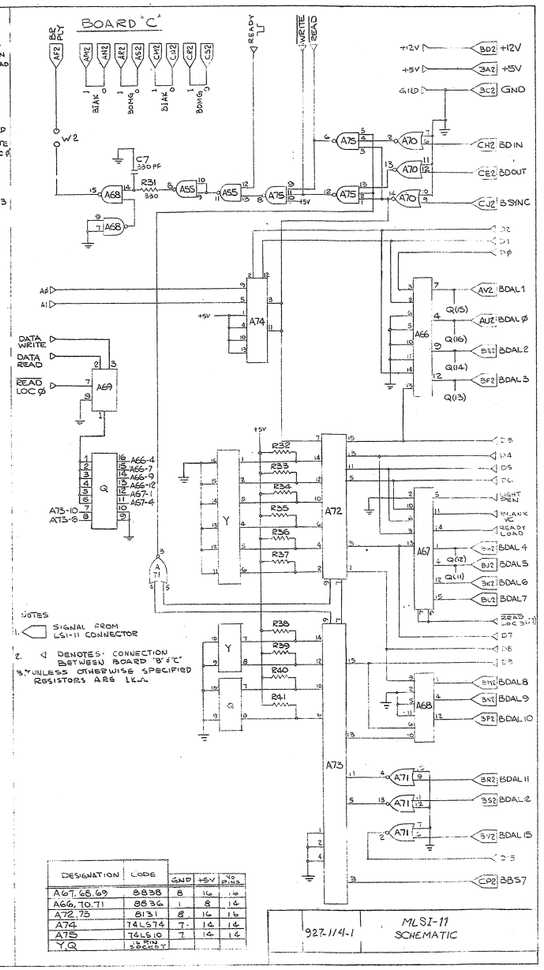
3. CONRAC Corporation, Conrac Div.,
   600 N. Rimsdale Avenue
   Covina, California 91722
   (213) 966-3511

4. Motorola Inc., Display Products
   455 E. North Avenue
   Carol Stream, Illinois 60187
   (312) 690-1400

5. SC. Electronics Incorporated
   530 5th Avenue
   N.W. New Bighton, Minnesota 55112
   (612) 633-3131







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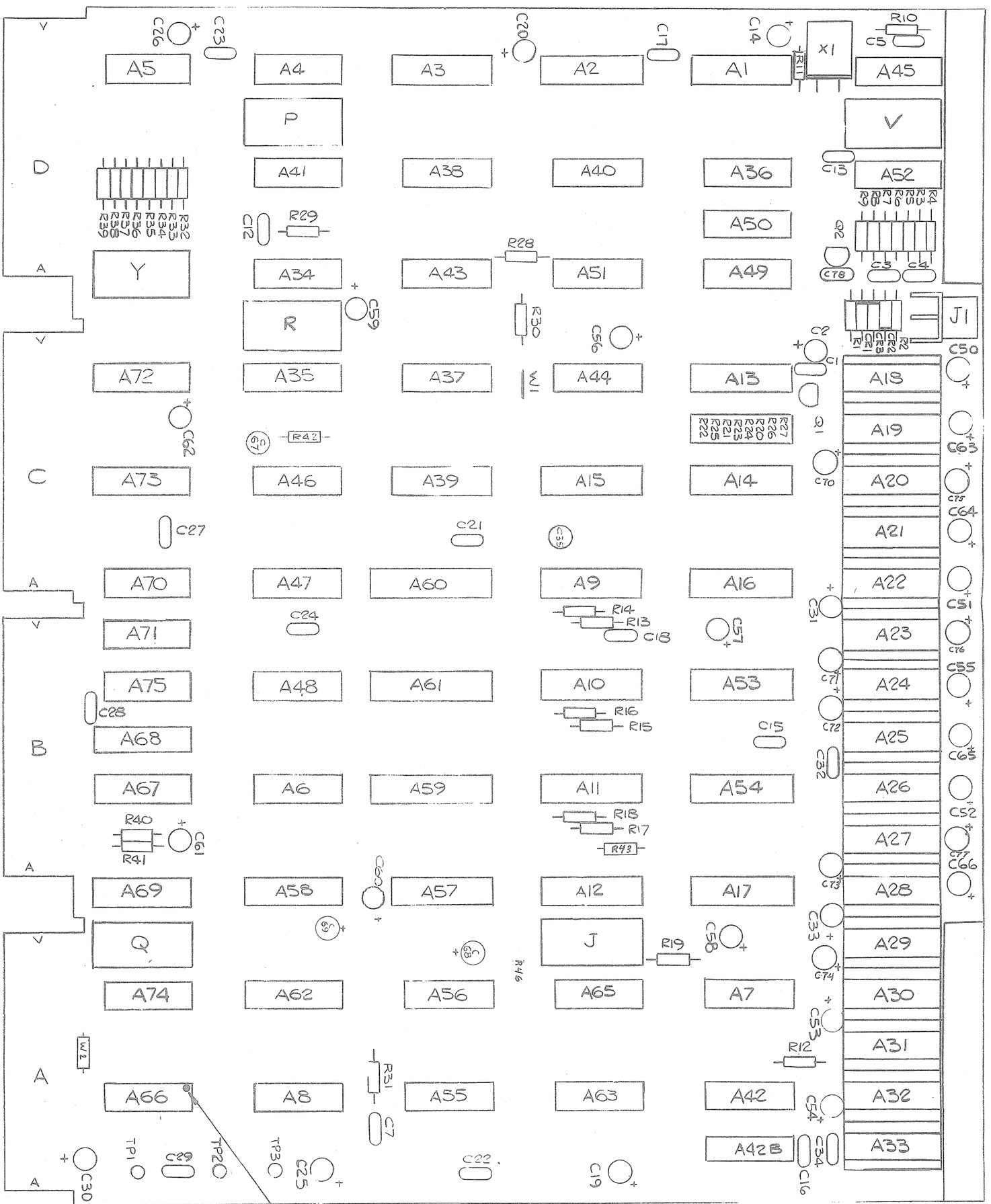
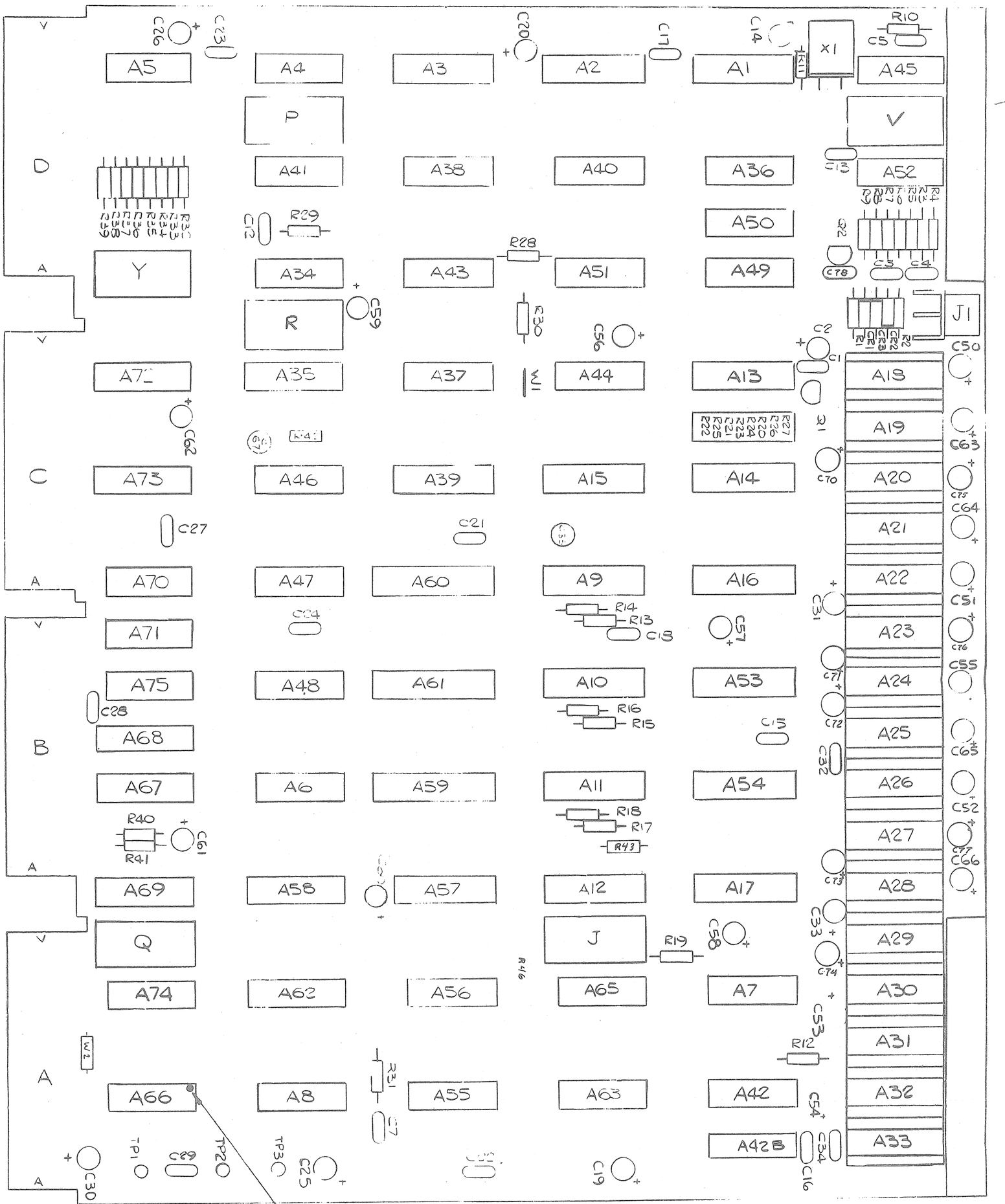
MLSI-11 SCHEMATIC



MLSI-11
COMPONENT
OVERLAY

REV. 1



MLSI-11
COMPONENT
OVERLAY

REV. 2