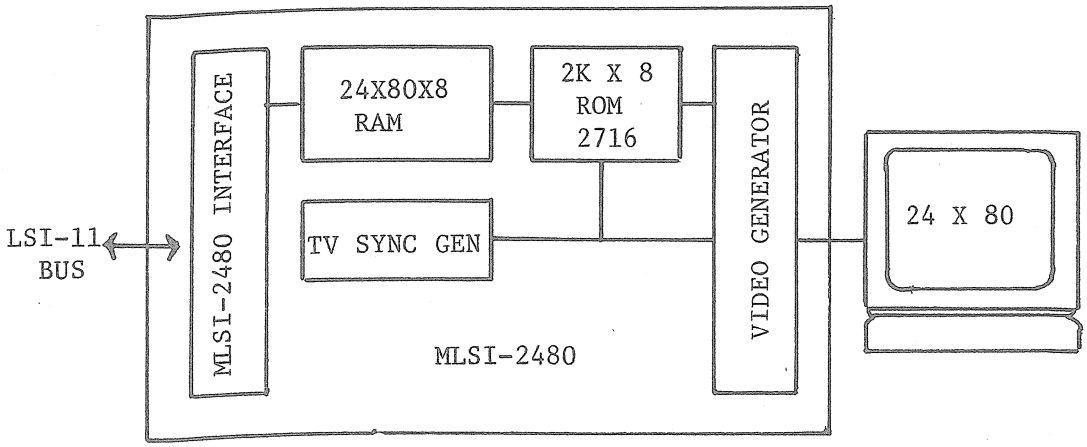
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

MLSI-2480

MTX CRT CONTROLLER — ALPHANUMERIC DISPLAY

* NEW EXCLUSIVE TRANSPARENT MEMORY FEATURE



MLSI-2480 is a unique single board video interface between LSI-11 computer and a TV monitor. This board allows LSI-11 users to add a video display or CRT terminal to their computer at a very low cost. The MLSI-2480 incorporates a revolutionary display memory design which is completely transparent. Alphanumeric video display boards made by virtually all other manufacturers suffer from interference or streaking when the board is accessed. This occurs because the display memory must be accessed by both the computer and sync generator. Standard solutions are to access the card during blanking or to use DMA. Both approaches add complexity and drastically reduce CPU thoughput. The Matrox transparent memory is a revolutionary new solution to this classic problem. It is not necessary to wait for blanks, no DMA is used, the CPU operates at full speed, and there is no streaking on the screen, no matter how often you access the board.

* Plugs directly in LSI-11 bus.
* 24 lines X 80 characters.
* Upper/lower case/graphics.
* Byte mapped (4K X 8)
* Built-in R/W refresh memory
* User programmable character generator (2716 EPROM)
* Full software control
* External/internal sync.
* Normal/inverse control.
* Drives TV monitor directly
* Dual size.
* 800 nsec access time.
* Single +5V, .9A
* Can be combined with MLSI-512 X 512 graphics.

March/79

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LSI-11

SBC-80

SPECIFICATION FOR MLSI-2480 DISPLAY INTERFACE

INTRODUCTION : The MLSI-2480 provides an alphanumeric video interface between an LSI-11 bus microcomputer and a TV monitor. It outputs the industry standard 24 line X 80 character display which is invaluable for professional applications such as intelligent CRT terminals and word processors. The MLSI-2480 is compatible with the MLSI-512 graphics interface permitting a powerful combined alphanumeric/graphics display.

DISPLAY FORMAT : 24 lines X 80 characters each.

ADDRESSING : Matrox VRAM organization. Each character position on the screen is equivalent to a memory location (byte). The content of the memory location (byte) determines the character to be displayed. The card occupies 4K bytes or 2K X 16 RAM address space. On board jumpers permit address positioning.

REFRESH MEMORY : Built-in on the card (2K X 8 RAM). 800 nsec. access. (500 nsec. without transparent memory)

BUS : LSI-11 bus plug-in.

CHARACTER GENERATOR : Upper and Lower case, limited graphics, 128 different characters inside 6 X 10 or 8 X 10 dot matrix. The character generator is a 2K X 8 (2716 EROM) programmed by Matrox. Custom made fonts can be easily incorporated by programming your own 2716 EROM.

CURSOR : Any character can be normal intensity or inverse video under software control.

TV STANDARD : American standard (60 Hz), non-interlaced. European standard (50 Hz) non-interlaced. MLSI-2480 will work with any standard TV monitor or modified TV set (10 mHz bandwidth).

OUTPUTS : Composite video; 75 Ohm, x-tals controlled, TTL video, horizontal and vertical sync and blank outputs.

REMOTE DISPLAY : 75 Ohm cable, up to 500 feet, multiple monitors up to 10 TV's.

GRAPHICS : Limited graphics capability built-in. For full graphics, add a graphics MLSI-512 board. Both boards can be synchronized together by a simple 6 wire connection.

DIMENSIONS : Standard LSI-11 card size (dual size). Will also fit LSI-11/2 card size.

DOCUMENTATION : 12 page manual, complete description, schematics.

WARRANTY : 90 days parts and labor.

DELIVERY : 2 to 4 weeks ARO

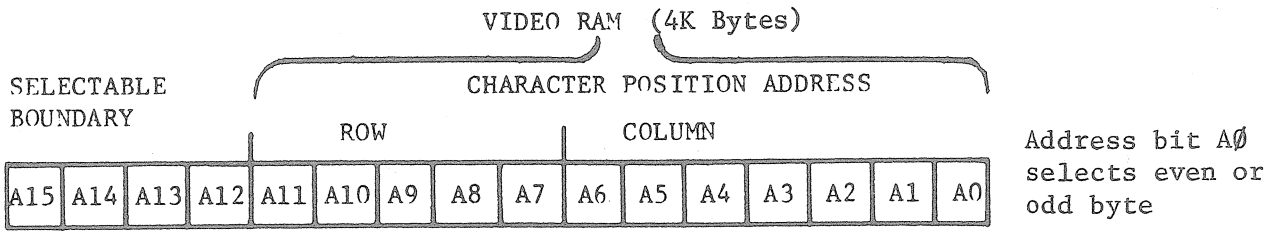
ORDERING : Available directly from Matrox Electronics Systems Limited, Montreal, Quebec

1.0 FUNCTIONAL DESCRIPTION

To the LSI-11 CPU, an MLSI-2480 looks like a byte organized static random access memory. Each character position on the screen is equivalent to a memory location. Byte instructions can be used to read or write to the MLSI-2480 the same way as any other RAM in the CPU address space. The MLSI-2480 will respond to word instructions, but only the even numbered byte which matches the word address will be accessed.

This Matrox video RAM organization allows the programmer to use all LSI-11 byte instructions to manipulate data on the display. This powerful feature can significantly simplify display drivers and save valuable CPU time.

The MLSI-2480 has a special organization designed to minimize on board memory while simplifying software. Figure 1 shows this organization. Address lines A0-A6 are for column addressing, A7-A11 are for row addressing. A12-A15 are the jumper programmable address boundary. The 12 address lines (A0-A11) of the MLSI-2480 occupy a block of 4K bytes or 2K words of memory space. Note that only 2K bytes of active memory are used in the VRAM. The seven lines (A0-A6) used for column addressing could theoretically address 128 locations. Only the first 80 column locations contain active memory. Column addresses 80-127 should not be accessed. Similarly, row address 24-31 should not be accessed. Note that the separate row and column address lines make it easier to calculate the address of a particular location on the screen. Reading or writing data to the illegal VRAM addresses may result in erroneous data being display on the screen.



NOTE: Column addresses 80-127 and row addresses 24-31 are illegal addresses for the VRAM.

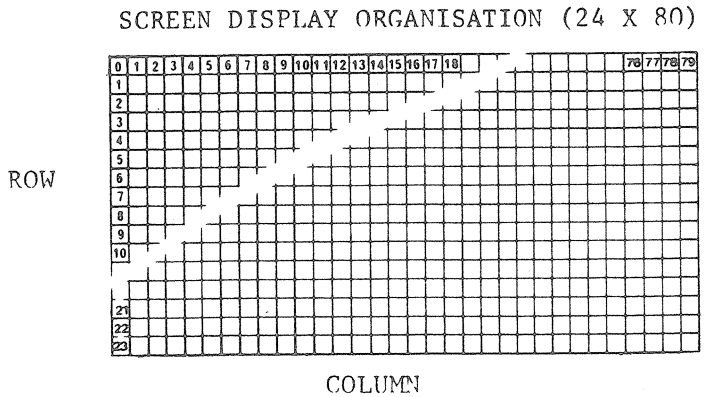


FIG. 1 ADDRESSING THE MLSI-2480 FOR A 24 X 80 ORGANIZATION

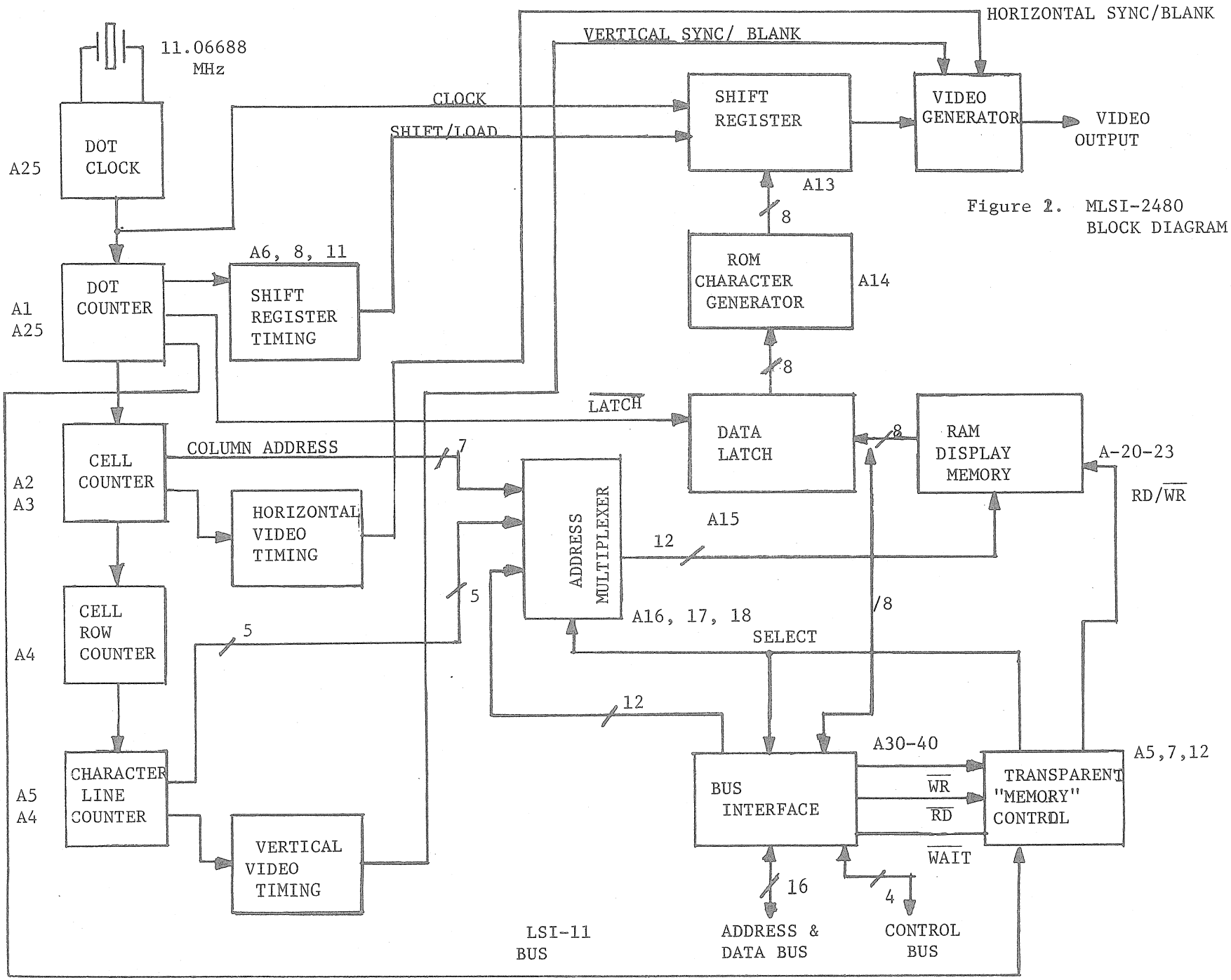


Figure 2. MLSI-2480
BLOCK DIAGRAM

2.0 THEORY OF OPERATION

The MLSI-2480 has four major blocks: The TV sync generator, scanning circuitry, video generator and interface and refresh memory. The sync generator is formed of X-tal oscillator A25 and a divider chain A1, 2, 3, 4, 5. This divider chain produces all timing signals for the memory scanning as well as horizontal and vertical sync. The TV sync generator can be programmed for the European or American Tv standard.

The scanning circuitry consists of multiplexers A16, 17, 18 and address stearing logic A19, 24, 29.

The video generator consists of an EPROM character generator A14, shift register A13 and associated electronics A7, 12, 28.

Horizontal sync is decoded at the output of A10-6 and vertical sync is decoded at the output of A28-3.

The refresh memory A20-23 consists of 4 4K RAM's (2114's) which are organized as a 4K X 8 RAM. However, since the 24 X 80 display uses 1920 locations, only 2K X 8 of RAM is used. The remaining locations (columns from 80 to 127 and rows from 24 to 31) are empty. Stearing logic A19, 24, 29 maps the 4K input address lines to 2K memory.
The interlaced circuitry consists of A5, A7 and A42.

3.0 PROGRAMMABLE OPTIONS

The MLSI-2480 can be user programmed (by jumpers) for several configurations. The following parameters are user programmable:

3.1 Address Mapping

The MLSI-2480 occupies 2K of word locations (4K X 8 bytes). This 2K can be positioned anywhere in the address space by selecting chip select lines. This is done by decoding A12-A15 address lines. (socket S1).

ADDRESS BIT	JUMPER ACROSS (for Ø)	JUMPER ACROSS (for 1)
A12	8-9	7-10
A13	6-11	5-12
A14	4-13	3-14
A15	2-15	1-16

3.2 TV Standard

The MLSI-2480 can be programmed for American standard (60 Hz) refresh rate or European standard (50 Hz) by jumpers (socket S3, 20 pin). No x-tal change is required.

Jumpers in: (S3)

American Standard: 1-20; 3-18; 6-15; 8-13; 10-11; (E Std. jumpers out)
European Standard: 2-19; 4-17; 5-16; 7-14; 9-12; (A Std. jumpers out)

3.3 EPROM Character Generator

The Matrox MLSI-2480 uses an EPROM character generator. This permits easy modifications of the character set. Following is information that permits the user to custom program his own character font.

The MLSI-2480 divides up the screen into an array of 24 lines by 80 characters (see Fig. 1). Each character position is called a cell and is itself composed of a dot matrix. The MLSI-2480 can have either a 6 X 10 or 8 X 10 dot matrix. The contents of the dot matrix are programmed into the character generator EPROM. Figure 3 shows an example of the character cell dot matrix for the letter B. The 8 EPROM data outputs contain a horizontal slice through the characters. The EPROM address lines are divided into two groups: four lines are used for row selection, seven lines are used for selecting one of 128 characters.

The standard character generator supplied with the MLSI-2480 contains the full ASCII alphabet plus lower case characters, and 32 special graphics characters. The font is designed for a 6 X 10 cell. Row Ø is normally blank to allow for a vertical space between lines of characters. Rows 8 and 9 are for the descenders of lower case characters. Output Ø8 is normally blank to allow for intercharacter spacing along a line. Outputs 1 and 2 are not visible when the MLSI-2480 is set up for a 6 X 10 cell. Note that the graphic characters utilize all dots including those normally reserved for spaces to allow for drawing continuous lines.

For cell size, selection jumpers are (S4 socket)

A: 6 X 10 cell jumpers (socket S4) 8-11; 6-13; 2-17; wire jumper W3 (8 X 10 cell jumpers out); X-tal is 11.06688 mHz.

B: 8 X 10 cell jumpers (socket S4) 9-10; 7-12; 1-18; wire jumper W2 (6 X 10 cell jumpers out); X-tal is 14.75584 mHz.

EPROM PIN ASSIGNMENT

PIN		FUNCTION	
01	9	Character outputs which form a horizontal slice through the character.	
02	10		
03	11		
04	13		
05	14		
06	15		
07	16		
08	17		
A0	8	Row select 0	Select one of 10 horizontal slices through character cell.
A1	7	Row select 1	
A2	6	Row select 2	
A10	T120/Intel 19	Row select 3	
A3	5	D0 LSB	Selects one of 128 characters from the character generator. These lines are connected to the data bus lines indicated.
A4	4	D1 LSB	
A5	3	D2 LSB	
A6	2	D3 LSB	
A7	1	D4 LSB	
A8	23	D5 LSB	
A9	22	D6 LSB	

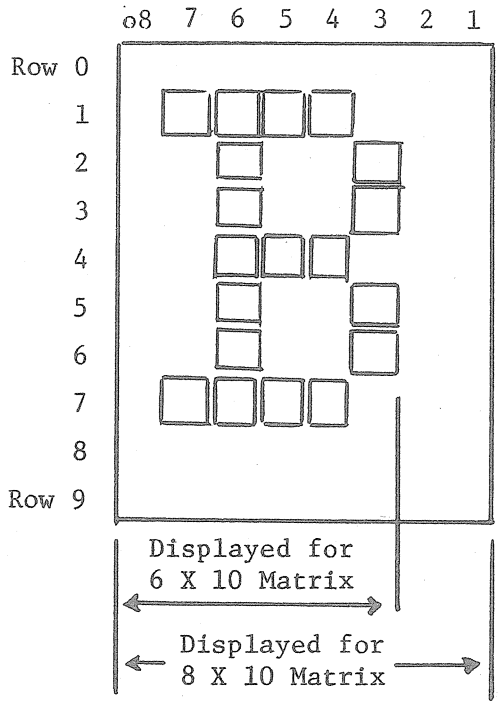
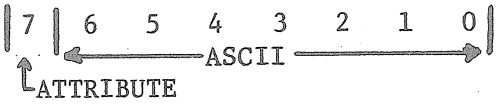


Fig. 2

7 BIT CODE FOR LETTER "B" IS 1000010

Figure 3

Display Data Bus Format



128 ASCII set

Attribute bit: Specifies if the character is normal or inverse.

	(S4 jumpers	(+ = in)
128 ASCII set (D7 disabled display always normal	4	5
display always normal		+
128 ASCII set (D7 = 0 normal, 1 inverse)	+	

Interlaced Memory

This mode can be enabled or disabled by the two jumpers W4 and W5.
Interlaced memory W5 on, W4 out (use fast memories 2114-2)
Non-interlaced memory W4 on, W5 out (use normal 2114 memories.

MATROX PROGRAMMED CHARACTER GENERATOR (MCH-001)

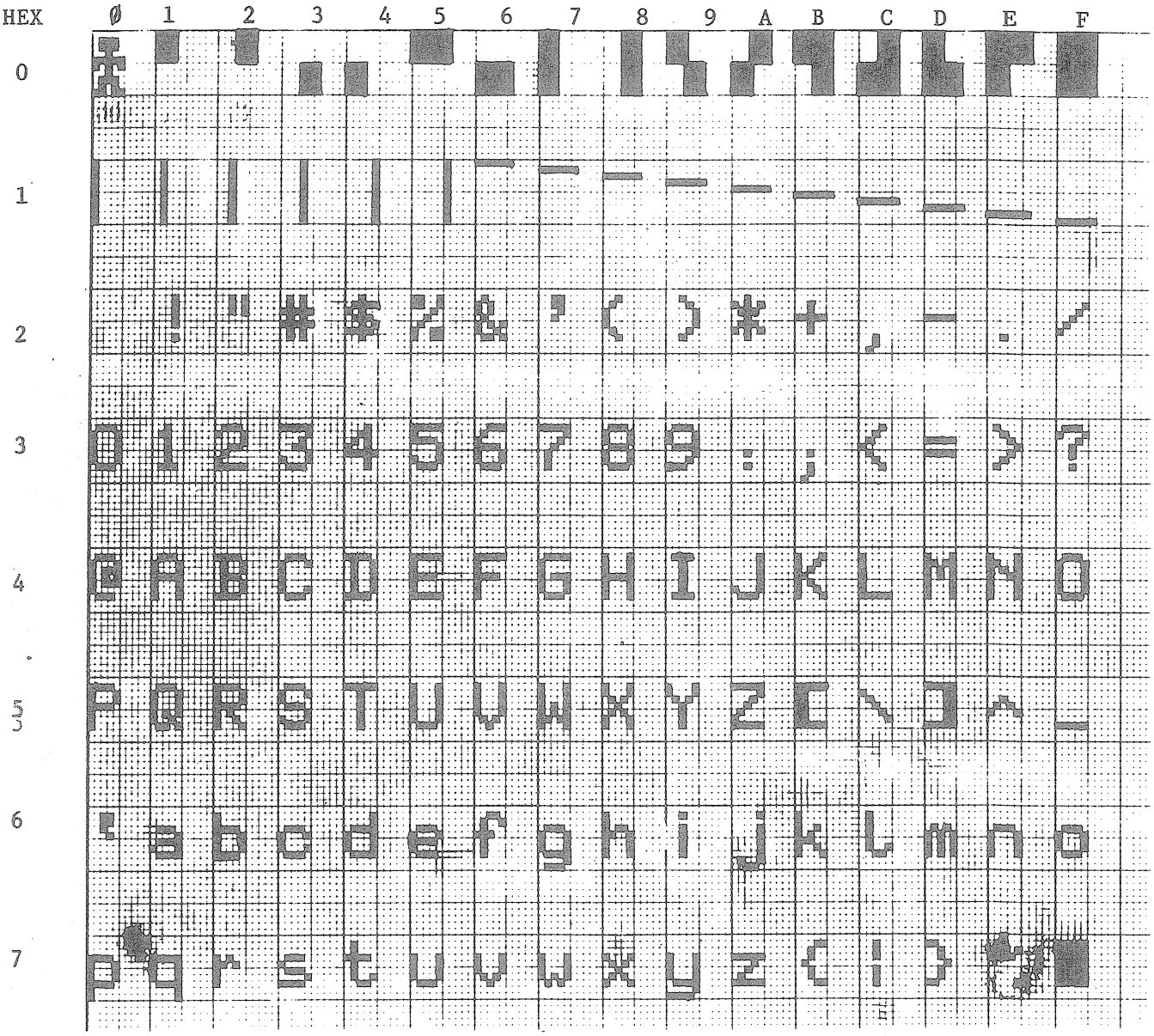
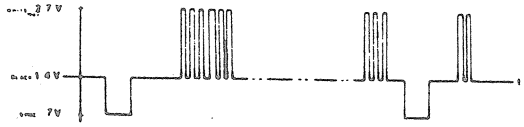


Figure 4

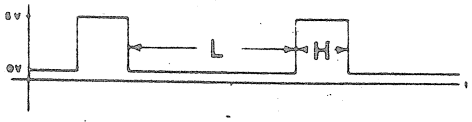
4.0 VIDEO SIGNALS (S2 Socket)

The following table gives timing information for the video signals which are present on Socket S2.

VIDEO SIGNALS



Composite video signal. Output impedance 75 Ohms.
Short circuit protection built in. Pin V - 16



Horizontal and Vertical Sync signals.

Table 1

SIGNAL	FREQ.	HIGH	LOW	STD.	S2 PIN NO.
SH Horizontal Sync	15.8 KHZ	4.3 us	59 us	AS	14
	15.8 KHZ	4.3 us	59 us	ES	
SV Vertical Sync	60 HZ	255 us	16.4 ms	AS	13
	50.2 HZ	255 us	19.7 ms	ES	
$\overline{BH}$ Blank Horizontal	15.8 KHZ	43 us	20 us	AS	12
	15.8 KHZ	43 us	20 us	ES	
$\overline{BV}$ Blank Vertical	60 HZ	1.4 ms	15.3 ms	AS	11
	50.2 HZ	4.7 ms	15.2 ms	ES	
DRC Dot Clock	11.06688 MHZ			AS	1
	11.06688 MHZ			ES	

* For 14.755 mHz timing is same.

4.1 Pinouts for S4 Video Expansion Socket

PIN	NAME	DESCRIPTION
1	DTC	Dot clock (bi-directional)
2	HR	Horizontal reset (bi-directional)
3	VR	Vertical reset (bi-directional)
4		
5	CSYNC	Composite sync
6	+5V	
7		
8	GND	Ground
9	LVID	Logic video (TTL level)
10		
11	VB	Vertical blank
12	HB	Horizontal blank
13	SV	Vertical sync
14	SH	Horizontal sync
15	ES	External Sync
16	CVDO	Composite video

5.0 COMBINING MLSI-2480 AND MLSI-512 GRAPHICS BOARDS

Alphanumeric video can be mixed with graphics video generated by MLSI-512 boards. (any resolution MLSI graphics boards can be used).

The MLSI-512 is configured as a master board (jumper W1 connected) and bi-directional signals. (DTC, H reset, V reset, and O/E) from MLSI-512 are driving slave MLSI-512 boards and the MLSI-2480 board. (Up to 24 graphics boards can be slaved).

COMBINING MLSI-2480 WITH MLSI-512

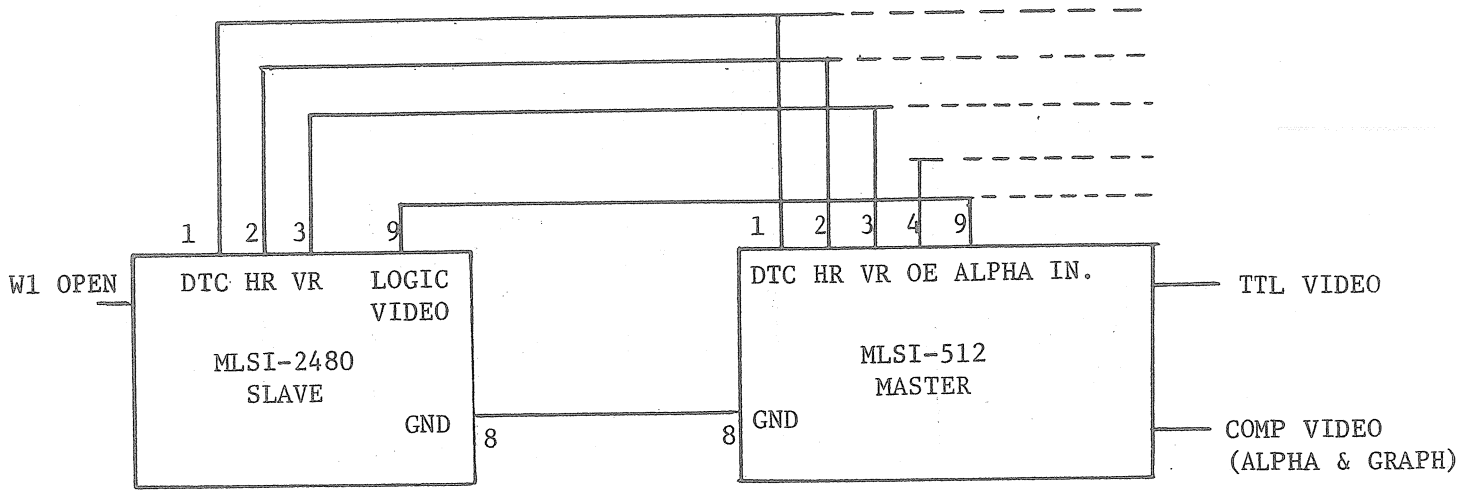


Figure 5

6.0 EXTERNAL SYNC MODE

The MLSI-2480 can be synchronized to external sync source such as a TV camera or master sync generator in a TV studio for video mixing or similar.

This is accomplished by forcing MLSI-2480 in slave mode and adding PLL-01 module. (Can be ordered from Matrox). PLL-01 is a phase lock loop which will lock on external sync source and generate dot clock and vertical reset for MLSI-2480.

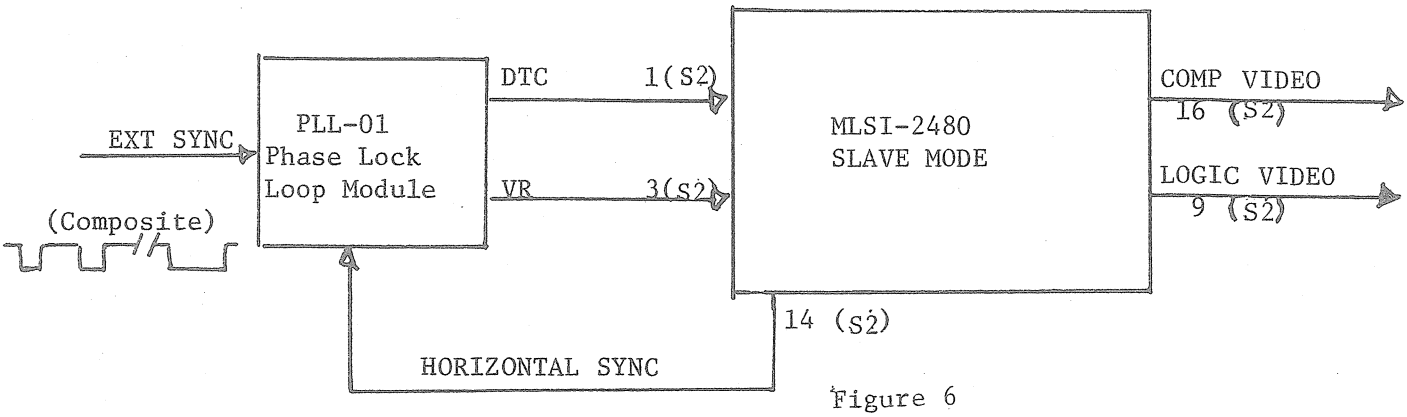


Figure 6

The MLSI-2480 is forced to slave mode by taking our jumper W1, shorting together pins 4 of A37 and 1 of A3 and cutting pin 8 of A25.

7.0 MAINTENANCE AND WARRENTY

The MLSI-2480 is a fairly complex card and to understand its operation requires extensive knowledge of TV scanning, static memories and hardware. The complete circuit and assembly schematics are supplied to allow a competent user to trouble-shoot the board if necessary. However, each board is fully tested, assembled, and burned in for 48 hours before shipping to ensure reliability. In case of trouble, a warranty is provided.

Matrox products are warranted against defects in materials and workmanship for a period of three months from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damage.

Non-warranty repairs are billed at a minimum of $50 and according to time and materials required.

8.0 SCHEMATICS TABLES AND OTHER DATA

8.1 Pin Assignement Table MLSI-2480

The following table gives the pin assignments for the MLSI card and a brief definition of the function of each connection.

8.1 Pin Assignment Table MLSI-2480

MLSI-2480 CARD I/O SIGNAL SUMMARY

SIGNAL	PIN NO.	DEFINITION
BDAL 0	AU2	Data/address lines: The 16 address/data lines are used by the CPU to select the MLSI card. (A unique memory or device register). The master then receives or sends data on these bus lines. Address and data are multiplexed on these lines. Peripheral devices are normally assigned addresses in 28-32K range (160000-177777).
BDAL 1	AV2	
BDAL 2	BE2	
BDAL 3	BF2	
BDAL 4	BH2	
BDAL 5	BJ2	
BDAL 6	BK2	
BDAL 7	BL2	
BDAL 8	BM2	
BDAL 9	BN2	
BDAL 10	BP2	
BDAL 11	BR2	
BDAL 12	BS2	
BDAL 13	BT2	
BDAL 14	BU2	
BDAL 15	BV2	
BSYNC	AJ2	Bus Sync: A control signal asserted by the CPU to indicate that it has placed an address on the BDALO-15 lines.
BBS7	AP2	Bank Select 7: The CPU asserts this signal when an address in 28-32K range is placed on the bus. This signal enables address decoders on the MLSI-512 interface. It is not used on MLSI-2480.
BDIN	AH2	Bus Data In: This control signal is asserted by the CPU during a DATA INPUT or read cycle (DATI)
BDOUT	AE2	Bus Data Out: This control signal is asserted by the CPU during a DATA OUT PUT or write cycle (DATO)
BRPLY	AF2	Bus Reply: This control signal is asserted by the slave device in response to BDIN or BDOUT. This indicates that the slave has placed its data on the bus or that it has accepted data from the bus.
BIAK	AM2, AN2	Interrupt acknowledge I/O lines are jumpered together to provide continuity for other devices used on the LSI-11 bus.
BDGM	AR2, AS2	DMA I/O lines are jumpered together to provide continuity for other devices used on the LSI-11 bus.

8.1 Pin Assignments (Continued)

SIGNAL	PIN NO.	DEFINITION
+12V	BD2	
+5V	BA2	
GND	BC2	

8.2 Timing Diagram

The timing diagrams for input/output operations to the MLSI card are given below. The following is a brief functional description of the MLSI timing. Note that the MLSI bus uses negative true logic.

DATI or Read Cycle

The CPU asserts the address on the address/data bus (BDALØ-15). After a delay to allow the address information to settle, the bus sync (BSYNC) signal causes the address information to be latched for the complete duration of the input cycle. Once the address is latched on the MLSI interface, the CPU asserts the bus data in (BDIN) signal. The BDIN signal requests the interface to place data onto the bus. After a delay for access time, the MLSI-11 placed valid data in the bus. (BDALØ-15) and then asserts BRPLY. The CPU then negates BDIN. The MLSI-11 removes data from the bus and negates BRPLY. The dropping of BRPLY ends the bus cycle causing BSYNC to negate from the CPU.

DATO or Write Cycle

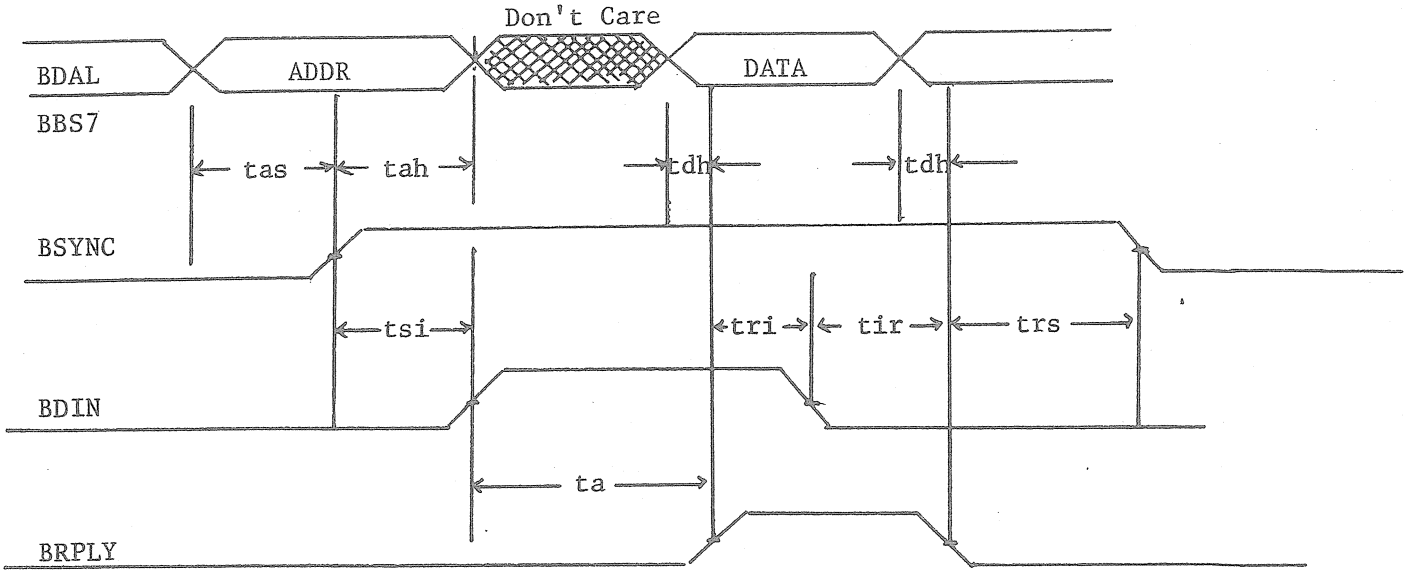
Similar to the read cycle, the CPU asserts the address (BDALØ-15) and the bus sync (BSYNC). After the address has been latched on the MLSI-11 interface, the CPU negates the address and asserts bus data out (BDOUT). The BDOUT signal enables the interface to receive data being sent to the BDAL bus from the CPU. When the interface has received the data, it acknowledges with a bus reply. (BRPLY) signal. On receipt of BRPLY, the CPU negates the BDOUT. The MLSI-11 responds by negating BRPLY. The dropping of BRPLY ends the bus cycle causing the CPU to negate BSYNC.

Note that all bus outputs from the MLSI cards are open collector drivers. All inputs are high impedance receivers with TTL compatible levels. The bus utilizes negative true logic.

READ CYCLE

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Address setup	tas	75		ns
Address hold	tah	25		ns
Sync to DIN	tsi	50		ns
Access Time	ta		500	ns
Reply to DIN	tri	150		ns
DIN to reply	tir	150		ns
Reply to sync	trs	50		ns
Data hold	tdh	150		ns

DATA IN (READ) CYCLE



DATA OUT (WRITE) CYCLE

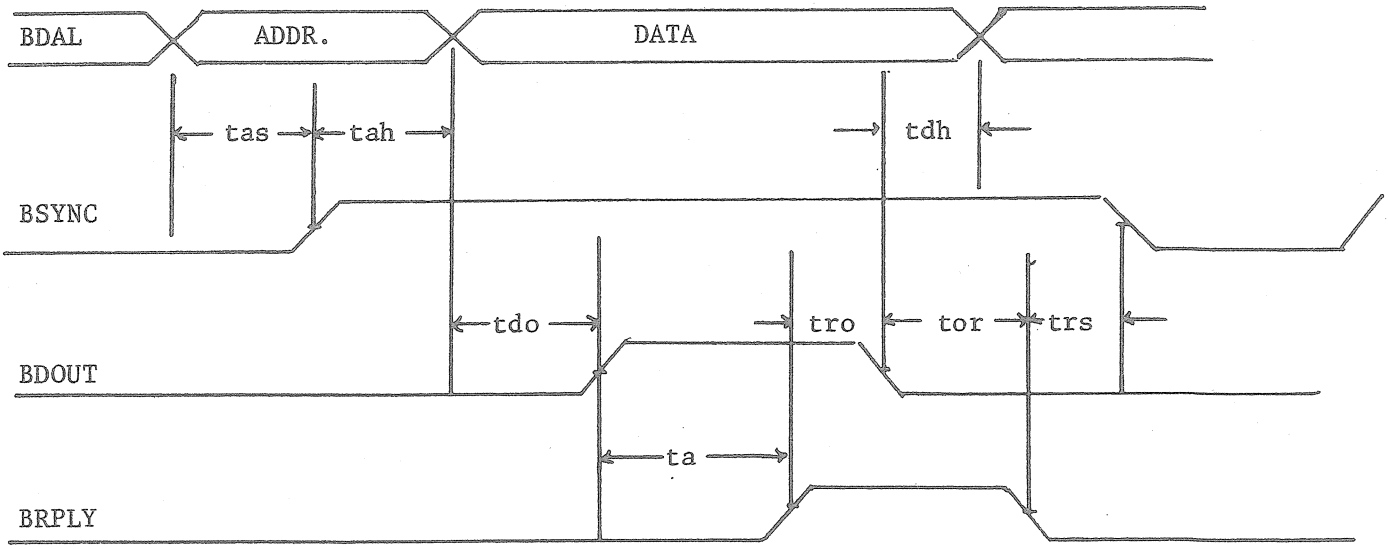


Figure 7

WRITE CYCLE

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNIT
Address Setup	tas	75		ns
Address hold	tah	25		ns
Data to DOUT	tdo	25		ns
Access Time	ta		500	ns
Reply to DOUT	tro	150		ns
DOUT to reply	tor	150		ns
Reply to sync	trs	50		ns
Data hold	tdh	25		ns

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

MTX-512

MTX TV CRT CONTROLLER FAMILY

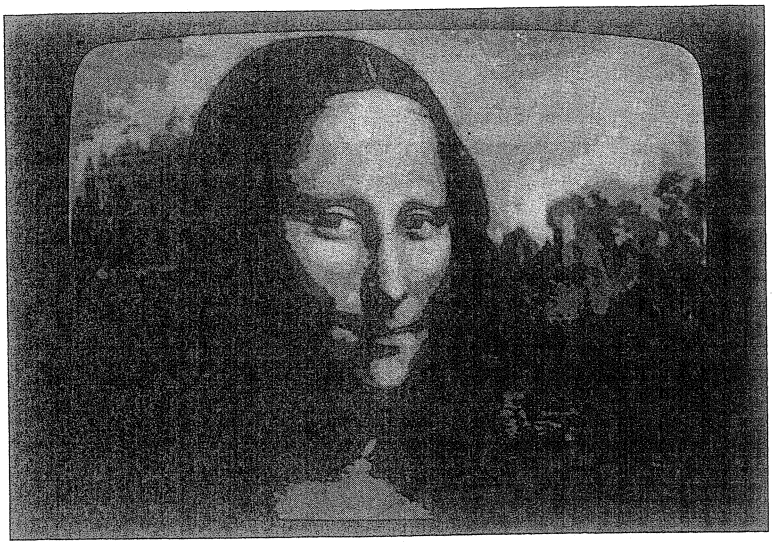
GRAPHIC DISPLAY

INTRODUCTION

The MTX-512 graphics family incorporates the revolutionary new concept of variable resolution graphics on a single controller card. The family of cards is designed to interface a mini or microcomputer to a TV type monitor and produce a graphics raster with selectable resolution. Any card in the MTX-512 family can be user programmed to produce a dot matrix of 256 X 256; 256 X 512; 512 X 512; or 256 X 1024 points. The family consists of a series of cards which are plug compatible with industry standard buses. These include the DEC PDP-11, LSI-11 and Intel SBC-80 buses. All cards in the family can be readily interfaced to other mini/microcomputers. Stand alone controllers can be configured by combining MTX-512 series cards and Intel or DEC card cages.

FEATURES:

- Resolutions of 256 X 256; 256 X 512; 512 X 512; 256 X 1024 points.
- Multiple cards stackable for color/grey scale applications.
- Single command image memory erase.
- Image memory can be read back.
- Vertical scroll built into hardware.
- Can be used as intelligent stand alone graphic controller.
- American/European TV standard operation field programmable.
- Compatible 24 line X 80 character display available.
- Can be synchronized to external sync generator.
- Powerful X-Y addressing technique.



BLOCK DIAGRAM

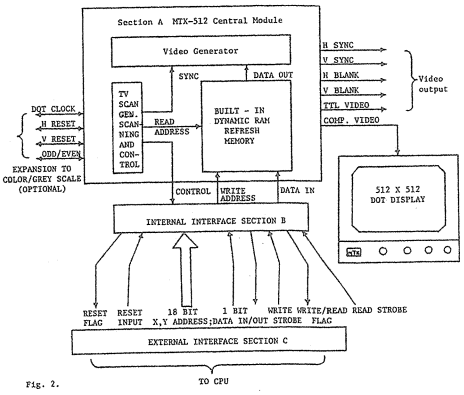


Fig. 2.

1.0 MTX-512 FAMILY TECHNICAL SPECIFICATION

Nominal Resolution:	256 Vertical X 256 Horizontal; 256 X 512; 512 X 512; and 256 X 1024 factory or field programmable. Note that on American Standard card, the number of displayed lines is reduced. The actual resolutions displayed are 240 X 256; 240 X 512; 480 X 512; and 240 X 1024.
Write Time:	Dot write time 1.4 usec. max.
Erase:	Single instruction erases screen; 48 msec. max.
Scroll:	Built-in scroll register allows display to be shifted vertically with one line resolution.
Read/Write:	Image memory is fully read/write addressable.
Dimensions:	PC board $7\frac{3}{4}$ X $10\frac{1}{2}$ inches (MDC and MLSI), or 12 X $6\frac{1}{4}$ inches (MSBC).
Power:	+5V 800mA, +15/12V 200mA.
Outputs:	75 Ohm composite video, TTL video, horizontal and vertical sync and blank outputs, light pen
TV Standard:	American or European standard available.
Synchronzation:	Built-in crystal controlled TV scan generator, or external sync.
Color/Grey Scale:	Up to 24 bits/pixel (2^{24} different colors or grey scale levels/dot by using identical multiple boards.)
Busses:	Digital Equipment PDP-11 (MDC); LSI-11 (MLSI) or Intel SBC-80 (MSBC). 2480 text display also available on same busses.
Documentation:	A 24 page manual providing a complete functional description circuit schematics and other information is available separately for $10.00. Additional color/grey scale application note available on request.
Software:	A software package for 8080 based systems which features vector plot, alphanumeric generation and animation synchronization package using PDP-11 software will be available 1st quarter '78.
Warranty:	90 days parts and labor.
Ordering:	Available directly from Matrox Electronic Systems Ltd. or its worldwide network of distributors. Specify options desired. Delivery 2-6 weeks.
Prices:	Quantity of one: 256 X 256 $ 895 256 X 512 $1095 512 X 512 $1390 256 X 1024 $1390

matrox
electronic systems ltd.
5800 ANDOVER AVE., MONTREAL, QUE. H4T 1H4, CANADA
TEL.: (514) 735-1182 TELEX: 05-825651

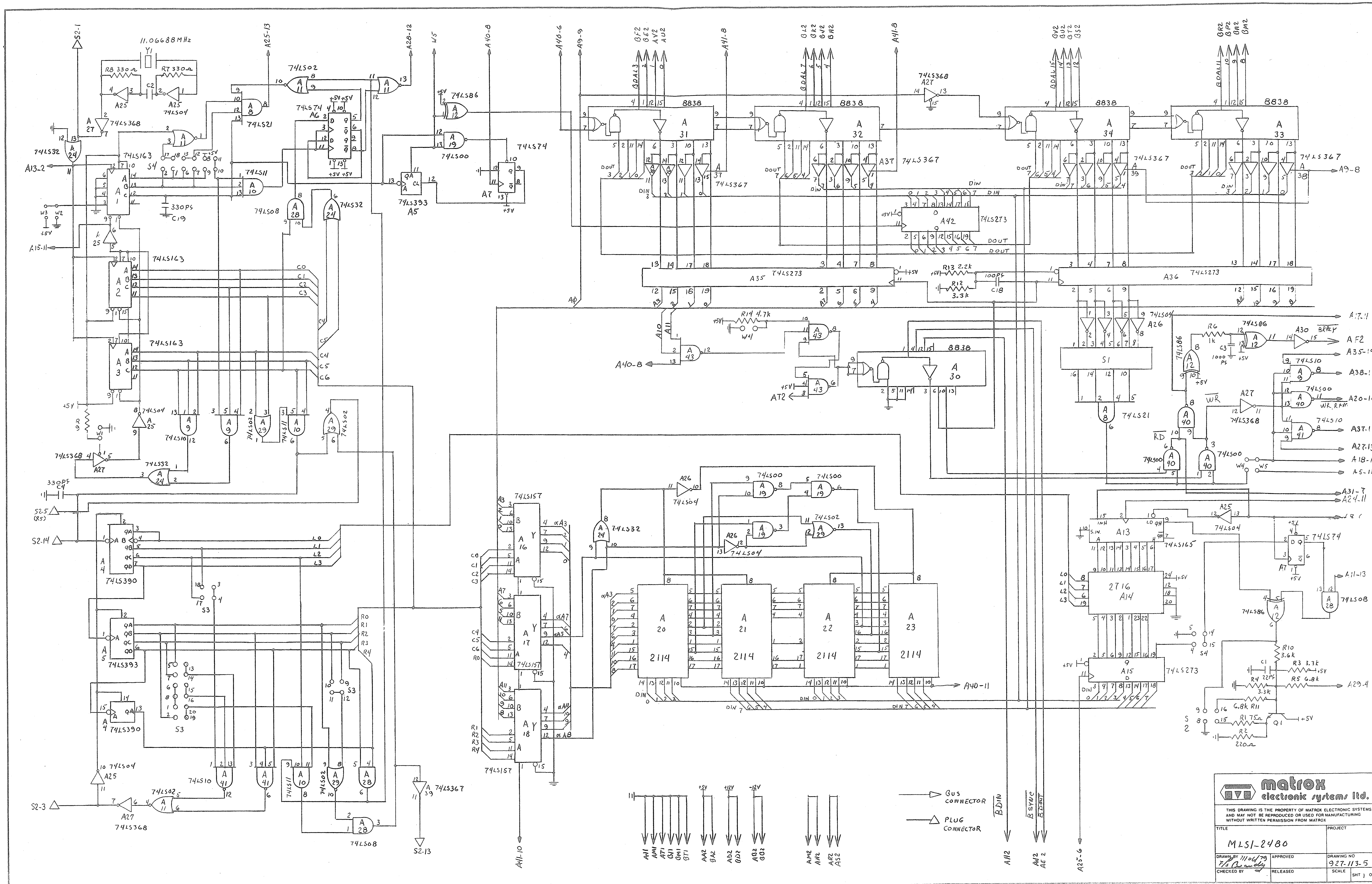
August 13th, 1979

Dear Customers:

Due to the general industry wide shortage of low power Shottky TTL devices, Matrox has been forced to substitute regular TTL devices in some instances. This substitution will slightly increase overall board power consumption and also increase loading of the system bus. Matrox believes that these marginal specification changes will not affect the great majority of users. Substitutions are made in the interest of maintaining reasonable delivery time to our customers. All regular TTL devices are mounted on sockets. This permits them to be readily identified and also allows them to be easily replaced with LS devices if this should be necessary.

We regret any inconvenience this may cause our customers.

MATROX ELECTRONIC SYSTEMS LTD.



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TITLE: MLSI-2480	PROJECT
DRAWN BY 11/06/79 F/S Brandy	APPROVED
CHECKED BY	RELEASED
DRAWING NO 927-113-5	SCALE / SHT 1 OF 1

TRANSLAR 003