MDB

MLSI-DRV11P

GENERAL PURPOSE INTERFACE MODULE

INSTRUCTION MANUAL

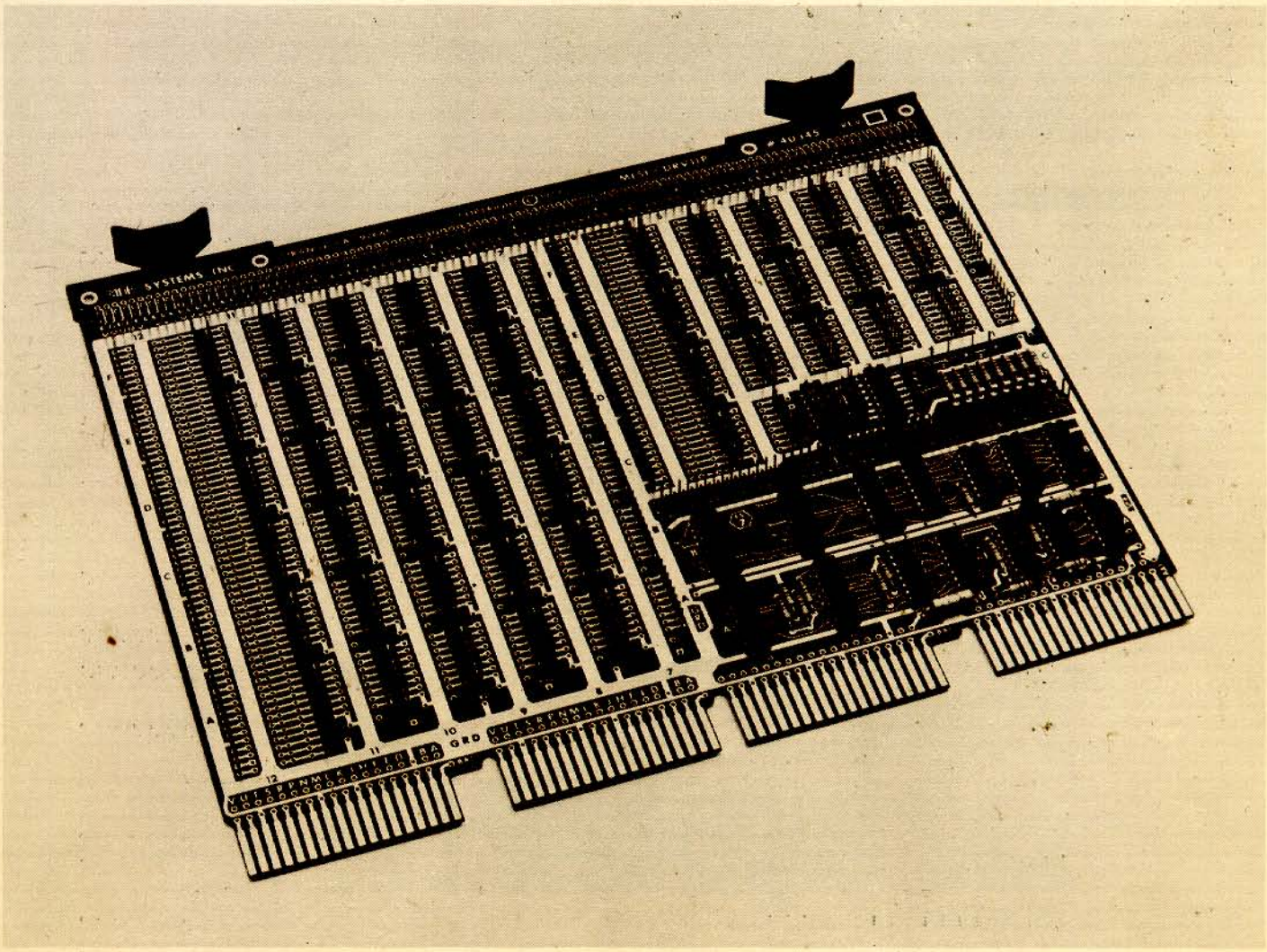

TABLE OF CONTENTS

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MLSI-DRV11P
GENERAL-PURPOSE INTERFACE MODULE

INTRODUCTION

The MDB MLSI-DRV11P General-Purpose Interface Module acts as an interface to transfer information between the bus of an LSI-11 processor, and the user's peripheral device.

The MSLI-DRV11P consists of a single quad module containing the following:

a. Fixed logic to interface with the processor, and with the user-built peripheral device interface on the module. Fixed logic includes bus receivers and drivers, device address selection and decoding logic, and dual interrupt control logic, (see figure 1).

b. Circuit board facilities and wire-wrap posts to accommodate up to fifty-five 14-pin or 16-pin DIP devices. Up to four 20-pin devices; or three 24-pin devices; or two 40-pin devices, along with a smaller number of 20-pin or 24-pin devices; may be installed in place of a number of smaller devices. The user may use these facilities to build logic interfacing the fixed logic on the module with the peripheral device.

Control and data points are brought out from the fixed logic to wire-wrap posts to give the user considerable flexibility in using the wire-wrap (user's logic) section of the module. Two-hundred pins are available for interfacing with the peripheral device through standard ribbon cable connectors.

The quad module fits into any slot in an MDB BPA-84 backplane/card guide assembly.

PREPARING USER LOGIC

Refer to the printed circuit board assembly drawing in this manual for the layout of available DIP device locations. Note that there are 55 device locations for 14-pin or 16-pin DIPs, with pads to accommodate a number of discrete components. Remove etch connections from DIP pads to ground where they are not appropriate.

Observe good wire dressing practices, especially when speed is important. Decouple the +5V dc line to ground pads (using 0.01-microfarad disc capacitors) at at least one point in each DIP column.

Refer to the logic diagram for signals available at wire-wrap pins. Typical user logic may include an output data register, a status register, vector address selection a multiplexer to the IDAT lines, and logic to set or reset interrupt requests.

INSTALLATION

SELECTING DEVICE ADDRESS

The assigned device address must be configured on the module in order to prepare the module for its application. Bits 03 through 12 must be jumpered to AND gate inputs. Bits 01 and 02 are etch-connected to the decimal function decoder, along with an enable from decoding higher-order digits. Using only these inputs, the decoder will decode any even-numbered address from XXXXX0 through XXXXX6. Up to ten different odd or even

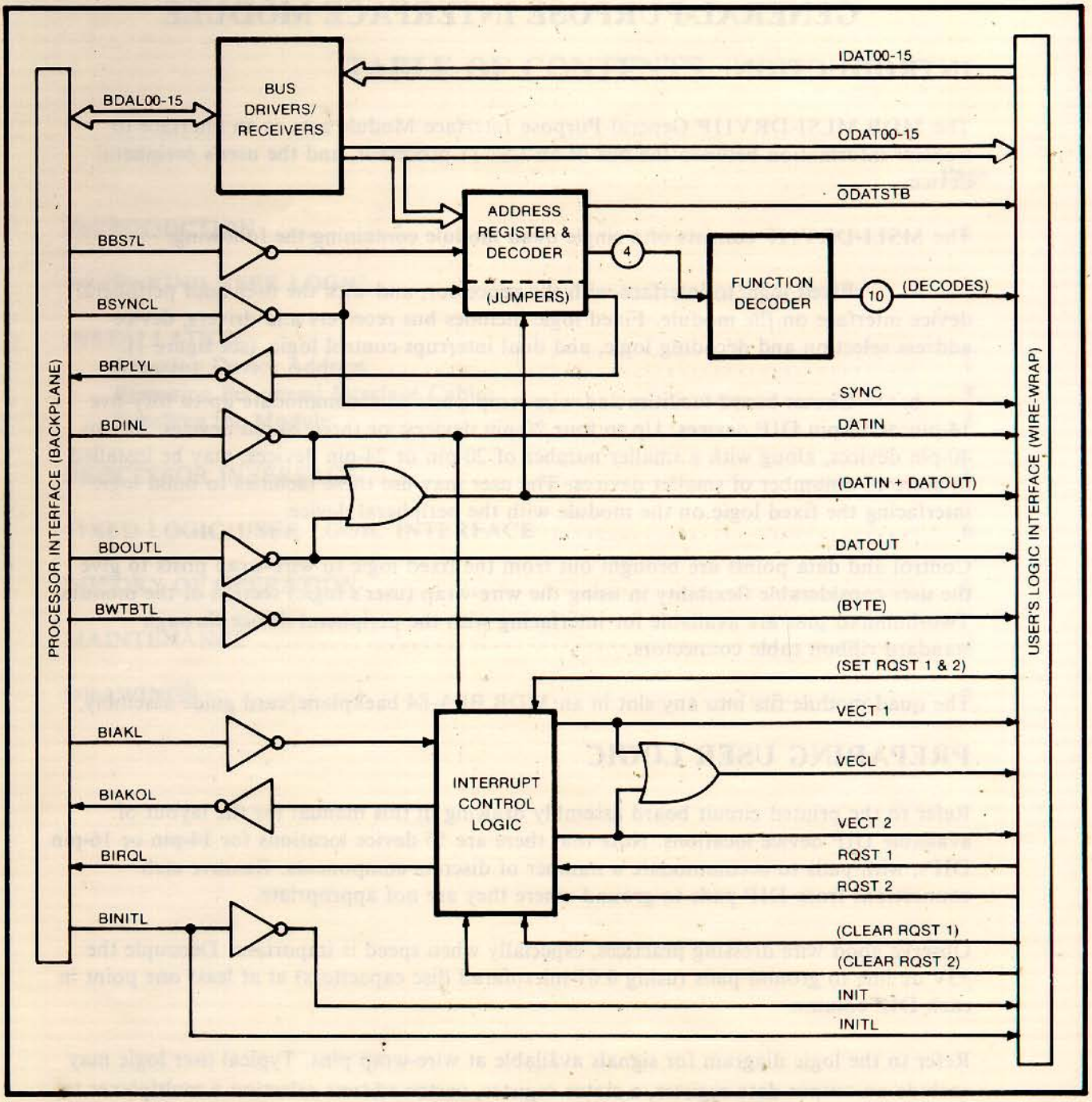


Figure 1. MDB MLSI-DRV11P General-Purpose Interface Module, Functional Block Diagram

numbered addresses may be decoded if additional address inputs are connected to spare address register inputs, and other appropriate wire-wrap jumpers are connected (refer to logic diagram).

To encode a "1", connect the Q output of the stored bit to the AND gate. To encode a "0", connect the $\overline{Q}$ output to the gate.

The Bank 7 Select signal (BBS7L) identifies information from the upper 4K bank (28K to 32K) and is etch-connected to the decoder AND gate.

Wire-wrap terminations give the user almost total freedom in addressing. The module is furnished etch-connected so that the address decoder is enabled by either DATIN or DATOUT, but the user may change this requirement by cutting the etch connections.

PREPARING PERIPHERAL INTERFACE CABLES

The user determines wire-wrap connections at the peripheral device interface. The 200-pin array accommodates standard ribbon cable connectors in any configuration chosen by the user. Where more than one connector is used, be sure to plan pin-outs so that interface signals are grouped together at appropriate connector locations.

INSTALLING THE MODULE

After user logic has been completed and appropriately terminated at the cable connector pins, install the module in the slot in the backplane that gives the module the selected priority. The device controller nearest the KD11 processor board has the highest priority, with decreasing priority at successively more distant slots (see figure 2).

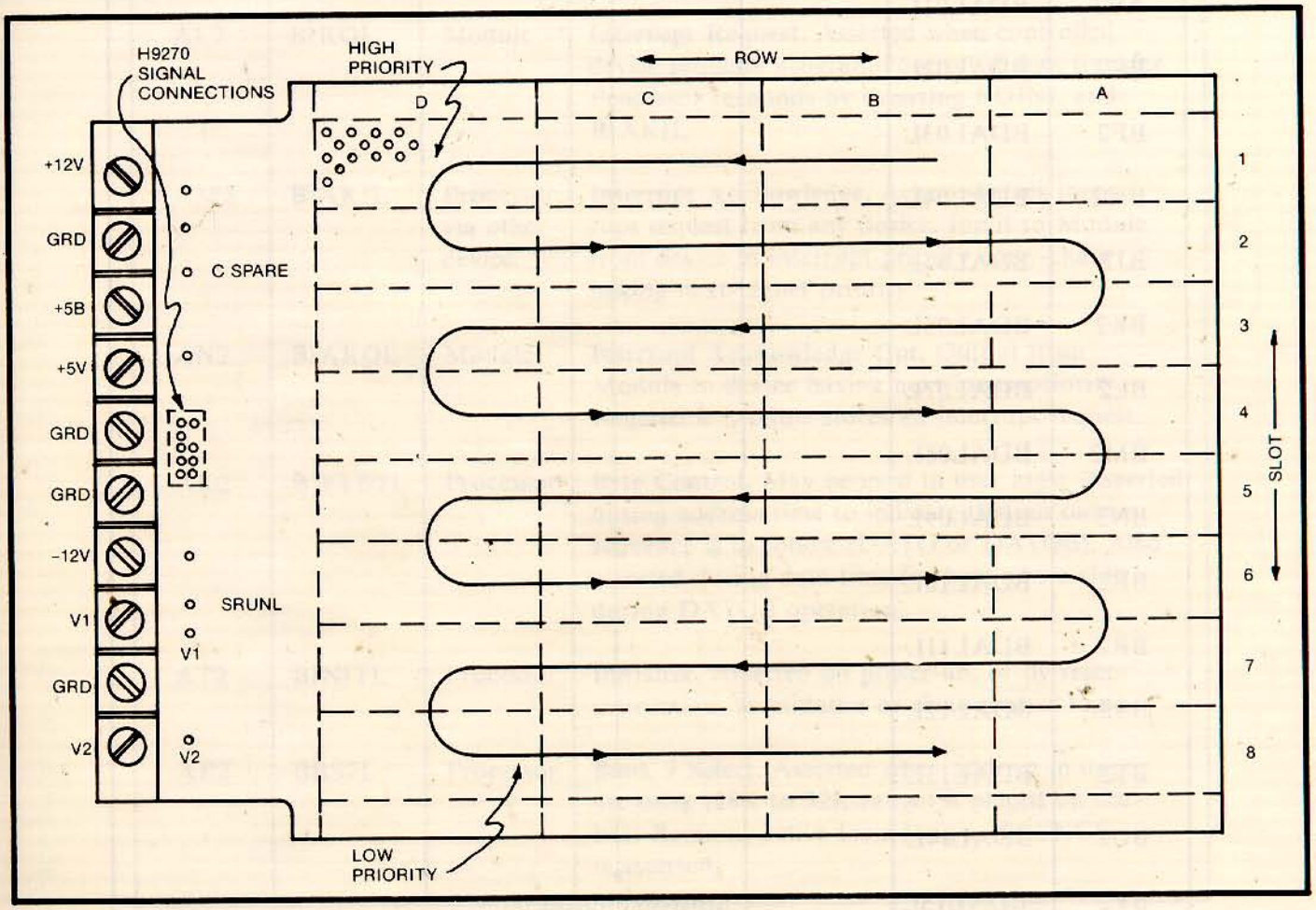


Figure 2. Typical Module Mounting

NOTE

If the module does **not** use DMA and/or Interrupt operations, the appropriate "Acknowledge" lines must be jumpered at connector locations A and C.

Connect the ribbon cables to the device interface connector pins, and to the peripheral device or another MDB module. The module is now ready for check-out and operation.

The MLSI-DRV11P draws 0.4 ampere from the +5V supply bus.

PROCESSOR INTERFACE

Table 1 lists and describes signals at the processor/module interface. For additional detailed information, refer to the appropriate manuals for the LSI-11 Processor.

Table 1. Processor/Module Interface Signals

Bus Pin	Signal	Source	Description
	BDALnnL	Processor or Module	**Bus Data/Address.** Sixteen bidirectional lines for data or address.
AU2	BDAL00L		Least-significant bit.
AV2	BDAL01L		
BE2	BDAL02L		
BF2	BDAL03L		
BH2	BDAL04L		
BJ2	BDAL05L		
BK2	BDAL06L		
BL2	BDAL07L		
BM2	BDAL08L		
BN2	BDAL09L		
BP2	BDAL10L		
BR2	BDAL11L		
BS2	BDAL12L		
BT2	BDAL13L		
BU2	BDAL14L		
BV2	BDAL15L		Most-significant bit.

Table 1. Bus Interface Signals, (cont'd)

Bus Pin	Signal	Source	Description
AJ2	BSYNCL	Processor	**Synchronize.** Asserted to indicate that address is on data/address lines. Transfer remains in process until BYSNCL is negated.
AF2	BRPLYL	Module	**Reply.** Asserted to indicate that it has put data on the bus, or that it has accepted data from the bus. Response to BDINL or BDOUTL, or to interrupt acknowledge.
AH2	BDINL	Processor	**Data Input.** When asserted, along with BSYNCL, an input transfer (with respect to current bus master) is in process. Asserted when processor is ready to accept data. Requires reply BRPLYL. When asserted without BSYNCL, an interrupt operation is in process.
AE2	BDOUTL	Processor	**Data Output.** When asserted, data is available on the bus and an output transfer (with respect to the current bus master) is in process. Module must respond with BRPLYL to complete transfer.
AL2	BIRQL	Module	**Interrupt Request.** Asserted when controlled device requests program-controlled data transfer. Processor responds by asserting BDINL and BIAKIL.
AM2	BIAKIL	Processor, via other device.	**Interrupt Acknowledge.** Acknowledges interrupt request from any device. Input to Module from device in interrupt-priority daisy-chain having next-higher priority.
AN2	BIAKOL	Module	**Interrupt Acknowledge Out.** Output from Module to device having next-lower priority. Negated if Module stores an interrupt request.
AK2	BWTBTL	Processor	**Byte Control.** May be used in user logic. Asserted during address time to indicate that an output sequence is to follow (DATO or DATOB). Also asserted during data time for byte addressing during DATOB operation.
AT2	BINITL	Processor	**Initialize.** Asserted on power-up, or by reset instruction, to initialize or clear control logic.
AP2	BBS7L	Processor	**Bank 7 Select.** Asserted when address in upper 4K bank (28K to 32K range) is placed on the bus. Remains active for a long as BSYNCL is asserted.

FIXED LOGIC/USER LOGIC INTERFACE

This interface consists of a large number of signals available at wire-wrap pins. Signals include the following (refer to the logic diagram).

a. Data bus driver inputs (IDAT00-IDAT15).

b. Data bus receiver outputs (ODAT00-ODAT15).

c. Address register Q and $\overline{Q}$ outputs.

d. Ten function-select signals obtained by decoding the address.

e. Received control signals from the bus, and signals applied to the bus, as follows:

- BBS7L
- BSYNCL
- BDINL
- BDOUTL
- BWTBTL
- BINITL
- BRPLYL

f. Other interface signals as follows:

- RQST1 and RQST2, plus signals to preset both interrupt requests, and individual request clear signals.
- VECT1 and VECT2 signals, to be used to gate selected interrupt vector addresses to the IDAT lines.
- $\overline{\text{ODATSTB}}$, which may be used to load a user-supplied output register.
- Inputs and outputs of two spare address register flip-flops, and the stored address bit ODAT00.
- Inputs and outputs of a spare 2-input NAND gate, and a spare 2-input NOR gate.

THEORY OF OPERATION

(Refer to figure 1, and to the logic diagram, Dwg. No. 40345).

The device address on the bus is loaded into the address register when the processor asserts BSYNCL. When either a BDOUTL or BDINL command is received at the bus, the address decoder is enabled, and address bits 01 and 02 (and, optionally, one or two user-generated bits) are decoded to cause one of up to ten function-select signals to go low.

The module acknowledges receipt of any recognized address, after a short delay, by asserting BRPLYL at the bus. (BRPLYL is also asserted to notify the processor that the interrupt vector address has been placed on the bus.)

The user's logic requests service by asserting either RQST1 or RQST2. Either signal is ORed to the BIRQL line to inform the processor that service is required.

The processor responds by asserting BDINL and BIAKIL, loading the interrupt request flip-flop and then raising the related VECT1 or VECT2 signal. This signal (in user logic) gates a preset vector address (supplied by user logic) to the IDAT lines, and also causes BRPLYL to be asserted. The processor then enters the addressed subroutine to transfer data to or from the user's peripheral device.

When the operation is completed, the processor drops the BSYNCL line, restoring the fixed logic to its idle state.

Note that the user's logic may set, or clear, an interrupt request at any time.

The term ODATSTB goes low when BRPLYL is asserted in response to a DATIN or DATOUT command. This signal may be used to load the user's output data register.

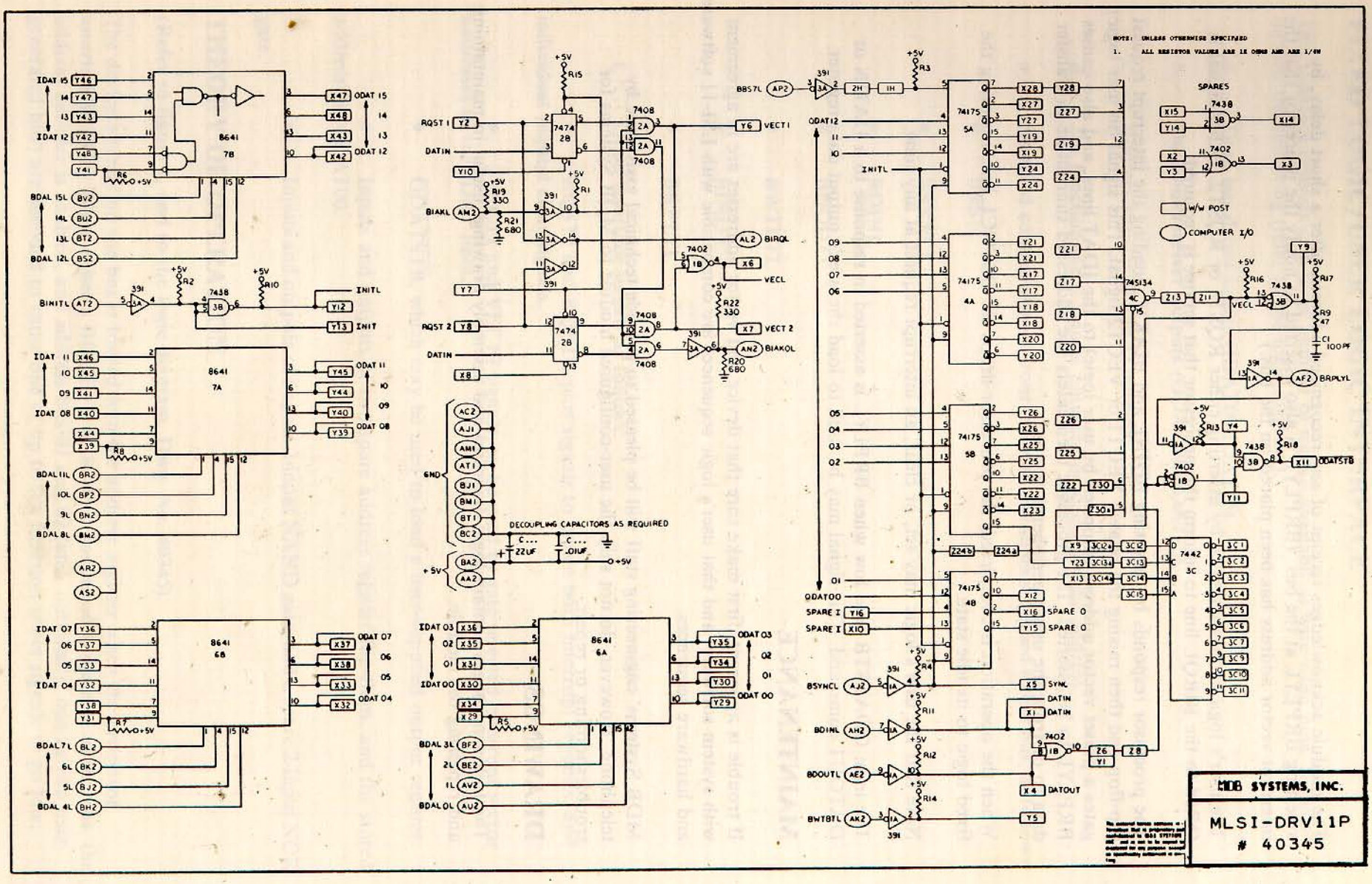
MAINTENANCE

If trouble is apparent, first make sure that device and vector addresses are in agreement with system software, and that user's logic sequences are compatible with LSI-11 software and hardware sequences.

MDB Systems' engineering staff will be pleased to provide technical assistance by telephone. However, do not ship the user-configured module to MDB Systems for troubleshooting or repair.

DRAWINGS

The following pages contain logic diagrams and assembly drawings useful in maintaining and repairing the module.


NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4W
SPARES
W/W POST
COMPUTER I/O
DECOUPLING CAPACITORS AS REQUIRED
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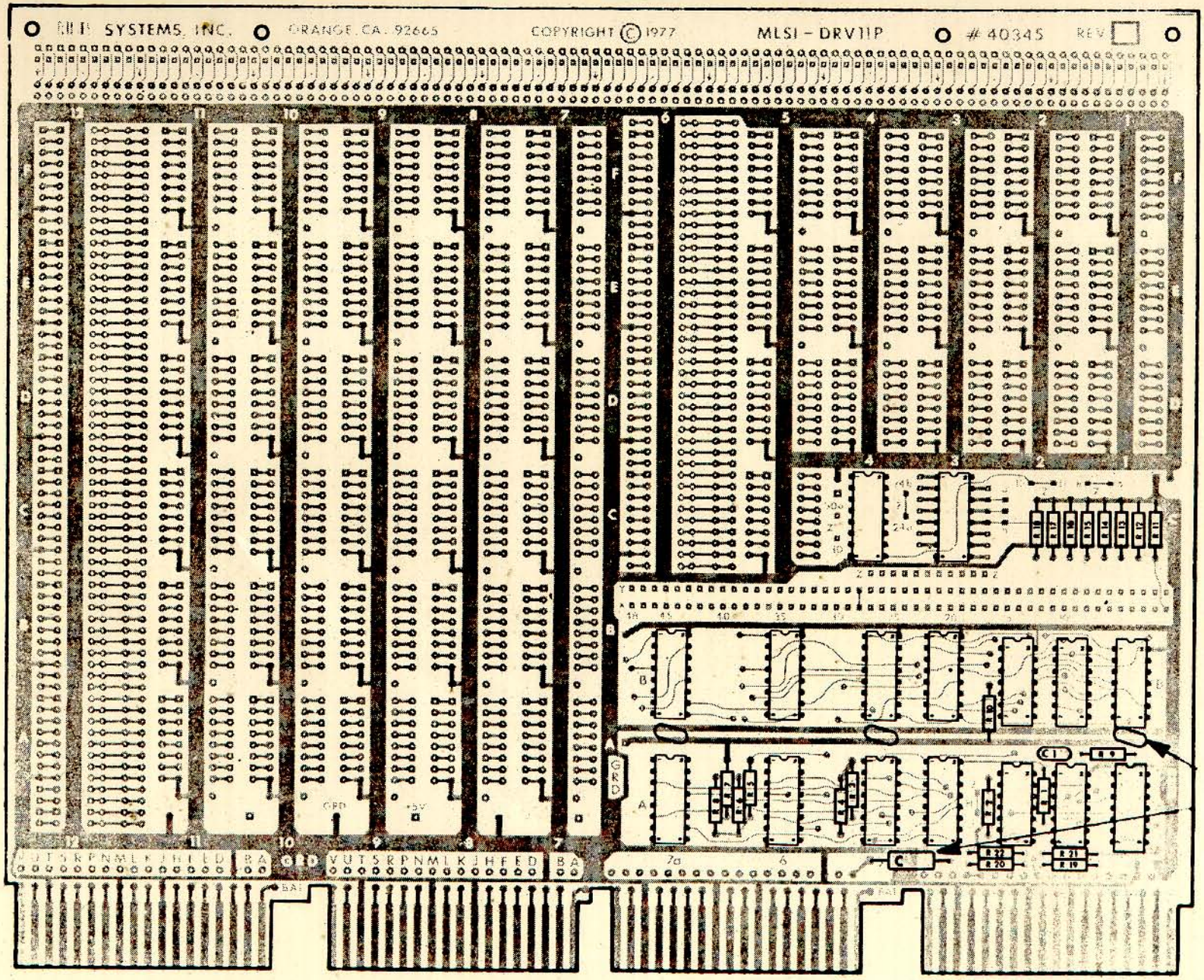
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