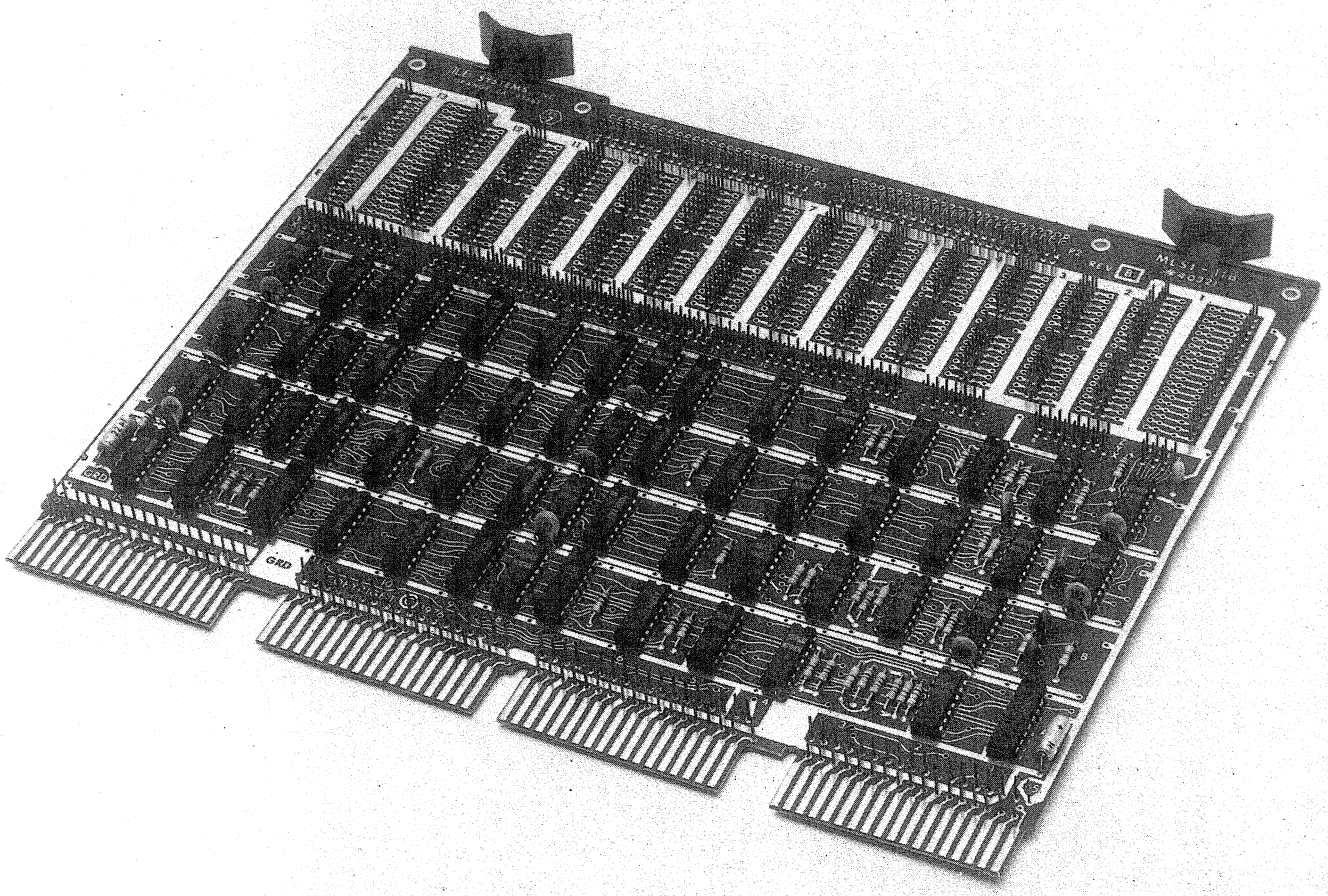
MDB

MLSI-11B

GENERAL-PURPOSE DMA INTERFACE

INSTRUCTION MANUAL



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MLSI-11B
GENERAL-PURPOSE DMA INTERFACE MODULE

INTRODUCTION

The MDB MLSI-11B General-Purpose DMA Interface Module is an interface for the direct-memory-access transfer of data between an LSI-11 processor memory and the user's peripheral device.

The MLSI-11B consists of a single quad module containing fixed logic to interface with the processor, and with user's interface logic to be built on the module's wire-wrap facilities. Fixed logic includes the following:

- bus drivers and receivers;
- five registers:
  - Device Address Register
  - Output Data Register
  - Word Count Register
  - Input Data Register
  - Bus Address Register
- a multiplexer to select bus address, word count, input data, or command/status information onto the bus;
- logic to decode the contents of the Device Address Register;
- interrupt and bus-master control logic.

The module also includes wire-wrap facilities to accommodate up to 26 sockets or directly-mounted DIP devices in 14- or 16-pin configurations. Two device locations will accommodate two 40-pin devices in place of 14- or 16-pin devices.

Control and data points are brought out from the fixed logic to wire-wrap posts to give the user considerable flexibility in using the wire-wrap (user's logic) section of the module.

The quad module fits into any slot in an MDB BPA-84 backplane/card guide assembly.

FIXED LOGIC

Facilities provided on the module consist of integrated-circuit devices in dual in-line (DIP) packages; and wire-wrap posts used to select the device address, and to make bus driver inputs and receiver outputs, and interface address and control lines, available for connection to user logic.

Fixed logic is connected to the bus through etched fingers on the printed-circuit board. User logic signals (TTL-compatible) are available at connectors P2 and P3 on the end of the board opposite the etched fingers. These two 50-pin ribbon connectors may be used for interconnection to the peripheral device, or to other MDB modules (such as expansion modules).

USER LOGIC

User logic (logic designed and built by the user) is to be built in the 26 device locations set aside for wire-wrap connection.

NOTE

Jumpers connecting pins 7 and 8 to supply and ground busses must be opened for any location that is to contain a 16-pin device.

Inputs to the Input Data Register, and outputs from the Output Data Register, are available at wire-wrap posts for making I/O connections. Normal careful design techniques should be used in connecting these signals to other modules.

NOTE

User logic must include a command/status register, logic to assert interrupt and bus requests, and logic to provide DMA Data In and Data Out commands to the bus.

INSTALLATION

JUMPER CONNECTIONS

The device address must be configured on the module in order to prepare the module for its application. The module is furnished with jumpers connected to decode addresses having least-significant bits 0, 2, 4, and 6. Usual addresses are 16xxxx, or 17xxxx.

Referring to the logic diagram, connect wire-wrap jumpers from address register outputs A03M through A12M to the AND gate to encode the four most-significant address digits.

To encode a "1," connect Q output of the bit to the AND gate. To encode a "0," connect the $\overline{Q}$ output to the gate.

Address register outputs are all available at wire-wrap posts to give the user almost total freedom in addressing. The module is furnished jumpered so that the device decoder must be enabled by DATIN or DATOUT, but the user may change this requirement.

Other wire-wrap pins permit the user to utilize various signals generated in the fixed logic, enabling considerable control over fixed logic operation.

INSTALLATION

After user logic has been completed and wired to the two 50-pin connectors, install the module in the slot in the backplane that gives the MLSI-11B the appropriate priority. The device controller nearest the KD11 processor board has the highest priority, with decreasing priority at successively more distant slots.

Prepare cables, terminated with standard 50-pin flat ribbon connectors, for connection to the controlled device or other MDB module, and connect to the module connector pins.

The MLSI-11B draws 1.6 amperes from the +5V dc supply.

THEORY OF OPERATION

The MLSI-11B permits transferring data between the processor and the controlled device in programmed I/O transfers, or in transfers directly between the device and the processor memory without intervention by the processor (direct memory access, or DMA).

In programmed transfer, the processor acts as bus master, commanding Data In or Data Out transfers with or without device interrupts.

In DMA transfer, the MLSI-11B acts as bus master, generating memory addresses and controlling timing of transfer operations.

Refer to the Digital Equipment Corporation *Microcomputer Handbook* for details of interface timing.

The logic diagram (Dwg. No. 40321) in this manual shows details of fixed logic furnished in the MLSI-11B module, and identifies wire-wrap posts at which data, address, and control signals are terminated and are available for connection to user logic.

The block diagram, figure 1, shows the different functional logic elements. Each element shown in the block diagram is described in the following paragraphs.

Table 1 lists signals at the bus interface, and other signals that pass between the processor or other master device, and the MLSI-11B.

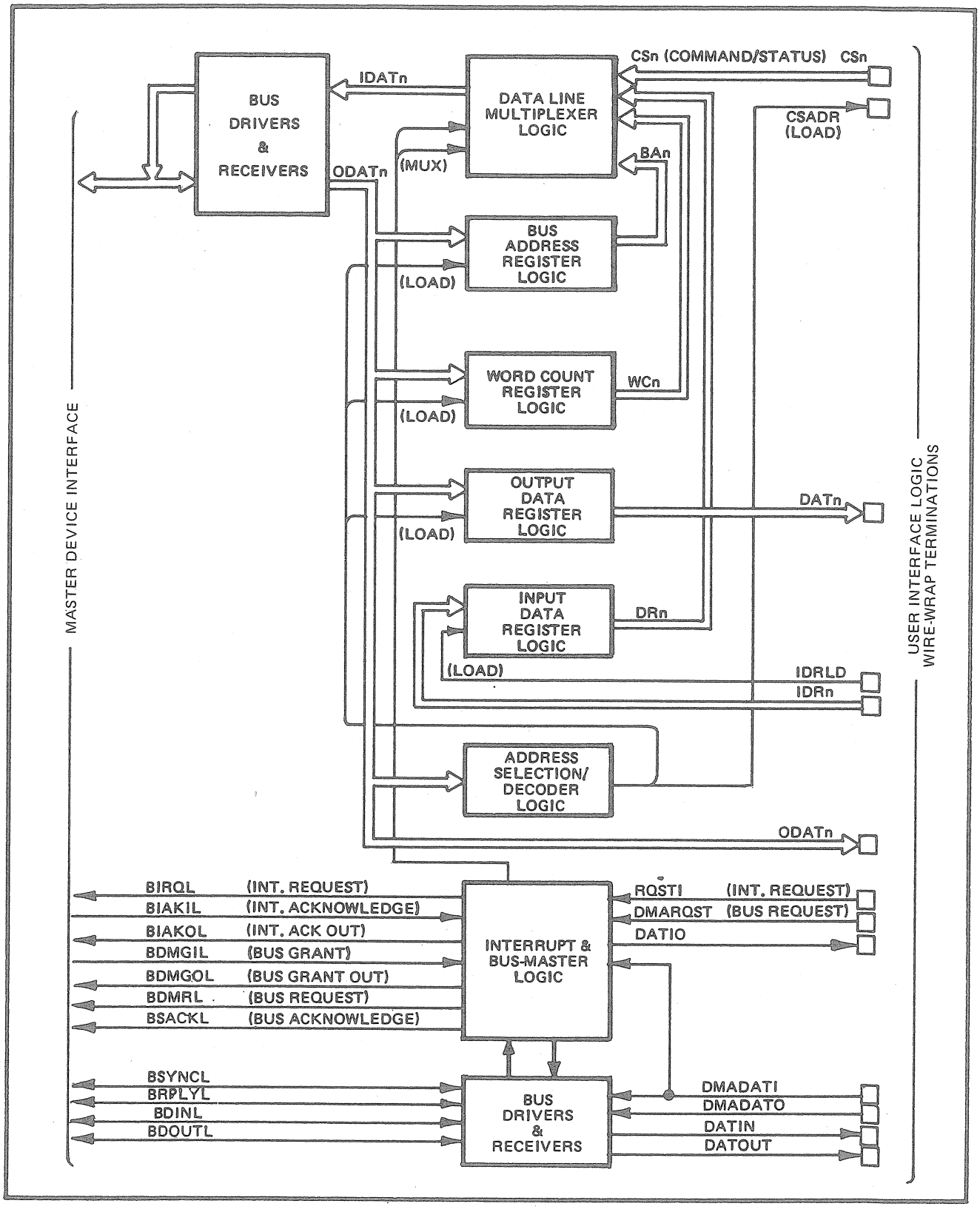


Figure 1 MLSI-11B General Purpose DMA Interface, Block Diagram

Table 1 Bus Interface Signals

Bus Pin	Signal	Source	Description
	BDALnnL	Processor or MLSI-11B	Bus Data/Address. Sixteen bidirectional lines for data or address.
AU2	BDAL00L		Least-significant bit.
AV2	BDAL01L		
BE2	BDAL02L		
BF2	BDAL03L		
BH2	BDAL04L		
BJ2	BDAL05L		
BK2	BDAL06L		
BL2	BDAL07L		
BM2	BDAL08L		
BN2	BDAL09L		
BP2	BDAL10L		
BR2	BDAL11L		
BS2	BDAL12L		
BT2	BDAL13L		
BU2	BDAL14L		
BV2	BDAL15L		Most-significant bit.
AJ2	BSYNCL	Processor or MLSI-11B	Synchronize. Asserted by bus master to indicate that address is on data/address lines. Transfer remains in process until BYSNCL is negated.
AF2	BRPLYL	Processor or MLSI-11B	Reply. Asserted by slave device to indicate that it has put data on the bus, or that it has accepted data from the bus. Response to BDINL or BDOUTL, or to interrupt acknowledge.

Table 1 Bus Interface Signals (cont'd)

Bus Pin	Signal	Source	Description
AH2	BDINL	Processor or MLSI-11B	**Data Input.** When asserted, along with BSYNCL, an input transfer (with respect to current bus master) is in process. Asserted when master device is ready to accept data. Requires reply BRPLYL. When asserted without BSYNCL, an interrupt operation is in process.
AE2	BDOUTL	Processor or MLSI-11B	**Data Output.** When asserted, data is available on the bus and an output transfer (with respect to the current bus master) is in process. Slave device must respond with BRPLYL to complete transfer.
AL2	BIRQL	MLSI-11B	**Interrupt Request.** Asserted when controlled device requests program-controlled data transfer. Processor responds by asserting BDINL and BIAKIL.
AM2	BIAKIL	Processor, via other device.	**Interrupt Acknowledge.** Acknowledges interrupt request from any device. Input to MLSI-11B from device in interrupt-priority daisy-chain having next-higher priority.
AN2	BIAKOL	MLSI-11B	**Interrupt Acknowledge Out.** Output from MLSI-11B to device having next-lower priority. Negated if MLSI-11B stores an interrupt request.
AK2	BWTBTL	Processor	**Byte Control.** May be used in user logic. Asserted during address time to indicate that an output sequence is to follow (DATO or DATOB). Also asserted during data time for byte addressing during DATOB operation.
AT2	BINITL	Processor	**Initialize.** Asserted on power-up, or by reset instruction, to initialize or clear control logic.
AP2	BBS7L	Processor	**Bank 7 Select.** Asserted when address in upper 4K bank (28K to 32K range) is placed on the bus. Remains active for a long as BSYNCL is asserted.
AN1	BDMRL	MLSI-11B	**Bus Request (DMA).** Asserted when controlled device requests DMA data transfer and is to be bus master. Processor responds by asserting BDMGIL.

Table 1 Bus Interface Signals (cont'd)

Bus Pin	Signal	Source	Description
AR2	BDMGIL	Processor via other device	Bus Grant (DMA). Asserted to permit MLSI-11B to become bus master when current bus activity has ended. Input to MLSI-11B from device in bus master priority chain having next-higher priority.
AS2	BDMGOL	MLSI-11B	Bus Grant Output (DMA). Asserted (when BDMGIL is asserted) unless MLSI-11B stores a bus request. Output to device having next-lower priority in bus master chain.
BN1	BSACKL	MLSI-11B	Bus Acknowledge (DMA). Asserts that MLSI-11B has, following receipt of bus request and BDMGIL, become bus master. Controls bus until cleared by user-furnished signal.

BUS INTERFACE AND MULTIPLEXER LOGIC

The 16-bit data word BDALnL at the bus (figure 2) is received and made available (as ODATn) at wire-wrap posts for connection to user logic, and appears at inputs of bus address, word count, output data, and command and status registers (in user logic).

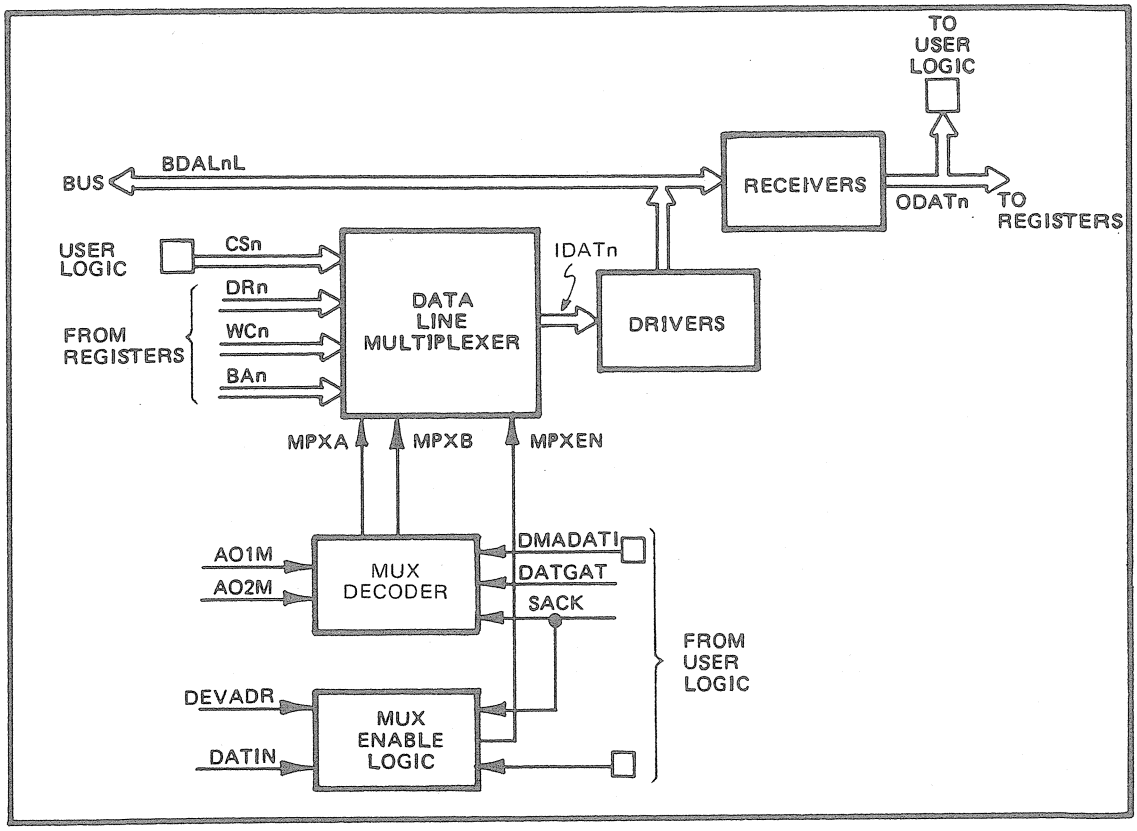


Figure 2 Bus Interface and Multiplexer Logic, Block Diagram

Input data transferred from user logic through the multiplexer is applied through drivers to the bus. In an interrupt sequence, a user-supplied vector address may be applied directly to the bus.

The data line multiplexer selects a specified one of four kinds of information to put onto the bus, as follows:

- WCn, the accumulated word count from the word count register;
- CSn, the control and status word from user logic;
- BAn, the bus address from the bus address register; and
- DRn, the data word from the input data register.

The multiplexer is enabled for normal bus communications by the device address DEVADR and a DATIN command. When the MLSI-11B is acting as the bus master, however, SACK (and a user-selected control) enables the multiplexer.

In normal bus communications (with the processor addressing), multiplexer selection is controlled entirely by address bits A01M and A02M, with WCn selected by $\overline{A01M} \cdot \overline{A02M}$, and CSn bits selected by $\overline{A01M} \cdot A02M$.

When the MLSI-11B is acting as bus master, $\overline{SACK}$ and the user-furnished signal DMADATI, along with DATGAT, control the multiplexer. When $\overline{SACK}$ and DMADATI are true, and DATGAT is false, the multiplexer transfers BAn bits to the bus. When all three signals are true, DRn bits appear on the bus.

DEVICE ADDRESS LOGIC

This logic decodes assigned addresses on the ODATn lines. Addresses formed in the logic, by means of jumper connections, are:

- Word Count Register ..... 16xxx0 or 17xxx0
- Bus Address Register ..... 16xxx2 or 17xxx2
- Status and Control Register..... 16xxx4 or 17xxx4
- Input Data Register..... 16xxx6 or 17xxx6.

Bits ODAT00 through ODAT12 are loaded into the address register (figure 3) by SYNC (derived from the BSYNCL signal at the interface). Each stored bit ODAT03 through ODAT12 is strapped from either the Q ("1") output, or the $\overline{Q}$ ("0") output to an AND gate.

When an assigned device address appears at the register, and either a DATIN or DATOUT command is present, and AND gate asserts DEVADR. That signal is delayed through a series of inverters to provide DEVRPLY. DEVRPLY is applied through a bus driver to the BRPLYL line to indicate recognition of the address.

Bits received on lines ODAT01 and ODAT02 are decoded to obtain the four register address signals WCADR, BAADR, DRADR, and $\overline{CSADR}$ which load the respective registers. The

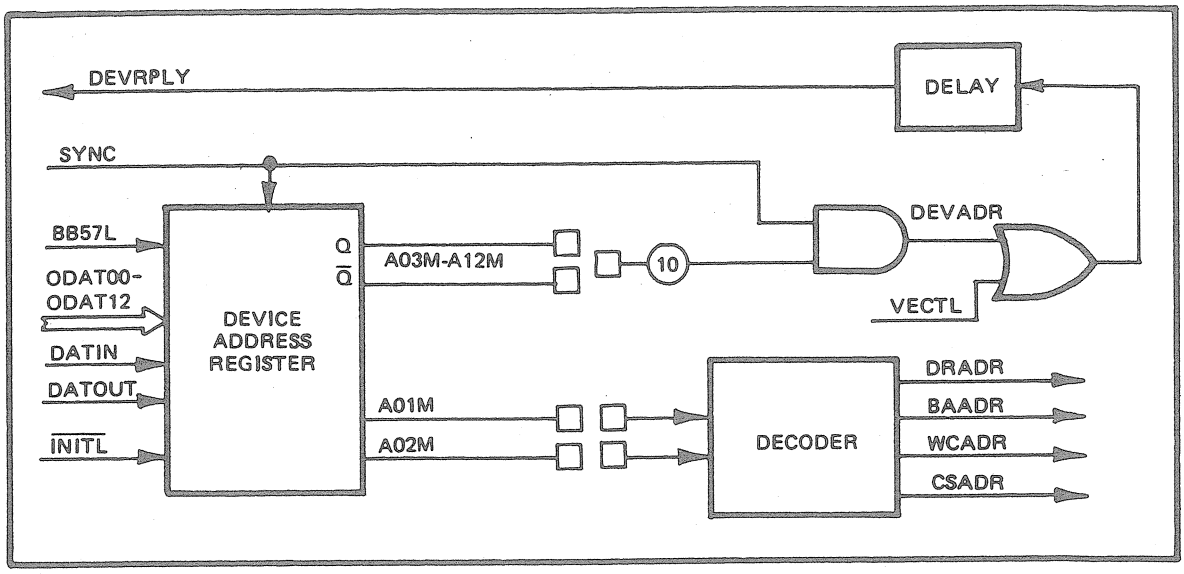


Figure 3 Device Address Logic, Block Diagram

stored bits A01M and A02M are also used to control the data line multiplexer. The ODAT00 bit is not utilized but is available at a wire-wrap post.

The signal BBS7L, also part of the device address, defines the case when the address is from the upper 4k bank (28k - 32k).

The availability of stored address bits, and decoder outputs, at wire-wrap posts offers the user a wide choice of addressing selections.

BUS ADDRESS REGISTER

The bus address register (figure 4) is a 16-bit read/write register used to specify the bus address. The bus address designates a location to, or from, which data may be transferred. The register is loaded with bits from ODATn lines when the address decoder has decoded BAADR, and a BDOUTL (DATOUT) command is received.

The register is normally incremented after each bus cycle, advancing the address to the next word location on the bus. The user interface must furnish the incrementing signal BA+1INC, or BA+2INC, to advance the address by one count, or two counts, respectively. The address is incremented on the negative transition of a positive pulse.

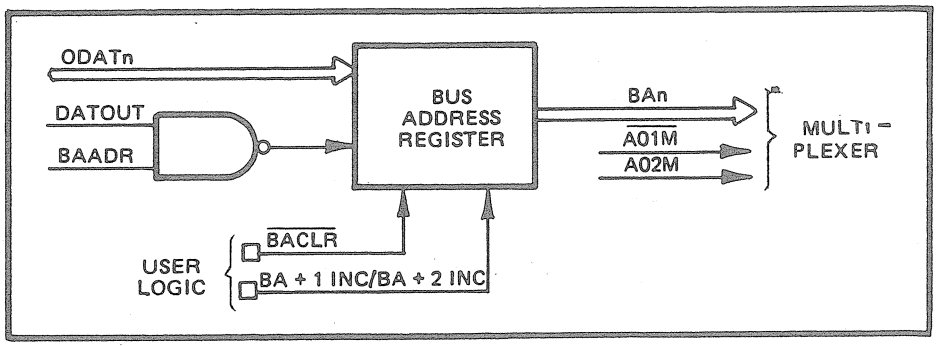


Figure 4 Bus Address Register Logic, Block Diagram

The contents of the bus address register (BAn) are applied to the data line multiplexer for transfer to the bus.

The bus address register is cleared by $\overline{\text{BACLR}}$ from the user logic.

WORD COUNT REGISTER

The word count register (figure 5) is a 16-bit read/write register. It is loaded from ODATn lines with the 2's-complement of the number of transfers to be executed, and is incremented towards zero after each bus cycle.

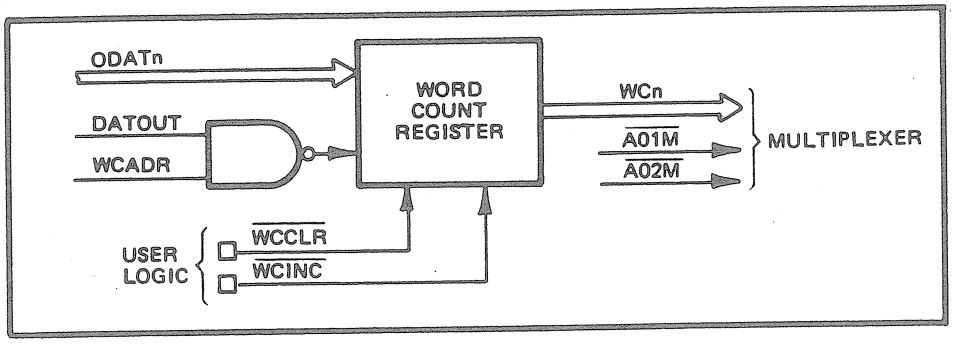


Figure 5 Word Count Register Logic, Block Diagram

The register is loaded by a DATOUT command when the decoded address WCADR is present. The loaded number is then incremented by the negative-going edge of a pulse ($\overline{\text{WCINC}}$) furnished by the user logic.

The register output WCn appears for transfer at the data line multiplexer, and at the zero detector (wired-AND bus) which sends $\overline{\text{WCZRO}}$ to the user logic when the preset number of words has been transferred.

The word count is transferred through the multiplexer to the bus when address bits are $\overline{\text{A01M}} \cdot \overline{\text{A02M}}$.

The word count register is reset by $\overline{\text{WCCLR}}$ from the user logic.

OUTPUT DATA REGISTER

The 16-bit output data register (figure 6) receives and stores data from the ODATn lines and presents the stored data (DATn) to the user logic.

The register is loaded by a DATOUT command when the related address is decoded (DRADR) in an output cycle, or by DMSYNC when the MLSI-11B is bus master and performing a Data In cycle to transfer data or a vector address to the bus.

The register is cleared on power-up by $\overline{\text{INITR}}$.

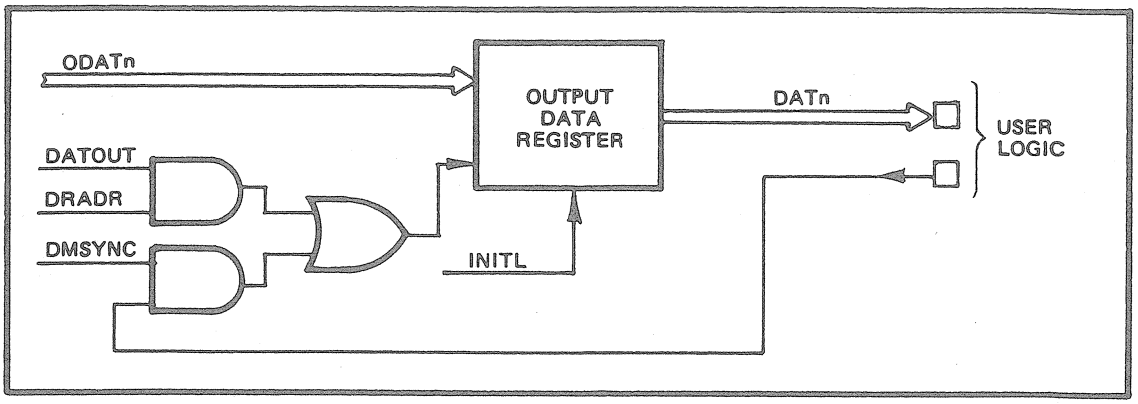


Figure 6 Output Data Register Logic, Block Diagram

INPUT DATA REGISTER

The input data register (figure 7) is a 16-bit register loaded from, and by, the user logic. The contents of the register are presented to the multiplexer for transfer to the bus when the bus master requests a DATIN cycle.

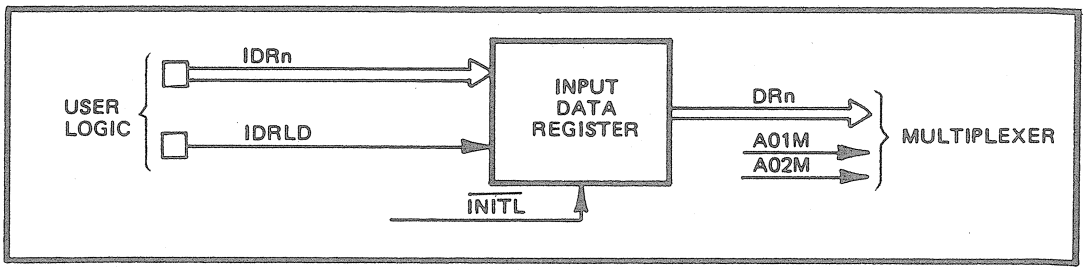


Figure 7 Input Data Register Logic, Block Diagram

The input data bits IDRn are loaded into the register by the negative-going edge of a $\overline{\text{IDRLD}}$ pulse from the user logic. The register is cleared on power-up by $\overline{\text{INITL}}$.

The stored data bits DRn are transferred through the multiplexer to the bus.

INTERRUPT CONTROL LOGIC

An interrupt cycle is begun when the controlled device requests service by asserting RQSTI. This sends BIRQL to the processor and set-enables the request flip-flop 3C-5. The processor responds with a DATIN instruction, setting the flip-flop and generating VECTL when BIAKIL is low at the interface.

If the MLSI-11B has priority (BIAKIL is low), this negates BIAKOL and, after a delay, VECTL causes DEVRPLY to appear on the BRPLY line at the bus interface.

The interrupt request is cleared by a user-furnished signal at 3C-1, negating VECTL and again asserting BIAKOL on the daisy-chained priority line.

BUS ARBITRATION AND DMA TRANSFER LOGIC

The controlled device calls for DMA transfer by asserting DMARQST. This signal causes BDMRL to be asserted at the bus master, and set-enables the DMAS flip-flop (½ of 4D).

When the bus master asserts the bus grant signal BDMGIL, the DMAS flip-flop is set, set-eanbling the BSACK flip-flop (½ of 4D) and negating the daisy-chained BDMGOL signal to the device having the next-lower priority. The logic then waits until bus activity is ended.

When bus activity ends, both SYNC and RPLY become false, setting the SACK flip-flop. BSACKL then is asserted at the interface, and SACK transfers the bus address through the multiplexer to the bus.

SACK, delayed approximately 100 nanoseconds by one-shot 2B-6, then raises DMSYNC, asserting BSYNCL at the interface and causing the processor to store the bus address.

After a further delay of $\overline{\text{DMSYNC}}$, the DATGAT flip-flop is set. If DMADATI is true (from the controlled device), the contents of the input data register (DRn) are put on the bus by DATGAT. DATGAT also causes DGPUL to trigger one-shot 2B-10 which, after a 100-nanosecond delay, causes flip-flop 3C-9 to assert DATIO. This signal causes the device to raise either DMADATO, or DMATATI, at the bus drivers to assert either BDINL, or BDOUTL, at the interface, depending on the required direction of data transfer.

When the processor acknowledges with BRPLY, $\overline{\text{RPLY}}$ triggers one-shot 2B-10 to reset the DATIO flip-flop and end the cycle.

The SACK flip-flop must be reset (through wire-wrap pin X9) at the discretion of the user. Either of the uncommitted flip-flops (1D) may be utilized to implement this function.

MAINTENANCE AND REPAIR

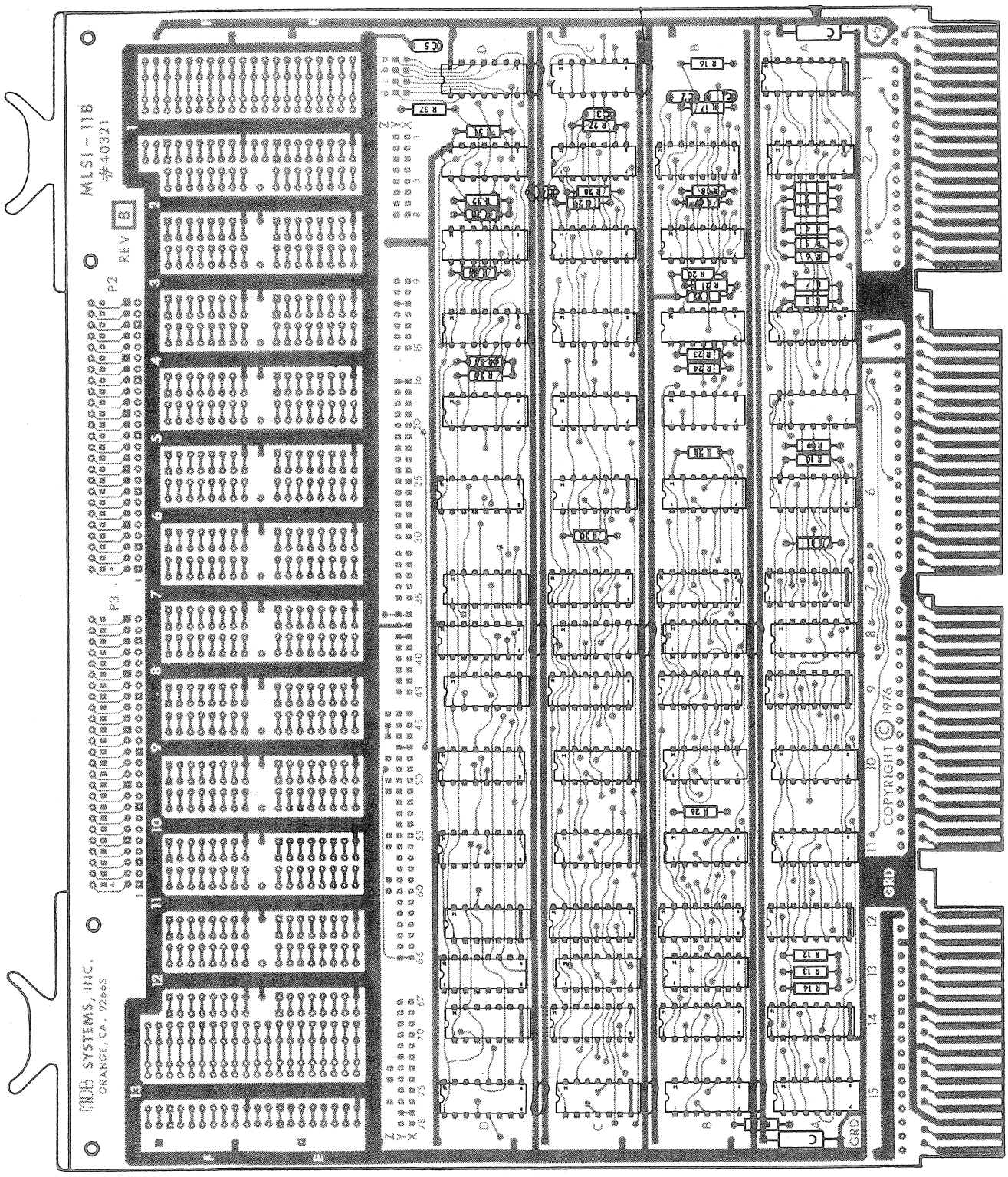
Verify correct operation, and troubleshoot, the MLSI-11B General-Purpose DMA Interface using diagnostic software developed for the system.

If a failure is evident, refer to the assembly and logic diagrams contained in this manual. Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems.

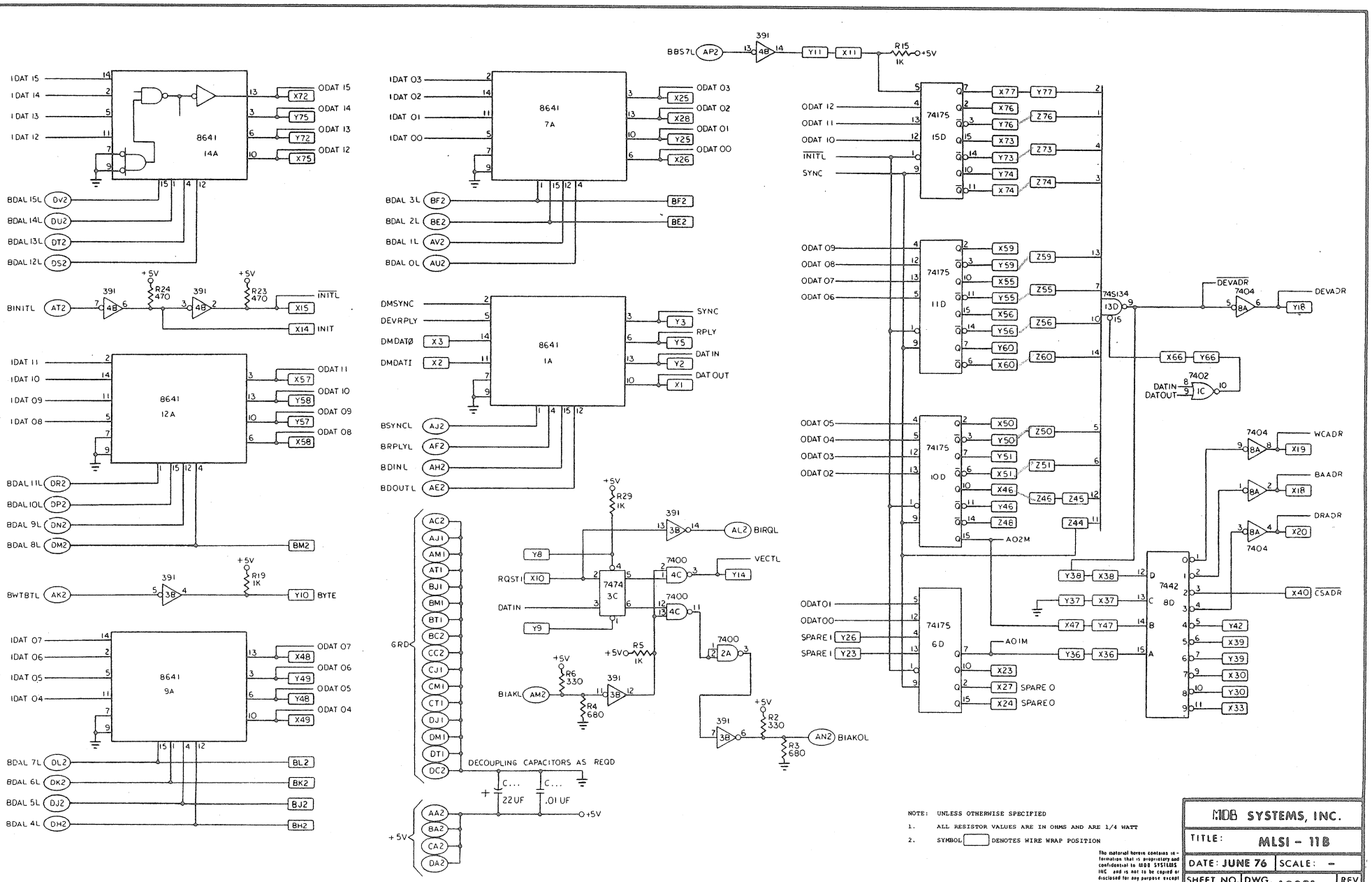
Table 2 lists signal assignments at the backplane connector to aid in troubleshooting.

Table 2 Backplane Connector Pin Assignments

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
BDAL0L	AU2	BINITL	AT2	+5V DC	AA2	GROUND	AC2
BDAL1L	AV2	BWTBTL	AK2		BA2		AJ1
BDAL2L	BE2	BBS7L	AP2		CA2		AM1
BDAL3L	BF2	BSYNCL	AJ2		DA2		AT1
BDAL4L	BH2	BRPLYL	AF2				BJ1
BDAL5L	BJ2	BDINL	AH2	jumper	CS2/		BM1
BDAL6L	BK2	BDOUTL	AE2		CR2		BT1
BDAL7L	BL2	BIRQL	AL2				BC1
BDAL8L	BM2	BIAKIL	AM2	jumper	CN2/		CC2
BDAL9L	BN2	BIAKOL	AN2		CM2		CJ1
BDAL10L	BP2	BDMGIL	AR2				CM1
BDAL11L	BR2	BDMGOL	AS2				CT1
BDAL12L	BS2	BDMRL	AN1				DJ1
BDAL13L	BT2	BSACKL	BN1				DM1
BDAL14L	BU2						DT1
BDAL15L	BV2						DC2



MLSI-11B General-Purpose DMA Interface, Assembly



NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT
2. SYMBOL ☐ DENOTES WIRE WRAP POSITION

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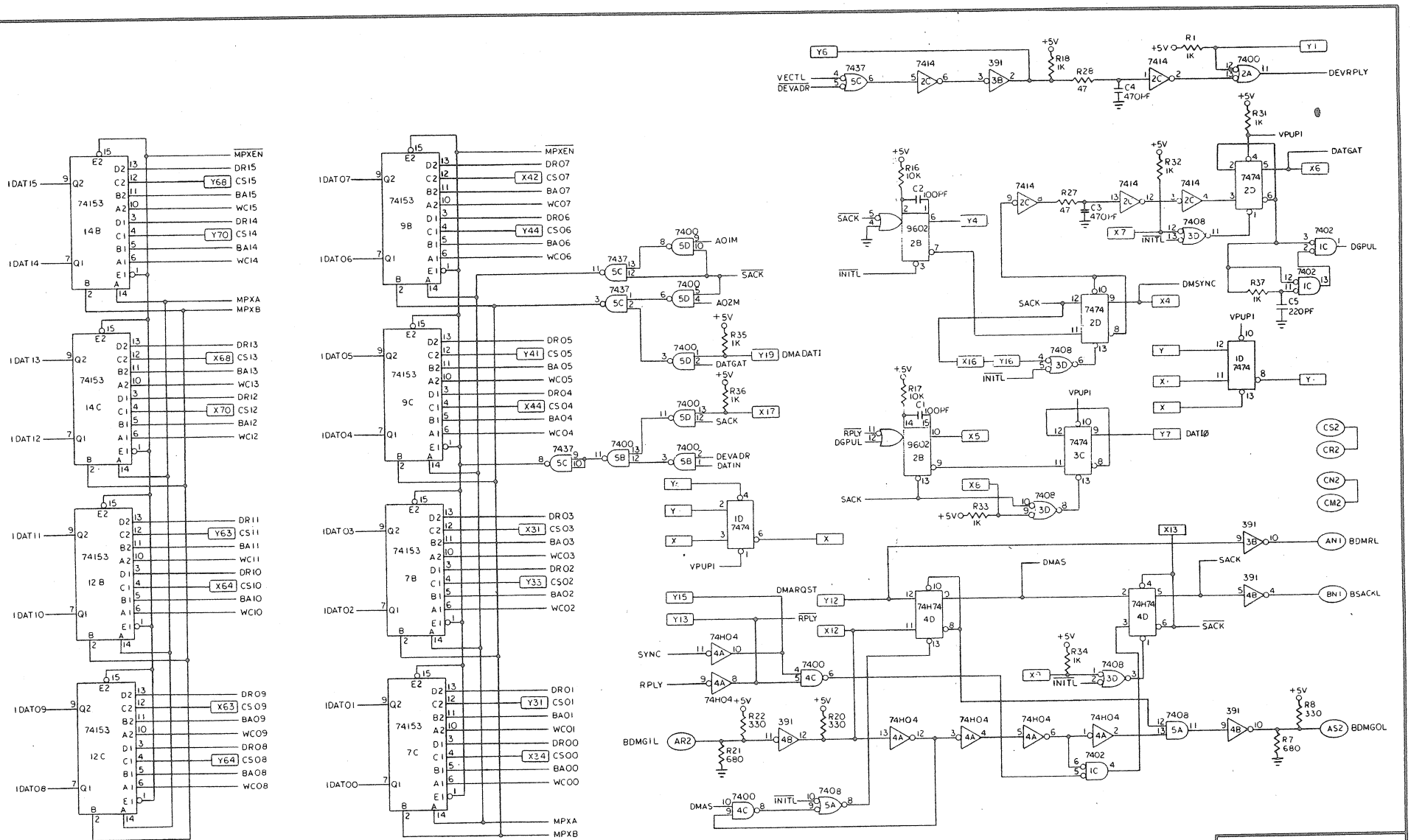

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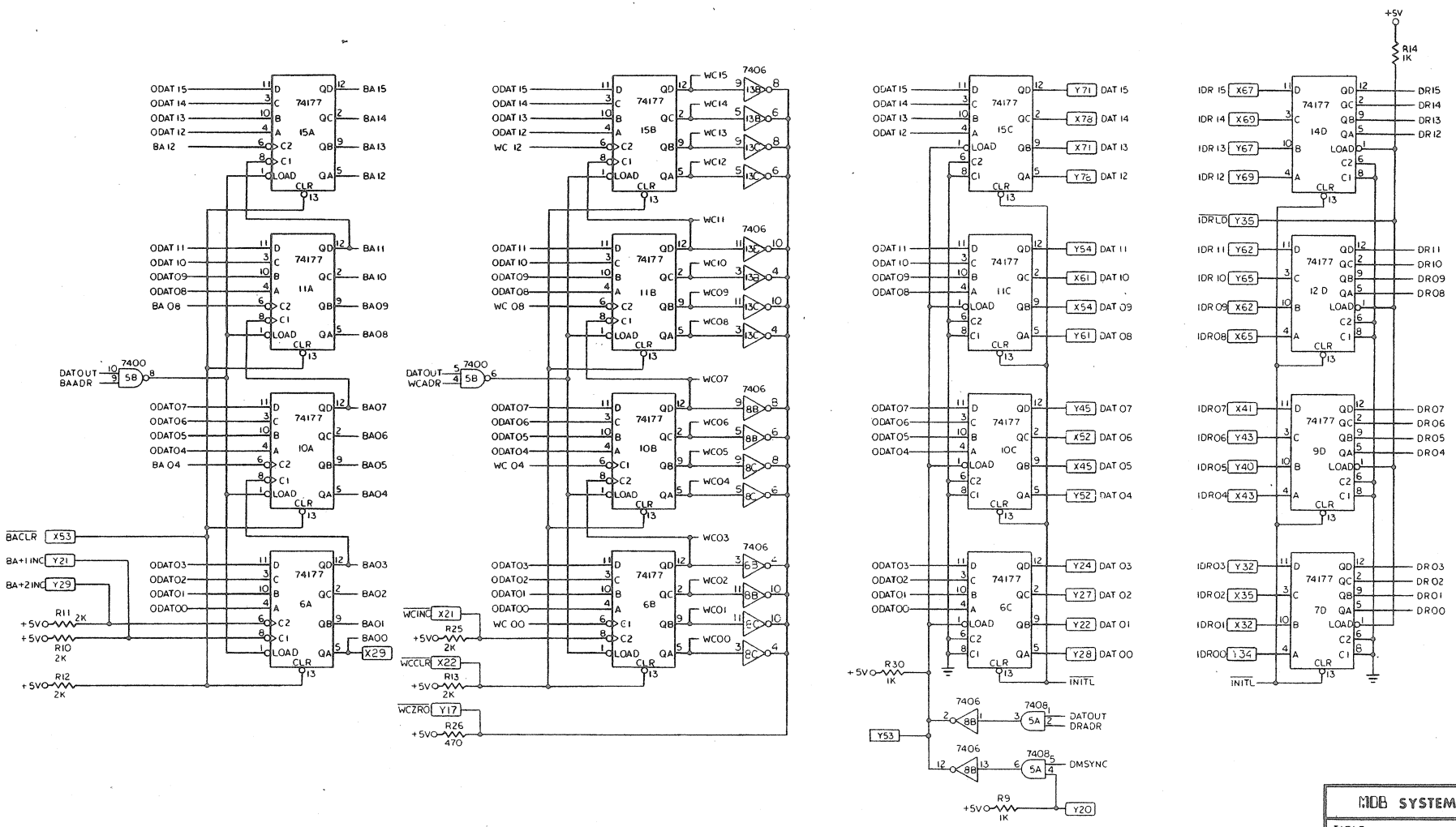

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