Model WH27
FLOPPY DISK

595-2167

OPERATION/SERVICE MANUAL

616-982-3309

HEATH
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HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

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INTRODUCTION

The Heath Model H27 Floppy Disk is a mass storage device that stores programs and other digital information for the Heath H11 Computer on 8 inch, oxide-coated diskettes. Each diskette has 77 tracks that permit it to store 256K bytes. The two floppy disk drives therefore provide a 512K byte storage capacity.

An interface circuit board, which is installed in the H11 Computer, communicates to the controller circuit board in the floppy disk unit through a 34-conductor flat cable. This interface board handles the communications between the controller circuit board and the H11 bus. In addition, the interface board also has bootstrap, processor diagnostic, and absolute loader programs stored in ROM (read only memory).

A photosensor in the drive units detects the presence or absence of a notch in the diskette to insure read/write protection. If it detects a notch, a signal is transmitted to the controller to indicate a read only operation. If it does not detect a notch, the signal indicates that a write operation is permitted.

The diskettes load quickly and easily through the door in the front panel. The interface circuit board is easy to install in the computer and connections between the Floppy Disk and the computer are simple.

The Floppy Disk is an ideal accessory for your H11 Computer. It adds another level of capability to an already powerful tool.

SPECIFICATIONS

DISKETTE

Capacity (8-bit bytes, IBM 3740 format)	Per diskette: 256,256 bytes. Per track: 3,328 bytes. Per sector: 128 bytes.
Recording Surfaces Per Diskette	1.
Tracks Per Diskette	77 (0-76) or (0-114_8).
Sectors Per Track	26 (1-26) or (1-32_8).
Bit Density	3200 bpi at inner track.
Track Density	48 tracks per inch.
Recording Technique	Double frequency.

DATA TRANSFER RATE

Diskette To Controller Buffer	4 μs/data bit (250k bps).
Track-to-Track Move	6 ms/track maximum.
Head Settle Time	15 ms maximum.
Rotational Speed	360 rpm ÷ 2.5%; 166 ms/revolution nominal.
Average Access	252 ms, computed as follows:

Seek		Settle		Rotate		Total
(77 tks/3)	×	3 ms + 15 ms	+	(166 ms/2)	=	252 ms

ENVIRONMENT

Temperature	
Operating	15° to 32°C (59° to 90°F) ambient; maximum temperature gradient = 20°F/hr (−6.7°C/hr).
Non-operating	−35° to + 60°C (−30° to +140°F).
Diskette Non-operating	−35° to +52°C(−30° to +125°F).

NOTE: The diskette temperature must be within the operating temperature range before you use it.

Relative Humidity	
Operating	25°C (77°F) maximum wet bulb, 2°C (36°F) minimum dew point, 20% to 80% relative humidity.
Non-operating	5% to 98% relative humidity (no condensation).
Diskette Non-operating	10% to 80% relative humidity.
Magnetic Field	A diskette exposed to a magnetic field strength of 50 oersteds or greater may lose data.

POWER REQUIREMENTS

Floppy Disk	100-135 volts or 200-270 volts, 60 Hz, 240 watts maximum.
Interface Module	1.5 A maximum, 1 A typical, at 5 VDC.

GENERAL

Overall Dimensions	18" W × 20-3/4" D × 7-3/4"H (45.7 cm × 52.7 cm × 19.7 cm.).
Net Weight	61 lbs. (27.67 kgs)

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

INSTALLATION AND TESTING

INSTALLATION

Refer to Pictorial 1-1 (Illustration Booklet, Page 1) for the following steps.

(✓) Refer to Detail 1-1A, position the Floppy Disk Drive up on its side as shown, and remove its bottom cover (if not already done).

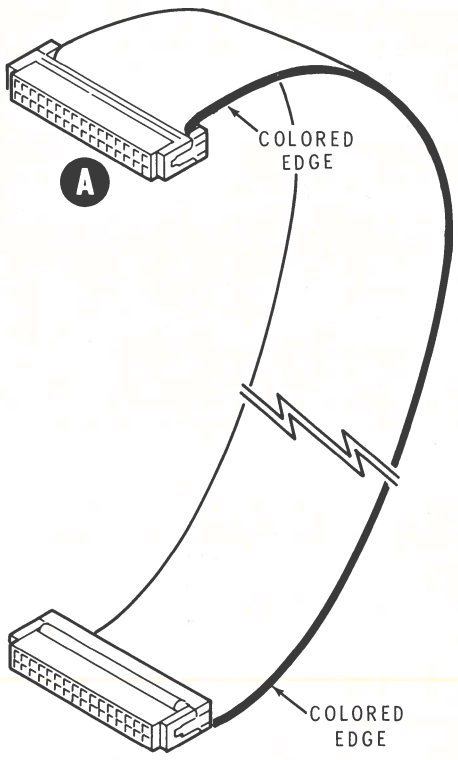
NOTE: The two connectors of the 34-conductor flat cable are mounted on the cable differently. Be sure you use the proper ends of the cable in the following steps.

( ) Refer to Detail 1-1B and position the cable so the connectors are as shown.

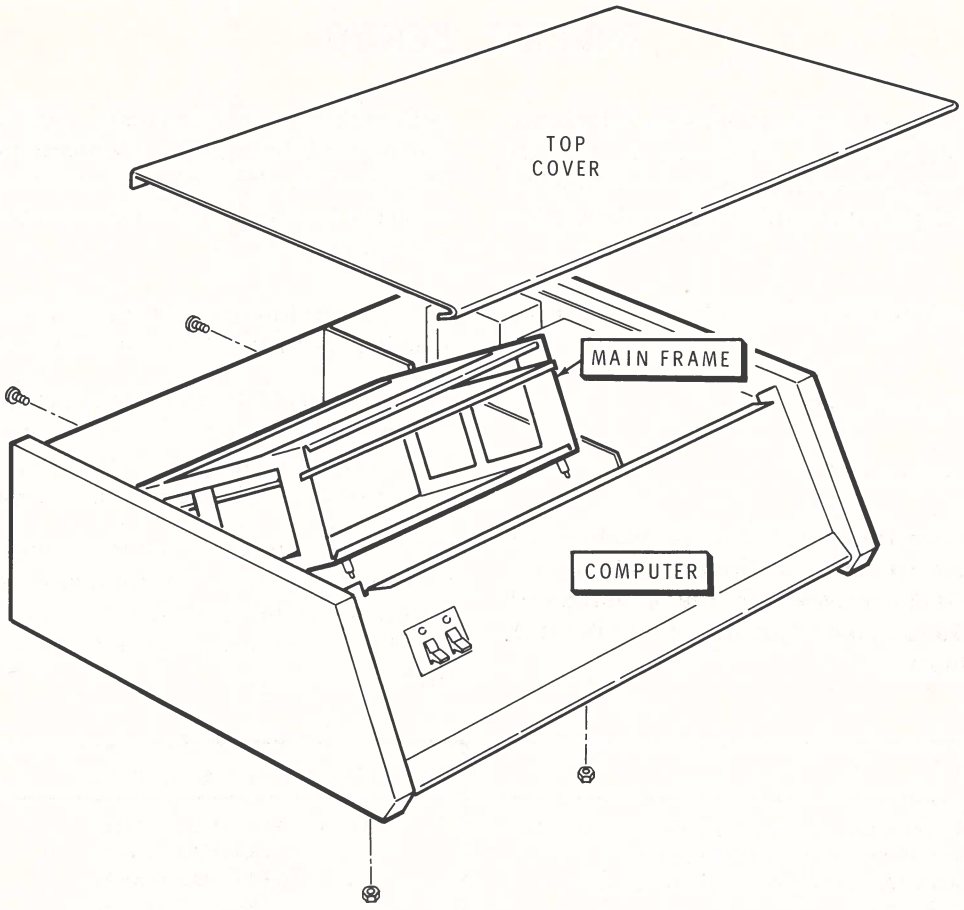
( ) Route connector A through the rear panel opening (loosen the clamp if necessary) of the Floppy and connect it with the colored edge as shown in the Pictorial.

( ) Refer to Detail 1-1C and remove the top cover from the Computer and the two nuts that hold the front edge of the main frame.

( ) As before, route the free end of the cable through the rear panel opening of the Computer, hold the Floppy I/O module near the Computer, and then plug the cable into the circuit board as shown.



Detail 1-1B



Detail 1-1C

( ) Plug the Floppy I/O module into the computer main frame. (Refer to your Computer Operation Manual if necessary.) Use the following recommended locations:

MODULE	H11 SLOT	H11A SLOT
Processor	1 and 2	2 only
Serial I/O	3	3
Floppy I/O	**4**	**4**
Parallel I/O	5	5
Memory Modules	6, 7, 8	1, 6, 7, 8

Although we suggest the above arrangement, you can use other priority arrangements. However, there must be no unused slots electrically between the processor and any module capable of requesting an interrupt. Also, none of these modules can be located in a lower numbered slot than the processor. The number etched in the computer backplane foil between the two edge connectors denotes the electrical priority. The lower the number, the higher the priority.

( ) Dress the cable as desired and secure the rear panel cable clamps.

( ) Replace the covers and main frame nuts, and set the Floppy down on its feet. This completes the "Installation." Proceed to "Initial Tests."

INITIAL TESTS

Remove the cover from the Floppy Disk unit if it is not already removed. This will allow you to see the read/write heads move as you perform the following test. Do not install diskettes until you are instructed to do so.

Set the front panel switches on the Floppy Disk Drive as follows:

SYSTEM switch to RX-01.

FORMAT switch to OFF.

NOTE: It is assumed that the Floppy I/O Module has been installed in a properly functioning H11 Computer and that the H11 Processor Module is configured for Power-Up Mode 2 (see "Appendix C" in the H11 Operation Manual).

Although it is not absolutely necessary, it is a good idea to read through the "Bootstrap ROM Programs" section of this Manual (Page 13) to become familiar with the bootstrap ROM commands you will use in the following steps.

CR, in the following tests, means to push the RETURN (carriage return) key on the terminal.

All keyboard entries must be upper case. The computer responses are underlined in the following tests. This convention helps you distinguish between your entries on the keyboard and the computer responses.

NOTE: Only the most probable causes of a problem have been listed in the following tests. If you are unable to locate a problem, refer to "Customer Service" inside the rear cover of this Manual and return the unit for service.

TEST	POSSIBLE CAUSE OF A PROBLEM
1. Turn on the power and place the RUN/HALT switch in the RUN position. Place the DC ON/OFF switch in the ON position. A $ prompt character will appear on the console device.	1. If the display is 173002 check: a. The RUN/HALT switch. b. The Processor Module. c. The Floppy I/O Module. 2. For any other incorrect display: a. The Floppy I/O Module. b. The Processor Module.
2. Type XC (CR) . The console device will respond with a $ prompt character.	1. Refer to the XC command in "Table 1" on Page 15.
3. Type XM (CR) . After a short pause (depending on the amount of memory) the terminal will respond with a $ prompt character.	1. Refer to the XM command in "Table 1" on Page 14.
4. Type OD . The terminal will respond with: 165240 @	1. Check the bootstrap ROM, U8, and U13.
5. Type P . The terminal will respond with a $ prompt character.	1. Refer to the OD command in "Table 1" (on Page 14) and restart using the G (GO) command. 2. Check the bootstrap ROM, U8, and U13.
6. Type OD . The terminal will respond with: 165240 @	1. Check the bootstrap ROM, U8, and U13.

Even though all of the commands in the ROM have not been tested at this time, sufficient testing has been done to prove that the ROM is being accessed by the processor and that the ROM address and data lines are functioning correctly. Also, it has verified that the processor and the main memory are functioning.

Floppy Buffer Register RXDB 177 172 264

ROM Programs (165 000 → 165 776 / 173 000 → 173 776)

The following tests will be performed using ODT. They will test the various H27 commands and responses.

TEST	POSSIBLE CAUSE OF A PROBLEM
7. NOTE: This test checks to see if the H27 will communicate with the data buffer (177172) and the status register (177170). Make sure there is no diskette installed in drive 0 (left-hand drive). Type: 177170/ . The H11 will respond with 000040 (the contents of the status register-memory location 177170). Then type: 40000 ⏎. The H11 will respond with a @ prompt character. @ 177170/ 000040 40000 ⏎ @	000 040 = done bit set 040 000 = initialize H27 1. If a ? is displayed, the Floppy I/O Module did not generate a reply.
Type: 177170/ . The H11 will respond with 000040 (the contents of 177170). @ 177170/ 000040	1. If 100040 is displayed, repeat test 7. If an error still exists, check the interface cable. 2. If 000000 is displayed, check the interface cable.
Type: ⏎ . The H11 will respond with a prompt. @	
Type: 177172/ . The H11 will respond with 000004. @ 177172/ 000004	why? (probably bit 2 of RXES) @ p. 29 1. If 000000 is displayed, check the cable to the disk drive units.
Type: ⏎ . The H11 will respond with a prompt. @	
8. NOTE: This test checks to see if the H27 will read sector 1 of track 1. Install a formatted diskette in drive 0 (the left drive). Type: 177170/. The H11 will respond with 000040. Type: 40000 ⏎. The read/write head should momentarily engage on drive and the H11 will respond with a prompt. @ 177170/ 000040 40000 ⏎ @	NOTE: The blank diskettes supplied with your Floppy Disk unit have been properly formatted. 1. The diskette is not properly inserted in the drive unit. 2. Drive unit door open.
Type: 177172/ . The H11 will respond with 000204. @ 177172/ 000204 drive ready (see p. 29)	1. If 000000 is displayed, the diskette is not properly formatted. 2. If 000040 is displayed, the diskette is inserted upside-down.
Type ⏎ . The H11 will respond with a prompt. @	

TEST	POSSIBLE CAUSE OF A PROBLEM
9. NOTE: This test, which will be performed on both drives, moves the read/write head toward the center of the diskette approximately 1 inch. Make sure a formatted diskette is still installed in drive 0. Type: 177172/. The H11 will respond with 000204. Then type 1 ⏎. The H11 will respond with a prompt. @ 177172/ 000204 1 ⏎ @ Type: 177170/. The H11 will respond with 000040. Then type: 7 ⏎. The H11 will respond with a prompt. @ 177170/ 000040 7 ⏎ @ Type: 177172/. The H11 will respond with 000007. Then type: 53 ⏎. The read/write head on drive 0 will move toward the center of the diskette and it will momentarily engage. @ 177172/ 000007 53 ⏎ @	just 0 000 001 in Data Buffer Reg (this is the sector address for the next step) 7 = ~~000~~ 0 ~~000~~ 111 = function 011 = Read sector track 53? 1. If the read/write head does not move, finish test 9. If the rest of test 9 passes, replace drive 0.
Remove the diskette from drive 0 and insert it in drive 1. Type: 177172/. The H11 will respond with 000000. Then type: 1 ⏎. The H11 will respond with a prompt. @ 177172/ 000000 1 ⏎ @ Type: 177170/. The H11 will respond with 000040. Then type: 27 ⏎. The H11 will respond with a prompt. @ 177170/ 000040 27 ⏎ @ Type: 177172/. The H11 will respond with 000047. Then type: 53 ⏎. The read/write head on drive 1 will move toward the center of the diskette and it will momentarily engage. @ 177172/ 000047 53 ⏎ @	selects second disk drive; tells to read sector 1. If the first part of test 9 (for drive 0) passed and this part failed, replace drive 1. If both parts of test 9 failed, perform test 10.

TEST	POSSIBLE CAUSE OF A PROBLEM
10. NOTE: This test checks to see if the TR bit functions properly. (↑ Command & Status Register) Type: 177170/ . The H11 will respond with 000040. Then type: 3 ⏎ . The H11 will respond with a prompt. @ 177170/ 000040 3 ⏎ (000003 = Initiate the emptying of the buffer) @ Type: 177170/ . The H11 will respond with 000200. (TR bit only is set)	1. If both test 9 and test 10 fail, the problem is most likely on the Floppy I/O Module. If only one of the two tests failed (9 or 10), the problem is on the controller circuit board.
Type: ⏎ . The H11 will respond with a prompt. @	
Type: 177172/ . The H11 will respond with 000345. Then type: ⏎ . The H11 will respond with a prompt. @ 177172/ 000345 ⏎ @	
Press the / and REPEAT keys to open location 177172 **exactly** 126 times.	
Type: ⏎ . The H11 will respond with a prompt. @	
Type: 177170/ . The H11 will respond with 000200.	
Type: ⏎ . The H11 will respond with a prompt. @	
Type: 177172/ . The H11 will respond with 000345. @ 177172/ 000345	
Type: ⏎ . The H11 will respond with a prompt. @	
Type: 177170/ . The H11 will respond with 000040. @ 177170/ 000040	
Type: ⏎ . The H11 will respond with a prompt. @	

TEST	POSSIBLE CAUSE OF A PROBLEM
11. NOTE: This test checks to see if the H27 will reset the drives when the H11 is turned on and off. Remove the diskette from drive 1. Turn the H11 DC ON/OFF switch OFF. The read/write heads on both drives should move toward track 0 (outward). Manually turn the lead screws (the motor shafts with the long spirals) of both drives until the read/write heads are at least 1/2" from track 0. Insert the formatted diskette in drive 0 and close the door. Turn the DC ON/OFF switch ON. The read/write head on drive 1 should return to track 0; then the read/write head on drive 0 should return to track 0. The read/write head on drive 0 will momentarily engage.	1. A problem exists on the Floppy I/O Module or in the H11 power supply.

Remove the diskette from drive 0.

Your Floppy Disk unit appears to be operating properly. If you purchased your software from the Heath Company, proceed to the appropriate software manuals.

MAINTENANCE

Periodically clean the air filters over the fans. These filters can be removed and replaced from the back of the unit. Wash them in a mild detergent and squeeze them dry.

NOTE: If you ever replace or change either drive mechanism, make sure they are configured as explained in "Configuring The Drives" on Page 35.

BOOTSTRAP ROM PROGRAMS

The primary purpose of the bootstrap ROM is to boot-up the H27 operating system. This eliminates the need to type in a separate bootstrap program. However, the bootstrap program is not its only function. The ROM also contains several diagnostic tests that check the H11 memory and processor. It is a good idea to read through and perform the bootstrap commands to become familiar with them.

You can configure the H11 processor to begin execution at address 173000 (the starting address of the ROM programs) whenever the system is turned on (powered up). Refer to "Appendix C" in the H11 Operation Manual for a description of "Power-Up Mode 2" and for the necessary jumper wire on the processor circuit board. Specifically, you must install a jumper at location W6.

If your H11 is not configured for "Power-Up Mode 2," you must first enter the starting address of the ROM programs. To do this, type 173000G. The H11 will respond with a $ prompt character, indicating that the ROM programs have been accessed. If you enter an invalid command following the $ prompt character, the system responds by displaying a ? after the command and then issues a new $ prompt character on a new line. For example:

```
$ XJ ?

$
```

The specific commands that call up the various programs contained in the ROM are explained in Table 1.

TABLE 1

Bootstrap ROM Programs

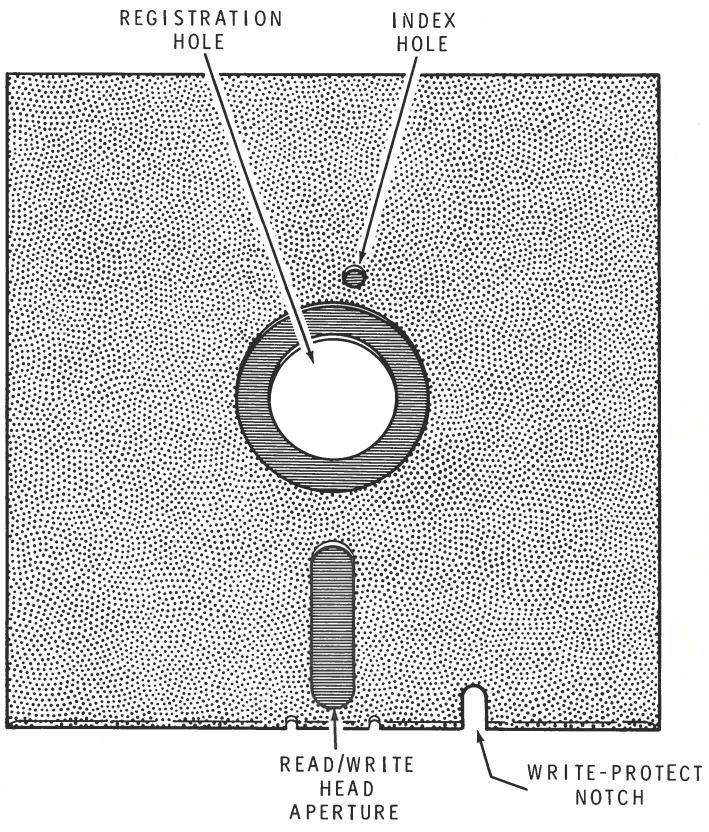
COMMAND	FUNCTION
OD	ODT (Halt). This allows you to examine and/or alter the memory and register locations using the console device. NOTE: ODT responds to upper case characters only. If you are using an H36 as the console device, make sure the CAPS LOCK key is down. If the Program Counter (PC) has not been altered, you can return control to the ROM program by entering the ODT P (Proceed) command. The console device will respond by displaying a $ prompt character. If the PC has been altered, you can start program execution by entering the starting address 165006 and the G (Go) command as follows: @ 165006G $ The processor responds by displaying the $ prompt character on a new line, signifying that another ROM command can be entered.
XM CR	Memory Diagnostic program. After successfully completing this program, the system displays the $ prompt character on the console device. Errors are indicated by the following displays on the console device: 1. 173732 @ This is an address test error. The expected (normal) data is in R3 and the invalid data is in the memory location pointed to by R2. If you desire, continue the diagnostic program execution by entering the ODT P command. 2. 173756 @ This is a data test error. The expected (normal) data is stored in R3 and the invalid data is in the memory location pointed to by R2. If you desire, continue the diagnostic program execution by entering the ODT P command.

Error info retrieval p. 29

COMMAND	FUNCTION
	3. Program halts in trap vector area (0-376) and displays one of several error indications — such as: 000010 @ A timeout trap has occurred in testing memory locations outside the first (lowest) 4K memory. 4. nnnnnn @ A timeout trap has occurred in testing memory locations within the first 4K memory. The nnnnnn displayed is an indeterminate number. The actual memory test consists of an address test and a data test. The address test first writes all memory locations with addresses; it then reads and verifies the addresses. The data test consists of two parts. In the first part, an "all 1's" word is walked through all memory locations, which are initialized as all 0's. In the second part, an "all 0's" word is walked through all memory locations which are initialized as all 1's.
XC ⏎	Processor Diagnostic test. This is a memory-modifying instruction test. Successful execution of the diagnostic program results in the $ prompt character being displayed on the console device. Errors are indicated as follows: 1. The program halts when an instruction sequence is not correctly executed. 2. The program halts in the trap vector area for various traps — such as: 000010 @ This indicates a timeout trap has occurred. NOTE: When a halt occurs, you can use the console ODT M command to determine how the halt mode was invoked. When the system fails to successfully execute the above diagnostics, refer to the "In Case of Difficulty" section in the H11 Operation Manual.

COMMAND	FUNCTION
DXn ⏎	H27 Floppy Disk System Bootstrap. Entering the DXn command starts the memory-modifying CPU instruction test and memory test execution (see the XC and XM commands). Successful test execution results in execution of the bootstrap program for disk drive n, where n = 0, 1. If n is not specified, the system assumes disk drive 0. Floppy disk bootstrap errors are indicated as follows: 1. The program halts and the console device displays: 165316 @ This indicates that the device Done flag in the H27 interface circuit board was not set within the required time (approximately 1.3 seconds). You can restart the bootstrap by entering the P command; the $ prompt character is then displayed and you can re-enter the bootstrap command (DXn) . 2. The program halts and the console device displays: 165644 @ This indicates that a bootstrap error occurred. The H27 Error Register contents are stored in R2. Examine the contents of R2 and use the information contained in the "Operation" section of this Manual to determine the exact nature of the error. Examine the contents of R2 (nnnnnn) as follows: @ R2/nnnnnn ⏎ @ P $ DXn ⏎ After you examine R2, close R2 with a ⏎ and then restart the bootstrap by issuing the P command followed, after the $ prompt character, by the desired bootstrap command.

COMMAND	FUNCTION
	3. The program halts in the trap vector for traps; a timeout trap returns the program to the $ prompt character. You should make sure the interface module and cables are properly installed; then again attempt to bootstrap the system by entering the desired bootstrap command. NOTE: When the program diskette is in disk drive 0, you can start bootstrap programs from the Halt (console ODT) mode (refer to the OD command) without first executing the diagnostic programs. To do this, start DX bootstrap program by first loading R4 with the DX bootstrap starting address (165264). Then start the ROM program at 165242. This sequence of operations is shown below: $ OD @ R4/xxxxxx 165264 ⓒⓡ @ 165242G



PICTORIAL 2-1

FLOPPY DISK TECHNOLOGY

THE MEDIA

An industry-compatible "diskette" (floppy disk), as shown in Pictorial 2-1, is the media that is used for floppy disk data storage and retrieval. The diskette was designed by applying magnetic tape technology to magnetic disk architecture. The result is a flexible oxide-on-Mylar surface encased in a plastic envelope with a hole for the read/write head, a hole for the drive spindle hub, and a hole for the "hard" (physical) index mark. The envelope is lined with a fiber material that cleans the diskette surface. The diskette is supplied to the customer preformatted (in IBM format) and pretested.

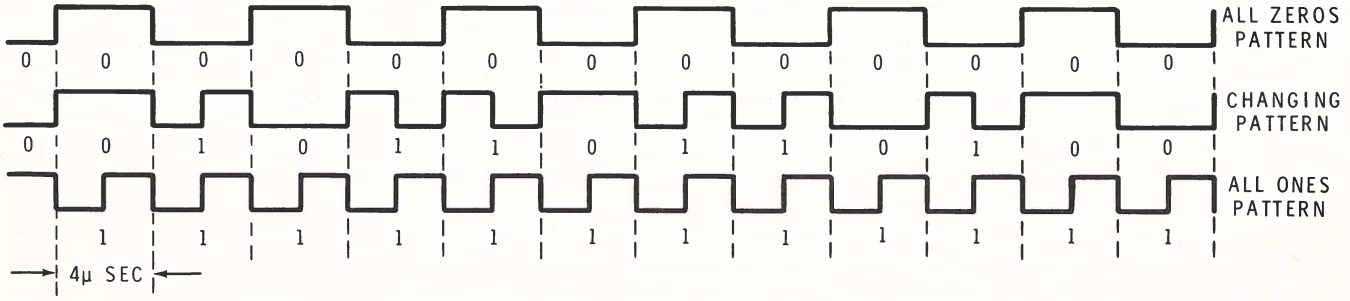
WRITE-PROTECT

Each diskette must be write-enabled before it can be written on. To do this, cover the indicated notch with a tab or opaque tape such as an adhesive-backed label. Do not use black plastic electrical tape. Leave the notch uncovered to "write-protect" the diskette.

RECORDING SCHEME

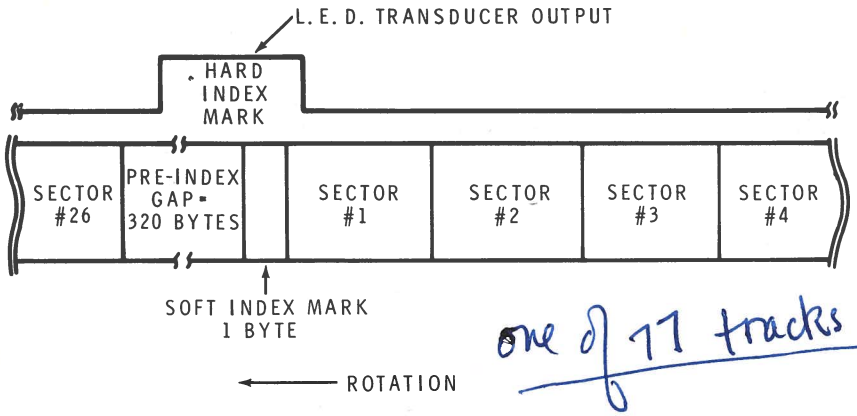
A "double frequency" recording scheme is used. In this method, data is recorded between bits of a constant clock stream. The clock stream consists of a continuous pattern of one flux reversal every four microseconds (Pictorial 2-2). A data "one" is indicated by an additional reversal between clocks (that is, doubling the bit stream frequency; hence the name). A data "zero" is indicated by no flux reversal between clocks.

A continuous stream of ones, shown in the bottom waveform in the Pictorial, would appear as a "2F" bit stream. A continuous stream of zeros, shown in the top waveform, would appear as a "1F" or fundamental frequency bit stream.



NOTE: A FLUX REVERSAL OCCURS AT EACH TRANSITION.

PICTORIAL 2-2



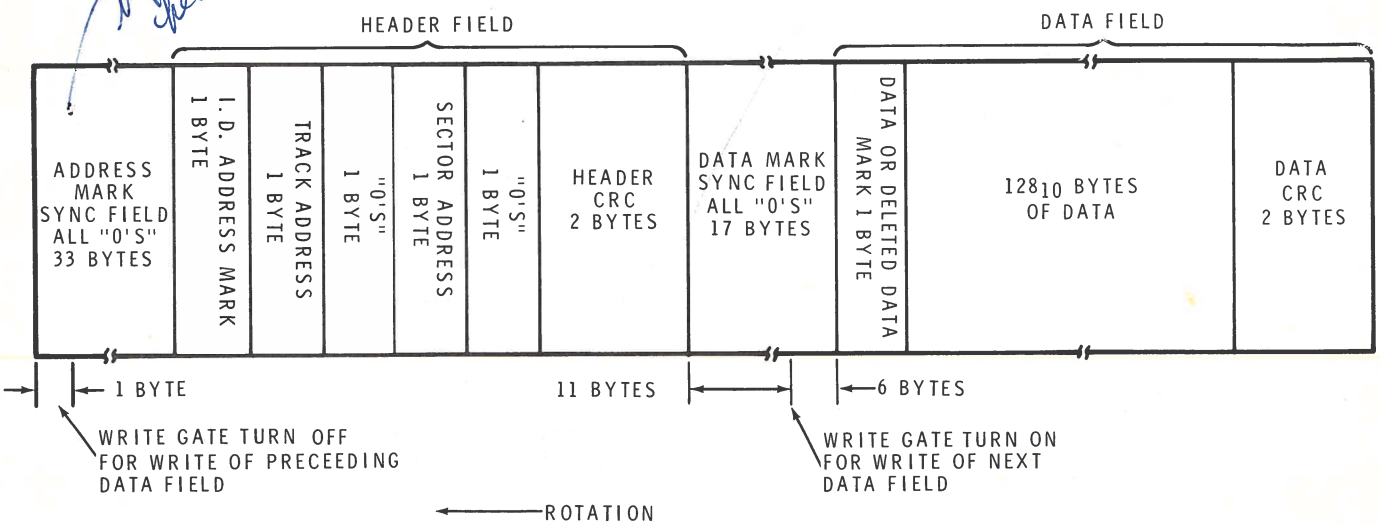
one of 77 tracks on a disk

PICTORIAL 2-3

RECORDING FORMAT

The H27 Floppy Disk System uses an industry-compatible recording format. Data is recorded on only one side of the diskette. This surface is divided into 77 concentric circles, or "tracks," numbered 0-76. Each track is divided into 26 sectors numbered 1-26 (Pictorial 2-3). Each sector contains two major fields; the header field and the data field. See Pictorial 2-4.

indicates beginning of header field



PICTORIAL 2-4

One of the 26 sectors on a track

HEADER DESCRIPTION

The header field is broken into seven bytes (eight bits/byte) of information and is preceded by a field of zeros for synchronization.

1. Byte number 1: ID Address Mark — This is a unique stream of flux reversals (not a string of data bits) that is decoded by the controller to identify the beginning of the header field.

2. Byte number 2: Track Address — This is the absolute ($0\text{-}114_8$) binary track address. Each sector contains track address information to identify its location on 1 of the 77 tracks.

3. Byte number 3: Zeros (one byte).

4. Byte number 4: Sector Address — This is the absolute binary sector address ($1\text{-}32_8$). Each sector contains sector address information to identify its circumferential position on a track.

5. Byte number 5: Sector Length — Written as one byte of zeros for a 128 byte sector length.

6. Byte numbers 6 and 7: CRC — This is the Cyclic Redundancy Check character that is calculated for each sector from the first five header bytes using a polynomial division algorithm designed to detect the types of failures most likely to occur with "double frequency" recorded data and the diskette.

DATA FIELD DESCRIPTION

The data field is broken into 131 bytes of information and is preceded by a field of zeros for synchronization and the header field (Pictorial 2-4).

1. Byte number 1: Data or Deleted Data Address Mark — This is a unique string of flux reversals (not a string of data bits) that is decoded by the controller to identify the beginning of the data field. The deleted data mark is not used during normal operation, but the H27 can identify and write deleted data marks under program control, as required. The deleted data mark is only included in the H27 system to be IBM-compatible. One or the other data address marks precedes each data field.

2. Byte numbers 2-129 — These bytes comprise the data field used to store 128 8-bit bytes of information.

   NOTE: Partial data fields are not recorded.

3. Byte numbers 130 and 131 — These bytes comprise the CRC character that is calculated for each sector from the first 129 data field bytes, using the industry-standard polynomial division algorithm designed to detect the types of failures most likely to occur in double-frequency recording on the floppy media.

TRACK USAGE

The H27 is capable of recording any system structure through the use of special systems programs, but normal operation will make use of all the available tracks as data tracks. Any special file structures must be accomplished through user software.

CRC CAPABILITY

Each sector has a two-byte header CRC character and a two-byte data CRC character to ensure data integrity. The CRC characters are generated by the hardware during a write operation and checked to ensure that all bits were read correctly during a read operation. The CRC character is the same as that used in the IBM 3740 series of equipment.

DISKETTE HANDLING PRACTICES AND PRECAUTIONS

GENERAL

To prolong diskette life and to prevent errors when recording or reading, use reasonable care when you handle the diskette. Keep the following precautions in mind to prevent unnecessary loss of data or interruptions of system operation.

1. Do not write on the envelope containing the diskette. Write any information on a label prior to affixing it to the diskette.

2. Do not use paper clips on the diskette. Most paper clips can be magnetic.

3. Do not use writing instruments that leave flakes, such as lead or grease pencils, on the jacket of the media.

4. Do not touch the disk surface exposed in the diskette slot or index hole.

5. Do not clean the disk in any manner.

6. Keep the diskette away from magnets or tools that may have become magnetized. Any disk exposed to a magnetic field may lose information.

7. Do not expose the diskette to a heat source or sunlight.

8. Always return the diskette to the envelope supplied with it to protect the disk from dust and dirt. Store diskettes not being used in a file box if possible.

9. When the diskette is in use, protect the empty envelope from liquids, dust, and metallic materials.

10. Do not place heavy items on the diskette.

11. Do not store diskettes on top of computer cabinets or in places where dirt can be blown by fans into the diskette interior.

12. If a diskette has been exposed to temperatures outside the operating range, allow five minutes for it to thermally stabilize before you use it. (The diskette must be removed from its shipping container during this time.)

DISKETTE STORAGE

Store diskettes in their envelopes in horizontal stacks of ten diskettes or less. If vertical storage is necessary, the diskettes should be supported so that they do not lean or sag, but should not be subjected to compressive forces. Permanent deformation may result from improper storage. Store diskettes in an environment similar to that of the operating system. When you do not need diskettes available for immediate use, store them within the specified non-operating environment range of the media.

SHIPPING DISKETTES

Diskettes (not originally packed with the H27) can be safely shipped in their original cartons. In general, the diskettes must be protected from magnetic fields and excessive temperatures during shipment. Good protection from magnetic fields is provided by physical separation. If you cannot use the original shipping carton, pack diskettes with at least three inches of packing material (or spacers) on both sides and along all edges. This separation will make special magnetic shielding unnecessary.

Avoid exposure of the diskettes to excessive temperatures. Label the packages with the following statement:

DO NOT EXPOSE TO PROLONGED HEAT OR SUNLIGHT.

Examine the diskette carton for damage as soon as you receive it. Deformation of the carton may indicate possible damage of the diskette(s). Retain the shipping carton (if it is intact) for diskette storage or for future shipping.

USING THE SYSTEM

OPERATION

FRONT PANEL SWITCHES

The system switch has two positions, RX-ϕ1 and EXTENDED. In the RX-ϕ1 position, the H27 is configured to be directly compatible with DEC® equipment and software. Any software designed to run on the PDP-11V03 will run on this unit. When the switch is in the EXTENDED position, additional capabilities are available which are required by the Heath Operating System.

The FORMAT switch is normally used in the OFF position. Its function allows you (from a hardware standpoint) to format (IBM 3740) a diskette. This switch only permits diskette formatting. It does not initiate it.

POWERLINE CONSIDERATIONS

If you change the position of the rear panel 120/240 switch, be sure you change fuse F1 to the proper value as follows:

For 120 VAC use a 5-ampere, 125-volt, slow-blow fuse.

For 240 VAC, use a 3-ampere, 250-volt, slow-blow fuse.

NOTE: The H27 can only be used on 60 Hz power sources.

FORMATTING A DISKETTE

To format a diskette, you must perform both a hardware operation and a software operation.

The hardware operation:

- Place the SYSTEM switch in the EXTENDED position.
- Select either of the drives and then place the FORMAT switch in the position of the drive you selected.
- Insert the diskette into the selected drive unit.

The software operation:

(This operation is performed at the console under micro-ODT.)

- Open location 177172_8 and enter 140_8. (Do this by typing 177172/140 ⏎.)
- Open location 177170_8 and enter,
  *11_8, if you selected drive 0.
  *31_8, if you selected drive 1.
- Open location 177172_8. This transfers 140_8, that you previously entered, to the controller.
- The formatting function takes approximately 30 seconds and then writes 40_8 into location 177170_8. (Repeat opening this location as necessary until a 40_8 appears.)

PROGRAMMING

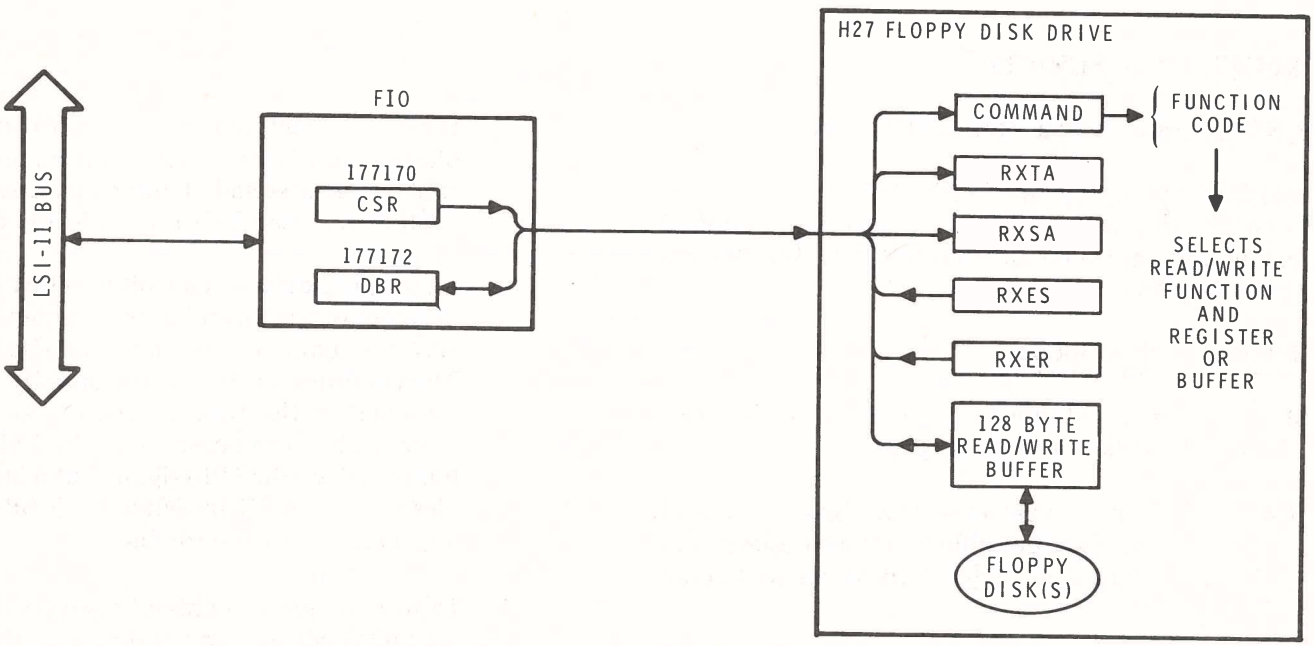
GENERAL

All software control of the FIO is performed by means of two device registers: the Command and Status register (CSR) and a multipurpose Data Buffer register (DBR). These registers can be read or loaded by programs using instructions referring to their device addresses. The H27 contains a read/write data buffer that can contain one full sector (128 bytes) of diskette data. This buffer and other H27 registers are located as shown in Pictorial 3-1. The program has direct access to the CSR and DBR registers only. Access to registers and the read/write buffer in the H27 is by the DBR.

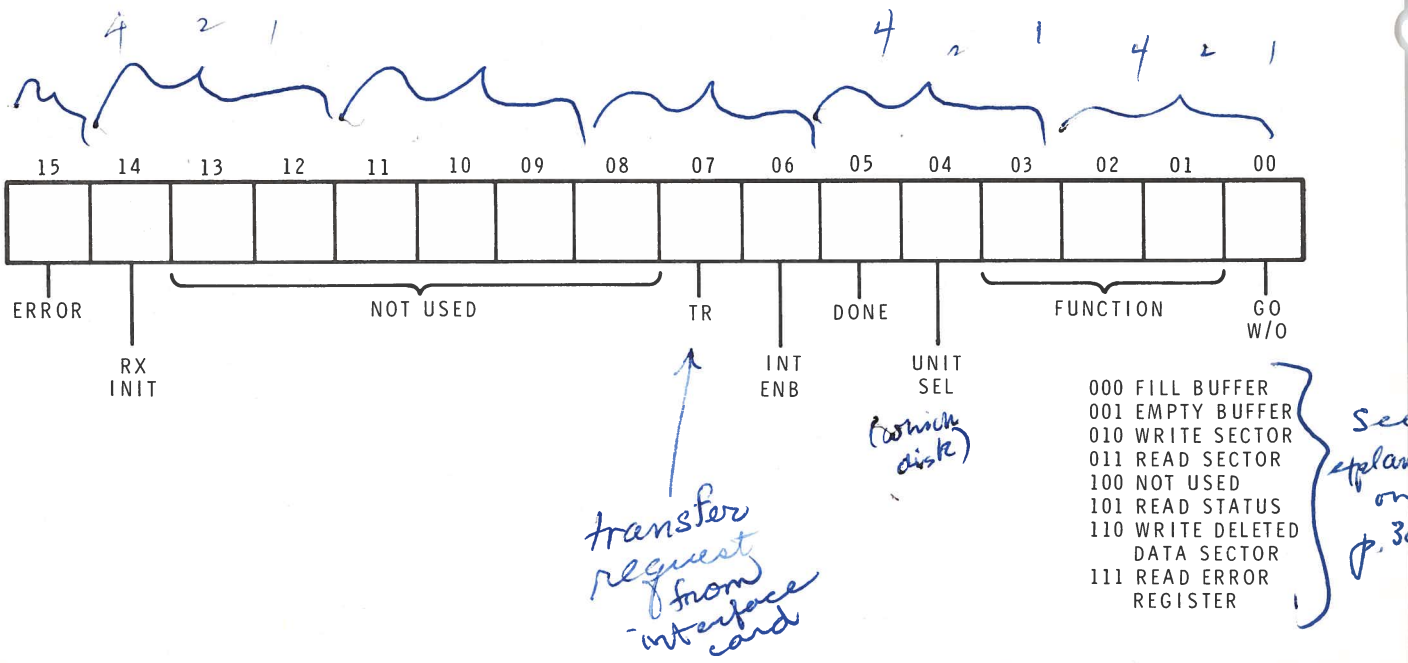
Read and write data transfers always require two steps. When writing data, the program first fills the buffer with write data by program transfers with the DBR. Once the buffer is filled, the program issues a write sector command via the CSR and the buffer's contents are written onto the diskette. During a read operation, the diskette data is first read into the buffer. The program then reads the data via the DBR.

REGISTER AND VECTOR ADDRESSES

The CSR register is assigned device address 177170_8, and the DBR register is assigned device address 177172_8. The vector address is 264_8.



PICTORIAL 3-1



PICTORIAL 3-2

REGISTER DESCRIPTION

CSR-Command and Status (177170)

Loading this register while the H27 is not busy and with bit 0=1 will initiate a function as described below and indicated in Pictorial 3-2. Bits 0-4 are write-only bits.

Bit No.	Description
0	Go — Initiates a command to the H27. This is a write-only bit.
1-3	Function Select — These bits code one of the eight possible functions described in "Function Codes." These are write-only bits.
4	Unit Select — This bit selects one of the two possible disks for execution of the desired function. This is a write-only bit.
5	Done — This bit indicates the completion of a function. Done will generate an interrupt when asserted if Interrupt Enable (CSR bit 6) is set. This is a read-only bit.
6	Interrupt Enable — This bit is set by the program to enable an interrupt when the H27 has completed an operation (Done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RX Initialize bit (CSR bit 14). This is a read/write bit.
7	Transfer Request — This bit signifies that the FIO needs data or has data available. This is a read-only bit.
8-13	Unused.

Bit No.	Description
14	RX Initialize — This bit is set by the program to initialize the H27 without initializing all of the devices on the LSI-11 Bus. This is a write-only bit.

CAUTION

1. Loading the lower byte of the CSR will also load the upper byte of the CSR.

2. Setting this bit (BIS instruction) will not clear the interrupt enable bit (CSR bit 06).

Upon setting this bit in the CSR, the FIO will negate Done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the H27 will zero the Error and Status register, set Initialize Done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 on drive 0.

15 Error — This bit is set by the H27 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the RX Initialize bit. When an error is detected, the RXES is automatically read into the DBR.

DBR-Data Buffer Register (177172)

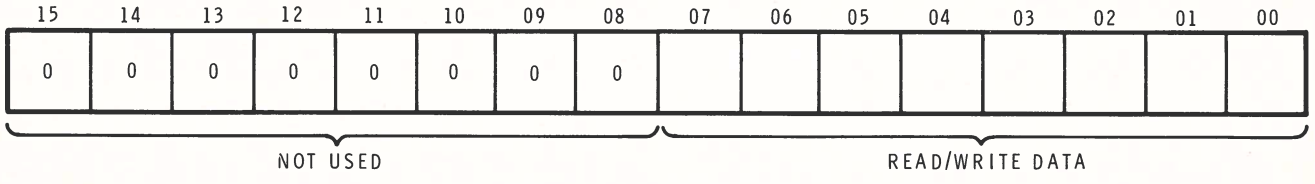
This H27 interface register serves as a general purpose data path between the H27 and the LSI-11 Bus. It may represent one of five H27 registers according to the protocol of the command function in progress. The H27 registers include DBR, RXTA, RXSA, RXES, and RXER.

This register is read/write if the H27 is not in the process of executing a command; that is, it may be manipulated without affecting the subsystem. If the H27 is actively executing a command, this register will only accept data if CSR bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

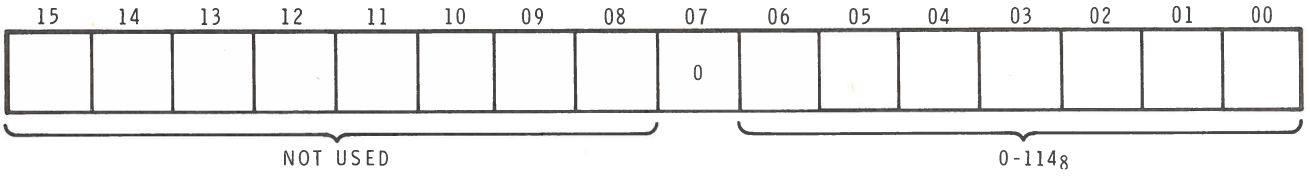
CAUTION: Violation of protocol in manipulation of this register may cause permanent data loss.

DBR-RX Data Buffer (Pictorial 3-3)

All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.



PICTORIAL 3-3



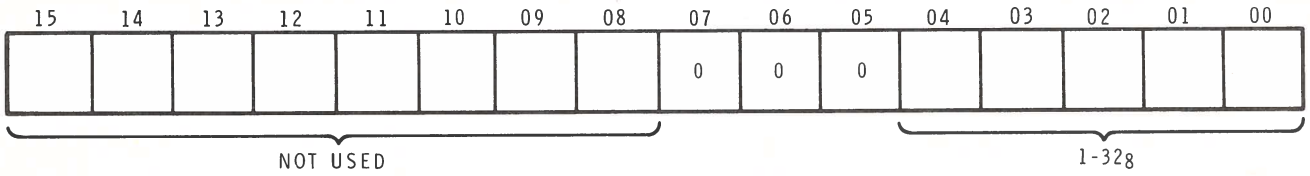
PICTORIAL 3-4

RXTA-TX Track Address (Pictorial 3-4)

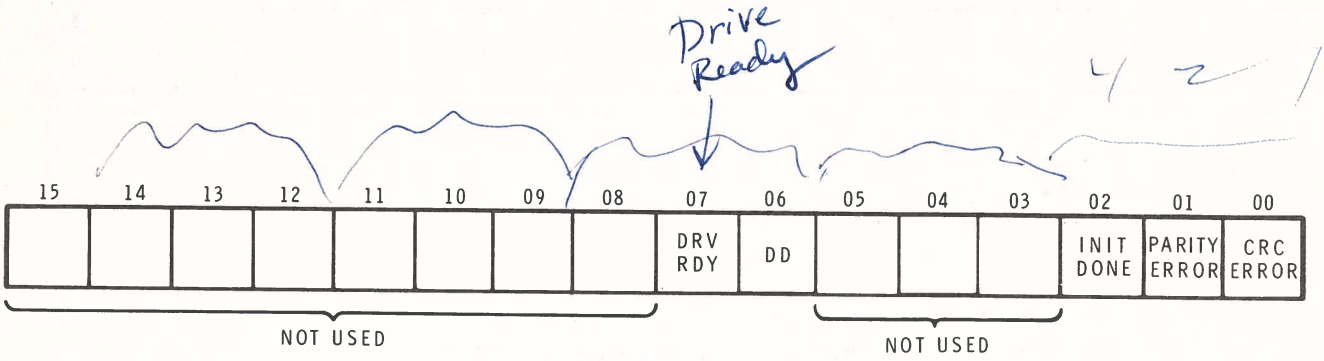
This register is loaded to indicate on which of the 114_8 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control. Bit 7 must be written as a zero.

RXSA-RX Sector Address (Pictorial 3-5)

This register is loaded to indicate on which of the 32_8 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control. Bits 5, 6, and 7 must be written as zero's.



PICTORIAL 3-5



PICTORIAL 3-6

RXES-RX Error and Status (Pictorial 3-6)

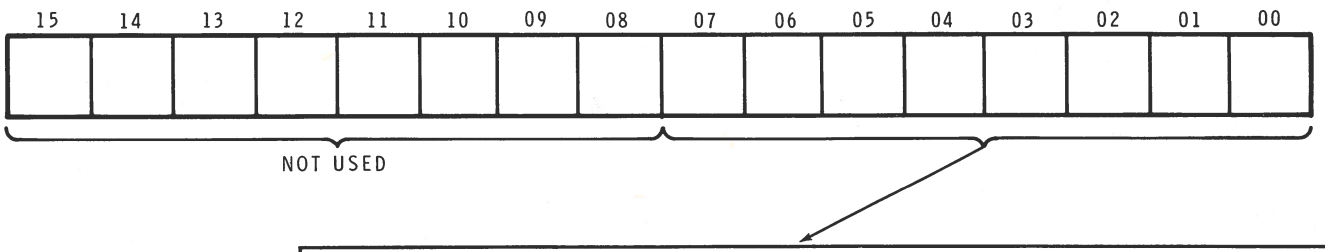
This register contains the current error and status conditions of the drive selected by bit 4 (Unit Select) of the CSR. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the DBR upon completion of a function.

RXES bit assignments are:

Bit No.	Description
0	CRC Error — A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the DBR, and Error and Done are asserted.
1	Parity Error — A parity error was detected on command or on address information being transferred to the H27 from the FIO. A parity error indication means that there is a problem in the interface cable between the H27 and the FIO. Upon detection of a parity error, the current function is terminated, the RXES is moved to the DBR, and Error and Done are asserted.
2	Initialize Done — This bit is asserted in the RXES to indicate completion of the Initialize routine, which can be caused by H27 power failure, system power failure, or programmable or LSI-11 Bus Initialize.
3-5	Unused
6	Deleted Data Detected — During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready — This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTES:

1. The Drive Ready bit is only valid when retrieved by a Read Status function or at completion of Initialize when it indicates status of drive 0.
2. If the Error bit was set in the CSR, but Error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the DBR by a Read Error Register function.



OCTAL CODE	ERROR CODE MEANING
0010	Drive 0 failed to see home on Initialize.
0020	Drive 1 failed to see home on Initialize.
0030	Found home when stepping out 10 tracks for INIT.
0040	Tried to access a track greater than 77.
0050	Home was found before desired track was reached.
0060	Self-diagnostic error.
0070	Desired sector could not be found after looking at 52 headers (2 revolutions).
0110	More than 40 μs and no SEP clock seen.
0120	A preamble could not be found.
0130	Preamble found but no I/O mark found within allowable time span.
0140	CRC error on what we thought was a header.
0150	The header track address of a good header does not compare with the desired track.
0160	Too many tries for an IDAM (identifies header).
0170	Data AM not found in allotted time.
0200	CRC error on reading the sector from the disk. No code appears in the ERREG.
0210	All parity errors.

RXER Format

PICTORIAL 3-7

RXER-RX Error (Pictorial 3-7)

This register is located in the H27 and contains specific error information. This information is normally accessed when the CSR error bit 15 is set but RXES error bits 0 and 1 are not set. This is a read-only register.

FUNCTION CODES

Data storage and recovery on the H27 system is accomplished by careful manipulation of the CSR and DBR registers according to the strict protocol of individual functions. The penalty for violation of protocol can be permanent data loss. Each of the functions are encoded and written into CSR bits 1-3, as shown in Pictorial 3-1. Programming protocol for each function is described below.

Fill Buffer (000)

This function is used to fill the H27 buffer with 128 8-bit bytes of data from the host processor. Fill Buffer is a complete function in itself; the function ends when the buffer has been filled. The contents of the buffer can be written onto the diskette by means of a subsequent Write Sector function, or the contents can be returned to the host processor by an Empty Buffer function.

CSR bit 4 (Unit Select) does not affect this function, since no diskette drive is involved. When the command has been loaded, CSR bit 5 (Done) is negated. When the TR bit is asserted, the first byte of data may be loaded into the data buffer. The same TR cycle will occur as each byte of data is loaded. The H27 counts the bytes transferred; it will not accept less than 128 bytes and will ignore those in excess. Any read of the DBR during the cycle of 128 transfers results in invalid data being transferred to the buffer.

Empty Buffer (001)

This function is used to empty the internal buffer of the 128 data bytes loaded from a previous Read Sector or Fill Buffer command. This function will ignore CSR bit 4 (Unit Select) and negate Done.

When TR sets, the program may unload the first of 128 data bytes from the DBR. Then the H27 again negates TR. When TR resets, the second byte of data may be unloaded from the DBR, which again negates TR. Alternate checks on TR and data transfers from the DBR continue until 128 bytes of data have been moved from the DBR. Done sets, ending the operation and initiating an interrupt if CSR bit 6 (Interrupt Enable) is set. RXES contents are moved to the DBR where they can be read.

NOTE: The Empty Buffer function does not destroy the contents of the sector buffer.

Write Sector (010)

This function is used to locate a desired track and sector and write the sector with the contents of the internal sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC Error, Parity Error, and Deleted Data Detected) and negates Done.

When TR is asserted, the program must first move the desired sector address into the DBR, which will negate TR. When TR is again asserted, the program must move the desired track address into the DBR, which will negate TR. If the desired track is not found, the H27 will abort the operation, move the contents of the RXES to the DBR, set CSR bit 15 (Error), assert Done, and initiate an interrupt if CSR bit 6 (Interrupt Enable) is set.

TR will remain negated while the H27 attempts to locate the desired sector. If the H27 is unable to locate the desired sector within two diskette revolutions, the H27 will abort the operation, move the contents of the RXES to the DBR, set CSR bit 15 (Error) assert Done, and initiate an interrupt if CSR bit 6 (Interrupt Enable) is set.

If the desired sector is successfully located, the H27 will write the 128 bytes stored in the internal buffer followed by a 16-bit CRC character that is automatically calculated by the H27. The H27 ends the operation by asserting Done and initiating an interrupt if CSR bit 6 (Interrupt Enable) is set.

NOTES:

1. The contents of the sector buffer are not valid data after a power loss has been detected by the H27. The Write Sector function, however, will be accepted as a valid function, and the random contents of the buffer will be written, followed by a valid CRC.

2. The Write Sector function does not destroy the contents of the sector buffer.

Read Sector (011)

This function is used to locate a desired track and sector and transfer the contents of the data field to the μCPU controller sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC Error, Parity Error, Deleted Data Detected) and negates Done.

When TR is asserted, the program must first move the desired sector address into the DBR, which will negate TR. When TR is again asserted, the program must move the desired track address into the DBR, which will negate TR.

If the desired track is not found, the H27 will abort the operation, move the contents of the RXES to the DBR, set CSR bit 15 (Error), assert Done, and initiate an interrupt if CSR bit 6 (Interrupt Enable) is set.

TR and Done will remain negated while the H27 attempts to locate the desired track and sector. If the H27 is unable to locate the desired sector within two diskette revolutions after locating the presumably correct track, the H27 will abort the operation, move the contents of the RXES to the DBR, set CSR bit 15 (Error), assert Done, and initiate an interrupt if CSR bit 6 (Interrupt Enable) is set.

If the desired sector is successfully located, the controller will attempt to locate a standard data address mark or a deleted data address mark. If either mark is properly located, the controller will read data from the sector into the sector buffer.

If the deleted data address mark was detected, the controller will assert RXES bit 6 (DD). As data enters the sector buffer, a CRC is computed, based on the data field and CRC bytes previously recorded. A non-zero residue indicates that a CRC error has occurred. The controller sets RXES bit 0 (CRC Error) and CSR bit 15 (Error). The H27 ends the operation by

moving the contents of the RXES to the DBR, setting Done, and initiating an interrupt if CSR bit 6 (Interrupt Enable) is set.

Read Status (101)

The H27 will negate CSR bit 5 (Done) and begin to assemble the current contents of the RXES into the DBR. RXES bit 7 (Drive Ready) will reflect the status of the drive selected by CSR bit 4 (Unit-Select) at the time the function was given. All other RXES bits will reflect the conditions created by the last command. RXES may be sampled when CSR bit 5 (Done) is again asserted. An interrupt will occur if CSR bit 6 (Interrupt Enable) is set.

Write Sector with Deleted Data (110)

This operation is identical to function 010 (Write Sector) with the exception that a deleted data address mark precedes the data field instead of a standard data address mark.

Read Error Register Function (111)

The Read Error Register function can be used to retrieve explicit error information contained in the RXER when the CSR error bit 15 is set. The function is initiated, bits 0-6 of the RXES are cleared, and Done is negated. The controller then transfers the specific error code from the RXER to the Interface register and completes the function by asserting Done. The DBR program can then read the error code to determine the type of failure that occurred (Pictorial 3-6).

NOTE: Be careful when you use this function since, under certain conditions, errors may result.

Power Fail

There is no actual function code associated with Power Fail. When the H27 senses a loss of power, it will unload the head and abort all controller action. All status signals are invalid while power is low.

When the H27 senses the return of power, it will begin a sequence to:

1. Move drive 0 head position mechanism to track 0.
2. Clear any active error bits.
3. Read sector 1 of track 1 of drive 0 into the sector buffer.
4. Set RXES bit 2 (Initialize Done) after which Done is again asserted.
5. Set Drive Ready of the RXES according to the status of drive 0.

There is no guarantee that information being written at the time of a power failure will be retrievable. However, all other information on the diskette will remain unaltered.

One way to abort a function is to use CSR bit 14 (RXV11 Initialize). However, this will not clear the interrupt enable bit (CSR bit 6). Another method is through the use of the system Initialize signal that is generated by the H11 RESET instruction, the console ODT Go command, or system power failure.

RESTRICTIONS AND PROGRAMMING PITFALLS

A set of restrictions and programming pitfalls for the H27 is presented below.

1. Depending on how much data handling is done by the program between sectors, the minimum interleave of two sectors may be used. However, to be safe, a three-sector interleave is recommended.
2. If an error occurs and the program executes a Read Error Register function (111), a parity error may occur for that command. The error status would not be for the error in which the Read Error Register function was originally required.
3. The DRV SEL RDY bit is present only at the time of a Read Status function (101) for both drives, and after an Initialize, depending on the status of drive 0.
4. It is not required to load the Drive Select bit into the CSR when the command is Fill Buffer (000) or Empty Buffer (010).
5. Sector Addressing: 1-26 *(No sector 0)*
   Track Addressing: 0-76

6. A power failure causing the recalibration of the drives will result in a Done condition, the same as finishing the reading of a sector. However, during a power failure, RXES bit 2 (Initialize Done) will set. Checking this bit will indicate a power fail condition.

7. Excessive usage of the Read Status function (101) will result in drastically decreased throughput, because a Read Status function requires between one and two diskette revolutions or about 250 ms to complete.

ERROR RECOVERY

There are two error indications given by the H27 system. The Read Status function will assemble the current contents of the RXES, which can be sampled to determine errors. The Read Error Register function can also be used to retrieve explicit error information from the RXER.

A list of error codes associated with the RXER is shown in Pictorial 3-7.

NOTE: A Read Status function is not necessary if the DRV RDY bit is not going to be interrogated, because the RXES is in the Interface register at the completion of every function.

IN CASE OF DIFFICULTY

This section of the Manual is divided into two parts. The first part, titled "General Troubleshooting Information," only pertains to your Floppy Disk if you built it from a kit. It describes what to do about difficulties that may occur during or right after you assemble the Floppy Disk.

The second part, titled "Troubleshooting Charts," lists problems or conditions that might occur. The "Possible Cause" column lists the components associated with the problem. This will help you relate a problem to the Schematic and Circuit Description.

Refer to the "X-Ray Views" (Illustration Booklet, Pages 2 thru 4) for the physical location of parts on the circuit boards.

Due to the complexity of the Floppy Disk drive units and the closed loop configuration of the control and interface circuit boards, we recommend that you return these parts for repair if necessary. Refer to the "Customer Service" information inside the rear cover of this Manual.

GENERAL TROUBLESHOOTING INFORMATION

This section of the Manual applies to your Floppy Disk only if you assembled it from a kit.

NOTE: The following checks will be most effective if you apply them to one part of the kit at a time.

1. Recheck the wiring. Trace each lead in colored pencil on the Pictorial as it is checked. It is frequently helpful to have a friend check your work. Some one who is not familiar with the unit may notice something you have consistently overlooked.

2. About 90% of the kits that are returned for repair do not function properly due to poor connections and soldering. Therefore, you can eliminate many troubles by carefully inspecting the connections to make sure they are soldered as described in the "Soldering" information at the beginning of the Assembly Manual. Reheat any doubtful connections. Be sure all wires are soldered at places where several wires are connected.

3. Check each circuit board foil to be sure there are no solder bridges between adjacent connections. Remove any solder bridges by holding a clean soldering iron tip between the two points that are bridged until the excess solder flows **down** onto the tip of the soldering iron.

4. Check each resistor value carefully. A resistor that is discolored, or cracked, or shows any sign of bulging would indicate that it is faulty and should be replaced.

5. Be sure each diode is carefully installed with the banded end positioned correctly.

6. Check all component leads connected to the circuit boards. Make sure the leads do not extend through the circuit board and come in contact with other connections or parts.

7. The components listed in the "Possible Cause" column of the "Troubleshooting Chart" are the most likely causes (but not necessarily the only causes) of a problem. When you check these components, look first for the following items:

   — Parts installed incorrectly or backwards. This pertains especially to diodes, electrolytic and tantalum capacitors, and integrated circuits.

   — Unsoldered or inadequately soldered parts. Reheat the connections in the area of a problem.

   — Incorrect or interchanged parts. Check the part numbers on the diodes and integrated circuits.

NOTE: In an extreme case where you are unable to resolve a difficulty, refer to the "Customer Service" information inside the rear cover of the Manual. Your "Warranty" is located inside the front cover.

Troubleshooting Chart

PROBLEM	POSSIBLE CAUSE
Fuse F1 blows. This is an indication that SCR D1 is firing.	1. +5-volt regulator malfunction. CAUTION: Disconnect power supply output cable P12 before you troubleshoot the +5-volt regulator. 2. Overvoltage sense circuitry malfunction. 3. SCR D1.
Improper +12 volts.	1. Output too high; check U3. 2. Output too low. This can be caused by U3 or excessive current being drawn from the +12-volt regulator. Check for shorts on the output side of the +12-volt regulator.
Improper −12 volts.	1. Output too high; check U4. 2. Output loo low. This can be caused by U4 or excessive current being drawn from the −12-volt regulator. Check for shorts on the output side of the −12-volt regulator.
Improper +24 volts.	1. No output voltage; Q5 or U2. 2. Output excessively high; Q5, Q4, or U2.
Improper +5 volts.	1. Q1 or U1.

CONFIGURING THE DRIVES

If you replace or change either drive mechanism, make sure they are configured as explained below.

DRIVE 0

Refer to Pictorial 4-1 (Illustration Booklet, Page 2) and make sure the jumper block is plugged onto the DS1 pins. Also, make sure the IC resistor pack is installed in socket 2F.

DRIVE 1

Refer to Pictorial 4-2 (Illustration Booklet, Page 2) and make sure the jumper block is plugged onto the DS2 pins. Also, make sure the IC resistor pack has been removed from socket 2F.

CIRCUIT DESCRIPTION

Refer to the Schematic Diagrams while you read this "Circuit Description."

POWER SUPPLY

The power supply provides the DC operating power for the Floppy Disk. It can operate from either a 120 VAC, 60 Hz or a 240 VAC, 60 Hz power source.

PRIMARY CIRCUITS

Dual primary windings in the transformer permit both 120 VAC and 240 VAC operation. Switch SW2 connects the two primary windings in parallel for 120 VAC operation. Both fans and the Floppy Disk units are across the 120 VAC primary power line.

When switch SW2 is in the 240 VAC position, the transformer primaries are connected in series. Likewise, the two fans and the Floppy Disk drives are connected in series. The transformer primaries now function as a single center-tapped winding. This configuration insures that each fan motor and Floppy Disk drive receives one-half of the 240 VAC primary line voltage.

One multi-tapped secondary winding supplies AC power for the rectifiers and filters. A conventional full-wave rectifier, D21, and filter capacitor, C23, rectify and filter the AC to produce a 30-volt DC source for the +24-volt and the +5-volt regulator circuits. Another conventional full-wave rectifier, D22 and D23, and filter capacitor, C24, provide −20-volts for the −12-volt regulator circuits.

REGULATOR CIRCUITS

Transistors Q5 and Q4 form a complementary Darlington pair which serve as the pass element for the +24-volt regulator. Integrated circuit U2 is the controller for the pass element. The voltage at pin 6, which is a constant ratio of the output voltage, is compared with an internally generated reference voltage of approximately +1.75 volts. The difference is amplified and appears on pin 2. The resistor, R15, between pins 1 and 8 of U2 is a current-sensing resistor. When the voltage across this resistor exceeds approximately 350 mV, U2 begins to reduce the output voltage from the regulator. Thus limiting the current available from the supply.

The +5-volt regulator is a switching regulator that operates at approximately 40 kHz. The main controlling element is an adjustable, low-power, linear voltage regulator, U1, with external feedback to insure oscillation. Transistor Q1 acts as a switch to supply current to the output filter, L1, C8, C9, and C10.

Capacitors C3 and C6 change the circuit from a conventional linear regulator to a switching regulator. Assume that Q1 is turned on. The current flowing through R3 also flows through R4, causing the voltage at pin 5 to increase by approximately 140 mV, due to the coupling of C3. During this time, a DC current

flows through L1 and R9 to supply the +5-volt output. U1 compares the voltage at pins 5 and 6 and produces an error current at pin 2. Since the voltage at pin 5 increased, the error current at pin 2 must increase, thus increasing the drive to pass element Q1. As a result, the current through L1 increases, causing an increase in the voltage drop across R9. Capacitor C6 then couples this voltage change to pin 6 of U1. When the voltage at pin 6 exceeds the reference voltage at pin 5, the error current at pin 2 decreases. The gain of U1 is extremely high, consequently, only a few millivolts difference is required between pins 5 and 6 in order to turn Q1 from on to off.

As Q1 turns off, the 140 mV offset is removed from pin 5 of U1. The voltage at pin 1 of Q1 rapidly decreases (due to the flyback action of L1) until the catch diode (internal to Q1) turns on at −1 volt. L1 now begins releasing its stored energy through R9 to the load. As this energy is used by the load, the current through R9 decreases. The changing voltage across R9 is coupled though C6 to pin 6 of U1. When the voltage at pin 6 decreases to a few millivolts below the reference voltage at pin 5, transistor Q1 turns back on and the cycle is repeated.

Transistor Q2 detects the DC current through R9 and turns on when it exceeds approximately 3.5 amperes. This turns the regulator off via pin 7 of U1.

The −12-volt regulator, U4, incorporates an internal current-limiting feature. The +12-volt regulator, U3, also has current-limiting, although it is a lower power device. Its input power is supplied by the +24-volt regulator circuit.

OVERVOLTAGE PROTECTION CIRCUITRY

The +5-volt overvoltage circuitry uses a zener diode, ZD3, as the detector. When the output of the +5 volt regulator exceeds 6.2 volts, ZD3 begins to conduct and current flows through R10. This causes a voltage differential to develop between the gate and anode of Q3. Therefore, Q3 turns on, firing SCR D1. This places a short across the +30 volt line, which opens fuse F1. Resistor R8 limits the gate current of Q3, and capacitor C7 prevents Q3 from conducting as a result of the voltage spikes during normal regulator switching. Resistor R1 limits the gate current of SCR D1 to safe levels, while diodes D2 and D4 prevent reverse voltages from developing across the pass elements when SCR fires.

FLOPPY I/O MODULE

The Floppy Interface Module (FIO) interfaces the H11 16-bit bus to the H27 8-bit bus. In addition, it contains the interrupt arbitration logic, ROM bootstrap logic, and address decoding logic that are required by the H11.

GENERAL

Bus transceivers, U1, U2, U3, and U4, isolate the time-multiplexed data-address lines of the H11 but from the interface circuits. Bus receiver U6 and bus driver U5 perform a similar function on the bus control lines. U20, U21, U22, and U23 isolate the H11/H27 interface bus from the interface circuits. U20, U21, and U22 have additional functions which will be explained later.

ADDRESS DECODING

The Control Status Register (CSR) is located at address 177170_8. The Data Buffer Register (DBR) is located at address 177172_8. These two addresses are decoded by comparator U11 and U12 during the addressing portion of the H11 bus cycle. If a match occurs, FDE H is asserted high and this information is retained during the bus cycle while SYNC H is asserted high. Address bit 1 (AL1 L), which is latched by U9, determines whether the CSR or DBR has been addressed.

The bootstrap ROM (U13, low-byte and U8, high-byte) is located at addresses 173000_8 to 173776_8 and 165000 to 165776_8. These addresses are decoded by comparator U7. If a match occurs, RME H is asserted high and this information is retained during the bus cycle while SYNC H is asserted high. The 8-bit latch, U9, stores the particular address within the range of ROM addresses which are required for that particular bus cycle.

Decoder U14 receives the FDE H, RME H, and AL1 L signals and combines them with the data-in request (DIN H) and data-out request (DOUT H) control signals to determine which of its outputs should be asserted. The SYNC signal at pin 15 inhibits any output from being asserted until SYNCL is asserted low. The outputs from this decoder furnish the bus reply (RPLY L) signal required by the H11, turn on the bus drivers when required (XMIT L), enable the bootstrap ROM outputs (RMCS L), select the CSR (SEL 0 OUT L and SEL 0 IN L), select the DBR (SEL 2 OUT L and SEL 2 IN L), and clear the data transfer flip-flop (SEL2 L).

serted. The SYNC signal at pin 15 inhibits any output from being asserted until SYNC L is asserted low. The outputs from this decoder furnish the bus reply (RPLY L) signal required by the H11, turn on the bus drivers when required (XMIT L), enable the bootstrap ROM outputs (RMCS L), select the CSR (SEL ø OUT L and SEL ø IN L), select the DBR (SEL 2 OUT L and SEL 2 IN L), and clear the data transfer flip-flop (SEL 2 L).

CONTROL STATUS REGISTER (CSR) — 177170_8

Of the 16 bits available, only 10 bits are used in this register. Of these 10 bits, 6 are write only, 3 are read only, and only one is both read and write. Latch U28A handles this bit (INT ENB H). It is asserted when DAL6 L is asserted coincident with SEL ø OUT H.

The write-only bits (DAL ø L, DAL 14 L, DAL 1 L, DAL 2L, DAL 3 L, and DAL4 L) are latched by U26B, U26A, and U22 respectively whenever these bits are asserted coincident with SELø OUT L.

The read-only bits (DONE (ø) H-RD5 L, TR H-RD7 L, ERROR H-RD15 L) and the read-write bit (INT ENB H-RD6 L) are read by the H11 whenever SELø IN L is asserted low. U15 handles this function.

When SEL ø OUT L is asserted coincident with DALø L, U26B is toggled, setting pin 9-low. This negates DONE (ø) H via U24B and U18 and forces pin 1 of Q19A high; Thus, allowing U19A to be toggled when WS L is asserted. U26B, once toggled, remains set until U19A toggles. This lockout feature results by virtue of the feedback from pin 9 of U26B to pin 12 of U25D. Thus, U26B can only be reset by toggling U19A, which causes pin 10 of U26B to be asserted low. Resetting U26B, asserts DONE (ø) H and resets U19A. U19A is now inhibited from toggling, since pin 1 is held low.

U26A operates in a similar manner; however, it can be set in two different ways. First, by asserting SEL ø OUT L coincident with DAL14 L and, second, by asserting INIT L. The first method is identical with U26B, except DAL14 L is used rather than DAL ø L.

The second method uses the bus initialize signal (BINIT L) to directly force U26A's outputs to a set status. The rest of the cycle is the same as method 1.

DATA BUFFER REGISTER (DBR) — 177172_8

Of the 16 bits available, only the low byte is used. The H11 can both read and write to it. U20 is an 8-bit latch which is the write part of the buffer. Data will be written (latched) when SEL 2 OUT L is asserted low. The read operation is handled by U21. Data will be read when SEL 2 IN L is asserted.

INTERRUPT LOGIC

When DAL6 L is asserted low coincident with SELø OUT H, U28A is set (pin 6 goes high). This enables the FIO interrupt logic. As soon as DONE (ø) H is asserted, U28B toggles and pin 9 goes high. U27B's inputs are now all high; thus, an interrupt request (IRQ H) is generated and passed to the H11 bus via U5C. When the H11 acknowledges the request by asserting BDIN L; U10B toggles, which inhibits the acknowledge signal, IAKIH, from propagating U5D to lower priority modules. Assertion of IAKI H causes VECTOR L to be asserted low, initiating BRPLY L and placing the vector interrupt address on the H11 bus via U15. VECTOR L also clears U28B, negating IRQ H. The INT ENB H remains set. It can only be negated by either asserting INIT L or asserting SEL ø OUT H, while not asserting DAL6 L.

H27 HANDSHAKE LOGIC

When the H27 wishes to communicate with the H11, it does so by asserting one of four control lines: ZRS L, ZWS L, ZRD L, and ZWD L. Asserting ZRS L enables U23's and U22's outputs via U25B. This places the CSR on the interface bus data lines, ZBø-7 L, so that it can be read by the H27. Asserting ZRD L enables U20's output; thus placing the DBR on the interface data lines so that it can be read by the H27. Data is written into the DBR (U21) from the H27 when ZWD L is asserted. By asserting ZWS L, the H27 can also write to the CSR.

H11-H27 DATA TRANSFER

In order to facilitate rapid data transfers between the H11 and the H27, a synchronizing handshake is utilized. The H11 continuously interrogates bit 7 of the CSR (TR H). Then, depending on the operation being performed, the H11 either transfers data to or

data from the Floppy Interface circuit board when this bit is set. Transferring the data negates TR H U19B. The TR H signal is set by the H27, which results in the H27 forcing itself into a wait state by assertion of Z WAIT L. When the H11 negates TR H, and thus Z WRIT L, the H27 exits the wait state and another data transfer cycle begins.

When ZB7 L is asserted low coincident with ZWS L, U17B is set. This sets pin 12 of U19B high. If the DBR is accessed by either asserting ZRD L or ZWD L, U19B is set, resulting in TR H being asserted high and Z WAIT L assert low, via U18. When the H11 accesses the DBR, thereby asserting SEL 2 L, a 100 ns pulse is applied to pin 13 of U19B via U25A. This resets U19B and negates TR H and Z WAIT L. As long U17B remains set, U19B will set whenever the H27 accesses the DBR by asserting either ZRD L or ZWD L.

U17B can be reset by either of two methods: 1. Asserting ZWS L while negating ZB7 L; or 2. Asserting RX INIT L. Method 1 is used as part of the normal operating firmware in the H27. However, if TR H is asserted, this method cannot be used since the H27 is in a wait state.

Method 2 is a forced reset, since it also resets U19B: thus negating TR H. It causes the H27 to reset, resulting in the immediate cessation of any previous operation. This method is controlled by the H11.

MISCELLANEOUS

When the H11 writes to the CSR, the DBR reflects the just-written data. This is accomplished via U24C, U24D, and U25B. Asserting SEL 0 OUT H enables U24's and U22's outputs and toggles U21's inputs. Thus reflecting the CSR data into the DBR. However, if DAL 0 L or DAL 14 L is asserted coincident with SEL 0 OUT H, then DONE H is negated. Approximately 100 ns later, pin 9 of U24C goes low and inhibits any further SEL 0 OUT H transitions from writing data to the CSR. This function is restored when the H27 asserts DONE H coincident with ZWS L, which asserts DONE (0) H.

FLOPPY DISK CONTROLLER

The controller utilizes two MOS LSI integrated circuits to handle the routing of data between the H11 and the floppy disk drives. These IC's are a Z80 microprocessor, U117, and a 1771 floppy disk controller/formatter, U107. A crystal-controlled oscillator supplies precise timing signals for these IC's in order to meet IBM 3740 formatting requirements.

OSCILLATOR AND CHARGE PUMP

Inverters U104D and U104E, in conjuction with crystal Y101 form a 4 MHz crystal-controlled oscillator. R102, R103, and C102 form a low-pass negative feedback loop around U104D. This loop forces U104D to operate in its linear region while the low-pass feature of the loop inhibits spurious high frequency oscillations due to the delay of U104D. U105B divides the signal by two, resulting in a 2 MHz clock signal (CLK L) as required by U107.

Inverter U104F acts as a buffer between the divider and the charge pump. When pin 12 of U104F is high, C103 charges through D101 to approximately +10 volts. When pin 12 of U104F is low, C103 charges C104 through D102 to approximately −8 volts. Q01 regulates the +8 volts across C105 to −5 volts.

PROCESSOR

U118 decodes the high-order address lines during a memory cycle. Firmware ROM U121 is selected by CS1 L only if A15 H is not asserted. Thus, U121 is located in the lower 32K memory locations. Decoder U127 is used to decode the low byte address lines during an I/O read cycle, and decoder U126 is used to decode the low byte address lines during an I/O write cycle.

FLOPPY DISK CONTROLLER/FORMATTER

The various signals required by the floppy disk drive are furnished by U107. Its specific functions include:

1. Locating the disk read/write head over the proper track and sector.

2. Engaging the head against the disk at the proper time for read and write operations.

3. Transmitting serialized data (properly timed) to the drive.

4. Converting received serial data from the drive into byte format.

5. Generating CRC for the write data and checking CRC for the read data.

6. Providing the H11 with error information in case of a fault.

In order to insure that no data will be lost during transfers to and from U107, U117 is put in a wait state during each transfer. U108C, U111A, and U108D decode the data lines from U117, such that pin 2 of U105A is asserted whenever the data pattern corresponds to a disk read or write command. U108A decodes address lines A0 H and A1 H, such that U109C is only enabled when U107's command register is being addressed. Thus, a disk read or write command toggles U105A which sets pin 5 of U105A high. This toggles U112B which asserts pin 2 of U112A high. This inhibits the CTRL WR L and CTRL RD L signals from propagating to U107.

The processor, U117, immediately after issuing a disk read or write command to U107, begins a data read or write (depends on command) cycle. This asserts CTRL CS L, which toggles U112A; thus setting pin 5 of U111B low and asserting WAIT L low. This forces U117 into a wait state. The wait state is cancelled and the data read or write cycle completed when U107 asserts pin 5 of U108B high. This resets U112A, negating WAIT L. The processor, U117, then initiates another data read or write cycle, which forces another wait state. This process continues until all the data bytes have been transferred: at which time, U107 asserts pin 39 high. This action resets U112B and U112A and asserts INT L low. Assertion of INT L causes a processor interrupt, which terminates the present command.

DC POWER START

When DC power is first applied to the control logic, C110 begins to charge. Until C110 reaches approximately +2.5 volts (250 ms) pin 10 of U122C is held high. Thus, pin 4 of U122B is low; thereby insuring that U117, U107, and U114 remain reset until proper DC voltages have been established.

Gates U122D and U122A form a cross-coupled R-S flip-flop. When DC power is applied to the controller, pin 11 of U122D is low since C110 has not yet charged to +2.5 volts. Once RESET L is negated, U117 interrogates port 354_8 (SR RD L), U119. Since pin 11 of U122D is low, D2 H remains negated. This informs the processor that a DC power-up has just occurred. The processor then performs a diagnostic test on RAM and sets up its stack and interrupt routines. Once these operations are complete, U117 writes to port 354_8 (U114) (asserts DVS L), setting OUT 5 H. This sets R-S flip-flop (U122A and U122D) output, pin 11, high.

A reset can be initiated by the H11 by asserting Z INIT L. However, if a disk write operation is being performed (WG H asserted high), reset is deferred until completion of the write operation. This is accomplished by U113B and U123A.

SEMICONDUCTOR IDENTIFICATION

This section is divided into two parts; "Component Number Index" and "Part Number Index." The first section provides a cross-reference between semiconductor component numbers and their respective Part Numbers. The component numbers are listed in numerical order.The second section provides a lead configuration detail (basing diagram) for each semiconductor Part Number. The Part Numbers in the second section are also listed in numerical order.

COMPONENT NUMBER INDEX

This index shows the Part Number of each semiconductor in the Floppy Disk.

CHASSIS MOUNTED PARTS

Diodes

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D21	57-611
D22	57-65
D23	57-65

POWER SUPPLY

Diodes

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D1	57-86
D2	57-65
D3	56-58
D4	57-65

Transistors

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q1	417-895
Q2	417-821
Q3	417-823
Q4	417-819
Q5	417-856

Integrated Circuits

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U1	442-24
U2	442-24
U3	442-644
U4	442-664

INTERFACE CIRCUIT BOARD

Transistors

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q1	417-821

Integrated Circuits

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U1-U4	443-868
U5	443-77
U6	443-860
U7	443-866
U8	444-22
U9	443-837
U10	443-730
U11-U12	443-866
U13	444-21
U14	444-20
U15	443-754
U16	443-728
U17	443-730
U18	443-754
U19	443-730
U20	443-863
U21-U22	443-837
U23	443-754
U24	443-728
U25	443-780
U26	443-730
U27	443-864
U28	443-730

Resistor Packs

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
RP1-RP3	9-86

CONTROLLER CIRCUIT BOARD

Diodes

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D101-D102	56-56

Transistors

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q101	442-665

Integrated Circuits

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U101	443-824
U102	443-727
U103-U104	443-73
U105	443-6
U106	443-73
U107	443-876
U108	443-780
U109	443-875
U111	443-780
U112	443-730
U113	443-779
U114	443-879
U115	444-30
U116	443-880
U117	443-881
U118	444-26
U119	443-824
U121	444-27
U122	443-703
U123	443-727
U124-U125	443-764
U126-U127	443-887
U128	443-864

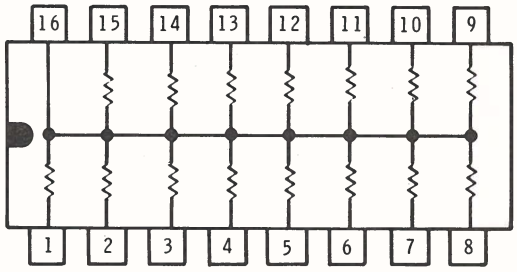
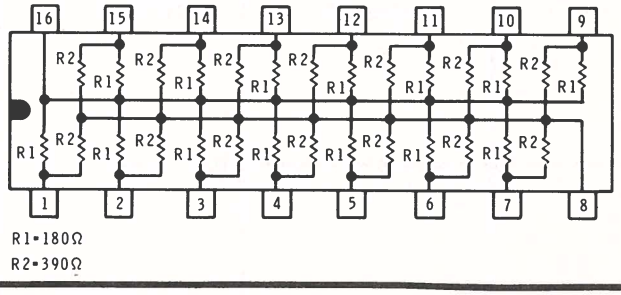
Resistor Packs

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
RP1	9-87
RP2	9-86

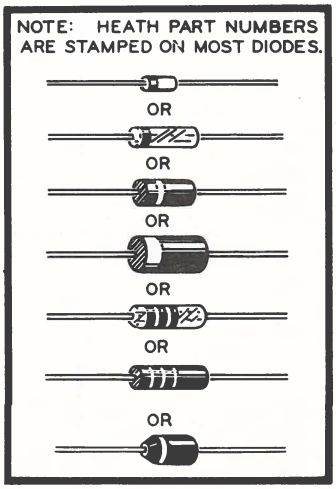
PART NUMBER INDEX

This index shows a load configuration detail (basing diagram) of each semiconductor Part Number.

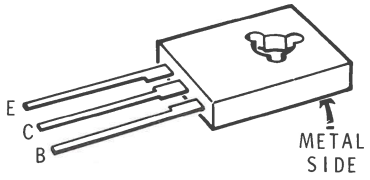
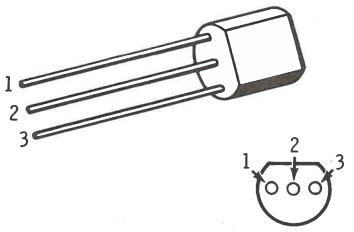
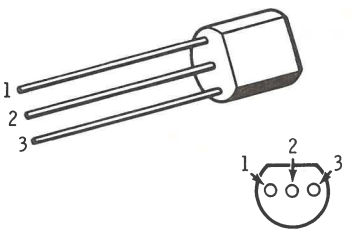
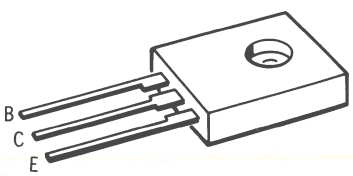
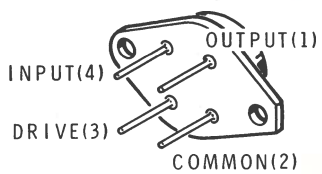
RESISTOR PACKS

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
9-86		680Ω RESISTOR NETWORK	
9-87		180Ω/390Ω RESISTOR NETWORK	

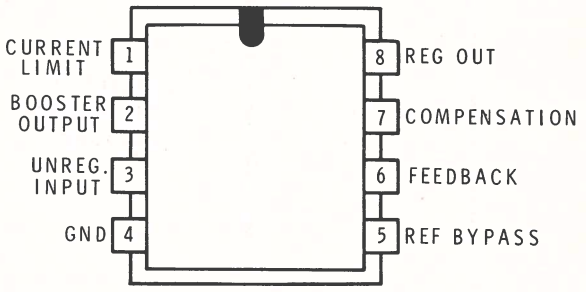
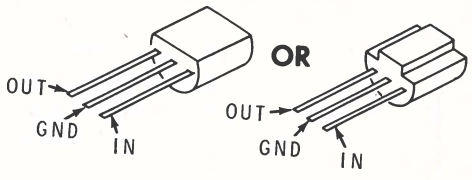
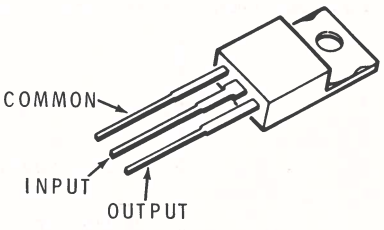
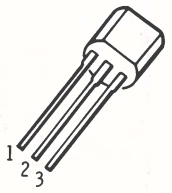
DIODES

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
56-58	1N709A	ZENER 6, 2 V, 25 mA	
57-65	1N4002	S I RECT 1A, 1000 V	
57-86	NLS76A	SCR 55A, 100 V	
57-611	SR711	SI RECT 30A, 100 V	
56-87	FH1100	SI RECT 10 mA, 5 V	

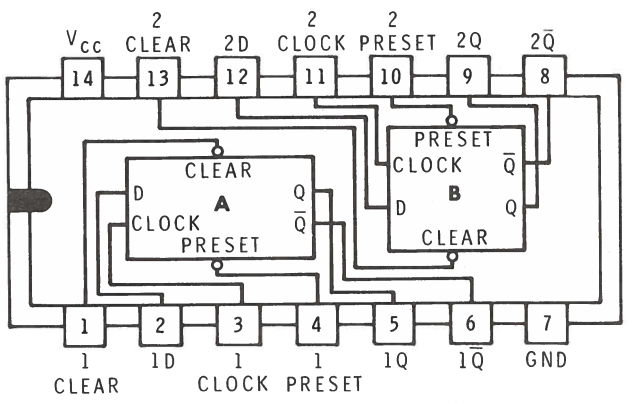
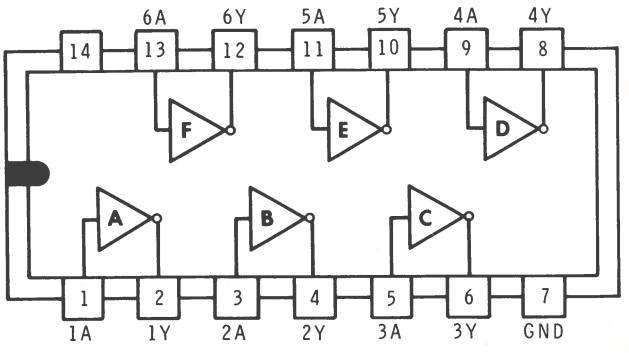
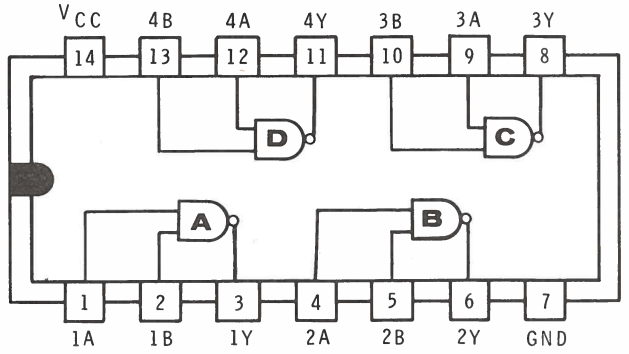
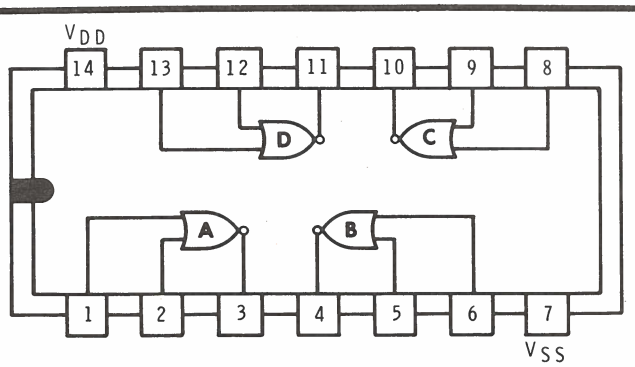
TRANSISTORS

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
417-819	MJE171	TRANSISTOR	
417-821	MPSA06	TRANSISTOR	
417-823	MPU131	TRANSISTOR	
417-856	MJE5979	TRANSISTOR	
417-895	PIC625	TRANSISTOR	

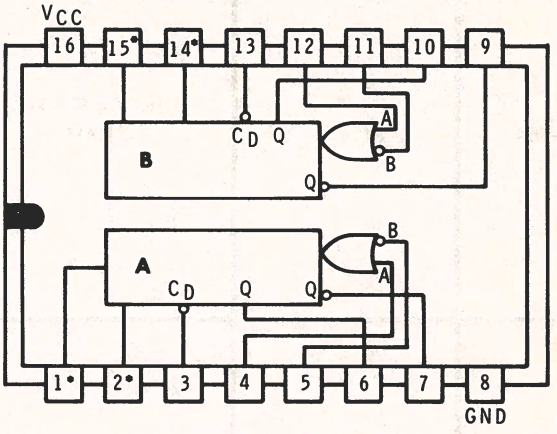
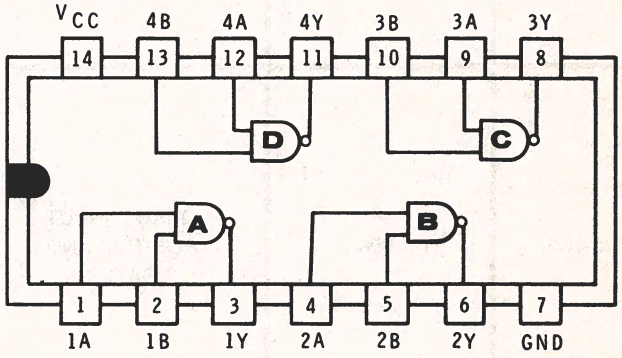
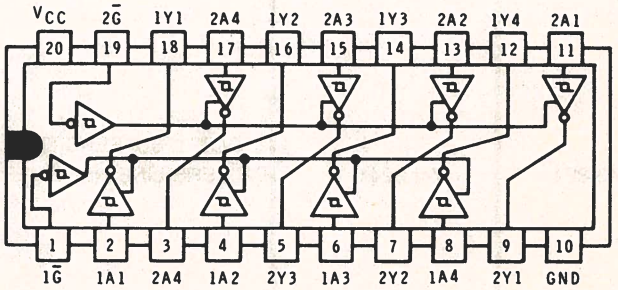
INTEGRATED CIRCUITS

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
442-24	LM376	+4.5 to 40 VOLT VOLTAGE REGULATOR	
442-644	78L12	12-VOLT REGULATOR	
443-664	79M12	−12-VOLT REGULATOR	
443-665	79L05	−5-VOLT REGULATOR	 1 GROUND 2 INPUT 3 OUTPUT

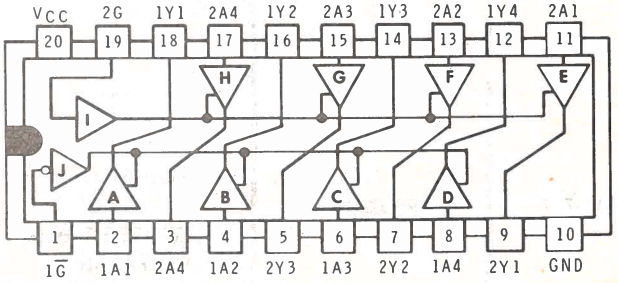
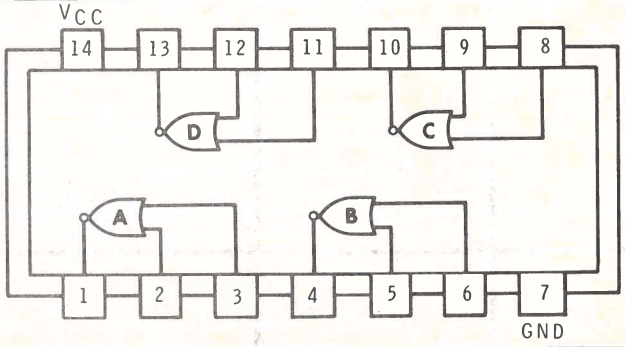
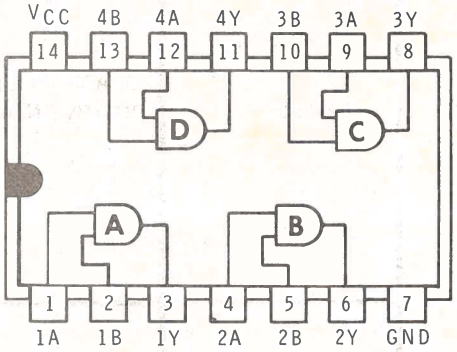
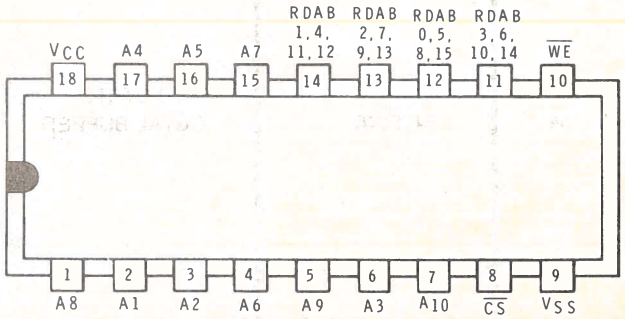
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-6	7474N	DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP	
443-73	7416	HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS	
443-77	7438	QUAD 2-INPUT POSITIVE NAND BUFFERS	
443-703	14001	QUAD 2-INPUT NOR GATE	

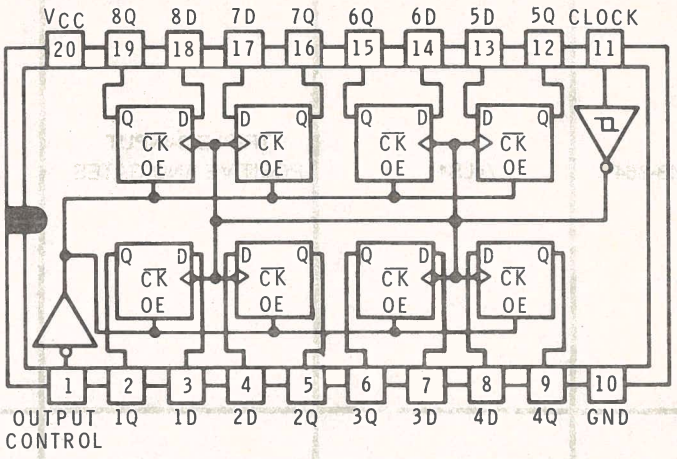
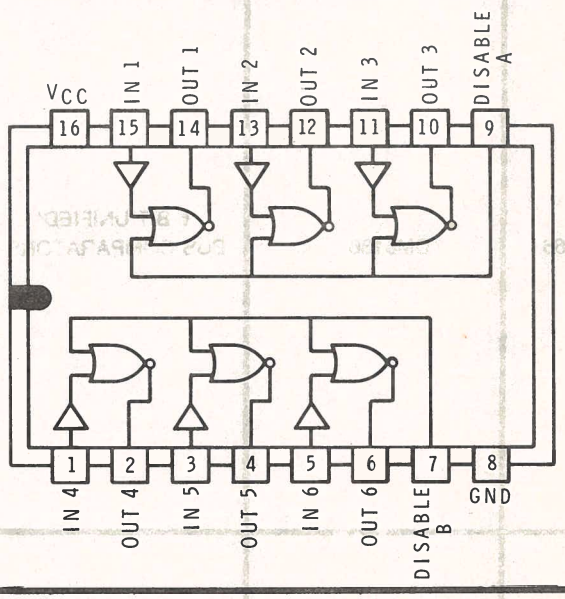
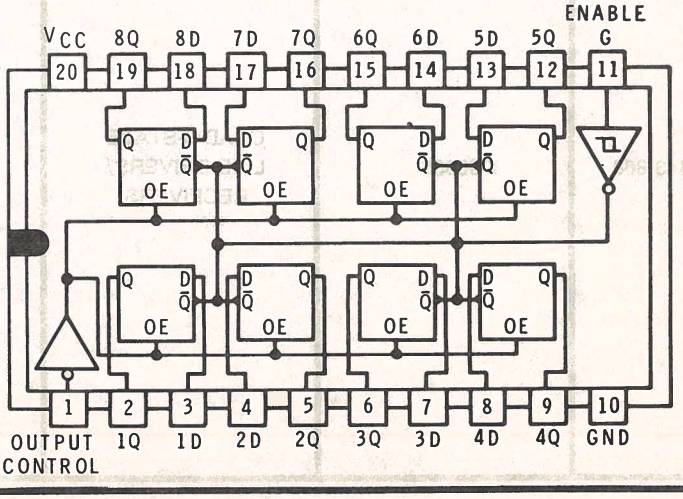
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-727	96L02	LOW POWER DUAL RETRIGGERABLE, RESETTABLE, MONOSTABLE MULTIVIBRATOR	 *PINS FOR EXTERNAL TIMING.
443-728	74LS00	QUADRUPLE 2-INPUT POSITIVE-NAND GATE	
443-754	74LS240	3-STATE OCTAL BUFFER	

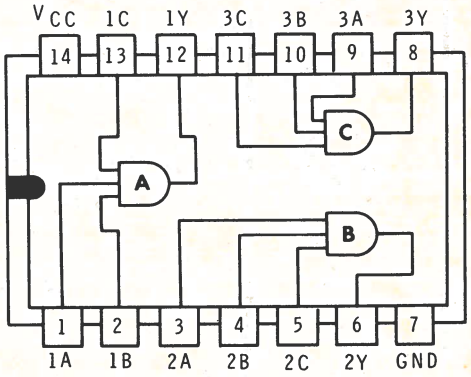
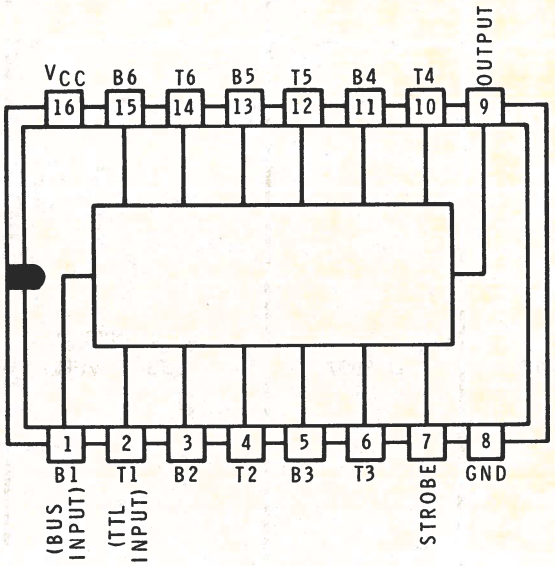
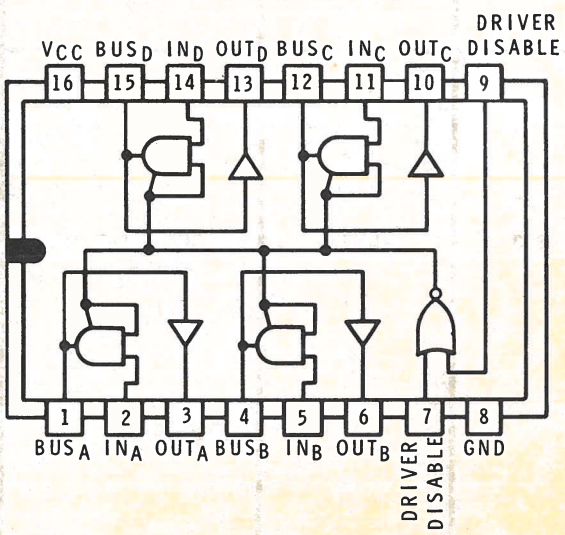
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-764	2114	1K × 4 STATIC RAM	
443-779	74LS02	QUAD 2-INPUT POSITIVE NOR GATES	
443-780	74LS08	QUAD 2-INPUT POSITIVE AND GATES	
443-824	74LS241	OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS	

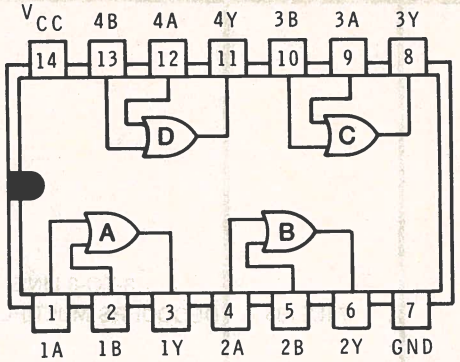
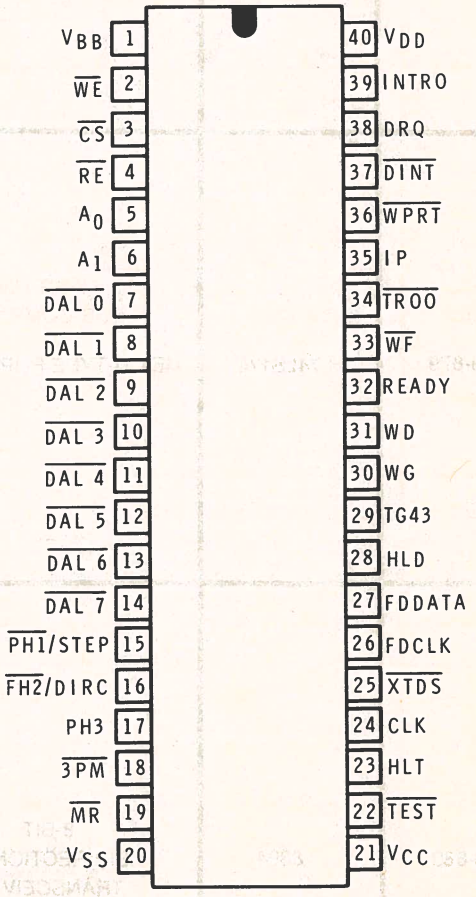
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-837	74LS373	OCTAL D-TYPE LATCHES	
443-860	DS8837	HEX UNIFIED BUS DRIVER	
443-863	74LS374	OCTAL D-TYPE FLIP-FLOPS	

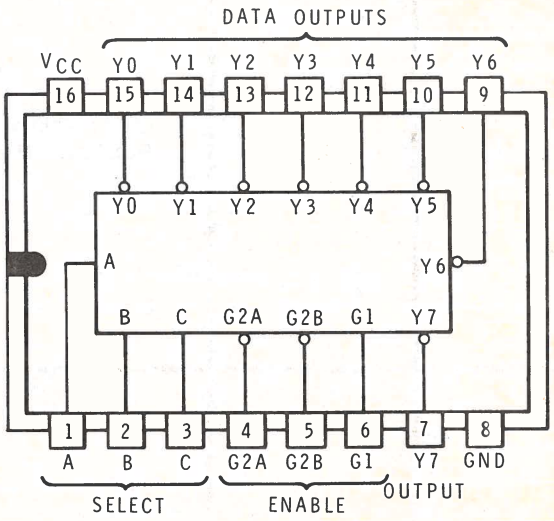
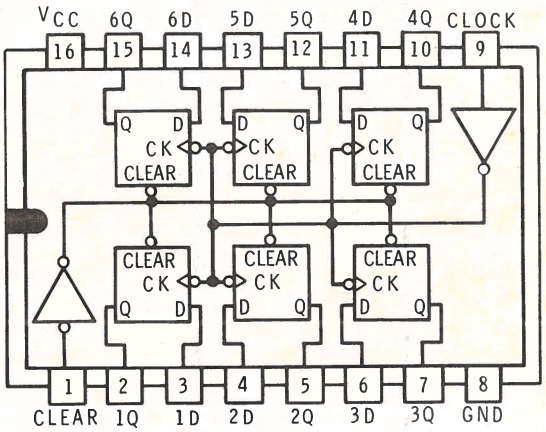
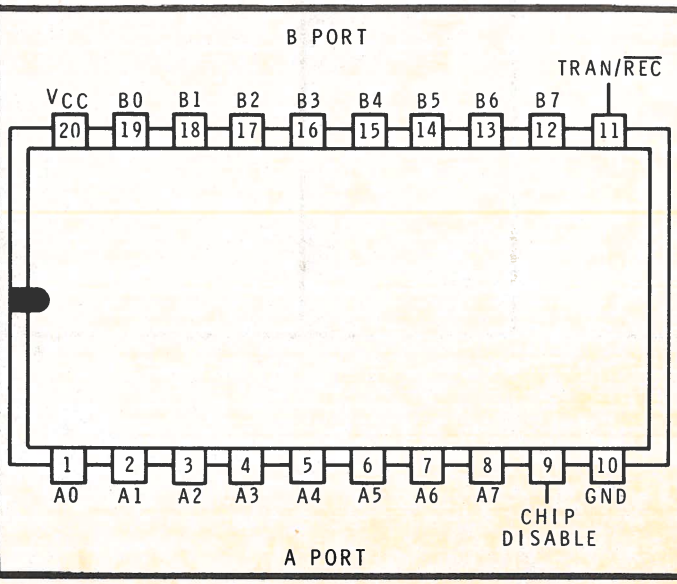
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-864	74LS11	TRIPLE 3-INPUT POSITIVE AND GATES	
443-866	DM8136	6-BIT UNIFIED BUS COMPARATORS	
443-868	DS8839	QUAD 3-STATE LINE DRIVERS/ RECEIVERS	

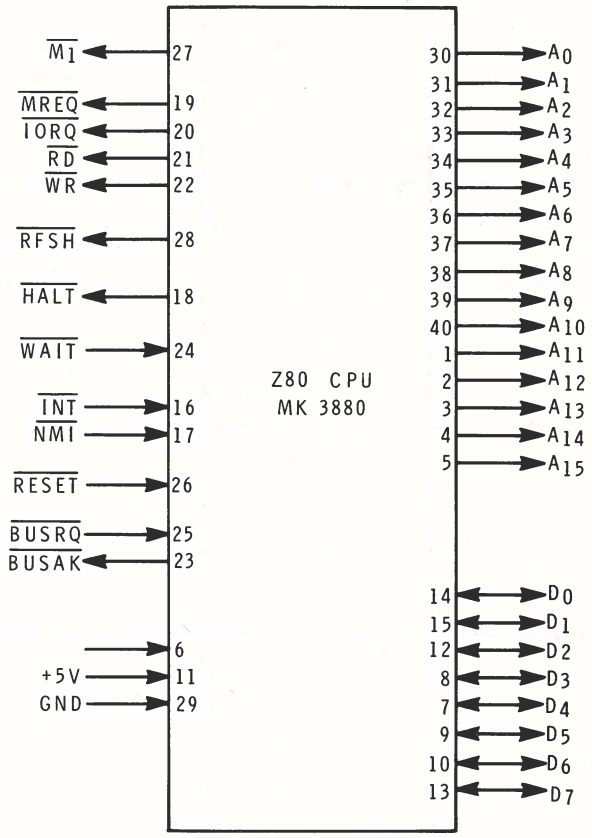
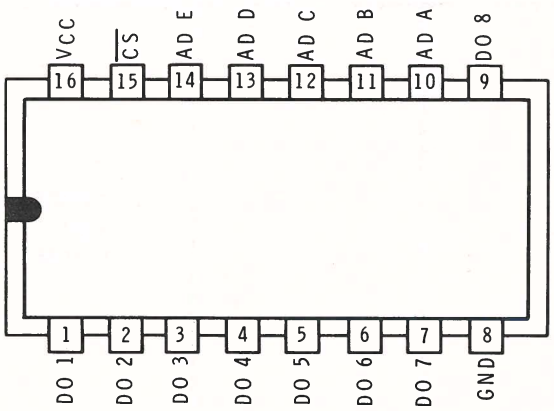
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-875	74LS32	QUADRUPLE 2-INPUT POSITIVE-OR GATES	
443-876	INS1771		

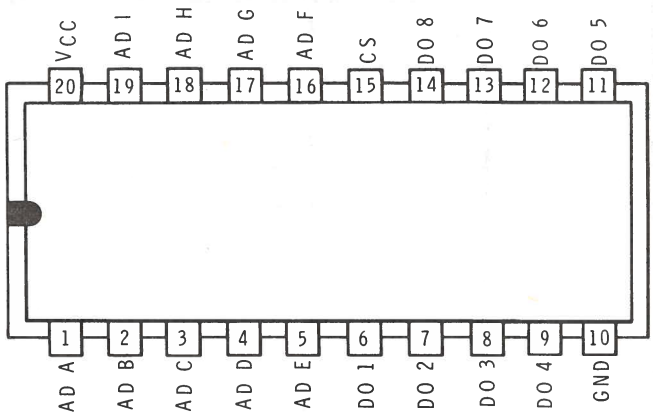
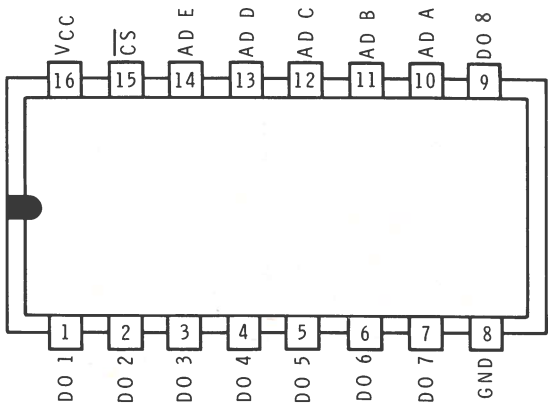
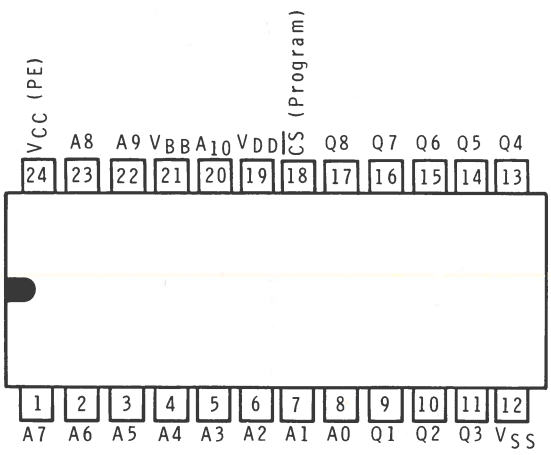
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-877	74LS138	3-TO-8 LINE DECODERS/MULTIPLEXERS	
443-879	74LS174	HEX D-TYPE FLIP-FLOPS	
443-880	8304	8-BIT BIDIRECTIONAL TRANSCEIVER	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-881	Z80	CPU	
444-20		256 WORD BY 4-BIT ROM	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
444-21		512 WORD BY 4-BIT ROM	
444-22		512 WORD BY 4-BIT ROM	
444-26		256 WORD BY 4-BIT ROM	
444-30		256 WORD BY 4- BIT ROM	
444-32		2K WORD BY 8-BIT E P ROM	

PARTS LISTS

NOTE: To order a replacement part, always include the part number and use one of the "Parts Order Forms" at the rear of this Manual. If a Parts Order Form is not available, refer to "Replacement Parts" inside the rear cover of this Manual. For prices, refer to the separate "Heath Parts Price List."

POWER SUPPLY CIRCUIT BOARD

DIODES-TRANSISTORS-INTEGRATED CIRCUITS

(See "Semiconductor Identification.")

RESISTORS

(All resistors are 1/4-Watt, 5% unless listed otherwise.)

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
R1	6-470	47 Ω, 1/2-watt
R2	6-102-12	1000 Ω
R3	2-13-11	10 Ω 1%, 1/8-watt
R4	2-741-12	4.7 Ω 1%
R5	6-662-12	6200 Ω
R6	10-994	1000 Ω control
R7	6-470-12	47 Ω
R8	6-102-12	1000 Ω
R9	3-8-3	.1 Ω 1%, 3-watt
R10	6-470-12	47 Ω
R11	6-302-12	3000 Ω
R12	6-122-12	1200 Ω
R13	10-994	1000 Ω control
R14	6-223-12	22 kΩ
R15	3-8-3	.1 Ω 1%, 3-watt
R16	6-470-12	47 Ω

CAPACITORS

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
C1	25-208	1500 μF electrolytic
C2	25-208	1500 μF electrolytic
C3	21-82	.02 μF ceramic
C4	21-21	200 pF ceramic
C5	21-192	.1 μF ceramic
C6	21-143	.05 μF ceramic
C7	21-192	.1 μF ceramic
C8	25-845	330 μF electrolytic
C9	25-845	330 μF electrolytic
C10	25-845	330 μF electrolytic
C11	21-75	100 pF ceramic
C12	25-276	4.7 μF tantalum
C13	25-276	4.7 μF tantalum
C14	25-276	4.7 μF tantalum
C15	21-192	.1 μF ceramic
C16	21-192	.1 μF ceramic

MISCELLANEOUS

F1	421-4	8-ampere fuse
L1	46-67	100 μH filter

INTERFACE CIRCUIT BOARD

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
DIODES-TRANSISTORS-INTEGRATED CIRCUITS-RESISTOR PACKS		
	(See "Semiconductor Identification.")	
RESISTORS		
	(All resistors are 1/4-watt, 5%.)	
R1	6-681-12	680 Ω
R2	6-331-12	330 Ω
R3	6-681-12	680 Ω
R4	6-103-12	10 kΩ
R5	6-103-12	10 kΩ
R6	6-103-12	10 kΩ
Resistors (cont'd.)		
R7	6-681-12	680 Ω
R8	6-681-12	680 Ω
R9	6-103-12	10 kΩ
R10	6-681-12	680 Ω
R11	6-472-12	4700 Ω
R12	6-681-12	680 Ω
CAPACITORS		
C1-C10	25-221	2.2 μF tantalum
C11	NOT USED	
C12	21-75	100 pF ceramic
C13	21-75	100 pF ceramic
C14	21-140	.001 μF ceramic
C15	21-140	.001 μF ceramic

CONTROLLER CIRCUIT BOARD

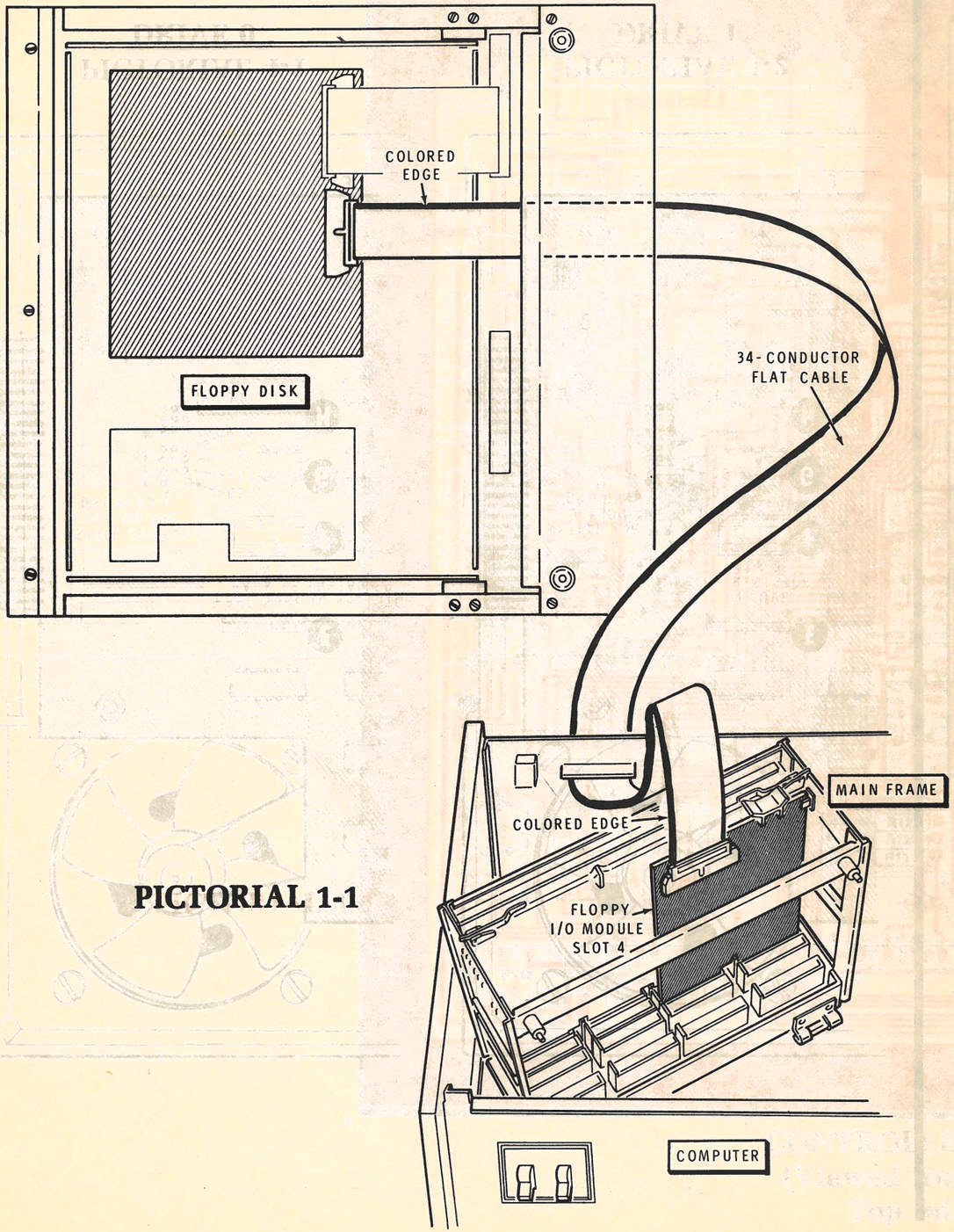
CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
DIODES-TRANSISTORS-INTEGRATED CIRCUITS-RESISTOR PACKS		
	(See "Semiconductor Identification.")	
RESISTORS		
	(All resistors are 1/4-Watt, 5%.)	
R101	6-331-12	330 Ω
R102	6-331-12	330 Ω
R103	6-331-12	330 Ω
R104	6-331-12	330 Ω
R105	6-271-12	270 Ω
R106	6-271-12	270 Ω
R107	6-392-12	3900 Ω
R108	6-562-12	5600 Ω
R109	6-393-12	39 kΩ
R110	6-124-12	120 kΩ
R111	6-102-12	1000 Ω
R112	6-102-12	1000 Ω
R113	6-102-12	1000 Ω
R114	6-103-12	10 kΩ
R115	6-102-12	1000 Ω
R116	6-102-12	1000 Ω
R117	6-102-12	1000 Ω
R118	6-393-12	39 kΩ
Resistors (cont'd.)		
R119	6-103-12	10 kΩ
R120	6-103-12	10 kΩ
R121	6-103-12	10 kΩ
R122	6-102-12	1000 Ω
R123	6-102-12	1000 Ω
R124	6-102-12	1000 Ω
R125	6-102-12	1000 Ω
R126	6-102-12	1000 Ω
R127	6-393-12	39 kΩ
R128	6-102-12	1000 Ω
CAPACITORS		
C101	21-61	6.8 pF ceramic
C102	21-147	47 pF ceramic
C103	21-27	.005 μF ceramic
C104	21-27	.005 μF ceramic
C105	21-95	.1 μF ceramic
C106	25-197	1 μF tantalum
C107	21-163	.001 μF ceramic
C108	25-223	47 μF tantalum
C109	25-223	47 μF tantalum
C110	25-223	47 μF tantalum
C111	21-27	.005 μF ceramic
C112	21-61	6.8 pF ceramic
C113-C119	25-220	10 μF tantalum

FILTER ASSEMBLY & CHASSIS MOUNTED PARTS

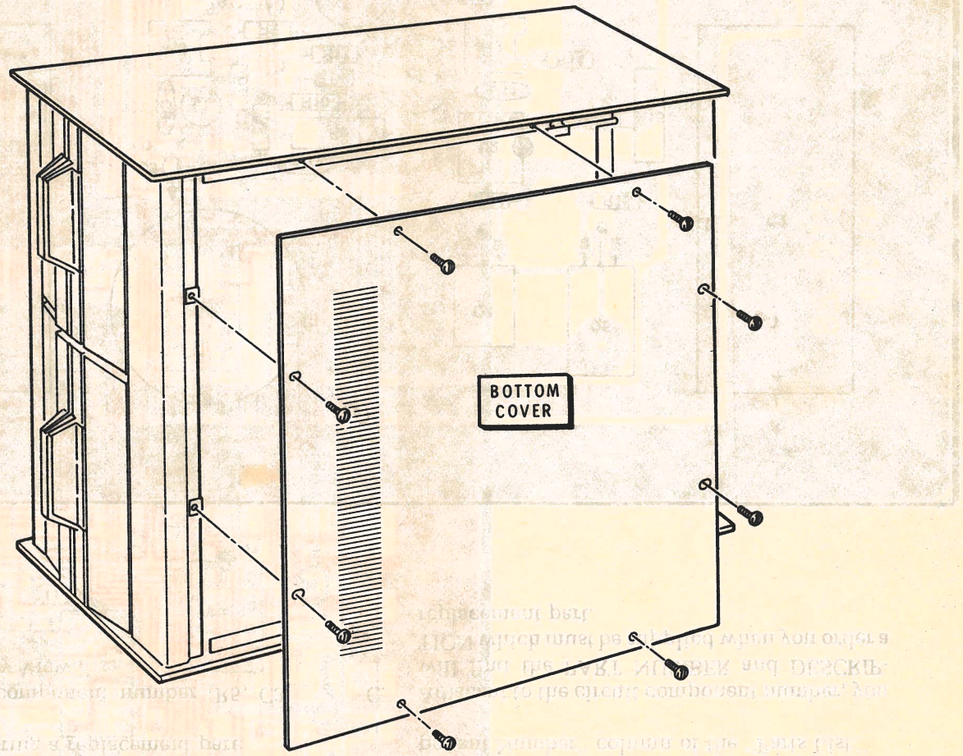
CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
DIODES		
	(See "Semiconductor Identification.")	
RESISTOR-CAPACITORS		
R21	3-45-5	1200 Ω, 5-watt
C21	21-70	.01 μF, 1400V ceramic
C22	21-70	.01 μF, 1400V ceramic
C23	25-847	39,000 μF electrolytic
C24	25-192	2000 μF electrolytic

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
MISCELLANEOUS		
SW1	60-619	On-off switch
SW2	60-54	120/240 VAC switch
SW3	61-37	SYSTEM switch
SW4	61-36	FORMAT switch
F2	421-32	5-ampere fuse (for 120 VAC operation)
F2	421-6	3-ampere slow-blow fuse (for 240 VAC operation)
T1	54-960	Power transformer
A1-A2	420-99	Fan
	266-1010	Fan filter
	134-1031	34-conductor cable
	134-1032	50-conductor cable
	150-73	Floppy disk drive mechanism

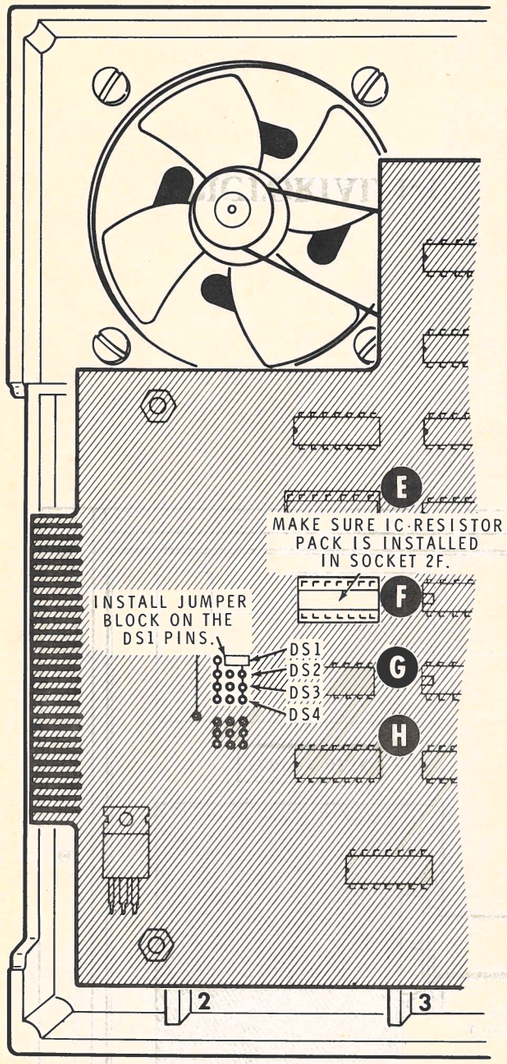
ILLUSTRATION BOOKLET



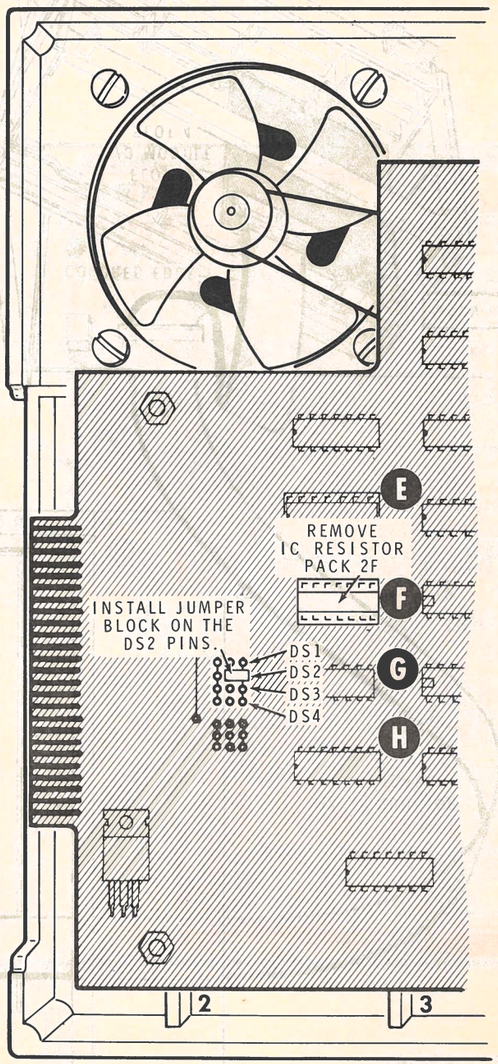
PICTORIAL 1-1



Detail 1-1A



PICTORIAL 4-1
DRIVE 0



PICTORIAL 4-2
DRIVE 1

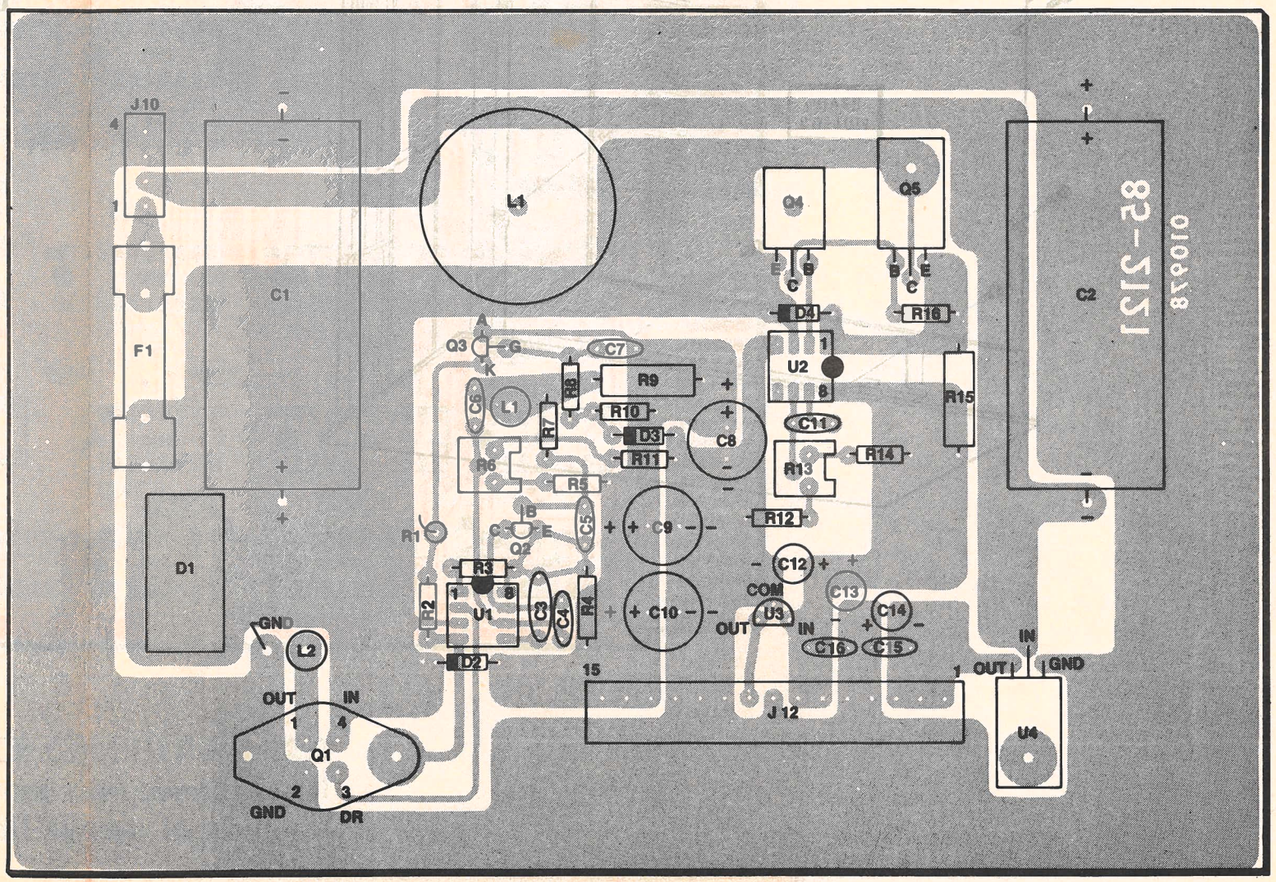
CIRCUIT BOARD X-RAY VIEWS

NOTE: To find the PART NUMBER of a component for the purpose of ordering a replacement part:

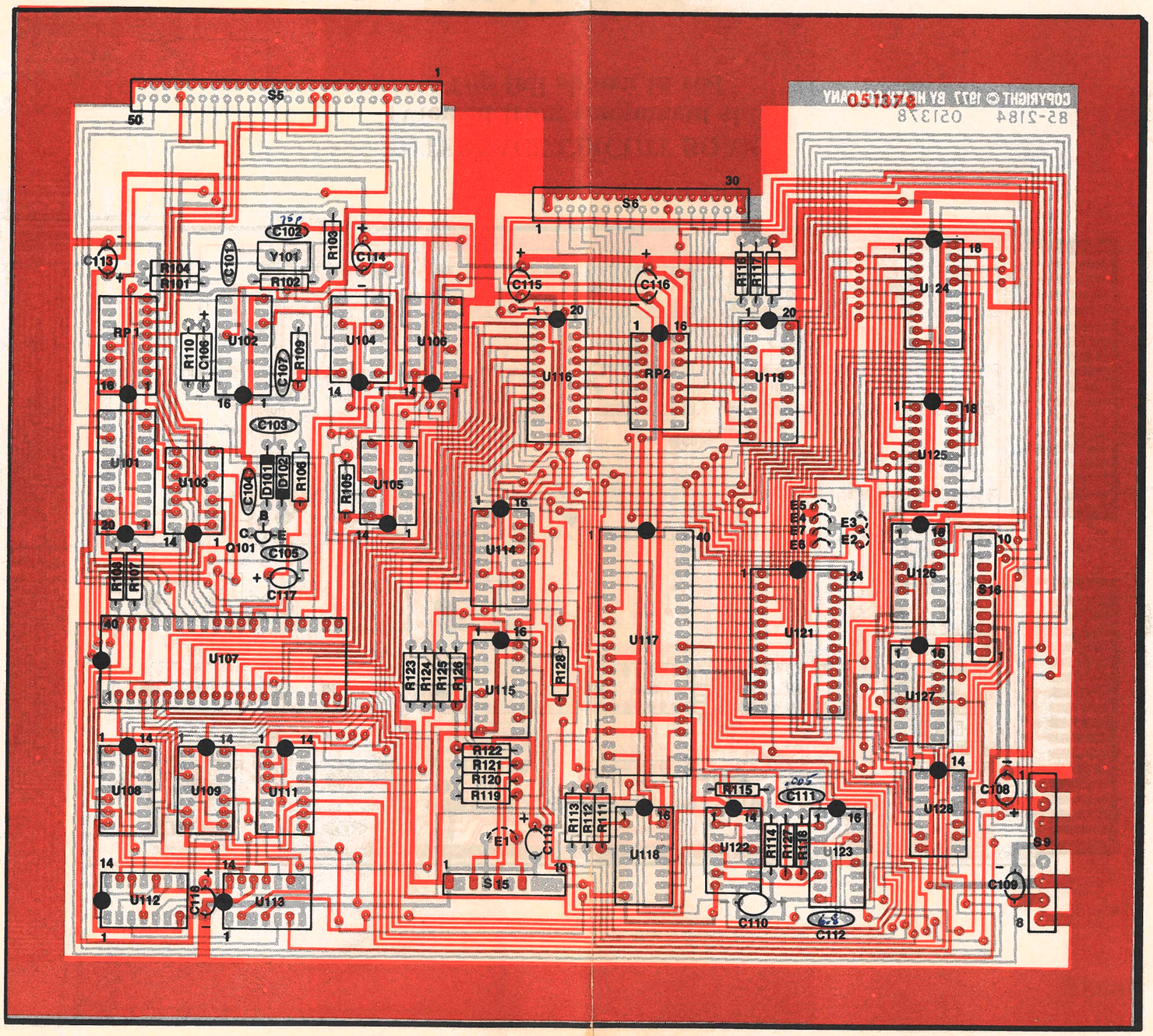
A. Find the circuit component number (R5, C3, etc.) on the "X-Ray View."

B. Locate this same number in the "Circuit Component Number" column of the "Parts List."

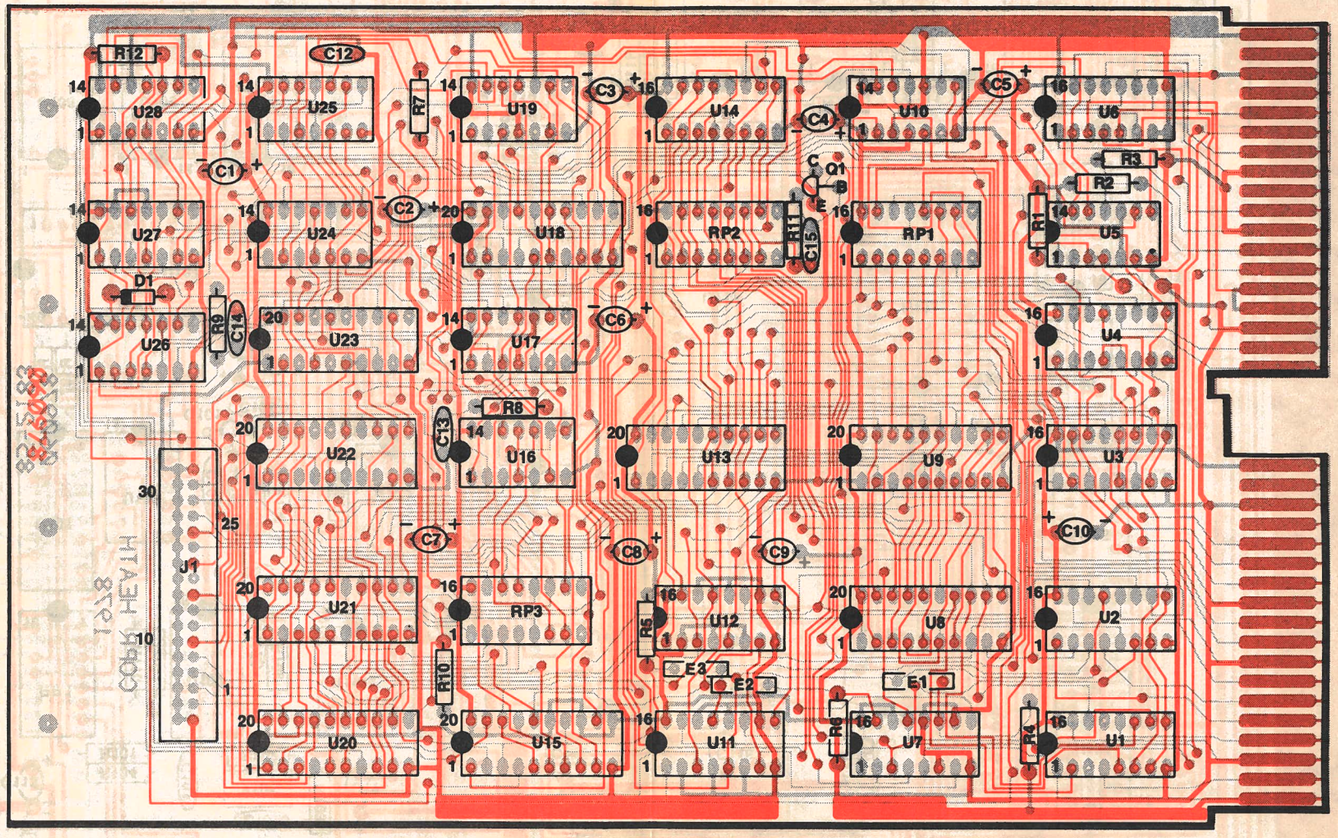
C. Adjacent to the circuit component number, you will find the PART NUMBER and DESCRIPTION which must be supplied when you order a replacement part.



POWER SUPPLY CIRCUIT BOARD
(Viewed from component side)



CONTROLLER CIRCUIT BOARD
(Viewed from component side)
Top foil shown in red



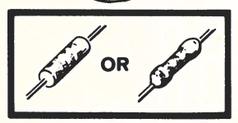
INTERFACE CIRCUIT BOARD
(Viewed from component side)
Top foil shown in red

ILLUSTRATION BOOKLET

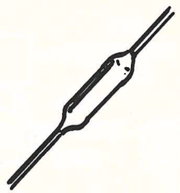
Part of 595-2608

PARTS PICTORIAL

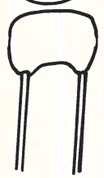
A1



A2

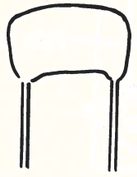


B1



B2

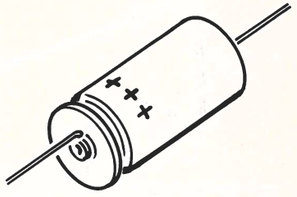
B3



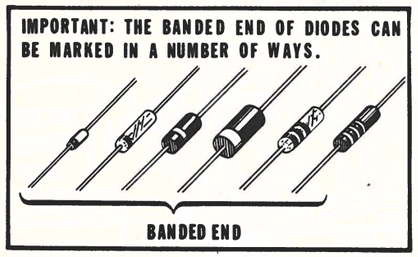
B4

B5

B6

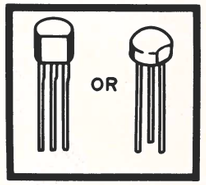


C1



C2

D1



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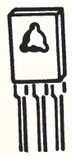
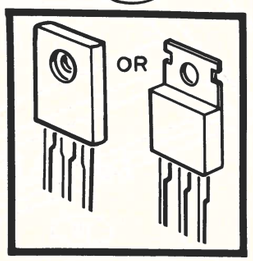


D3

D4



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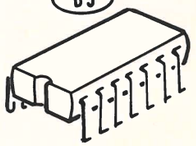
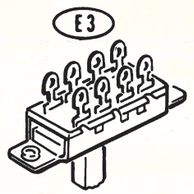


E1

E2

E3



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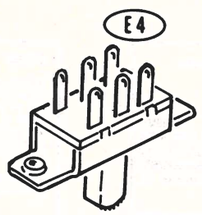

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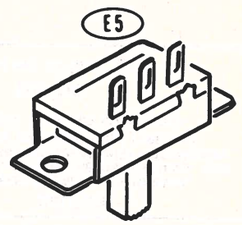

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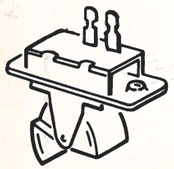

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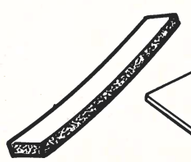

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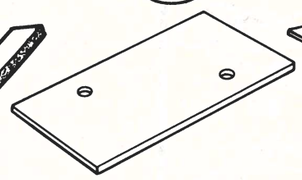
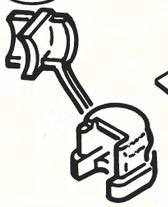
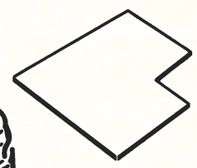


E9

E10



E11



F1

F2

F3

F4

F5

F6

F7

F8

F9

F10

F11

F12

F13

F14

G1

G2

G3

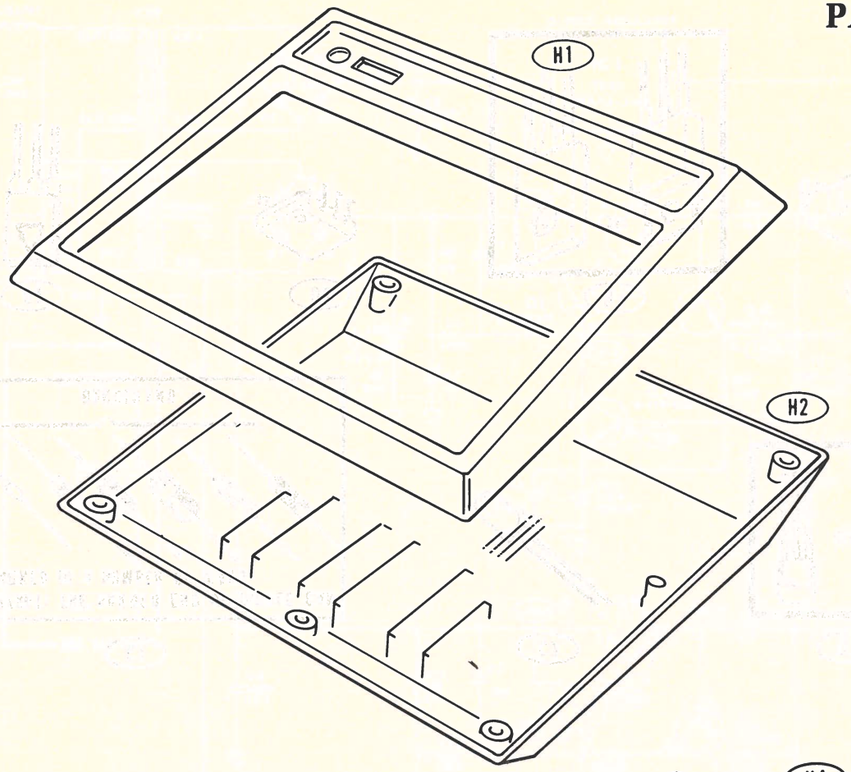
G4

G5

Model ET-3200A

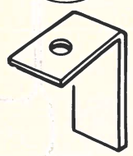
PARTS PICTORIAL (cont'd.)

H1



H2

H3



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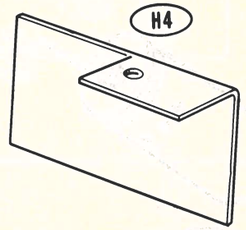
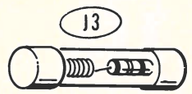


J1

J2

J3



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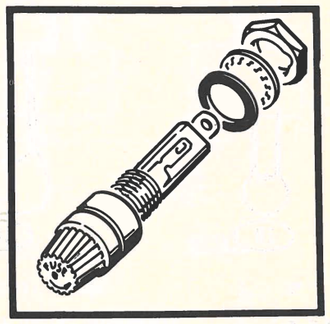
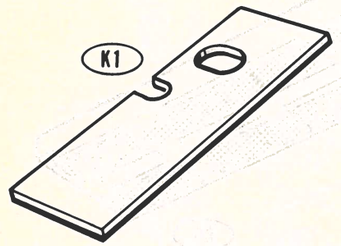


K1



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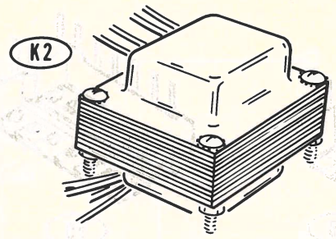
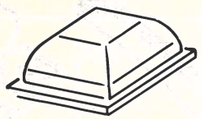


K3

K4

K5



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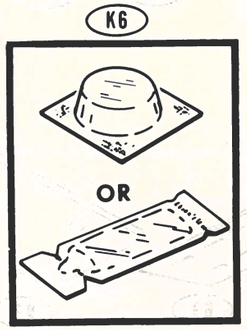

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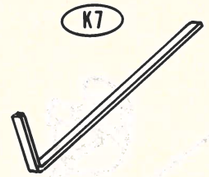

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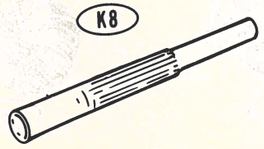


K9

HEATHKIT

Verification of Compliance with Federal Communications Commission Regulations, Part 15, Subpart J.

The Heath Company certifies that this equipment can be expected to comply with the emission limits for a Class B computing device persuant to Subpart J of Part 15 of the FCC rules when assembled in strict accordance with the instructions contained in the applicable Heath Company Instruction Manual, using only components and materials supplied with the kit or the exact equivalent thereof.

Heath Company, Benton Harbor, MI., 49022

K10

CAUTION

TO PREVENT ELECTRICAL SHOCK HAZARD. DISCONNECT LINE CORD BEFORE OPENING. FOR CONTINUED PROTECTION AGAINST FIRE HAZARD. REPLACE FUSE ONLY WITH SAME TYPE AND RATING. 250 V 3/16 AMP SLOW BLOW

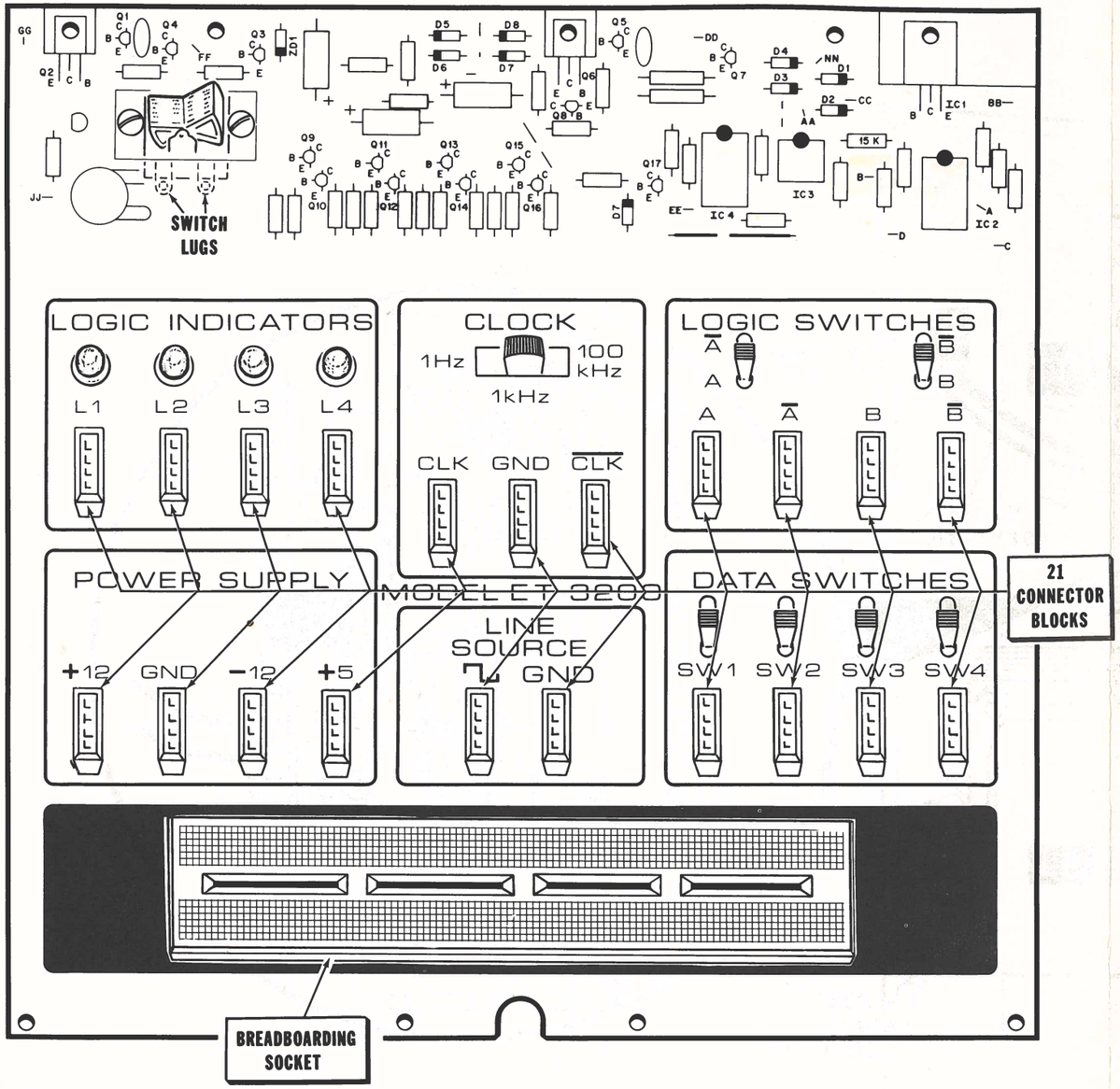
EIA-416

120/240 VAC 50/60 Hz 40 mA

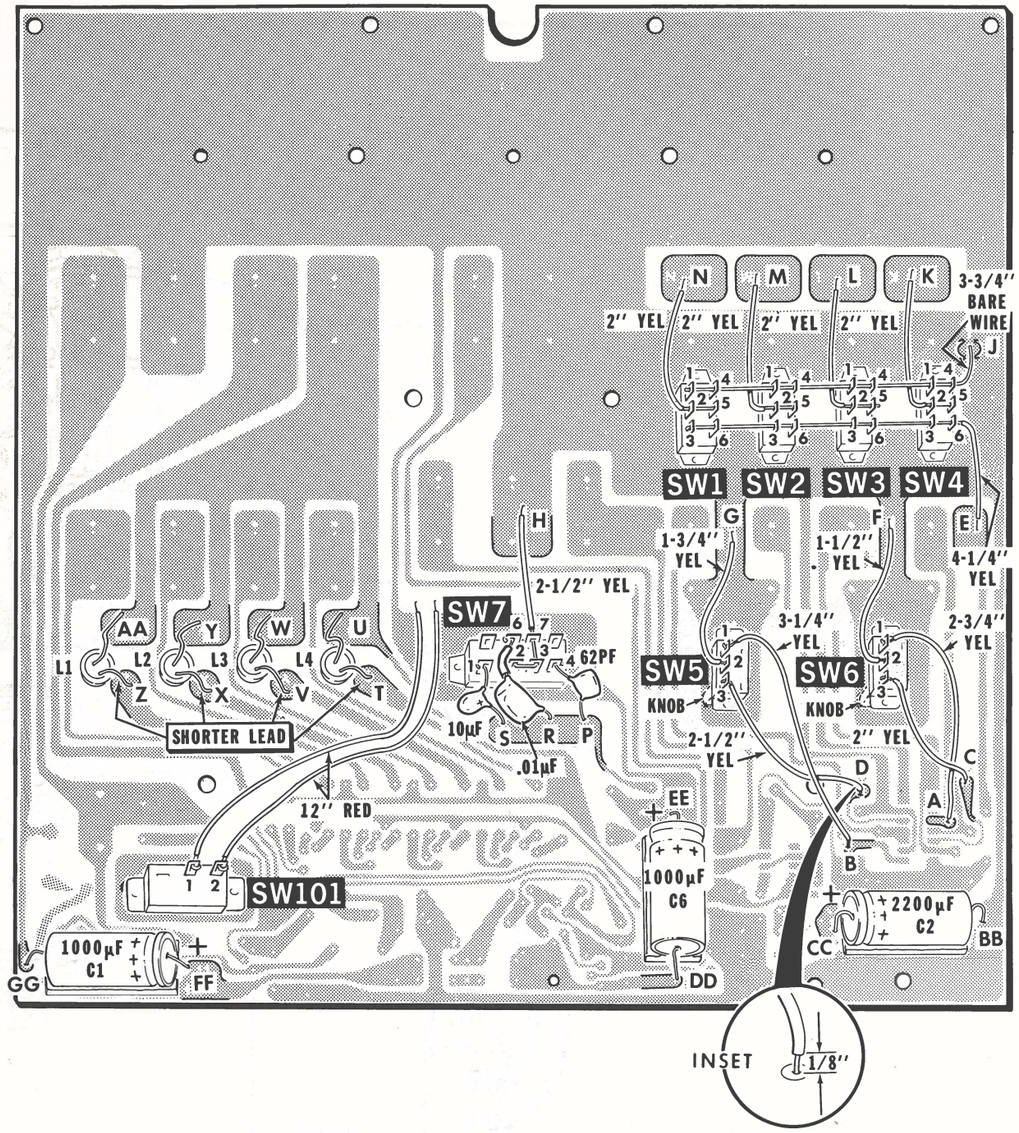
K11

Heathkit

MODEL	SERIES NO.



PICTORIAL 2-1



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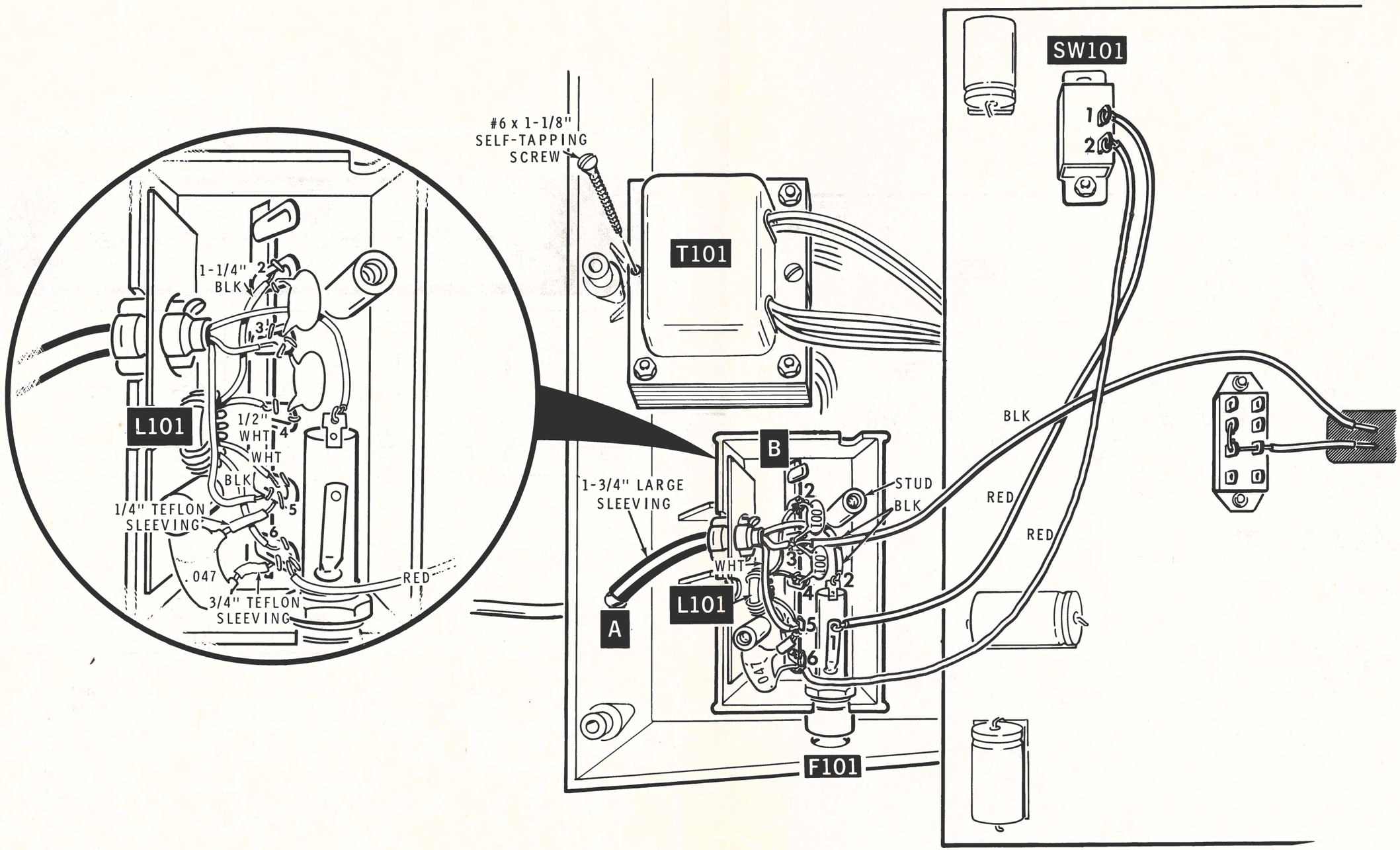

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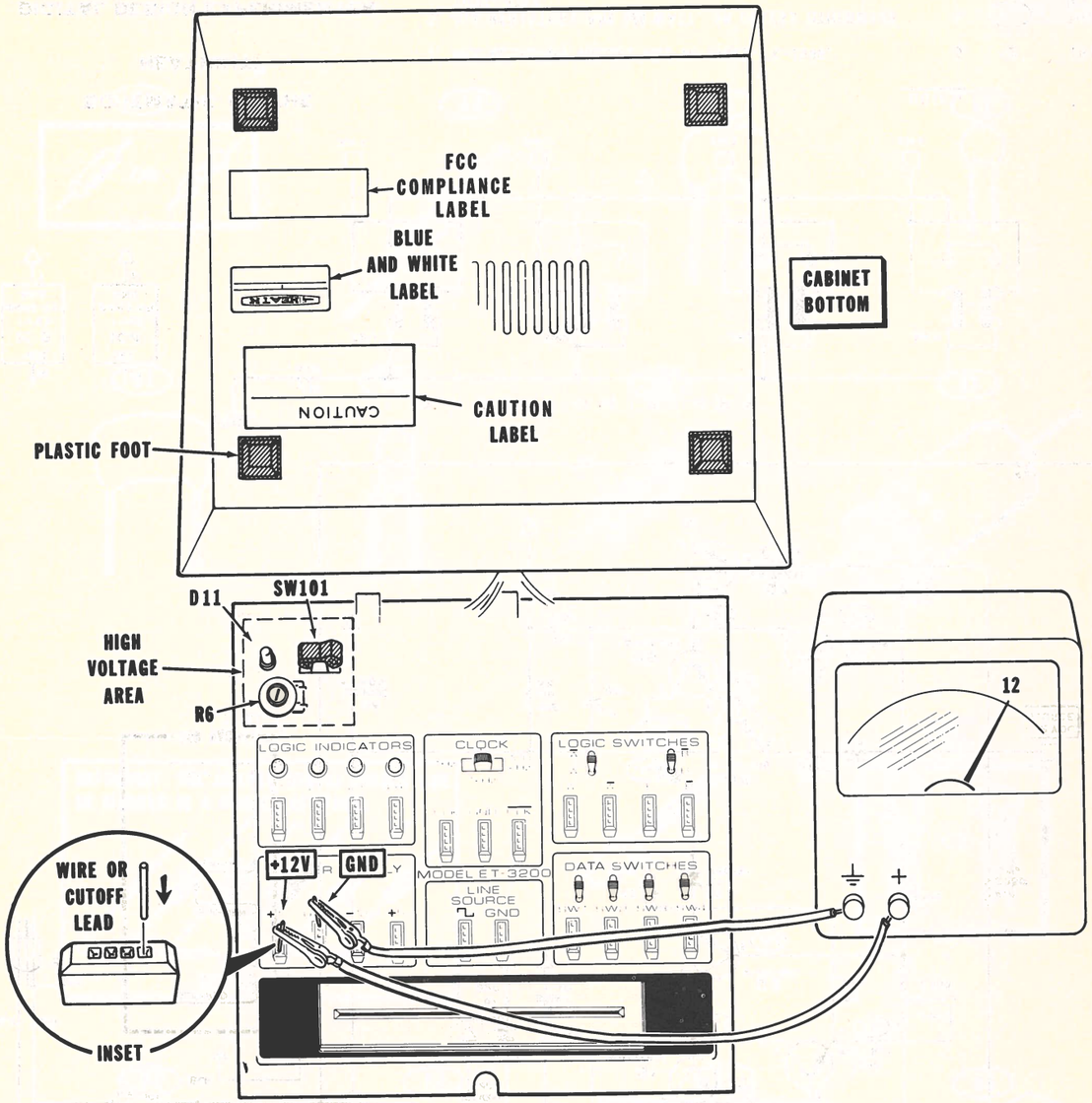
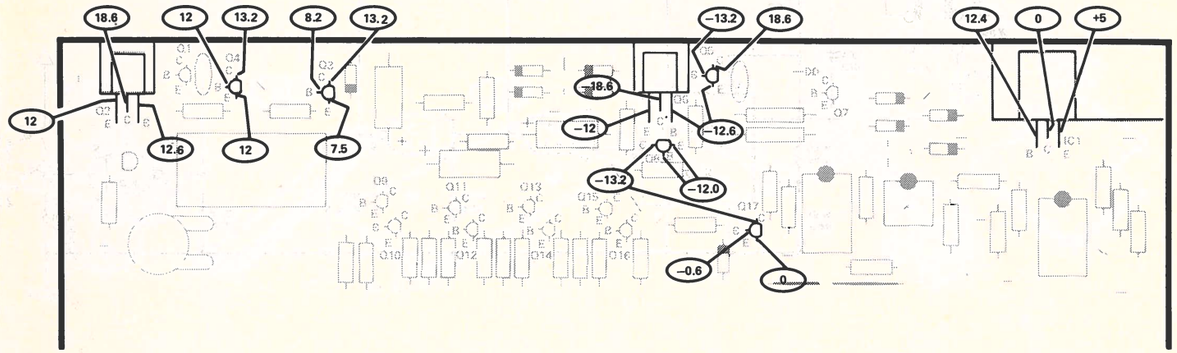
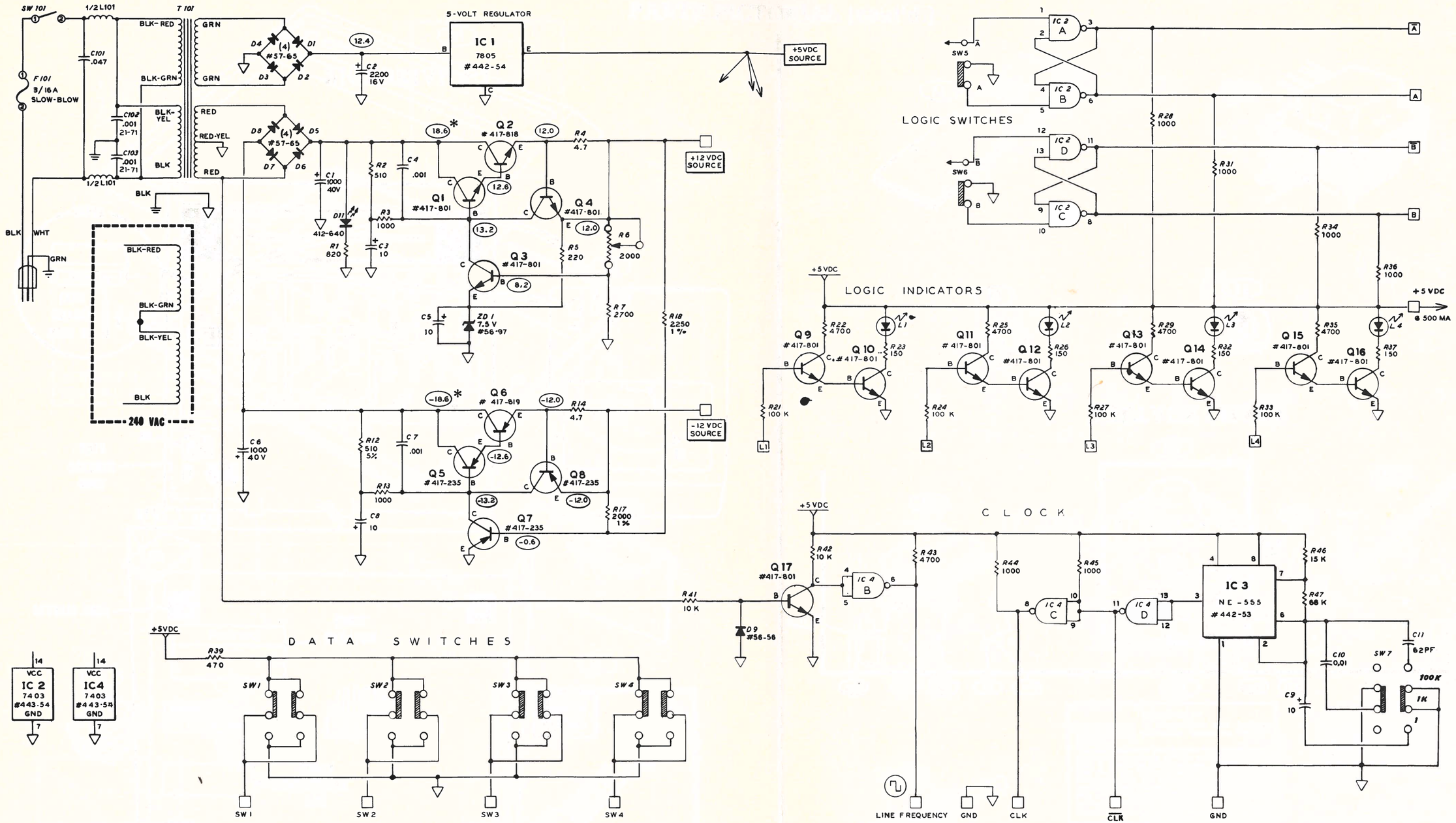


PICTORIAL 4-1



VOLTAGE CHART



SCHEMATIC OF THE

HEATHKIT®

DIGITAL DESIGN EXPERIMENTER

MODEL ET-3200A

NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS: K=1000.
2. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE INDICATED.
3. ALL CAPACITOR VALUES ARE IN µF UNLESS OTHERWISE INDICATED.
4. ⏚ THIS SYMBOL INDICATES CIRCUIT BOARD GROUND.
5. ⏚ THIS SYMBOL INDICATES CHASSIS GROUND.
6. ⬭ THIS SYMBOL INDICATES A DC VOLTAGE MEASURED WITH A HIGH IMPEDANCE VOLTMETER FROM THE POINT INDICATED TO CIRCUIT GROUND.
7. ⬭* THESE VOLTAGES WILL VARY WITH THE LOAD.

DATA BUS

ADDRESS BUS

U117
443-881
PROCESSOR
Z80

U121
444-32
ROM

U118
444-26

U125
443-764
RAM

U124
443-764
RAM

U116
443-880

U123A
443-727

U123B
443-727

U127
443-877

U126
443-877

U128A

U128B

U128C

U111B

U122A

U122B

U122C

U122D

U104D

U104E

U104F

U105B
443-6

S9

+5V VOLT SOURCE

+12VOLT SOURCE

C108 47µF

ALL RESISTORS 680Ω

SW3 EXTENDED

RX01

CLK L

CTRL WR L

CTRL RD L

SR RD L

FLOPPY

CONTROLLER CIRCUIT BOARD

Part of 595-2167
Model WH27 2 of 3

ALL RESISTORS 680Ω

RP-2 9-86

+5V

U116 3-880

A PORT

B PORT

CS

U119 443-824

SR RD L

S16-4

S16-6

R116 1000

R117 1000

U108A

U113B

Z INIT L

WG H

RESET L

CLK L

U104F

R106 270

D102 56-56

D101 56-56

C103 .005

C104 .005

-8V

Q101 443-665

-5 VOLT REGULATOR

C105 .1

-5VOLT SOURCE

-5V

ADDRESS

A0 H

A1 H

U109B

U109D

U109A

CTRL WR L

CTRL RD L

U101 443-824

PART OF RP-1 9-87

DSS L

U103F

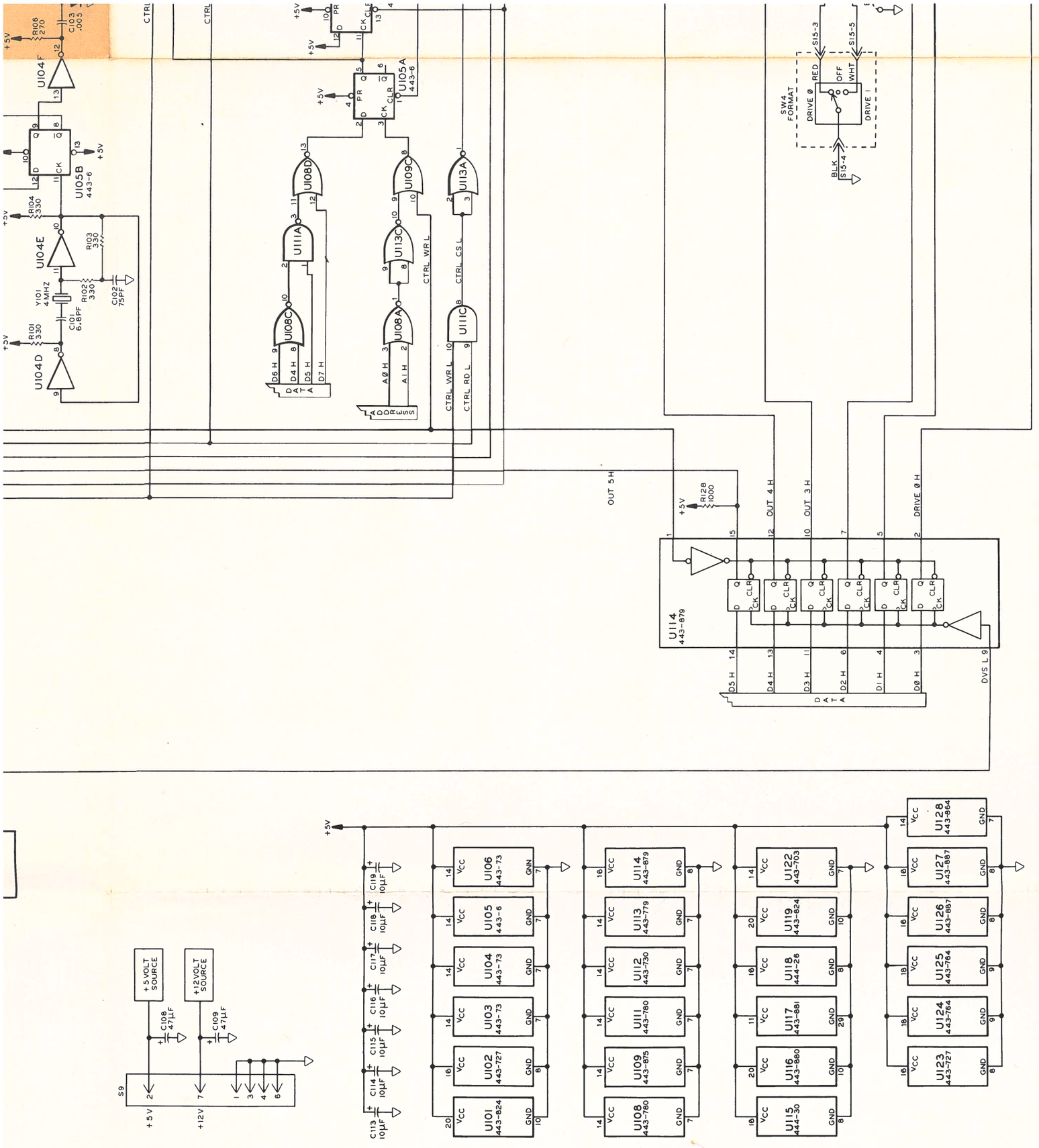
READY

S8

Z B0 L
Z B1 L
Z B2 L
Z B3 L
Z B4 L
Z B5 L
Z B6 L
Z B7 L
Z INIT L
Z RD L
Z WD L
Z WAIT L
Z RS L
Z WS L
GND

S5

TRACK 00
INDEX
WRT PRT
DBL. SIDED
READY


+5V
R106 270
C103 .005
U104F
U105B 443-6
R104 330
U104E
R103 330
Y101 4MHZ
R102 330
C102 75PF
C101 6.8PF
R101 330
U104D
CTRL
U105A 443-6
U108D
U111A
U108C
U109C
U113C
U108A
U113A
U111C
D6 H
D4 H
D5 H
D7 H
A0 H
A1 H
DATA
ADDRESS
CTRL WR L
CTRL CS L
CTRL RD L
OUT 5H
R128 1000
OUT 4 H
OUT 3 H
DRIVE 0 H
U114 443-879
D5 H
D4 H
D3 H
D2 H
D1 H
D0 H
DVS L 9
SW4 FORMAT
DRIVE 0
DRIVE 1
RED
WHT
OFF
S15-3
S15-5
S15-4
BLK

S9
+5 V
+12V
+5VOLT SOURCE
+12VOLT SOURCE
C108 47µF
C109 47µF
C113 10µF
C114 10µF
C115 10µF
C116 10µF
C117 10µF
C118 10µF
C119 10µF
U101 443-824
U102 443-727
U103 443-73
U104 443-73
U105 443-6
U106 443-73
U108 443-780
U109 443-875
U111 443-780
U112 443-730
U113 443-779
U114 443-879
U115 444-30
U116 443-880
U117 443-881
U118 444-26
U119 443-824
U122 443-703
U123 443-727
U124 443-764
U125 443-764
U126 443-887
U127 443-887
U128 443-864
VCC
GND
+5V

U104F
R106 270
C103 .005
D101 56-56
D102 56-56
C104 .005
Q101 443-665
-5 VOLT REGULATOR
C105 .1
-5VOLT SOURCE
-5V
+5V
-8V
VBB
ADDRESS
AØ H
AI H
AØ
AI
CTRL WR L
CTRL RD L
U109B
U109D
U109A
WE
RE
DATA
DØ H
D1 H
D2 H
D3 H
D4 H
D5 H
D6 H
D7 H
DA L Ø
DA L 1
DA L 2
DA L 3
DA L 4
DA L 5
DA L 6
DA L 7
U105A 443-6
U112A 443-730
U112B 443-730
R115 1000
R107 3900
R108 5600
U108B
U113D
DRQ
INTRO
PH 3
WF
WPRT
DSS L
PART OF RP-1 9-87
180
390
READY
FD DATA
FD CLK
U103F
U103E
U103D
D
A
J
F
E
G
H
I
WG
WD
TG 43
PH2/STEP
HLD
U103B
U103C
U104C
U104B
U106B
WRT PRT
DBL. SIDED
READY
SEP. DATA
SEP. CLOCK
WRT GATE
WRT DATA
TRACK 43
DIRECTION
HEAD LOAD
U107 443-876
HLT
OUT 4 H
FRMT H
U102B 443-727
U111D
C106 1
R110 120K
U104A
U102A 443-727
R109 39K
C107 .001
STEP
SW4 FORMAT
DRIVE Ø
RED
OFF
WHT
DRIVE 1
S15-3
S15-5
R119 10K
R120 10K
R121 10K
U115 444-30
ADC
ADE
ADF
ADB
ADA
D01
D02
D03
D04
D05
D06
D07
D08
R122 1000
R123 1000
R124 1000
R125 1000
R126 1000
DRIVE 1 H
DRIVE 2 H
DRIVE 3 H
DRIVE 4 H
DRIVE Ø H
U106A
U106D
U106E
U106F
U106C
DRIVE 1
DRIVE 2
DRIVE 3
DRIVE 4
SIDE Ø/1

from fr
panel - RX
EX

S16
Brown
Yellow
Oran

SERVICE INFORMATION

The following Heath Company services are available if you need them: Replacement Parts, Technical Consultation, and Factory Service. Address all correspondence to:

HEATH COMPANY
Benton Harbor, Michigan 49022

For prompt service, use a separate letter for each department you write to.

Replacement parts and repair service are also available at your nearest Authorized Service Center or Heath Electronic Center. These Centers are listed in your Heath Catalog.

REPLACEMENT PARTS

If a replacement part is needed, please include the following information in your letter:

1. Part number and description.
2. Model Number and Series Number of the equipment.

If your equipment is in the Warranty period, add:

3. Date of purchase.
4. Nature of defect.

Heath Company will fill your order promptly. Please DO NOT RETURN PARTS unless they are requested. Parts that are damaged through carelessness or misuse by the customer will not be replaced without cost.

TECHNICAL CONSULTATION

You can write to our Technical Consultants for help with any Heath equipment, or for answers to any questions about the use of this equipment.

The completeness and accuracy of the advice mailed back to you depends entirely on the information in your letter. Be sure to include:

1. The Model Number and Series Number of the equipment (on blue and white identification label).
2. Date of purchase.
3. An exact description of the difficulty. Include switch positions, connections to other units, operating procedures, voltage reading, and any other information you think might be helpful.
4. List everything you have done in attempting to correct the difficulty.

FACTORY SERVICE

If you do not have qualified repair services at your disposal, you can return your equipment to the Heath Company Service Department to have it repaired for a minimum service fee. (Equipment that has been modified will not be accepted for repair.) Refer to Shipping Instructions for details on how to package and ship the equipment.

To be eligible for replacement parts under the terms of the Warranty, equipment returned for factory service must be accompanied by the invoice or the sales slip, or a copy of either. (If you send the original invoice or sales slip, it will be returned to you.)

SHIPPING INSTRUCTIONS

Check the equipment to see that all parts are in place. Then, wrap the equipment in heavy paper. Place the equipment in a strong carton, and put at least three inches of resilient packing material (shredded paper, excelsior, etc.) on all sides between the equipment and the carton.

Seal the carton with gummed paper tape and tie it with a strong cord. Ship it by prepaid Express or insured Parcel Post to:

HEATH COMPANY
Benton Harbor, Michigan 49022

Attach a letter, containing the following information to the outside of the carton:

1. Your name and return address.
2. Date of purchase.
3. A brief description of the difficulty.
4. Your authorization to ship the repaired unit back to you C.O.D. for the service and shipping charges, plus the cost of parts not covered by the Warranty.

YOUR HEATH FACTORY ASSEMBLED PRODUCT ONE-YEAR LIMITED WARRANTY

If you are not satisfied with our service - warranty or otherwise, or with our products, write directly to our Director of Customer Services, Heath Company, Benton Harbor, Michigan 49022. He will make certain your problems receive immediate, personal attention.

Our attorney insists that we describe our warranty using all the necessary legal phrases in order to comply with the new warranty regulations. Fine. Here they are:

For a period of one year after purchase, Heath Company will replace or repair free of charge any product that is defective either in materials or workmanship. We warrant that during the first full year after purchase, our products, when used in accordance with our printed instructions, will meet published specifications.

If your Heath factory-assembled product malfunctions or fails to operate at any time during the warranty period, through no fault of yours, we will service it free upon proof of purchase and delivery at your expense to the Heath factory, or any Heathkit Electronic Center (units of Schlumberger Products Corporation), or any of our authorized overseas distributors.

You will receive free consultation on any problem you might encounter in the use of your Heath product. Just drop us a line or give us a call. Sorry, we cannot accept collect calls.

Our warranty does not cover and we are not responsible for damage caused by misuse or fire or unauthorized modifications to or uses of our products for purposes other than advertised. Our warranty does not include reimbursement for customer assembly or set-up time.

This warranty covers only Heath factory assembled products and is not extended to allied equipment or components used in conjunction with these products. **We are not responsible for incidental or consequential damages.** Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

HEATH COMPANY
BENTON HARBOR, MI. 49022

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

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