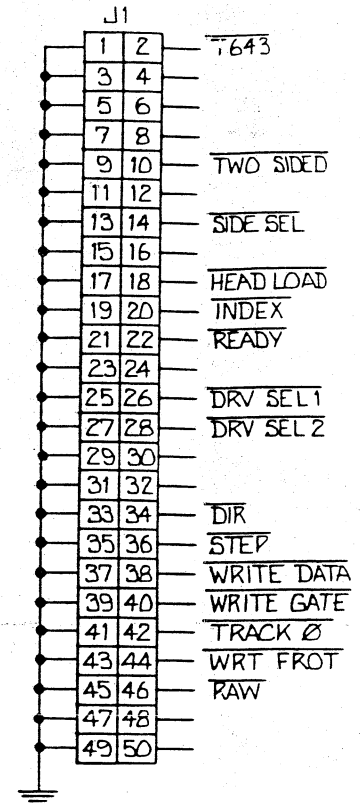
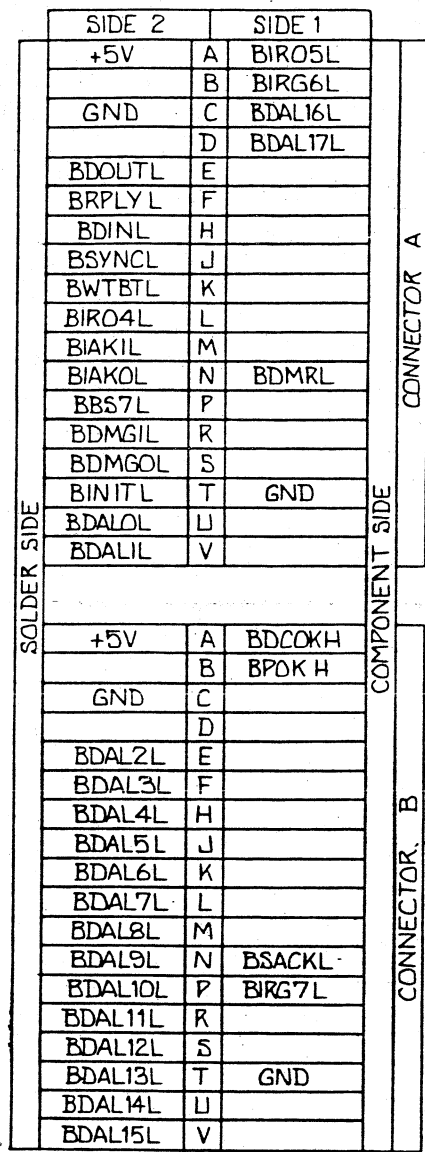


LAST REFERENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U71
CAPACITOR	C37
RESISTOR	R24
RESISTOR MODULE	RU2
TRANSISTOR	G4
DIODE	CR5
CONNECTOR	J1
OSCILLATOR	Y1

REF. DESIG.	GATES USED PER TOTAL	PART NUMBER
U12	NOT USED	SPARE
U29	2 / 4	74S32



ADDRESS	STANDARD	ALTERNATE
DEVICE	177170	177174
VECTOR	264	270

PRIORITY LEVEL	ASSERT LEVEL	MONITOR LEVEL	JUMPER													
			34/35	34/33	40/41	39/40	31/32	31/30	43/42	43/44	37/36	37/36				
4*	4	5,6	OUT	IN	OUT	IN	IN	OUT	OUT	IN	IN	OUT	IN	OUT		
5	4,5	6	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN		
6	4,6	7	IN	OUT	OUT	IN	OUT	IN	IN	OUT	IN	OUT	IN	OUT		
7	4,6,7	NONE	IN	OUT	IN	OUT	OUT	IN	IN	OUT	OUT	IN				

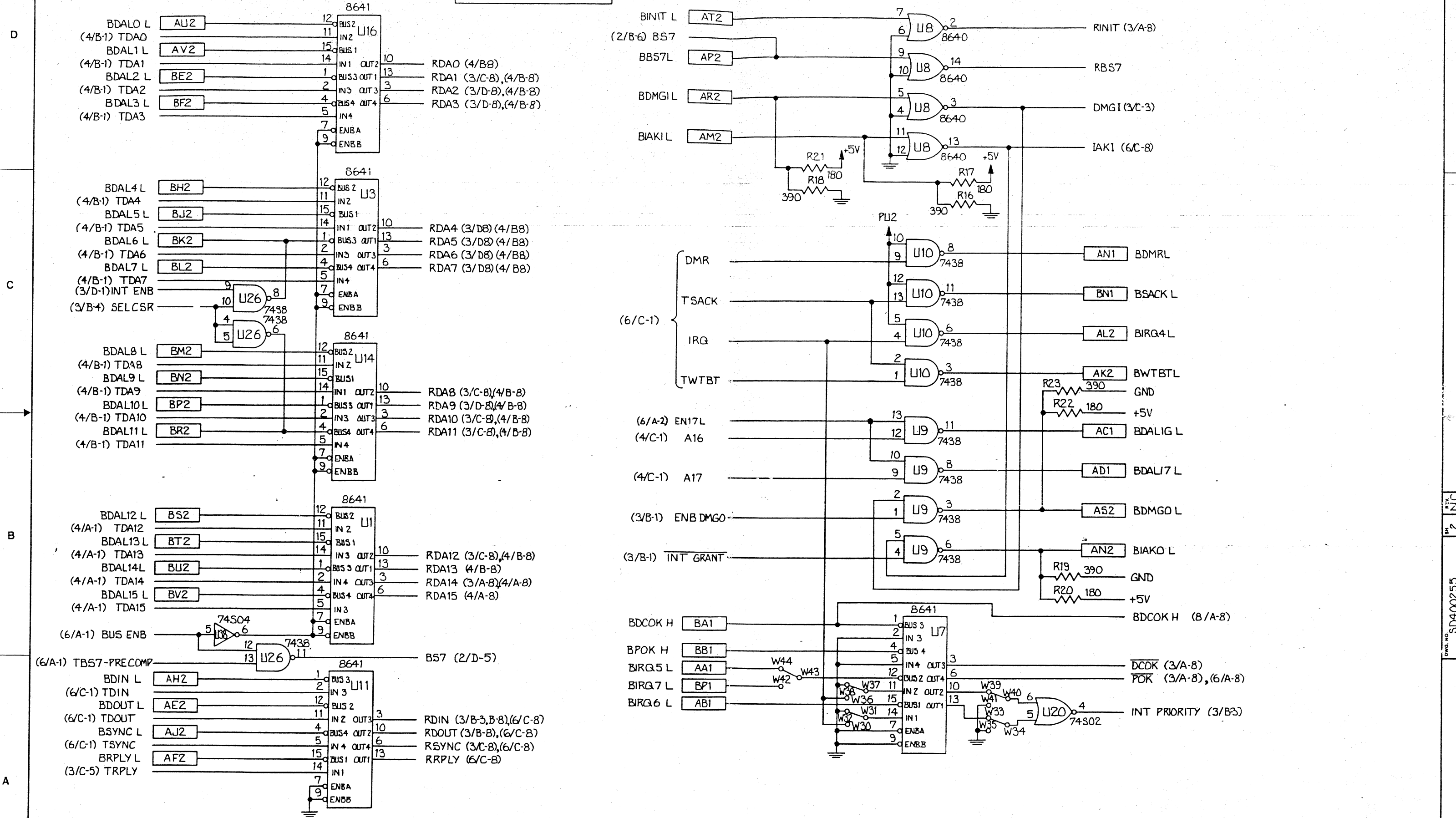
* FACTORY PRESET

OPTION	JUMPERS														22 BIT ADDRESS
	DRIVE SELECT	SIDE SELECT	WIRE CURRENT	BOOTSTRAP	WRITE PRECOMP	FACTORY TEST	DEVICE READY								
BOOTSTRAP ENABLED				IN	OUT										
BOOTSTRAP ** DISABLED				OUT	IN										
WRITE PRECOMP ** ENABLED					IN	OUT									
WRITE PRECOMP DISABLE					OUT	IN									
WRITE CURRENT CONTROL ENABLED						IN									
WRITE CURRENT ** CONTROL DISABLED						OUT									
SINGLE OR DOUBLE ** SIDED DRIVERS	OUT	IN	IN	OUT	OUT										
ONE DOUBLE SIDED DRIVE	IN	IN	OUT	IN	OUT										
DRIVE 0 = SIDE 0															
DRIVE 1 = SIDE 1															
STANDARD READY													OUT	IN	
TRUE READY													IN	OUT	
ENABLE 22 BIT ADDRESSING															OUT
DISABLE 22 BIT ADDRESSING															IN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES : 1/64 .XX ± .020 °0'30 .XXX ± .010		THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO SIGMA INFORMATION SYSTEMS, INC. AND MAY NOT BE REPRODUCED OR USED FOR OTHER THAN MAINTENANCE PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM AN OFFICER OF THE ABOVE FIRM.		Sigma Information Systems Inc.	
DRAWN: <i>[Signature]</i> J2-29-82		CHECKED:		TITLE: SCHEMATIC DIAGRAM - SDC-RXV31, FLOPPY CONTROLLER	
FINISH:		ENGINEER:		SIZE: D	
NEXT ASSY. USED ON:		APPROVED:		CODE IDENT. NO. SD400255	
APPLICATION:		APPROVED:		DRAWING NO. SD400255	
DO NOT SCALE DRAWING		APPROVED:		REV. NC	
				WORK ORDER NO.	
				SHEET 1 OF 8	

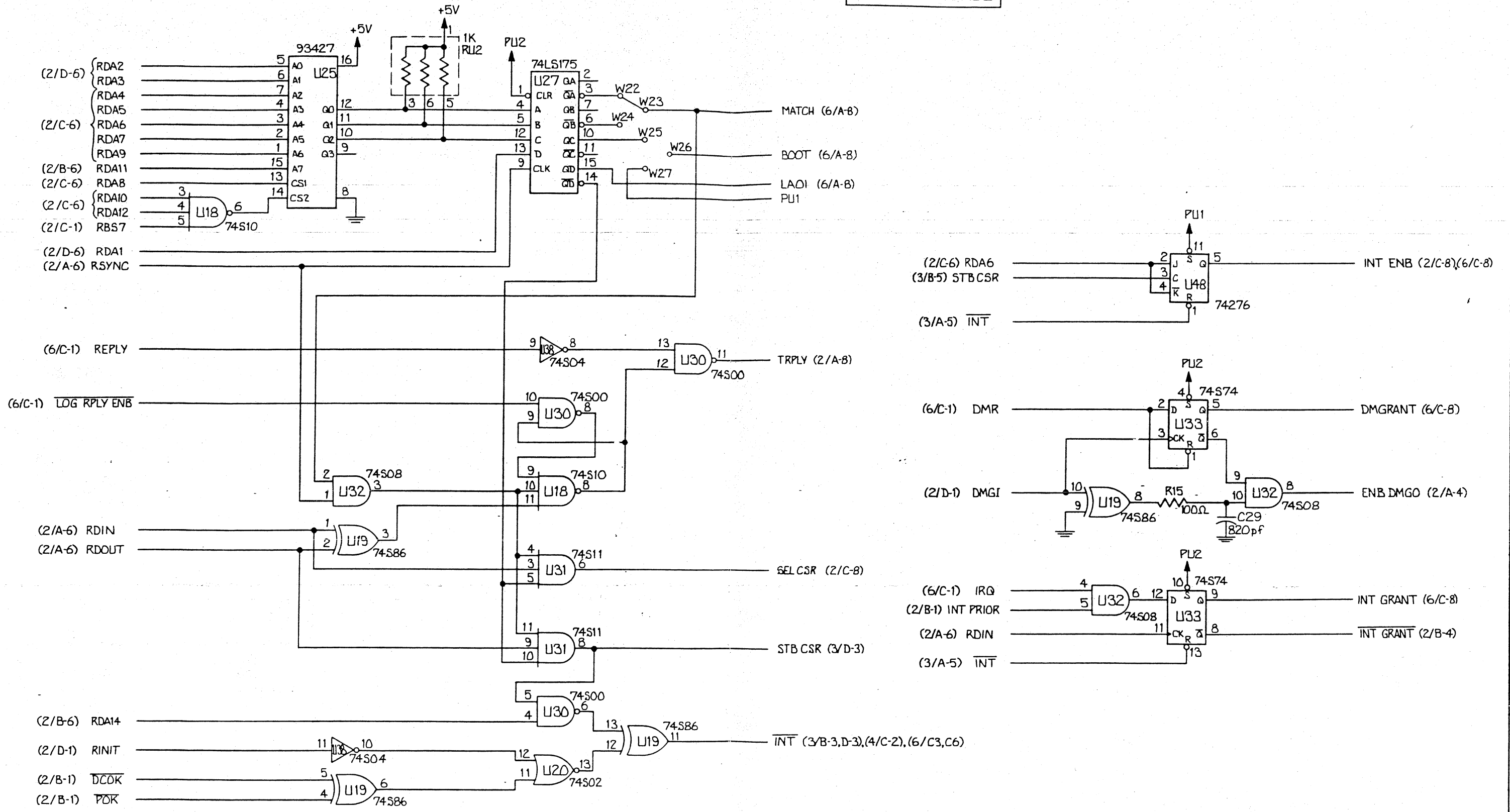
DRAW NO SD400255

Q BUS INTERFACE



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

Q BUS CONTROL

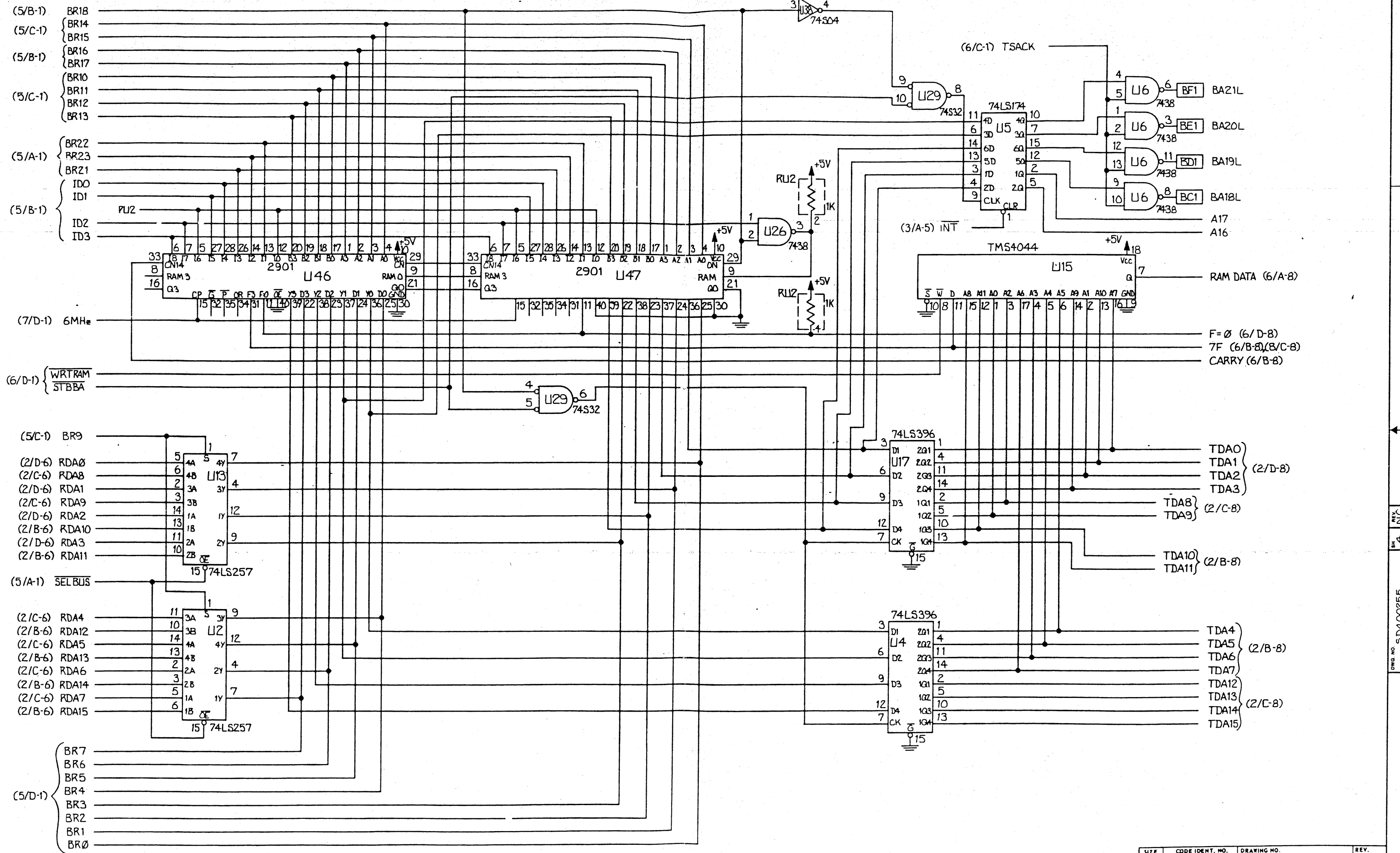


REV. 3 NC
DWG NO. SD400255

SIZE D	CODE IDENT. NO.	DRAWING NO. SD400255	REV. NC
SCALE NONE	WORK ORDER NO.	SHEET 3 OF 8	

MUP-8 BIT

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



D

D

C

C

B

B

A

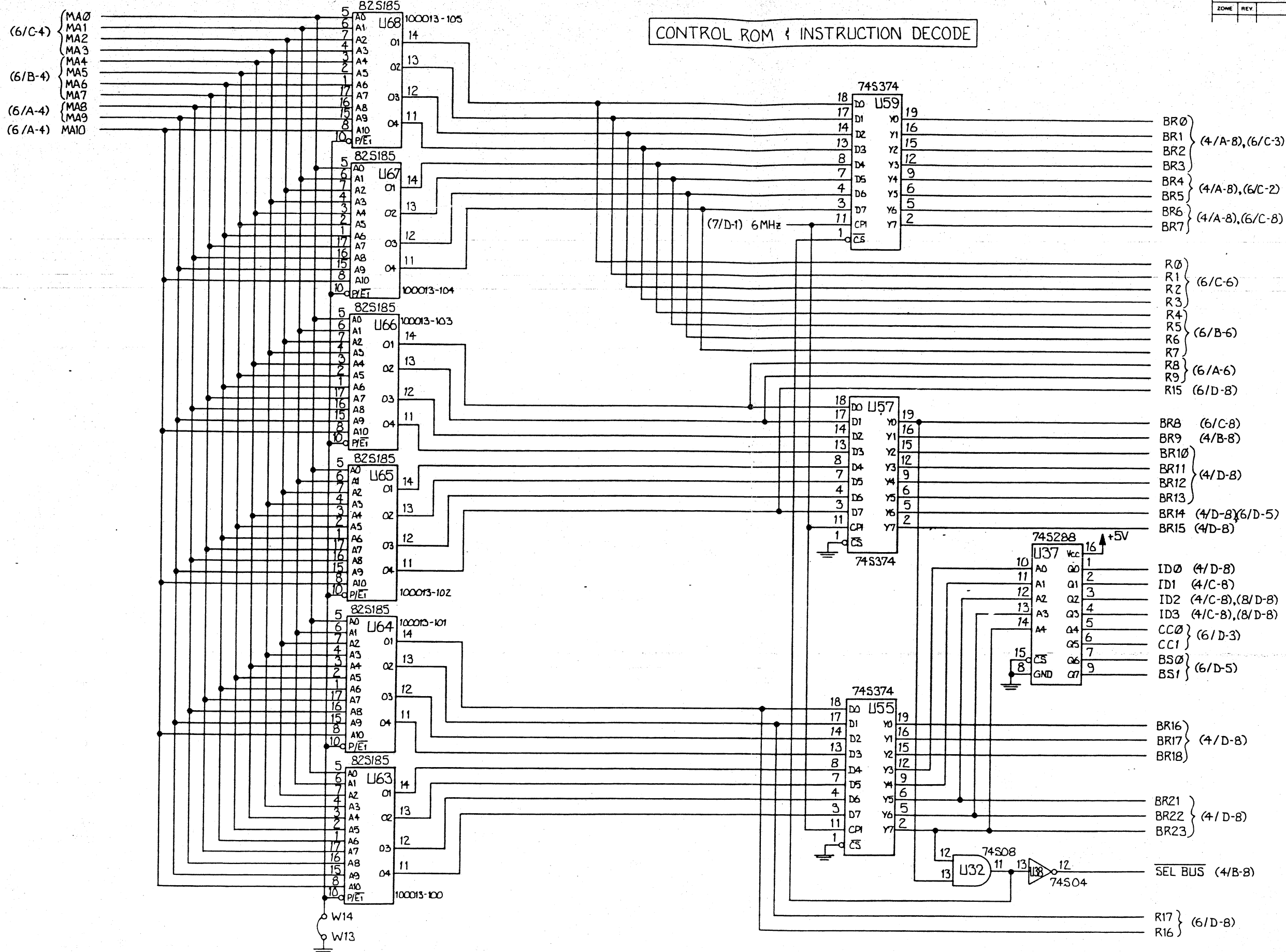
A

DWG. NO. 5D400255

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		5D400255	N.C
SCALE NONE		WORK ORDER NO.	SHEET 4 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

CONTROL ROM & INSTRUCTION DECODE



- BR0
- BR1 } (4/A-8), (6/C-3)
- BR2
- BR3
- BR4 } (4/A-8), (6/C-2)
- BR5
- BR6 } (4/A-8), (6/C-8)
- BR7

- R0
- R1 } (6/C-6)
- R2
- R3
- R4
- R5 } (6/B-6)
- R6
- R7
- R8 } (6/A-6)
- R9
- R15 } (6/D-8)

- BR8 } (6/C-8)
- BR9 } (4/B-8)
- BR10
- BR11 } (4/D-8)
- BR12
- BR13
- BR14 } (4/D-8), (6/D-5)
- BR15 } (4/D-8)

- ID0 } (4/D-8)
- ID1 } (4/C-8)
- ID2 } (4/C-8), (8/D-8)
- ID3 } (4/C-8), (8/D-8)
- CC0 } (6/D-3)
- CC1
- BS0 } (6/D-5)
- BS1

- BR16 } (4/D-8)
- BR17
- BR18

- BR21 } (4/D-8)
- BR22
- BR23

SEL BUS (4/B-8)

- R17 } (6/D-8)
- R16

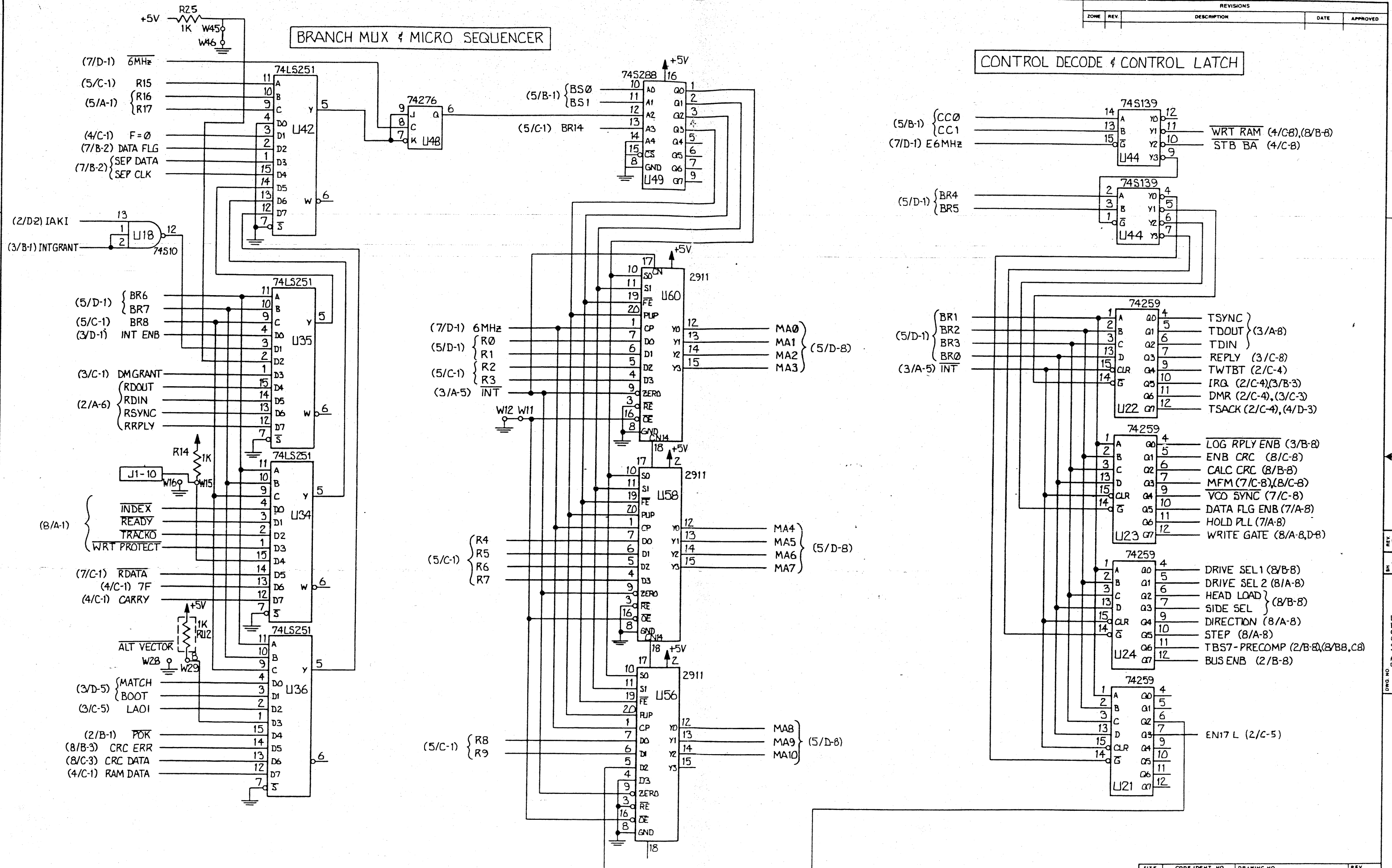
SIZE D	CODE IDENT. NO.	DRAWING NO. SD400255	REV. NC
SCALE NONE	WORK ORDER NO.	SHEET 5 OF 8	

Dwg No. SD400255 Rev. 5 NC

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

BRANCH MUX & MICRO SEQUENCER

CONTROL DECODE & CONTROL LATCH



(7/D-1) 6MHz
 (5/C-1) R15
 (5/A-1) {R16, R17}
 (4/C-1) F=0
 (7/B-2) DATA FLG
 (7/B-2) {SEP DATA, SEP CLK}

(5/D-1) {BR6, BR7, BR8}
 (5/C-1) BR8
 (3/D-1) INT ENB
 (3/C-1) DMGRANT
 (2/A-6) {RDOUT, RDIN, RSYNC, RRPLY}

(B/A-1) {INDEX, READY, TRACKO, WRT PROTECT}

(7/C-1) RDATA
 (4/C-1) 7F
 (4/C-1) CARRY

ALT VECTOR
 (3/D-5) {MATCH, BOOT}
 (3/C-5) LAOI
 (2/B-1) POK
 (8/B-3) CRC ERR
 (8/C-3) CRC DATA
 (4/C-1) RAM DATA

(7/D-1) 6MHz
 (5/D-1) {R0, R1, R2, R3}
 (5/C-1) R3
 (3/A-5) INT

(5/C-1) {R4, R5, R6, R7}

(5/C-1) {R8, R9}

(5/B-1) {CC0, CC1}
 (7/D-1) E6MHz

(5/D-1) {BR4, BR5}

(5/D-1) {BR1, BR2, BR3, BR0}
 (3/A-5) INT

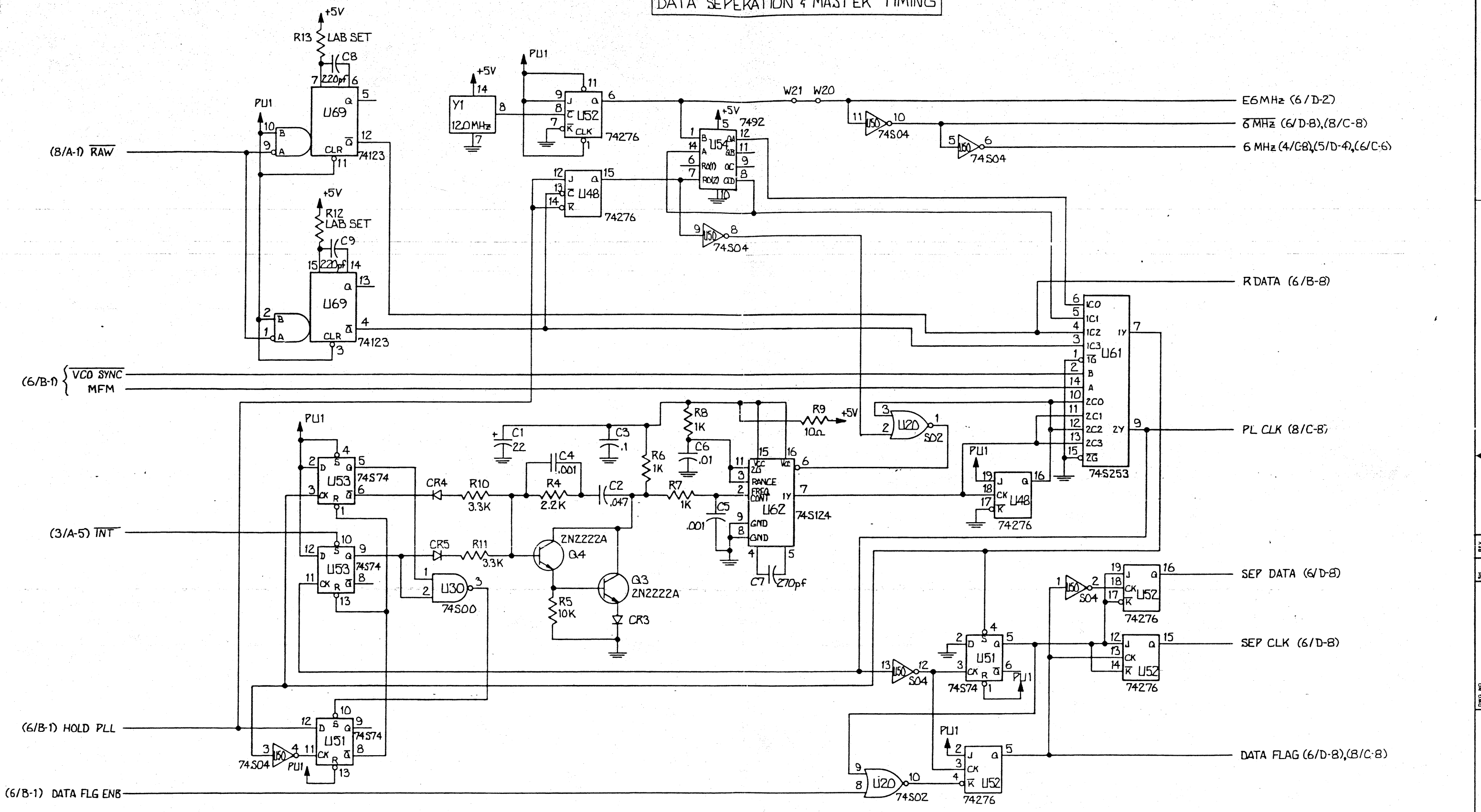
LOG RPLY ENB (3/B-8)
 ENB CRC (8/C-8)
 CALC CRC (8/B-8)
 MFM (7/C-8), (8/C-8)
 VCO SYNC (7/C-8)
 DATA FLG ENB (7/A-8)
 HOLD PLL (7/A-8)
 WRITE GATE (8/A-8, D-8)

DRIVE SEL 1 (8/B-8)
 DRIVE SEL 2 (8/A-8)
 HEAD LOAD } (8/B-8)
 SIDE SEL }
 DIRECTION (8/A-8)
 STEP (8/A-8)
 TBS7-PRECOMP (2/B-8), (8/B-8, C-8)
 BUS ENB (2/B-8)

EN17 L (2/C-5)

DATA SEPERATION & MASTER TIMING

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



(8/A-1) RAW → E6MHz (6/D-2)
→ 6MHz (6/D-8), (8/C-8)
→ 6MHz (4/C-8), (5/D-4), (6/C-6)

(6/B-1) VCO SYNC MFM → RDATA (6/B-8)

(3/A-5) TNT → PL CLK (8/C-8)

(6/B-1) HOLD PLL → SEP DATA (6/D-8)

(6/B-1) DATA FLG ENB → SEP CLK (6/D-8)

(6/B-1) DATA FLG ENB → DATA FLAG (6/D-8), (8/C-8)

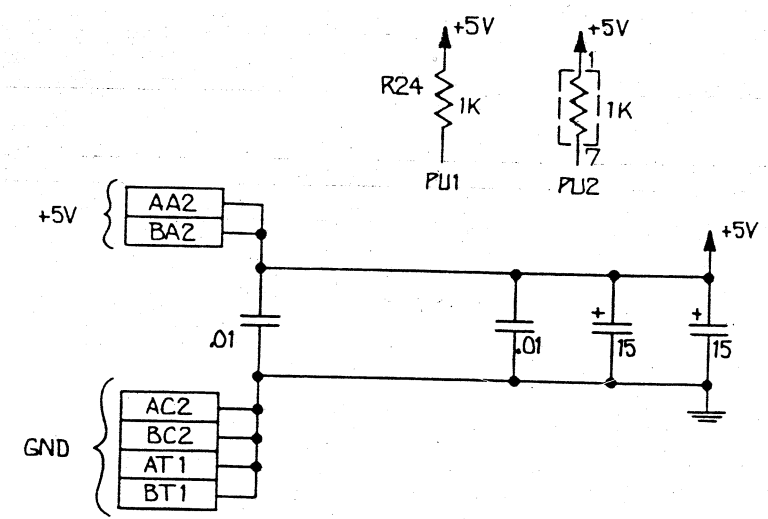
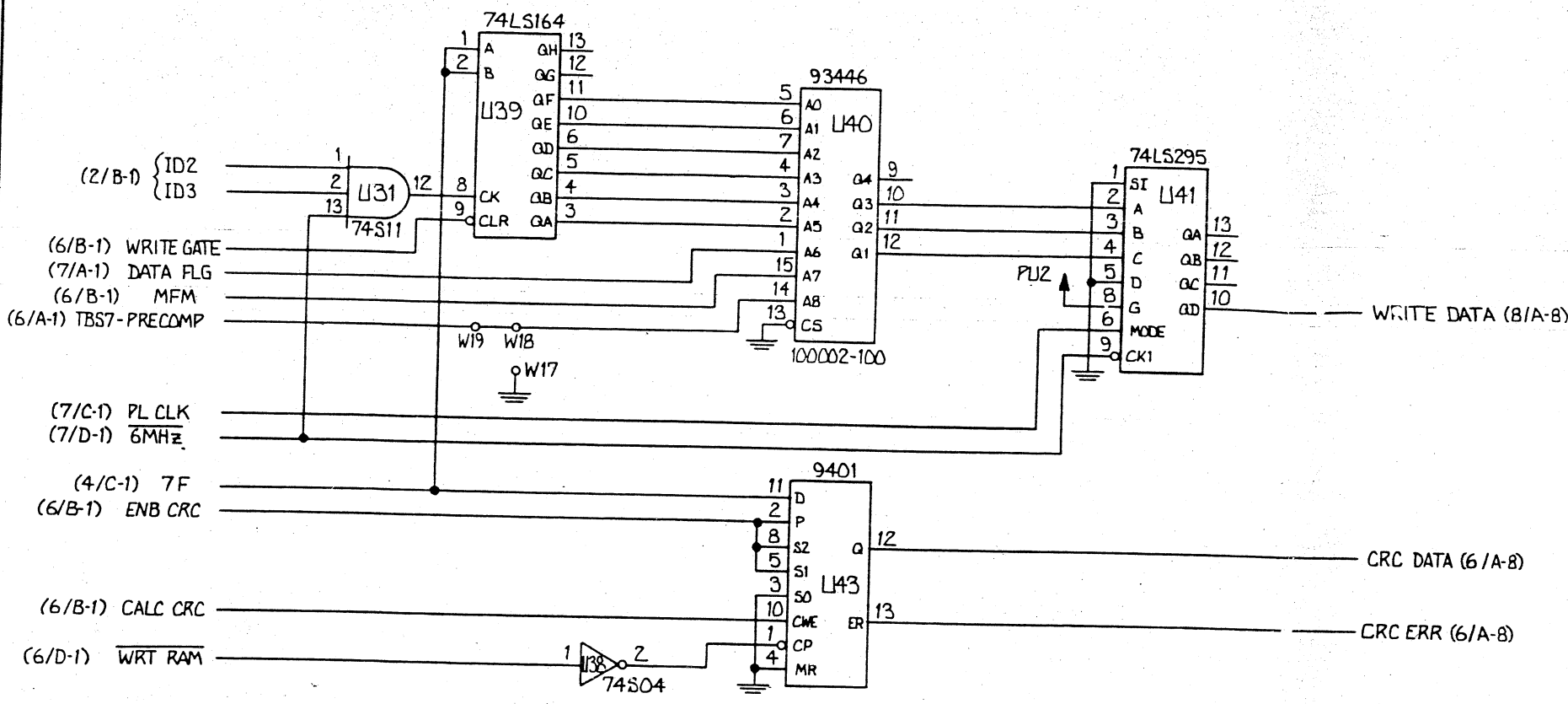
DWG NO. SD400255

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE	WORK ORDER NO.	SHEET 7 OF 8	
NONE			

FORM NO. 902 7 6 5 4 3 2 1

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

WRITE PRECOMP & CRC GENERATOR



DRIVE INTERFACE

