

DATARAM

DR-216
TECHNICAL MANUAL

P/N 06188 E

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SECTION 1 - GENERAL

Dataram Corporation's Model DR-216 Semiconductor Memory System operates in Digital Equipment Corporation's Q-BUS based mini-computers, including the MICRO/VAX I, and the MICRO/PDP-11. The DR-216 may be operated with or in place of DEC Model MSV11-L, MMV11-D, MSV11-E, and MSV11-P series memories.

The DR-216 is completely compatible with all Q-BUS computers and all standard DEC Q-BUS peripheral devices. The DR-216 operates in computers with 16, 18, or 22 address lines.

The DR-216 is a standard-height, dual-width board, which contains the following: a Q-BUS interface, timing and control logic, refresh circuitry, a MOS storage array, parity generation and checking logic, and a control and status register (CSR).

The DR-216 supports block mode for multiple DMA transfers.

SECTION 2 - ELECTRICAL SPECIFICATIONS

2.1 CAPACITY

128K X 18 (256 KB)
256K X 18 (512 KB)
512K X 18 (1 MB)
1024K X 18 (2 MB)

Two parity storage bits for parity generation and checking are included.

2.2 CYCLE TIME

Cycle time is the interval from SYNCH being received on-board (output of bus receivers) to the end of memory busy. During this interval no other cycles may start. The maximum cycle times for the DR-216 are 316 ns for a Read cycle and 391 ns for a Write cycle. Figures 2-1 through 2-8 define the bus timing when the DR-216 is operated in a Q-BUS computer.

2.3 ACCESS AND DATA VALID TIMES

Access time for a memory cycle is defined as the interval from SYNCH being received on-board (output of bus receivers) to REPLYH being generated on-board (input of bus drivers). Data valid time is the interval from the assertion of SYNC to the moment when data from memory is present on BDAL00-BDAL15. This interval is measured at the connectors of the board. The following table summarizes both access and data valid times for various memory cycles:

| | ACCESS TIMES | | DATA VALID TIMES | |
|----------|--------------|---------|------------------|---------|
| | TYPICAL | MAXIMUM | TYPICAL | MAXIMUM |
| DATI | 80 | 90 | 160 | 210 |
| DATO(B) | 85 | 121 | --- | --- |
| CSR DATI | 100 | 145 | 100 | 145 |
| CSR DATO | 70 | 105 | --- | --- |

NOTE

Cycle, access, and data valid times assume the minimum time between SYNCH and DINH/DOUTH which is 25/50 ns.

Figure 2-1. DATI (Read)

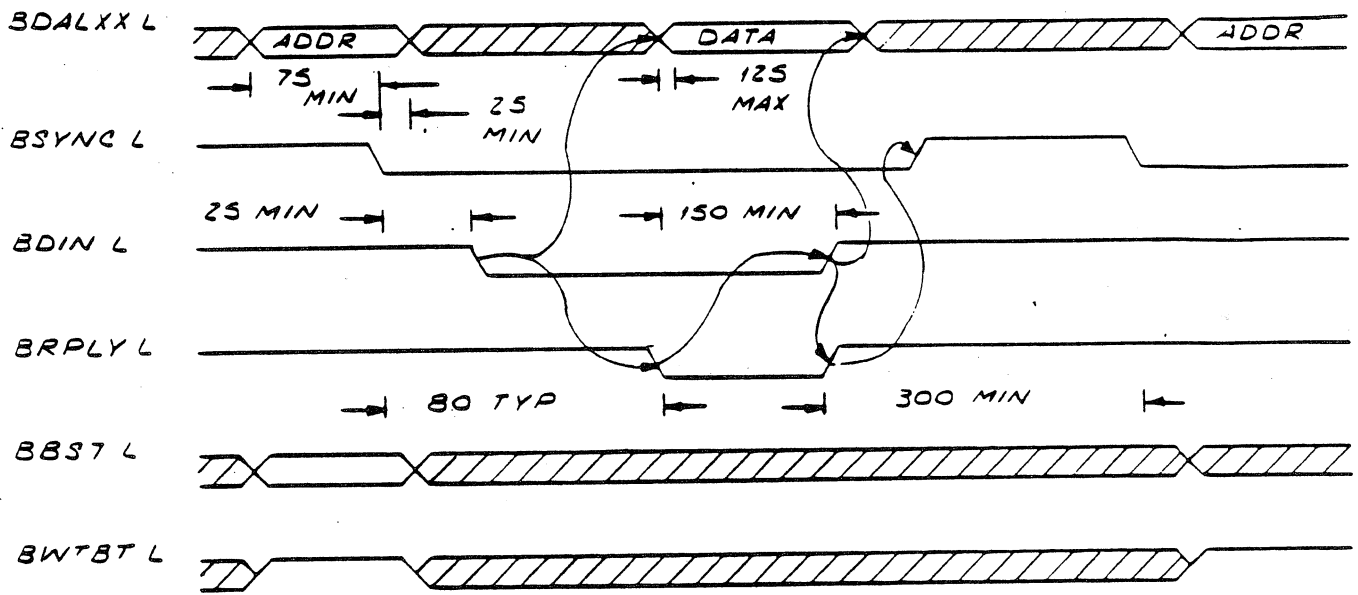


Figure 2-2. DATO (Write Word) or DATOB (Write Byte)

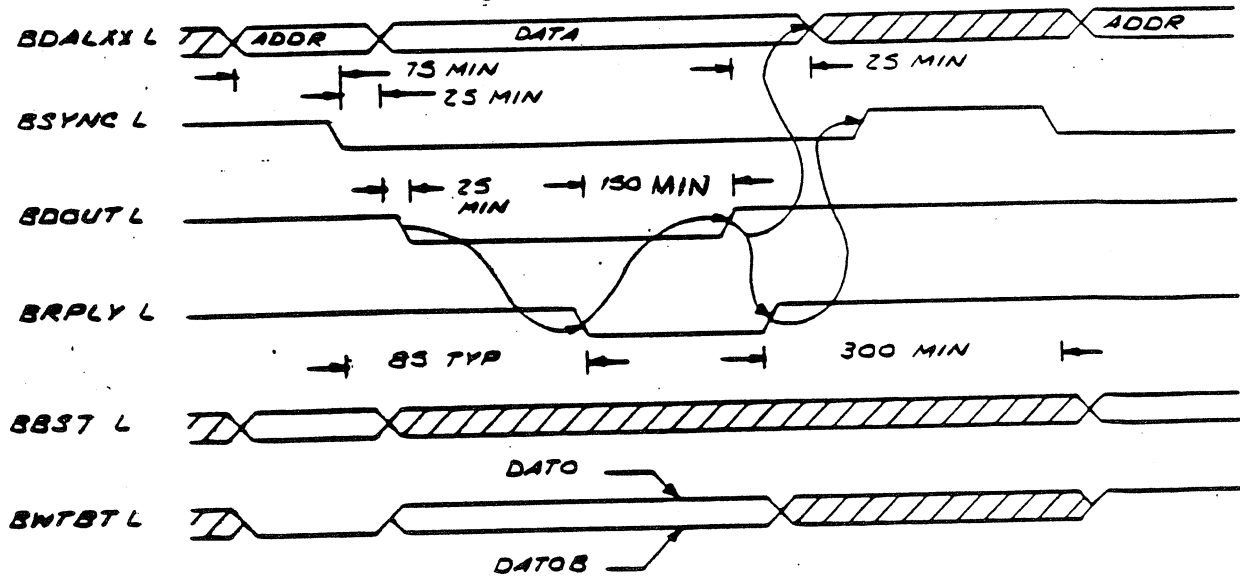


Figure 2-3. DATIO / DATIOB

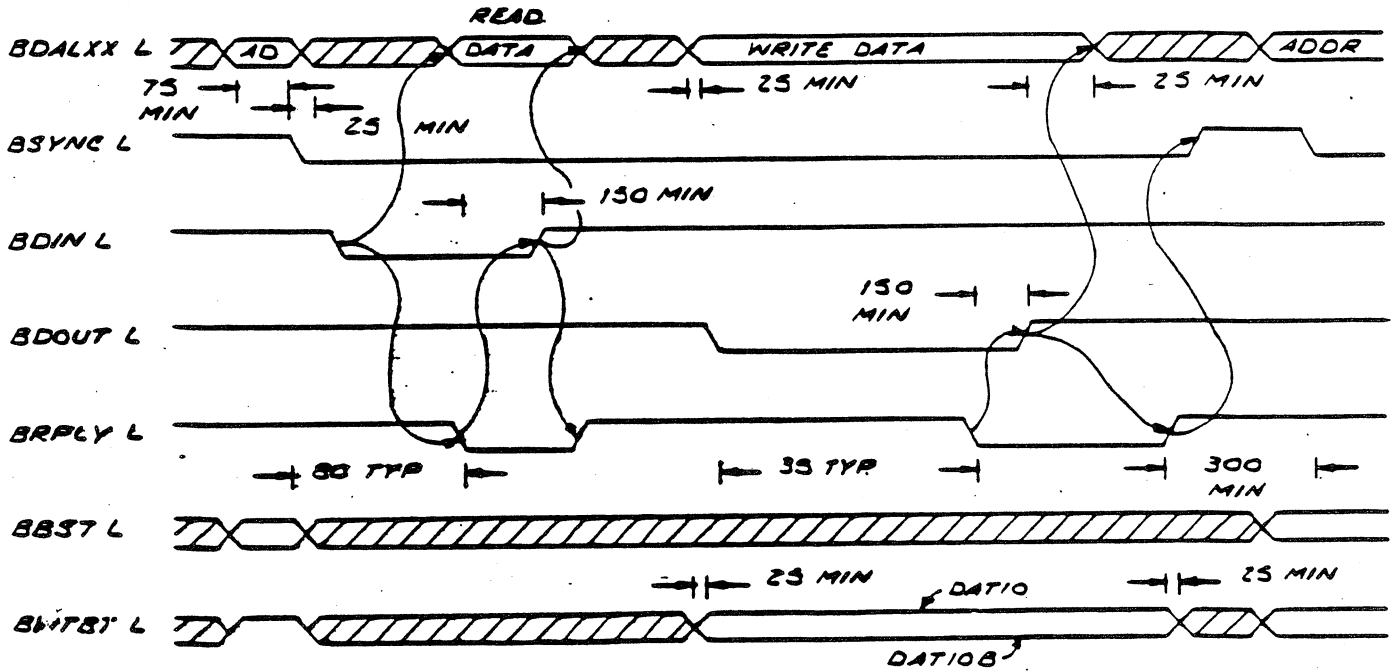
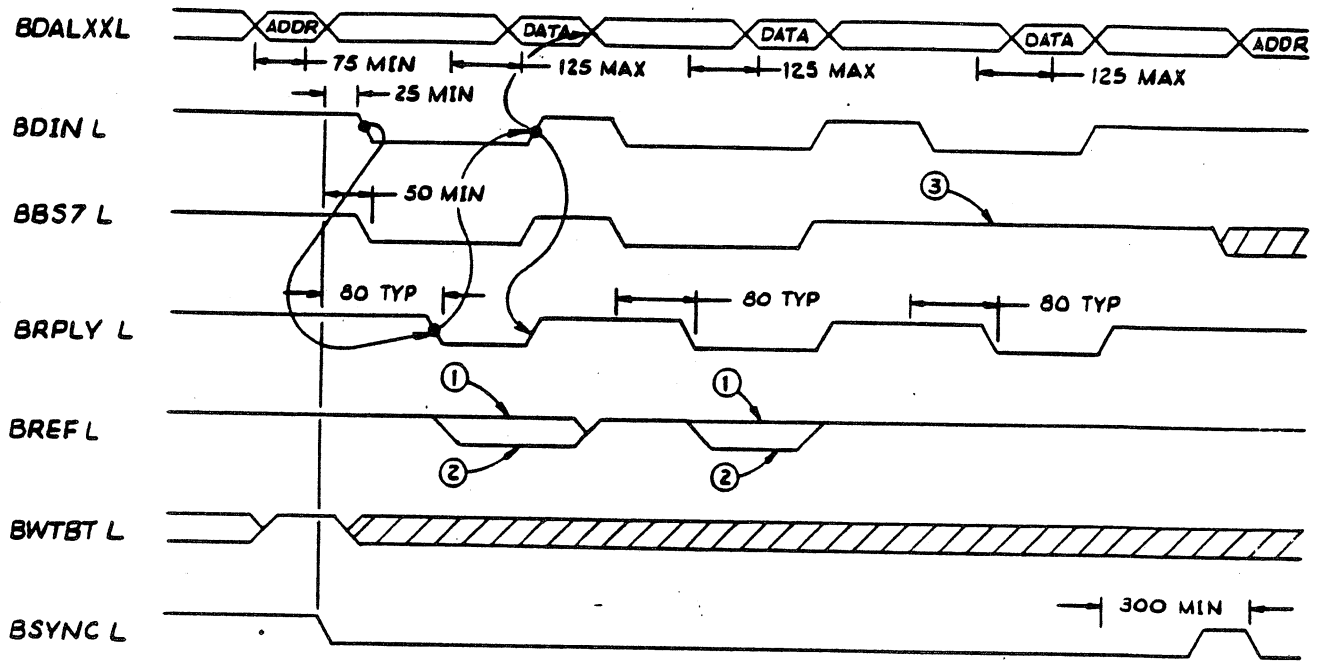
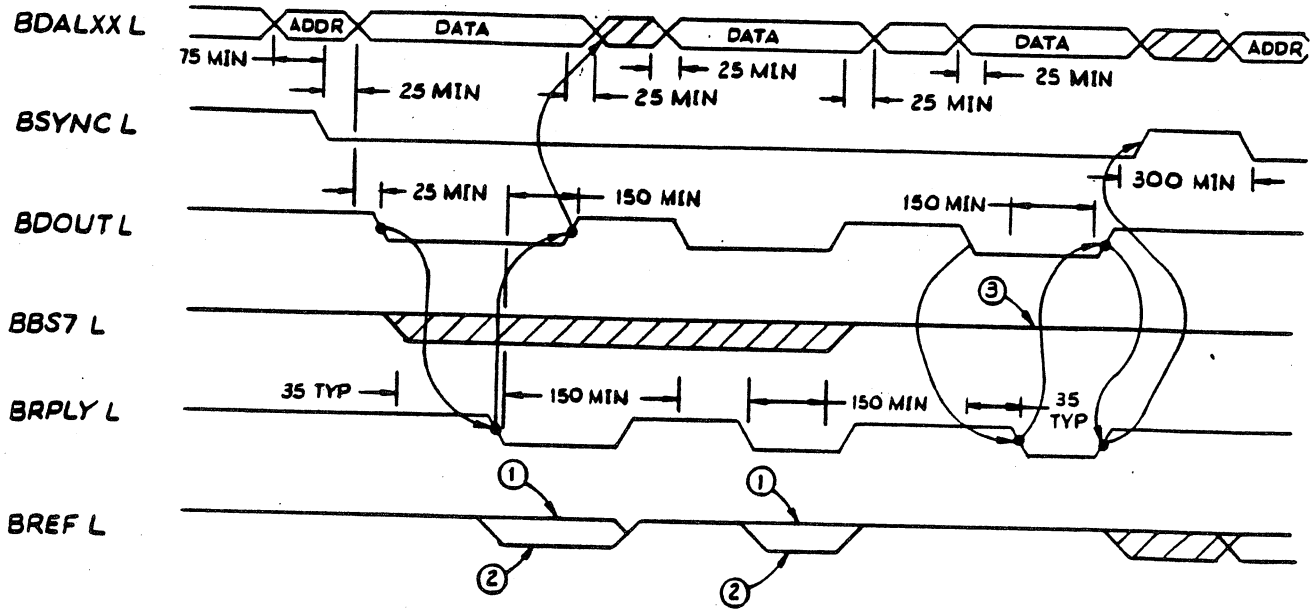


Figure 2-4. DATBI (Block Mode Read)



- ① UNABLE TO PERFORM DATBI
- ② ABLE TO PERFORM DATBI
- ③ LAST WORD TRANSFER

Figure 2-5. DATBO (Block Mode Write)



- ① UNABLE TO PERFORM DATBO
- ② ABLE TO PERFORM DATBO
- ③ LAST WORD OF TRANSFER

Figure 2-6. CSR DATI (Read)

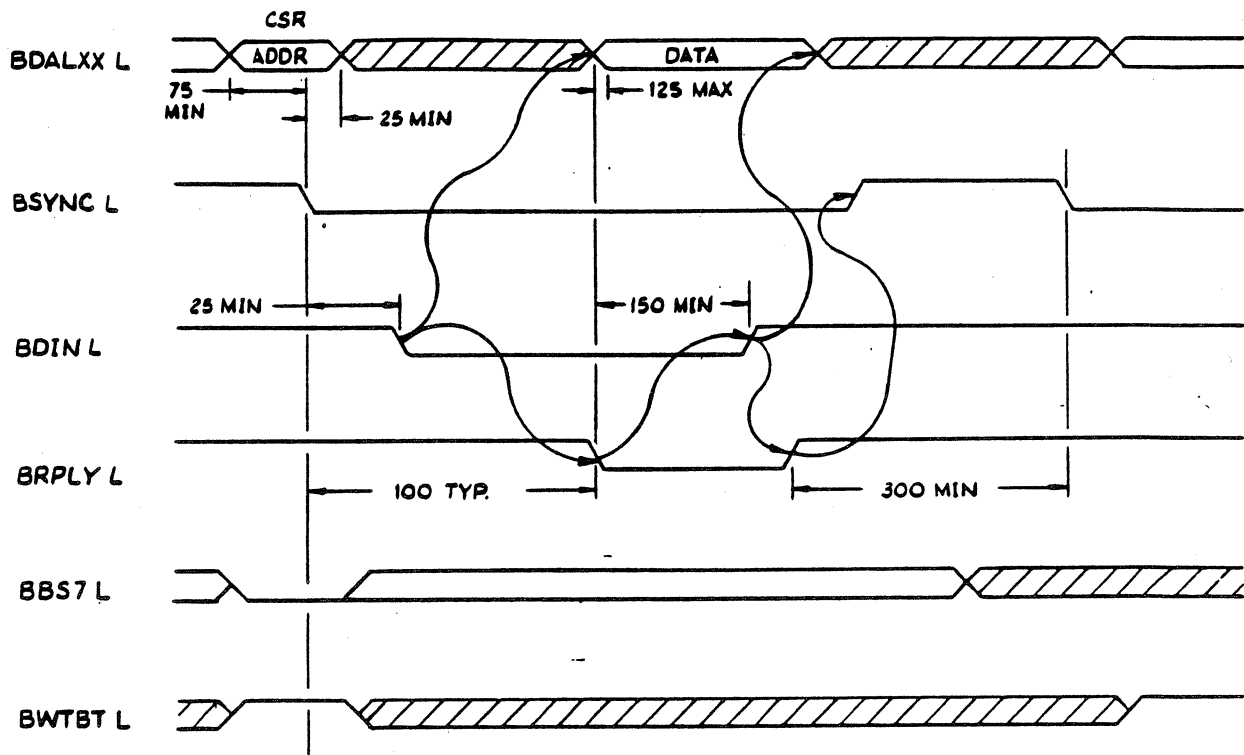


Figure 2-7. CSR DATO

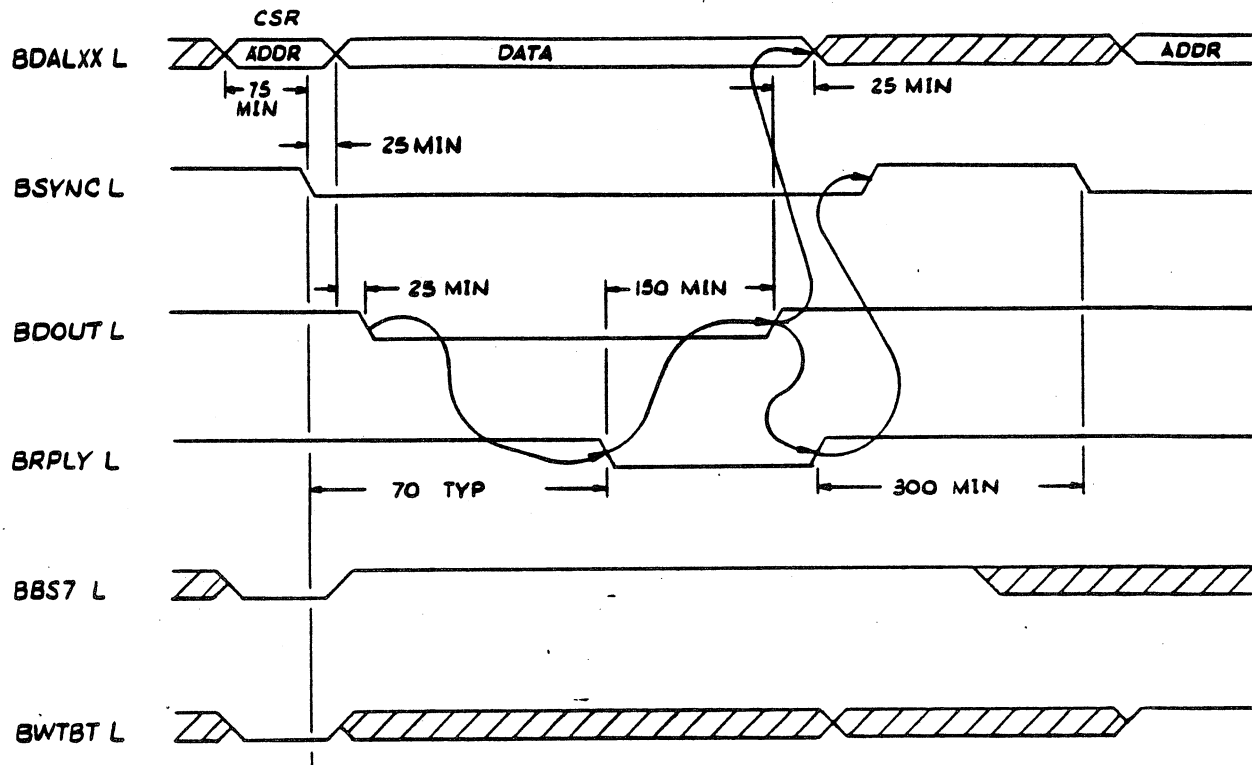
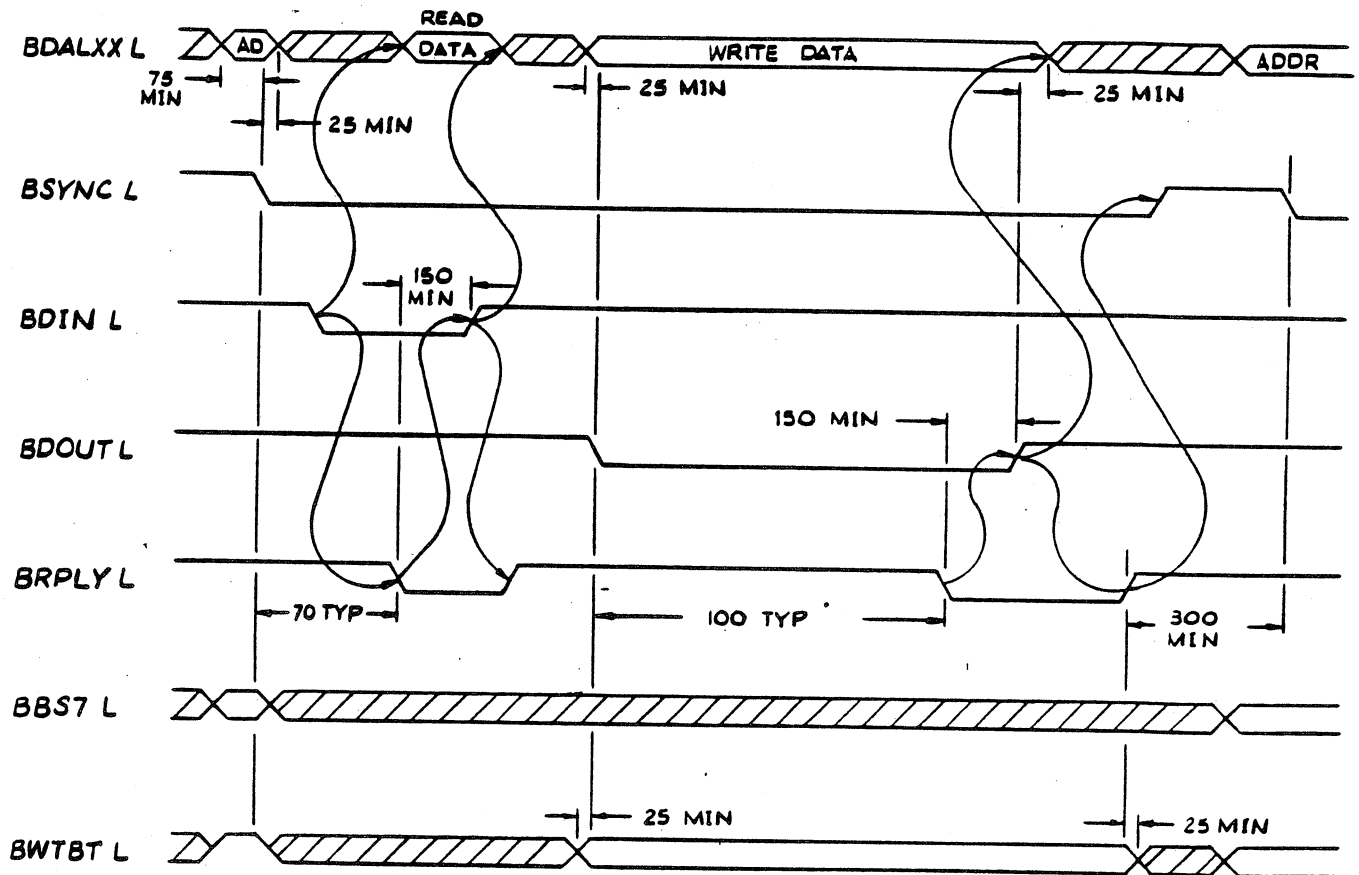


Figure 2-8. (Read-Modify-Write Word)



2.4 ADDRESSING

The DR-216 memory accepts 22 address lines. The first 16 address lines are time multiplexed with the data lines and are identified as BDAL0L through BDAL15L. The extended address lines are identified as BDAL16-21L. BDAL0L is used for upper or lower byte selection. BDAL1L through BDAL17L are decoded for 1 of 131,072 address locations within any memory module. BDAL13L through BDAL21 are used to set the initial address for a memory module. Addresses are offset in 8 KW increments using switches.

2.5 OPERATING MODES

The DR-216 performs the following operations:

| Command | Operation |
|---------|------------------------|
| DATI | Read |
| DATO | Write |
| DATOB | Write Byte |
| DATIO | Read-Modify-Write |
| DATIOB | Read-Modify-Write Byte |
| DATBI | Block Mode Read |
| DATBO | Block Mode Write |

These operations are controlled by bus signals BSYNCL, BWTBT, BDAL0L, BDINL, and BDOUTL. Figures 2-1 through 2-8 contain the timing diagrams for the above operations.

An additional mode, REFRESH, prevents loss of data stored in the NMOS storage chips. NMOS Random Access Memory (RAM) devices store data on the gate capacitance of a field-effect transistor (FET). A "1" is stored in the presence of charge and a "0" is stored in the absence of charge. The stored charge deteriorates over time and must be renewed on the DR-216 at least every two milliseconds. Therefore, one 1/128th of the memory (1/128th of each memory chip) is refreshed every 14 microseconds. This cycle is transparent to the CPU.

Refresh circuitry resides on the memory module. If a Read or Write cycle is requested during a refresh cycle, a maximum of 300 nanoseconds is added to the total cycle time.

2.6 CONTROL AND STATUS REGISTER

The control and status register (CSR) enables program control of parity functions and contains diagnostic information if a parity error occurs. The CSR is read or written to via the Q-BUS. CSR addresses are jumper-selectable within the range 172100-172136 for a 16 bit address, 772100-772136 for an 18 bit address, and 17772100-17772136 for a 22 bit address configuration. Jumper E12 determines the CSR address.

The CSR bit assignments are shown below:

| | | | | | | | | | | | | | | | |
|-----|------|------|----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAR | ERR | NOT | | A17 | A16 | A15 | A14 | A13 | A12 | A11 | NOT | WRT | NOT | PAR | |
| ERR | RTVL | USED | | OR | OR | OR | OR | OR | OR | OR | USED | WRG | USED | ENA | |
| | | | | 0 | 0 | 0 | A21 | A20 | A19 | A18 | | PAR | | | |

NOTE:

The CSR can be disabled using a strappable jumper.

Parity Enable - Bit 0

Enables parity error detection when set. The DR-216 asserts BDAL17L during data time of a DATI or DATIO cycle and allows the CPU to trap to 114g. This bit may be read or written via the Q-BUS and is cleared by BINIT.

Write-Wrong Parity - Bit 2

When set, bit 2 forces incorrect parity to be generated by the memory. Bit 2 is read or written to via the Q-BUS and is cleared by BINIT.

Error Address - Bits 5-11

These bits contain the most significant address bits within the memory location where a parity error has occurred. CSR bit 14 determines which addresses are read. Bits 5-11 may be read or written via the Q-BUS but are not cleared by BINIT.

Error Retrieval - Bit 14

Bit 14 determines which error addresses are read onto the Q-BUS. When bit 14 is reset, address lines A11-A17 are read. When bit 14 is set, A18-A21 are read. Bit 14 should be locked in a reset position for systems with only 16 or 18 address lines. Bit 14 is read or written to from the Q-BUS and is cleared by BINIT.

Parity Error - Bit 15

Bit 15 is set when a parity error occurs. It does not cause a parity trap in the processor. Bit 15 may be read or written via the Q-BUS and is cleared by BINIT.

Unused Bits - Bits 1,3,4,12 and 13

These bits are not used and are always read as a logical zero.

2.7 POWER REQUIREMENTS

The DR-216 Memory System requires the same DC voltages as the MSV11-L DEC memory. The necessary logic to operate with battery backup is provided on the memory module (+5B-AV1). The voltage-current requirements for each 1024K x 18 memory assembly are as follows:

| | Operating Amps | Standby Amps | Voltage Margin |
|-------------|-------------------|-----------------|-------------------|
| +5V | 1.3 | 1.3 | +5% |
| +5V Battery | 1.0 | .7 | +5% |
| +5V Total | 2.3 | 2.0 | +5% |

2.8 BUS SIGNALS

BDAL0L through BDAL21L Data/Address Lines

These 22 lines communicate address and data information. The device requesting the memory first places an address on these lines. Then the device either receives input data from the memory or outputs data to the memory over the same bus lines. Extended addresses BDAL16-21L enable addressing of up to 4MB of memory. BDAL16L is also used for parity error signal propagation.

BSYNCL Synchronize

Asserted by the bus master to instruct the memory to accept address information on the BDAL bus.

BWTBT Write/Byte

When asserted by the bus master prior to BSYNCL, it instructs memory to prepare for a DATO (Write) operation. If BWTBTL is asserted during BDOUTL in a DATO operation, then the operation becomes a DATOB (Write Byte) cycle.

BDCOKH DC Power OK

BDCOKH is asserted by the power supply. BDCOKH inhibits all memory operation except Refresh cycles.

BDINL**Data Input**

Asserted by the bus master when it is ready to accept data from memory. Memory must then respond with BRPLYL to complete the handshake.

BDOUTL**Data Out**

Asserted by the bus master to indicate that the data headed for memory is valid on the BDAL bus lines. The memory must respond with BRPLYL to complete the handshake.

BRPLYL**Reply**

Asserted by the memory to indicate to the bus master that data is available on the BDAL bus or that the memory has accepted data from the bus.

BBS7L**Bank 7 Select**

Asserted by the bus master when the selected address is on the I/O page. BBS7L is also used by memory to select the CSR and disable normal memory operation.

BREFL**Refresh**

Asserted during BDIN or BDOUT cycles to instruct the on-board address counter to increment, thus enabling a block mode transfer.

2.9 INDICATOR LAMPS

The DR-216 contains three LED indicator lamps, shown in Figure 3-1, which define the following conditions:

LED2 (RED) - When LED2 is lit, a parity error has occurred on the memory board. LED2 is reset (extinguished) by initializing the system with BINITL, or by writing a zero into bit 15 of the status register.

LED1 (RED) - When LED1 is lit, a memory cycle, is in progress.

LED3 (GREEN) - When LED3 is on, correct power is being supplied to memory. LED3 is powered by the +5 VB line. Thus, if the +5 VL supply fails, the LED remains lit if proper backup power exists.

2.10 OPTIONS**2.10.1 I/O Space**

I/O space size is strappable for 4K, 2K, 1K and .5K words.

2.10.2 Battery Backup

The DR-216 provides the necessary jumper-selectable logic to operate with battery backup. Battery backup provides a +5 VB power line to maintain the RAM array.

2.10.3 External Parity Control

Strapping options enable the DR-216 to operate in systems where an external parity controller controls parity functions on all memories within the system.

SECTION 3 - MECHANICAL SPECIFICATIONS

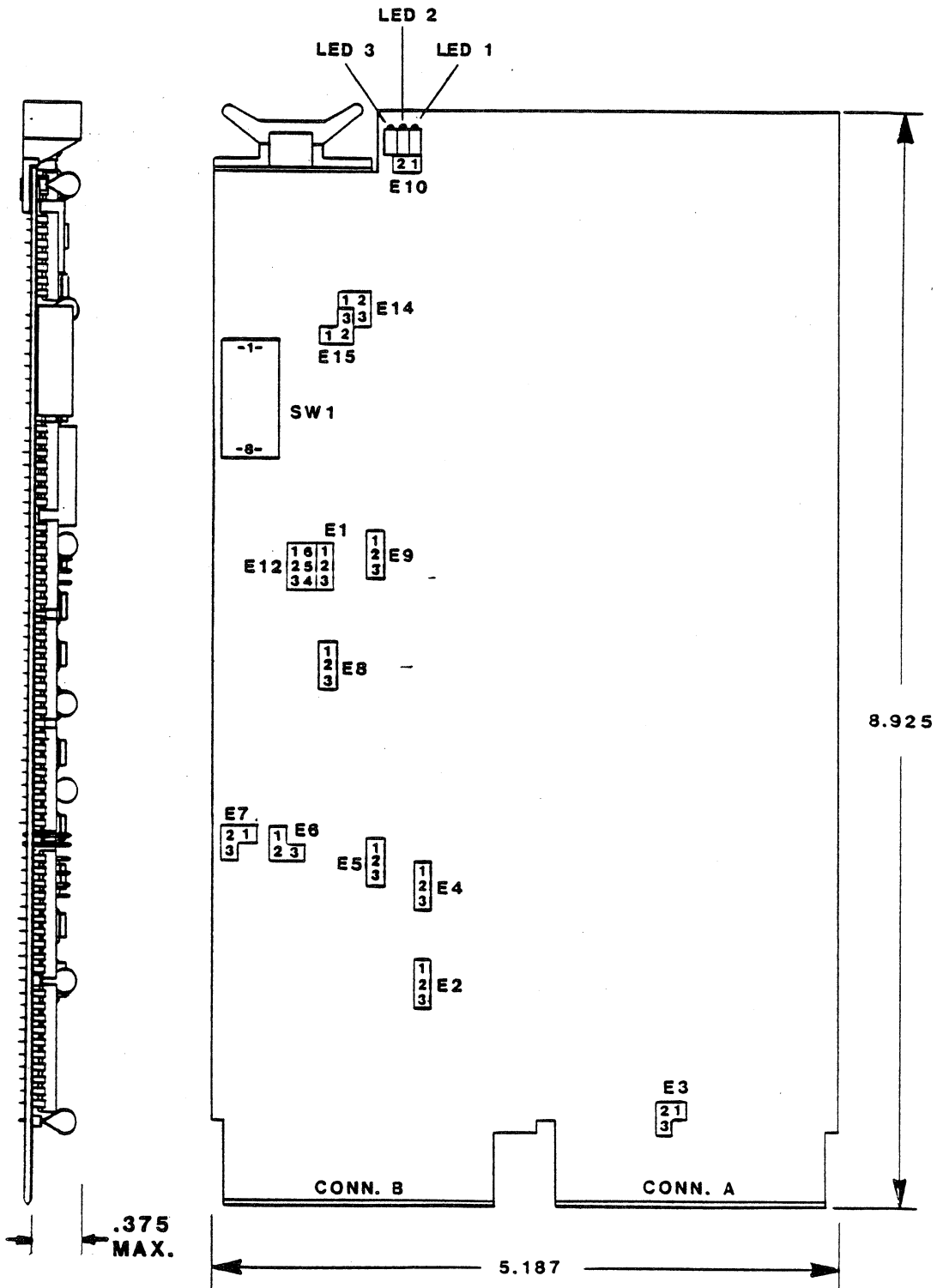
3.1 DIMENSIONS

The DR-216 fits into the Q-BUS chassis or equivalent, occupying a standard dual printed circuit board slot. The memory board dimensions are .466 in (11.84mm) x 8.92 in (226.57mm) x 5.186 in (131.72mm). See Figure 3-1.

3.2 WEIGHT

.72 pounds (.33 kg)

Figure 3-1. DR-216



SECTION 4 - ENVIRONMENTAL SPECIFICATIONS

4.1 TEMPERATURE

Operating: 0°C to +55°C
Storage: -40°C to +80°C

4.2 HUMIDITY

Operating: 0 to 90% (without condensation)
Non-Operating: 0 to 95% (without condensation)

4.3 ALTITUDE

Operating: 1000 ft (300 m) below to 10,000 ft (3000 m) above
mean sea level
Non-Operating: 1000 ft (300 m) below to 20,000 ft (6000 m) above
mean sea level

4.4 VIBRATION

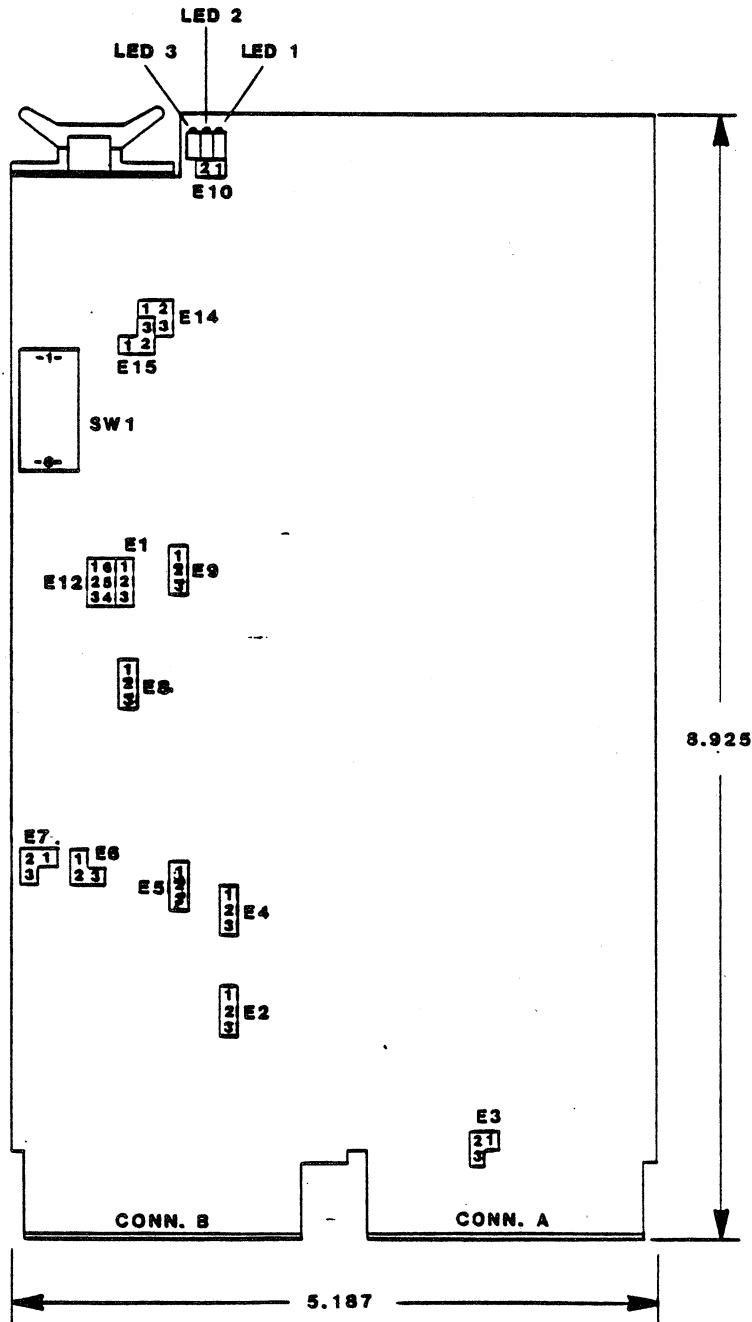
Withstands normal stresses encountered in transportation.

SECTION 5 - INSTALLATION

5.1 SWITCH SETTINGS/JUMPER OPTIONS

When installing the DR-216, set the starting address according to Table 5-1. Set the CSR address according to Table 5-2.

Figure 5-1. DR-216 Jumper Locations
(Boards at REV E and later)



Jumper Options

Table 5-3 summarizes all jumper functions. Figures 5-1 and 5-2 detail the jumper locations for the different revision levels of artwork.

To determine which drawing to use, inspect switch 1. If switch 1 is an 8 position DIP, use Figure 5-1. If switch 1 is a 10 position DIP, use Figure 5-2. For boards with a 10 position switch, positions 9 and 10 are not used.

Figure 5-2. DR-216 Jumper Locations
(Boards at REV D and earlier)

(10) R10-15
R11-100

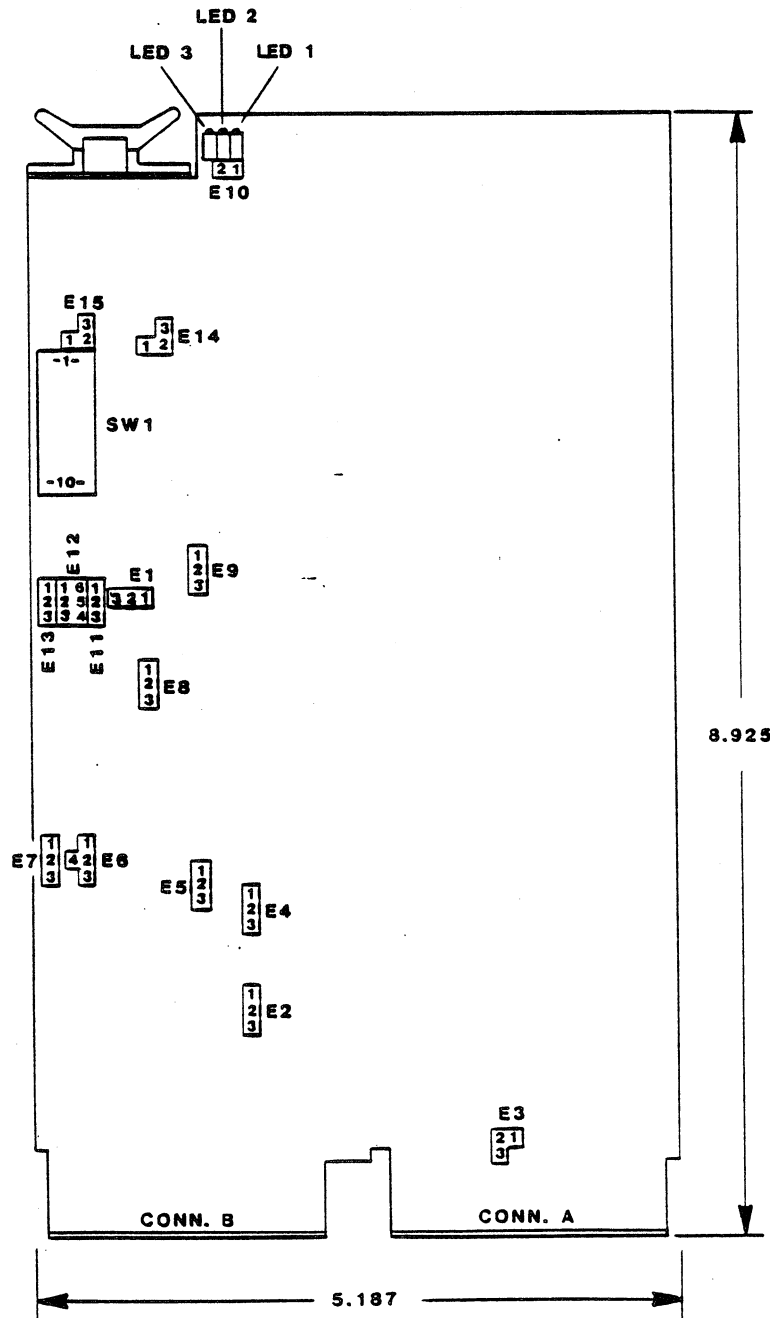


Table 5-1. Switch SW1

| STARTING ADDRESS | POS 8 | POS 7 | POS 6 | POS 5 |
|------------------|-------|-------|-------|-------|
| 0KW | OFF | OFF | OFF | OFF |
| 8KW | ON | OFF | OFF | OFF |
| 16KW | OFF | ON | OFF | OFF |
| 24KW | ON | ON | OFF | OFF |
| 32KW | OFF | OFF | ON | OFF |
| 40KW | ON | OFF | ON | OFF |
| 48KW | OFF | ON | ON | OFF |
| 56KW | ON | ON | ON | OFF |
| 64KW | OFF | OFF | OFF | ON |
| 72KW | ON | OFF | OFF | ON |
| 80KW | OFF | ON | OFF | ON |
| 88KW | ON | ON | OFF | ON |
| 96KW | OFF | OFF | ON | ON |
| 104KW | ON | OFF | ON | ON |
| 112KW | OFF | ON | ON | ON |
| 120KW | ON | ON | ON | ON |

For all other settings use equal increments of 128KW plus the appropriate 8KW increment from the above table.

| | POS 4 | POS 3 | POS 2 | POS 1 |
|---------------|-------|-------|-------|-------|
| 0 - 128KW | OFF | OFF | OFF | OFF |
| 128 - 256KW | ON | OFF | OFF | OFF |
| 256 - 384KW | OFF | ON | OFF | OFF |
| 384 - 512KW | ON | ON | OFF | OFF |
| 512 - 640KW | OFF | OFF | ON | OFF |
| 640 - 768KW | ON | OFF | ON | OFF |
| 768 - 896KW | OFF | ON | ON | OFF |
| 896 - 1024KW | ON | ON | ON | OFF |
| 1024 - 1152KW | OFF | OFF | OFF | ON |
| 1152 - 1280KW | ON | OFF | OFF | ON |
| 1280 - 1408KW | OFF | ON | OFF | ON |
| 1408 - 1536KW | ON | ON | OFF | ON |
| 1536 - 1664KW | OFF | OFF | ON | ON |
| 1664 - 1792KW | ON | OFF | ON | ON |
| 1792 - 1920KW | OFF | ON | ON | ON |
| 1920 - 2048KW | ON | ON | ON | ON |

ON = Closed
OFF = Open

Table 5-2. CSR Address Select

| 16 Bit Address | 18 Bit Address | 22 Bit Address | Jumper E12 | | | |
|-------------------|-------------------|-------------------|---------------|---------------|---------------|---------------|
| | | | Pin 1 to 2 | Pin 2 to 3 | Pin 4 to 5 | Pin 5 to 6 |
| 172100 | 772100 | 17772100 | OUT | OUT | OUT | OUT |
| 172102 | 772102 | 17772102 | IN | OUT | OUT | OUT |
| 172104 | 772104 | 17772104 | OUT | IN | OUT | OUT |
| 172106 | 772106 | 17772106 | IN | IN | OUT | OUT |
| 172110 | 772110 | 17772110 | OUT | OUT | IN | OUT |
| 172112 | 772112 | 17772112 | IN | OUT | IN | OUT |
| 172114 | 772114 | 17772114 | OUT | IN | IN | OUT |
| 172116 | 772116 | 17772116 | IN | IN | IN | OUT |
| 172120 | 772120 | 17772120 | OUT | OUT | OUT | IN |
| 172122 | 772122 | 17772122 | IN | OUT | OUT | IN |
| 172124 | 772124 | 17772124 | OUT | IN | OUT | IN |
| 172126 | 772126 | 17772126 | IN | IN | OUT | IN |
| 172130 | 772130 | 17772130 | OUT | OUT | IN | IN |
| 172132 | 772132 | 17772132 | IN | OUT | IN | IN |
| 172134 | 772134 | 17772134 | OUT | IN | IN | IN |
| 172136 | 772136 | 17772136 | IN | IN | IN | IN |

NOTE:

E5 Pin 2 to 3 disables CSR selection.
 E7 Pin 2 to 3 must be installed for 16 or 18 bit address operation.

Table 5-3. Jumper Function Summary

| FUNCTION | IN | OUT |
|----------------------------------|----------------|----------------|
| CSR Selection | | |
| Disable CSR | E5-2 to E5-3 | E5-1 to E5-2 |
| Enable CSR | E5-1 to E5-2 | E5-2 to E5-3 |
| Parity Error Reporting | | |
| Non-CSR | E1-2 to E1-3 | E1-1 to E1-2 |
| With CSR | E1-1 to E1-2 | E1-2 to E1-3 |
| Write Wrong Parity Enable | | |
| Enable | E6-1 to E6-2 | E6-2 to E6-3 |
| Disable | E6-2 to E6-3 | E6-1 to E6-2 |
| Parity | | |
| Disable | E4-2 to E4-3 | E4-1 to E4-2 |
| Enable | E4-1 to E4-2 | E4-2 to E4-3 |
| Memory Size | | |
| Fully Populated | E14-1 to E14-2 | E14-2 to E14-3 |
| Half Populated | E14-2 to E14-3 | E14-1 to E14-2 |
| Addressing | | |
| 16/18 Bit Address | E7-2 to E7-3 | E7-1 to E7-2 |
| 22 Bit Address | E7-1 to E7-2 | E7-2 to E7-3 |
| Battery Backup | | |
| Battery Backup | E3-2 to E3-3 | E3-1 to E3-2 |
| No Battery Backup | E3-1 to E3-2 | E3-2 to E3-3 |
| Block Mode | | |
| Enable | E2-1 to E2-2 | E2-2 to E2-3 |
| Disable | E2-2 to E2-3 | E2-1 to E2-2 |
| I/O Space Size | | |
| 4KW | E8-1 to E8-2 | --- |
| | E8-2 to E8-3 | --- |
| | E9-1 to E9-2 | E9-2 to E9-3 |
| 2KW | E8-2 to E8-3 | E8-1 to E8-2 |
| | E9-1 to E9-2 | E9-2 to E9-3 |
| 1KW | E8-1 to E8-2 | E8-2 to E8-3 |
| | E9-1 to E9-2 | E9-2 to E9-3 |
| .5KW | --- | E8-1 to E8-2, |
| | --- | E8-2 to E8-3 |
| | E9-1 to E9-2 | E9-2 to E9-3 |

Table 5-3. (Cont'd)

| FUNCTION | IN | OUT |
|----------------|----------------------------------|----------------------------------|
| 64K/256K DRAMs | | |
| 64K | E15-1 to E15-2 E10-1 to E10-2 | E15-2 to E15-3 --- |
| 256K | E15-2 to E15-3 --- | E15-1 to E15-2 E10-1 to E10-2 |

5.2 COMPUTER INSTALLATION

The DR-216 plugs into a dual-width Q-Bus (LSI-11) slot. Install the DR-216 into a LSI-11 computer as follows:

1. Set starting address. Take care not to overlap memory module addresses. If they do, the computer will not boot.
2. Set the CSR address if CSR is enabled. Each CSR must have a unique address. If more than one CSR is used, the CSR addresses must be in increasing order relative to the memory which it is monitoring. For example, if memory locations 0000 to 512K words have a CSR located at address 17772104, the next CSR must be at an address above 17772104 (i.e., 17772106, 17772110). In this configuration, CSR addresses 17772100 and 17772102 cannot be used.
3. Plug the DR-216 into the computer.

NOTE:

Due to a design change, jumper point E4 has been eliminated and should no longer be inserted on assembly numbers 61545, 61546, 61548 and 61549 revision levels C7 or D4. The assembly number and revision level are stamped on the solder side of the board along one edge.

All other revision levels still require jumper E4-1 to E4-2 to be inserted for parity to be enabled.

5.3 DIAGNOSTICS

The DR-216 is compatible with all DEC memory diagnostics. However some diagnostics will not exercise the entire memory board. The following is a list of recommended diagnostics for the DR-216:

11/23, 11,23+, 11/73 Processors and the MicroPDP.

Use either diagnostic ZMSD?? or VMSA??.

NOTE

The 11/73 processor has an on-board cache that must be disabled prior to running any diagnostics. The steps are as follows:

1. Boot the operating system, XXDP or XXDP+.
2. After the prompt, a period (.), press the break key if enabled or the halt switch on the front panel.
3. Deposit 14 in location 17777746, the cache control register. This will disable the cache on the 11/73.
4. Type P to return to XXDP or XXDP+. Do not use the GO command because a bus INIT will be issued which will clear the cache control register.

MICROVAX I

Use diagnostic EHXMS.

NOTE

The 2 megabyte DR-216 will fail with this diagnostic. The error message will be:

```
Error during test 2, subtest 5
Memory Configuration Test, Memory/CSR Correlation Test
Part 1
Too few memory CSRs present; expected at least 2, found 1
```

This error will occur on all boards larger than 1 megabyte, including DEC's. Later versions of the diagnostic should have this problem corrected. Presently, the only way around this problem is to disable the halt feature of the diagnostic.

5.3.1 Determining Bad Ram Locations

If a diagnostic uncovers a bad ram location it should be replaced to insure data integrity.

All DRAMs are socketed so replacement can be done with little trouble. To find the location of a defective DRAM on the DR-216 follow the procedure outlined below. All addresses are given in both octal and decimal to facilitate replacement.

All addresses are given in both octal and decimal to facilitate replacement.

1. Subtract the starting address of the DR-216 memory board from the address of the bad DRAM.
2. Determine which row the bad DRAM is in by using the appropriate table below. Table 5-4 is for DR-216 memory boards populated with 64k DRAMs and Table 5-5 is for boards with 256k DRAMs. Use only the first two entries in a table for half populated boards.

Table 5-4. 64K DRAMs

| Octal | Address | | Row |
|-----------------|-------------|---------|-----|
| | Octal | Decimal | |
| 0-377777 | 0-128KB | A | |
| 400000-777777 | 128KB-256KB | C | |
| 1000000-1377777 | 256KB-384KB | B | |
| 1400000-1777777 | 384KB-512KB | D | |

Table 5-5. 256K DRAMs

| Octal | Address | | Row |
|-----------------|---------------|---------|-----|
| | Octal | Decimal | |
| 0-1777777 | 0-512KB | A | |
| 2000000-3777777 | 512KB-1024KB | C | |
| 4000000-5777777 | 1024KB-1536KB | B | |
| 6000000-7777777 | 1536KB-2048KB | D | |

3. The row letter is silkscreened on the edge of the board opposite from the connector fingers. The bit numbers are silkscreened down the side of the DRAM array near the long edge of the board. The parity bits are designated by P0 and P1.

5.4 TROUBLESHOOTING GUIDE

The DR-216 is completely tested prior to shipping. However, sometimes problems do occur and the board fails to function correctly. If a problem does arise, the following sequence of steps should be followed to isolate the fault.

1. With power off, remove the DR-216 from the backplane and visually inspect it for damaged components and other obvious problems.
2. Check the strapping of the board against Table 5-3, and use Table 5-1 to insure that switch 1 (SW1) is set to the proper starting address.

3. Turn power on and check the backplane for proper voltages at the following pins:

| | |
|---------|-------------|
| +5V | AA2,BA2,BV1 |
| +5V BBU | AV1 |

4. Remove power from the backplane and replace the DR-216 in the computer. Turn the computer back on and verify that the DR-216 can be read from and written to under ODT.
5. If the fault has been isolated to the DR-216, run one of the diagnostics recommended in section 5.3. If the system will not boot with the DR-216, put a working memory board at location 000000 and set the address of the DR-216 in question to start above that of the lower board. Now boot and run the diagnostic.
6. If the problem persists, call the Dataram sales representative for help.

SECTION 6 - PROGRAMMING

A programmable control register, the control-and-status register (CSR) resides on the DR-216. The CSR monitors parity, and contains the diagnostic information if a parity error occurs. Programming involves addressing the CSR during a DATI, DATO, and DATIO bus cycle (see table 5-2). CSR bit assignments are described in Section 2.6.

SECTION 7 - THEORY OF OPERATION

The DR-216 operates in any of DEC's LSI-11 bus (Q-BUS) compatible computers. It performs DATI, DATO(B), DATIO(B), DATBO, and DATBI bus cycles as a slave device for any Q-BUS master. The following description details the operation of the DR-216 in a Q-BUS compatible computer.

7.1 HARDWARE

7.1.1 Bus Signals

BDAL00....used to select a single byte in a word when BWTBTL is asserted during a write operation. Data bit 00 is multiplexed on this line during the data portion of a memory cycle.

BDAL01-BDAL15L....multiplexed data and address lines.

BDAL16-BDAL21L....upper address lines used to extend addressing capability to 4 megabytes. BDAL16 is also used as a parity error signal during the data portion of a read cycle.

BSYNCL....a synchronizing control signal from the bus master to memory. BSYNCL indicates address information is stable on the bus and initiates a memory cycle.

BWTBTL....this signal is asserted during the addressing portion of a memory access cycle to signal a DATI or DATIO cycle is going to take place. It is asserted during the data portion of a memory cycle for a byte write operation.

BBS7L....a signal from the bus master that it is accessing data in the I/O page, 28K-32KW. It is also used to signify a DATBI cycle.

BDCOKH....a high asserted signal signifying that DC power is stable.

BDINL....a request from the bus master for memory read data to be placed on the BDAL bus lines. The memory must answer with BRPLYL for completion of the memory cycle.

BDOUTL....a request from the bus master for the memory to accept write data from the bus and store the data in memory. The memory must answer with BRPLYL to complete the memory cycle.

BRPLYL....a required response from the memory indicating read data is valid or write data has been accepted from the bus.

BREFL....a response from the memory indicating that it is able to continue a block mode transfer, either a DATBI or DATBO cycle.

7.1.2 Internal Signals

RDYN....asserted by the refresh controller when it is ready to do a refresh.

RDYD....RDYN delayed 100 ns and inverted, used for refresh arbitration.

REFREQ....signals refresh controller to start a refresh cycle.

VALADD....asserted if the bus master is addressing the memory board.

START....assertion of START initiates the DRAM timing chain.

A0-A8....address lines of DRAM array.

D2....timing pulse used to multiplex the row and column addresses onto A0-A8.

RASAN, RASBN, RASCN, RASDN....row address strobe, low asserted signal that determines which row is being accessed. Used to strobe row addresses into the DRAM array.

CASON, CASIN....column address strobe, asserted low when column addresses are valid on A0-A8.

WRAN, WRBN....write enable lines to the RAM array. For word writes, both WRAN and WRBN are asserted and for byte writes only one line is asserted.

RDCSRDN....a low asserted signal which gates the CSR data onto the internal data bus.

WRCSR....asserted to during a CSR write cycle to clock data into the CSR.

INCOUNT....leading edge increments the counter during a block mode operation.

MAXN....asserted low if the memory board cannot do another block mode transfer.

LATWTBT....WTBT latched on the leading edge of SYNCH, used to determine if the cycle is a memory read or memory write.

DIOLAT....used to determine which byte is being accessed during a byte write cycle.

LAD00-LAD21....addresses from the bus.

DI000-DI015....internal data bus.

CSRH....asserted when the CSR address is placed on the bus during the addressing portion of a memory access cycle.

IOSPCH....asserted when the address on the bus is in the I/O page (BBS7 asserted).

7.2 BLOCK DIAGRAM

The circuitry on the DR-216 can be broken up into five functional groups: the Q-BUS transceivers, the DRAM array, the CSR and associated control, control logic and refresh control. A functional block diagram of the DR-216 illustrating the five groups is on page one of the schematic.

7.2.1 Q-BUS Transceivers

The Q-BUS transceivers buffer all signal lines between the Q-BUS and the DR-216 memory board. This includes all data, address and control signals. The types of transceivers used include AM2908, DM8641 and 74LS340.

7.2.2 DRAM Array

The DRAM array occupies most of the board area and is laid out as four rows of eighteen chips. Each row accommodates sixteen data bits and two parity bits. In a half populated board only two of the four rows are occupied by DRAMs. The DR-216 is populated with either 64k x 1 or 256k x 1 DRAMs depending on the size ordered.

7.2.3 CSR And Associated Control

The CSR control logic monitors the DRAM array for possible parity errors. If an error does occur, the address of the location where the error occurred is loaded into the CSR and the processor is notified using BDAL16L. The CSR is also used in a diagnostic capability by many diagnostics and operating systems to size the board and determine if any DRAM locations are bad.

7.2.4 Control Logic

The control logic is shown on the block diagram as five separate blocks. These blocks are labeled Timing & Control, Memory Select & RAS Decode, CAS & WR Drivers, Address MUX & RAM Drive and Block Counter & Address Latch. This logic ties together the rest of the circuitry on the board so that the DR-216 will function properly. The control logic's main function is to arbitrate between a refresh cycle and a memory access cycle. Other functions include determining if the board is being accessed, determining which row the data is in, and generating parity to be written during a write cycle. The control logic is implemented in two high-speed PALs and two FPLAs.

7.2.5 Refresh Control

The refresh control signals the control logic when it is time to do a refresh operation. It also generates the control signals needed to do the refresh operation including RAS and the address. The refresh control is composed of one chip, a 74LS603 and a few discrete components.

7.3 MODES OF OPERATION

7.3.1 DATI (Read)

During a DATI cycle, the memory reads a full word of data at a location determined by the bus master and transfers this data onto the bus.

To initiate a read cycle, the bus master places the address (BDAL00-BDAL21) of the memory location to be accessed on the bus. At the same time, it asserts BWTBTL to signal a read operation and also BBS7L if the memory location resides in the I/O page. A minimum of 75 ns later the bus master asserts BSYNCL to start the memory access cycle. It then asserts BDINL a minimum of 25 ns after the assertion of BSYNCL and waits for the memory to assert BRPLYL to signify valid data on BDAL00-BDAL15.

The address, BWTBTL, and BBS7L is received by the memory Q-BUS transceivers and is latched by the address latches on the leading edge of SYNCH. If the address is within the memory space of the board, the address selection logic asserts VALADD. The control logic starts the DRAM timing chain if the latched WTBT (LATWTBT) and VALADD signals are asserted. The timing chain generates the control signals; RASxN, CASON, and CASIN which are routed to the ram array to access one word of data. The selected word is clocked into the Q-BUS transceivers and gated onto the bus. The memory board answers BDINL with BRPLYL a maximum of 125 ns before the data is available on the bus. After the master has received the data, it removes BDINL from the bus and the memory board negates BRPLYL. The bus master is now free to start another memory cycle a minimum of 300 ns after the negation of BRPLYL.

7.3.2 DATO (Write)

In a DATO cycle, the memory accepts a full word of data and stores it at the location specified by the bus master. Valid address information is placed on the bus by the bus master at least 75 ns before it asserts BSYNCL.

The address, BWTBTL, and BBS7L is received by the memory Q-BUS transceivers and is latched by the address latches on the leading edge of SYNCH. If the address is within the memory space of the board, the address selection logic asserts VALADD. Since LATWTBT is not asserted, the control logic waits for DOUTH to be asserted before initiating the DRAM memory timing chain. The memory

boards answers BDOCTL with BRPLYL to indicate that it has accepted the data. The master then removes BDOCTL from the bus and the memory board negates BRPLYL allowing the master to initiate another memory cycle after a 300 ns delay.

7.3.3 DATOB (Write Byte)

The DATOB cycle is the same as the DATO cycle except that the master asserts BWTBTL at the same time as BDOCTL to indicate that only a byte (8 bits) of data is to be written to memory. The memory board uses BDALOO to determine which byte the master wants to write data to. Data in the other byte of the word is not affected.

7.3.4 DATIO (Read-Modify-Write)

During a DATIO cycle, data is read from memory, modified by the bus master and then written back to the same location.

The first half of a DATIO cycle is the same as a DATI cycle, however a minimum of 300 ns after BRPLYL is negated by the memory board the bus master starts the write portion of the cycle by asserting BDOCTL. The memory control logic treats the write portion as if it were a separate DATO cycle. The assertion of DOUTH starts the DRAM timing chain and BRPLYL is asserted by the memory board to signify that the data has been accepted. The removal of BDOCTL from the bus by the bus master causes the memory board to remove BRPLYL from the bus and the master is now free to start another memory cycle after a minimum delay of 300ns.

7.3.5 DATIOB (Read-Modify-Write Byte)

This cycle is identical to the DATIO cycle outlined above except that a byte of data is written during the write portion of the cycle. BWTBTL is asserted during the time that BDOCTL is asserted to signify a DATIOB cycle. If BDALOO is asserted, byte 1 (bits 8-15) will be written, otherwise byte 0 (bits 0-7) is written.

7.3.6 Block Mode

Throughput of a Q-BUS based computer can be significantly increased by taking advantage of the DR-216's block-mode capabilities. Presently, there are many DMA devices that use block-mode to transfer data to and from memory. The MICROVAX I also uses block-mode in most of its CPU memory accesses. In a block-mode transfer, the address is placed on the bus and then up to sixteen sequential data transfers are executed before another address must be placed on the bus. A counter on the DR-216 is incremented automatically after every transfer, insuring that the accesses are to the correct location.

7.3.6.1 DATBI (Block Mode Read)

To initiate a DATBI cycle, the bus master first places the addresses on the bus and asserts BWTBTL. A minimum of 75 ns later BSYNCL can be asserted by the bus master to start the cycle. For each transfer desired, the bus master asserts BDINL and waits for the memory to answer with BRPLYL. If another transfer is desired after the present one, the bus master also asserts BBS7L along with BDINL. The bus master waits 300ns after the trailing edge of the last BRPLYL before starting another cycle.

The memory board receives the address from the bus and decodes it to determine if it is being addressed. If the memory location being accessed resides on the board the DRAM timing chain is started because BWTBTL was asserted along with the addresses. In response to BDINL being asserted by the bus master, the board asserts BRPLYL signifying that the data is valid on the bus. Along with BRPLYL, the memory board asserts BREFL if it can continue with the block-mode transfer. If BBS7L is asserted along with BDINL, the board prepares to do another read cycle at the next word address. When the board can no longer continue with the block-mode transfer, it does not assert BREFL with reply and the bus master halts the DATBI cycle after the transfer in progress.

7.3.6.2 DATBO (Block Mode Write)

In a DATBO cycle, the bus master places the addresses on the bus at least 75 ns before the start of the cycle. The master then places the data on the bus (BDAL00-BDAL15) a minimum of 25 ns before asserting BDOUTL to signal the transfer. After asserting BDOUTL, it then waits for the assertion of BRPLYL from the memory before removing BDOUTL and then the data from the bus. If the bus master has more data to transfer, and BREFL was asserted by the memory along with BRPLYL, it will again place the data on the bus and assert BDOUTL. This process continues until the memory does not assert BREFL with BRPLYL, the bus master is finished writing data to memory, or the maximum number of transfers (16) has occurred.

7.3.7 Refresh

Refresh is necessary to prevent loss of data stored in the NMOS memory chips. NMOS DRAM devices store data on the parasitic gate capacitance of a field-effect-transistor. A "1" (high) is stored as the absence of charge and a "0" (low) is stored by charging the parasitic capacitor. The stored charge deteriorates due to leakage and must be renewed at least once every 4 ms. The memory chip is divided into 128 rows and each row is refreshed every 14.5 microseconds. This refresh operation is transparent to the bus master. If the bus and the refresh operation both try to

access the DRAMS, the bus will win and the refresh operation is delayed until the memory access is finished. If a refresh

operation is in progress and the bus master tries to access the memory, the cycle will be delayed until the refresh operation is completed. In this case the memory access cycle will be delayed a maximum of 400 ns.

All refresh operations are controlled by a single chip. This refresh controller signals when a refresh operation is needed. If the memory is not being accessed, the control logic asserts REFREQ, signaling the refresh controller to proceed with the refresh operation.

SECTION 8 - PART NUMBERS/DOCUMENTATION

8.1 PART NUMBERS

The following Dataram part numbers have been assigned to the DR-216 Memory System:

| Part Number | Description |
|-------------|---------------------------|
| 61548 | DR-216, 128K x 18 (256KB) |
| 61545 | DR-216, 256K x 18 (512KB) |
| 61549 | DR-216, 512K x 18 (1 MB) |
| 61546 | DR-216, 1024K x 18 (2 MB) |

8.2 DOCUMENTATION

The following documentation numbers have been assigned to the DR-216 Memory System:

| Part Number | Description |
|-------------|---------------------------|
| 03445 | Schematic Drawings |
| 61545 | Assembly Drawing, DR-216 |
| 61545 | Bill of Materials, DR-216 |

| REV. | REVISIONS | | | |
|------|-----------|----------|------------------------|--------------|
| | SYM. | SHEET | DESCRIPTION | APPROV. DATE |
| G2 | X0 | | PRELIMINARY RELEASE | PTD 8/2/84 |
| | A0 | | RELEASED TO PRODUCTION | HBC 1-4-84 |
| | A1 | | ECN 3872 | |
| | B0 | | ECN 3863 | |
| | B1 | | ECN 3896 | |
| | B2 | | ECN 3897 | |
| | B3 | | ECN 3899 | |
| | B4 | | ECN 3900 | |
| | B5 | | ECN 3902 | |
| | B6 | | ECN 3919 | |
| | B7 | | ECN 3920 | |
| | C0 | | ECN 3931 | |
| | C1 | | ECN 3946 | JEJ 4/17/85 |
| | C2 | | ECN 3960 | |
| | C3 | | ECN 3961 | |
| | D0 | | ECN 3963 | |
| | D1 | | ECN 3968 | |
| | D2 | | ECN 3976 | |
| | D3 | | ECN 3993 | |
| | D4 | | ECN 3997 | JEJ 6/25/85 |
| E0 | | ECN 3998 | | |
| E1 | | ECN 4006 | JEJ 7/15/85 | |
| F0 | | ECN4029 | JEJ 8/30/85 | |
| F1 | | ECN 4063 | | |
| F2 | | ECN 4064 | | |
| G0 | | ECN 4068 | | |
| G1 | | ECN 4084 | | |
| G2 | | ECN 4136 | JLW 1/29/86 | |

8.2.84

| | | | | | |
|------------------|-----------------|---|--------------------------------------|-------------------|------------|
| DRAWN JEJ | DATE 7-11-84 | TITLE BILL OF MATERIALS DR-216 256K X 18 | DATARAM CORPORATION | DWG. NO. 61545 | REV. G2 |
| CHECKED C. H. | DATE 8.2.84 | | | SHEET 1 OF 4 | |
| ENGR. BC | DATE 4.29.85 | | | | |
| APPROVED EK | DATE 2.1.85 | | | | |

TITLE: B/M DR-216 256K X 18

| ITEM NO | QTY | PART NUMBER | DESCRIPTION | REFERENCE NOTES |
|---------|-----|-------------|--|---|
| 1 | 2 | 18401 | LED RED PC MT W/INTL RES | LED 1, 2 |
| 2 | 1 | 18408 | LED GREEN PC MT W/INTL RES | LED 3 |
| 3 | 72 | 12331 | CAP CER AXL .1UF -20/+80% | A0-A15, AP0, AP1, B0-B15, BP0, BP1, |
| 4 | 1 | 12343 | CAP CER .001UF +10% | C3 C0-C15, CP0, CP1, D0-D15, DP0, DP1 |
| 5 | 2 | 12602 | CAP SIL MICA 330PF +5% | C4, 20 |
| 6 | 19 | 18113 | DIODE SILICON SWITCHING | CR1, 3-20 |
| 7 | 10 | 12128 | CAP TANT 15UF 16V | C6, 7, 8, 10, 12, 14, 15, 17, 21, 23 |
| 8 | 6 | 12316 | CAP CER 0.1UF +20% | C9, 13, 16, 18, 19, 24 |
| 9 | 1 | 12609 | CAP SIL MICA 240PF +5% | C5 |
| 10 | 1 | 12611 | CAP SIL MICA 270PF +5% | C2 |
| 11 | 1 | 10113 | RES CC 1/4W 1K OHMS 5% | R5 |
| 12 | 1 | 10602 | RES CC 1/4W 120 OHMS 5% | R9 |
| 13 | 1 | 12326 | CAP CER 0.1UF +20% | C22 |
| 14 | | | NOT USED | R10 |
| 15 | 1 | | RES SAT | R1 |
| 16 | 1 | 10119 | RES CC 1/4W 3.3K OHMS 5% | R2 |
| 17 | 1 | 10118 | RES CC 1/4W 2.2K OHMS 5% | R3 |
| 18 | 1 | 14511 | INDUCTOR 22 UH (DD) | L1 |
| 19 | 1 | 16345 | IC 8641 QUAD UNIBUS XCVR | Z1 |
| 20 | 5 | 16380 | IC 2908 INTFC XCVR | Z8, 9, 10, 11, 13 |
| 21 | 72 | 16940 | IC DYNAMIC RAM 64K X 1 | A0-15, AP0, AP1, B0-B15, BP0, BP1, C0-15, CP0, CP1, D0-D15, DP0, DP1 |
| 22 | 72 | 23084 | SOCKET IC 16 PIN OPEN FRAME LOW PROFILE ST | A0-15, AP0, AP1, B0-B15, BP0, BP1, C0-15, CP0, CP1, D0-15, DP0, DP1 |
| 23 | 1 | 16291 | IC 74LS603 64K RAM REFRESH CONTROLLER | Z2 |
| 24 | 1 | 16271 | IC 74LS340 OCT INV BFR 3 STAT ST | Z4 |

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TITLE: B/M DR-216 256K X 18

| ITEM NO | QTY | PART NUMBER | DESCRIPTION | REFERENCE NOTES |
|---------|-----|-------------|------------------------------------|------------------|
| 25 | 1 | 16558 | IC 74S135 QUAD EXCL OR/NOR | Z24 |
| 26 | 1 | 16573 | IC 74AS646 OCT XCVR/REG | Z18 |
| 27 | 2 | 16574 | IC 74S730/2965 OCT 3 STAT RAM DRVR | Z3, 31 |
| 28 | 1 | 16511 | IC 74S260 DUAL 5I/P NOR | Z20 |
| 29 | 1 | 16514 | IC 74S38 QUAD 2I/P NAND | Z32 |
| 30 | 2 | 16153 | IC 74F373 OCTAL LATCH TS | Z7, 14 |
| 31 | 1 | 16140 | IC 74F191 U/D BIN CTR | Z12 |
| 32 | 1 | 16144 | IC 74F244 OCTAL BUS/LINE DR | Z15 |
| 33 | 1 | 16154 | IC 74F374 OCTAL D F/F TS | Z17 |
| 34 | 1 | 16134 | IC 74F174 HEX D F/F W/COM RST | Z19 |
| 35 | 2 | 16160 | IC 74F14 HEX ST INV | Z21, 29 |
| 36 | 1 | 16119 | IC 74F74 DUAL D TYPE F/F | Z34 |
| 37 | 1 | 16117 | IC 74F32 QUAD 2I/P OR GATE | Z27 |
| 38 | 2 | 16151 | IC 74F283 4 BIT FULL ADDER | Z26, 30 |
| 39 | 2 | 16150 | IC 74F280 9 BIT PARITY GEN CHECK | Z23, 28 |
| 40 | 2 | 16148 | IC 74F257 QUAD 2I/P MUX TS | Z5, 6 |
| 41 | 2 | 17702 | IC 16H8A PAL UNPROG | FOR ITEMS 45, 48 |
| 42 | 2 | 16957 | IC 82S153 FPLA 3 STAT UNPROG | FOR ITEMS 44, 47 |
| 43 | | | NOT USED | |
| 44 | REF | 08738 C | PROG CSR CONTROL | Z16 |
| 45 | REF | 08739 C | PROG CYCLE CONTROL | Z25 |
| 46 | 1 | 16116 | IC 74F20 DUAL 4I/P NAND | Z27A |
| 47 | REF | 08741 A | PROG CSR DECODING | Z22 |
| 48 | REF | 08742 B | PROG RAS/CYCLE DECODING | Z33 |
| 49 | 1 | 22917 | SWITCH DIP 8 POS LOW PROF | SW1 |
| 50 | 33 | 22623 | CONT MALE | E1-9, 12 |

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TITLE: B/M DR-216 256K X 18

| ITEM NO | QTY | PART NUMBER | DESCRIPTION | REFERENCE NOTES |
|---------|-----|-------------|-------------------------------|-----------------|
| 51 | 1 | 14108 | DELAY LINE DIGITAL 150NS | DL1 |
| 52 | 1 | 27434 | CARD HANDLE LOW PROFILE | |
| 53 | 1 | 40903 | P.C.B. DR-216 | |
| 54 | 1 | 11105 | RES MDL 10K OHMS 6 PIN | RM1 |
| 55 | 1 | 11993 | RES MDL 10K OHMS 2% | RM2 |
| 56 | 1 | 11108 | RES MDL 470 OHMS 6 PIN | RM4 |
| 57 | 1 | 10111 | RES CC 1/4W 470 OHMS 5% | R8 |
| 58 | 1 | 10152 | RES CC 1/4W 750 OHMS 5% | R6 |
| 59 | A/R | 24305 | WIRE TINNED COPPER BUS 30 AWG | |
| 60 | | | NOT USED | R11 |
| 61 | 1 | 10105 | RES CC 1/4W 100 OHMS 5% | R4 |
| 62 | 1 | 10111 | RES CC 1/4W 470 OHMS 5% | R12 |
| 63 | 1 | 10121 | RES CC 1/4W 4.7K OHMS 5% | R13 |
| 64 | 1 | 18214 | DIODE ZENER 1N703A 3.3V | CR2 |
| 65 | 1 | 20103 | XSTR PNP SWG 2N4403 | Q1 |
| 66 | A/R | 24504 | WIRE SOL GRN 30 AWG WW | |
| 67 | 1 | 11956 | RES MDL 10K OHMS | RM3 |
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| | | | | |
| * | REF | 06510 | INSTALLATION GUIDE | |
| * | REF | 02263 | PRODUCT SPECIFICATION DR-216 | |
| * | REF | 05187 | TEST SPECIFICATION DR-216 | |
| * | REF | 03445 | SCHEMATIC DR-216 | |

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