SEMICONDUCTOR MEMORY SYSTEM

DR-215

DATARAM
CORPORATION

SEMICONDUCTOR MEMORY SYSTEM

DR-215

06124A

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1.0 GENERAL

The Dataram Corporation Model DR-215 Semiconductor Memory System is designed to operate in Digital Equipment Corporation's LSI-11* computers. The DR-215 may be operated with the DEC* Model MMV11-A, MSV11-ED, MSV11-P, and MSV11-L series memories or in place of the MSV11-L series memories.

The DR-215 is completely compatible with all LSI-11 computers and all standard DEC LSI-11 peripheral devices. The DR-215 will operate in computers with 16, 18, or 22 address lines.

The system consists of a single height dual width card which contains the Q-BUS* interface, timing and control logic, refresh circuitry, MOS storage array, parity generation and checking logic, and a control and status register (CSR).

*Registered trademark of Digital Equipment Corporation

2.0 ELECTRICAL SPECIFICATIONS

2.1 Capacity

The maximum storage capacity of the DR-215 memory is 131,072 (128K) words by 16/18 bits available on a single dual board. The DR-215 is also available in a 64K depopulated version.

Two parity storage bits and parity generation and checking circuitry are included on the 18 bit models.

2.2 Cycle Time

The cycle time of the memory is 450 nanoseconds for a Read cycle and 500 nanoseconds for a Write cycle. BSYNC L (Bus Sync) initiates all memory cycles. The time delay between repetitive BSYNC L pulses is defined as cycle time. Cycle time is partially controlled by the memory being accessed. The positive transition of BRPLY L from the memory allows the processor, after a 300 nanosecond delay, to start the next memory cycle. Figures 2.1-2.3 define the LSI-11 Bus timing when the DR-215 is operated with the LSI-11 computer.

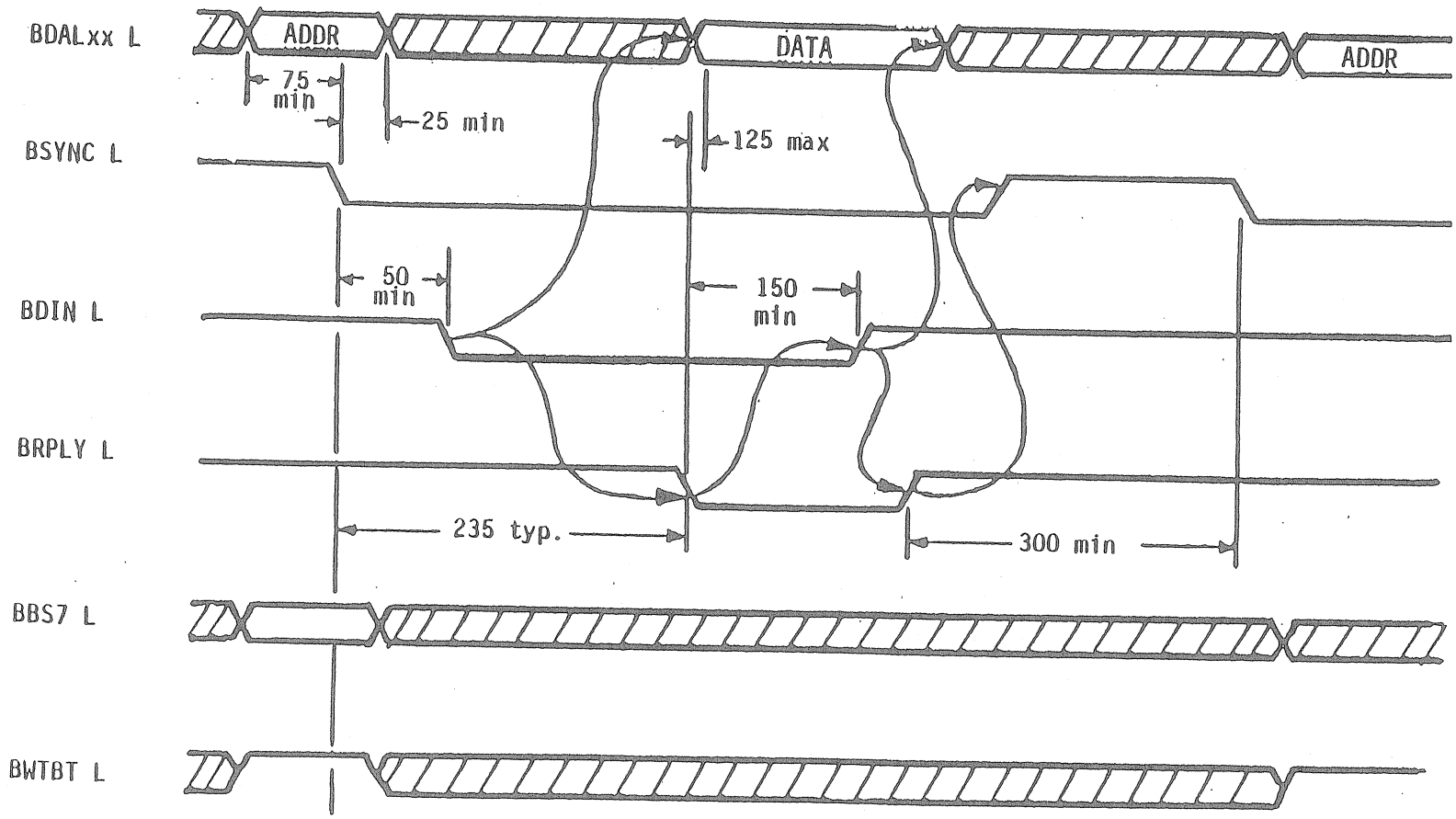
2.3 Access and Reply Times

The access time of the DR-215 memory is 325 nanoseconds typically. The access time is measured at the connector of the memory module. The time delay between the +1.5 volt levels of the BSYNC L pulse and data on the BDALX L lines during Memory Read cycles is defined as "access time".

The Reply time of the DR-215 is 235 nanoseconds (typ.) for a Read cycle assuming a maximum delay of 150 nanoseconds from the assertion of BSYNC L to the assertion of BDIN L. Write Reply time is 150 nanoseconds (typ.) assuming 50 nanoseconds delay from BSYNC L to the assertion of BDOUT L.

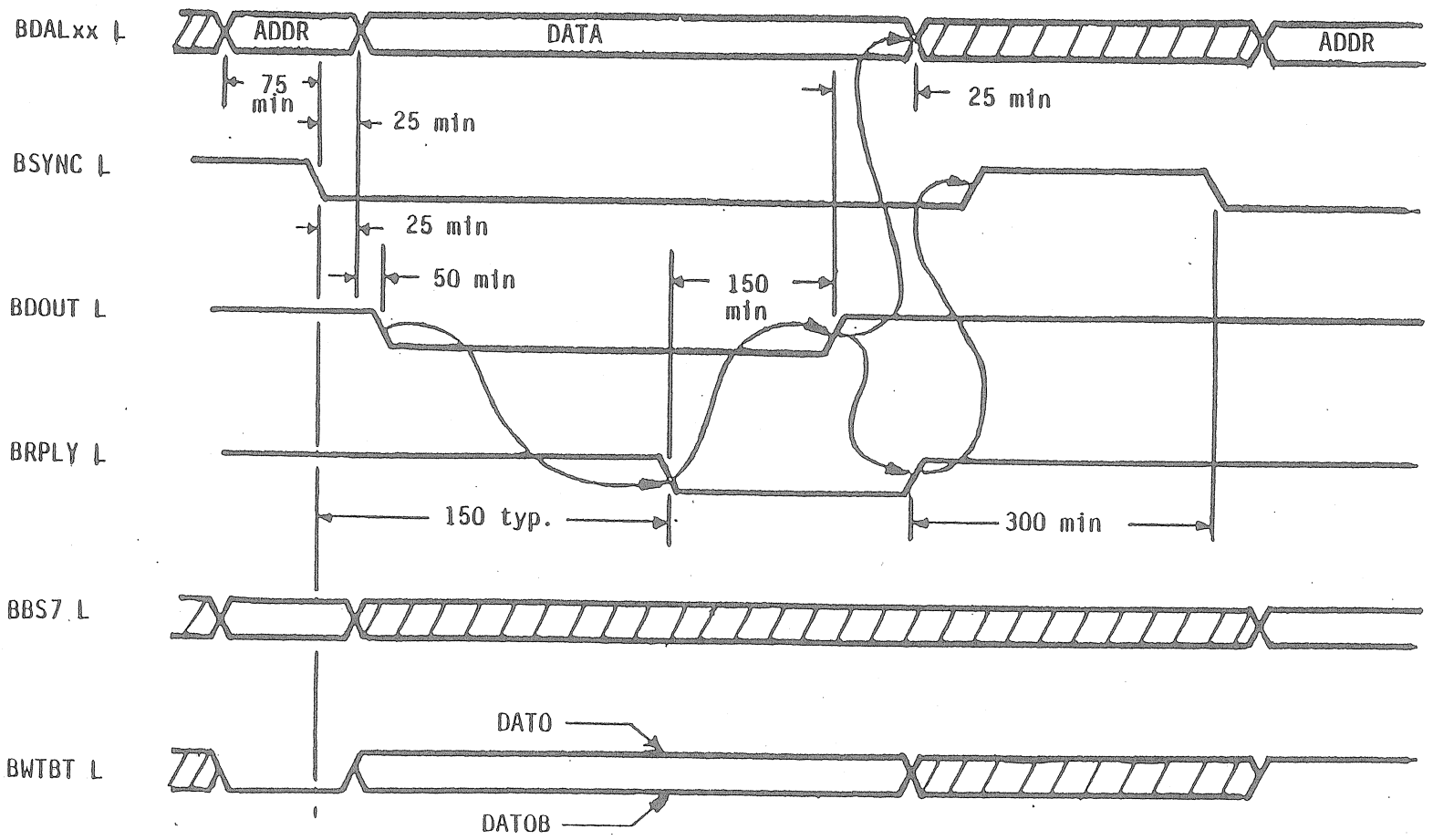
2.4 CSR Access and Reply Times

Access time to the CSR is 265 nanoseconds typically and 330 nanoseconds maximum. The CSR Read reply time is 230 nanoseconds maximum and write reply time is 130 nanoseconds maximum.



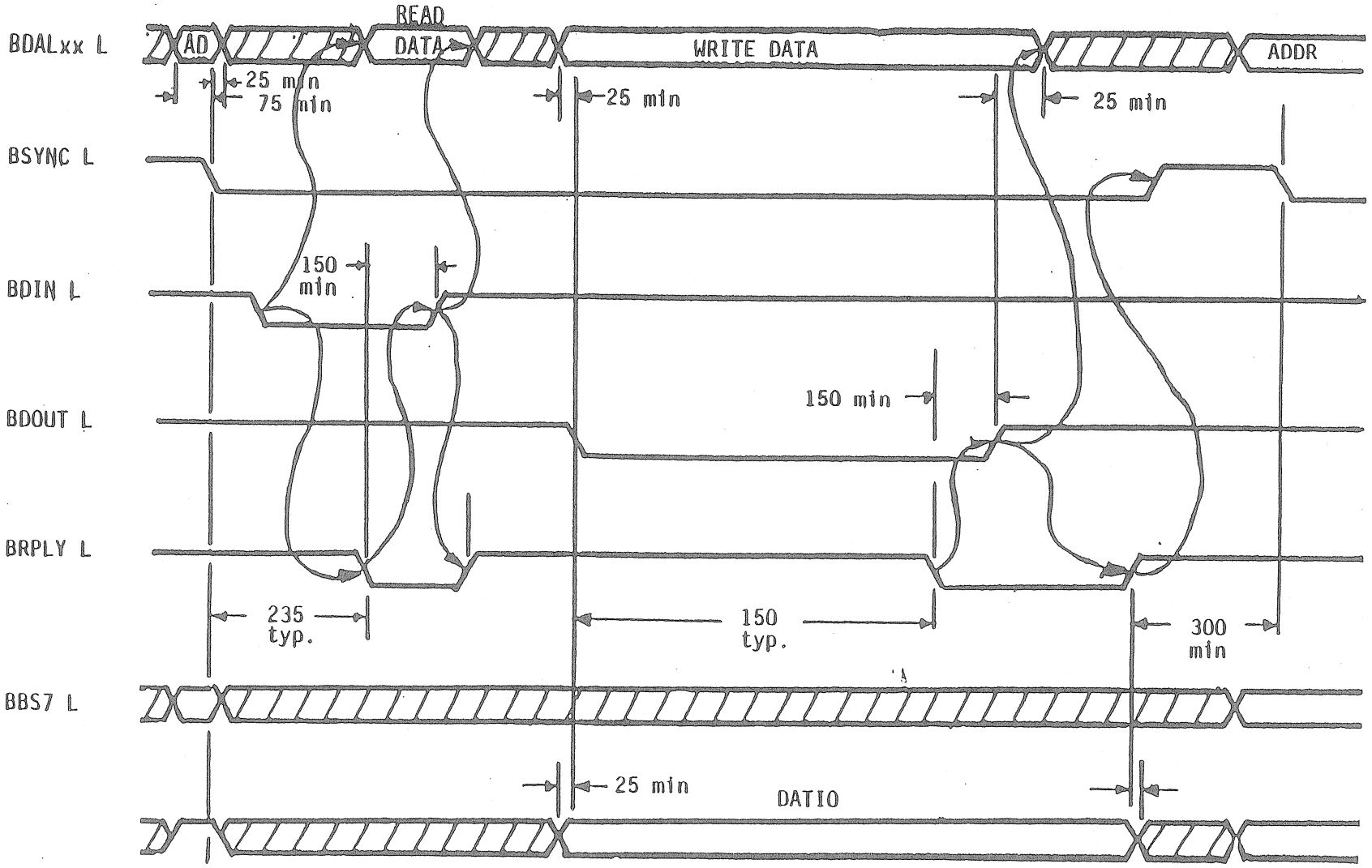
DATI (READ)

FIGURE 2.1



DATO (WRITE WORD) OR DATOB (WRITE BYTE)

FIGURE 2.2



DATIO (READ MODIFY WRITE WORD)

DATIOB (READ MODIFY WRITE BYTE)

FIGURE 2.3

2.5 Addressing

The DR-215 memory will accept 22 address lines. The address lines to the memory are single rail; the addressing mode may be random. The address lines are time multiplexed with the data lines and are identified as BDAL0 L through BDAL15 L. The extended address lines are identified as BDAL16-21 L. BDAL0 L is used for byte selection. BDAL1 L through BDAL17 L are decoded for 1 of 131,072 address locations within any memory module. BDAL13 L through BDAL21 L are used to set the initial address for a memory module. See Table 2.1 for offset information.

2.6 Operating Modes

The DR-215 is capable of performing the following operations:

Command	Operation
DATI	Read
DATO	Write
DATOB	Write Byte
DATIO	Read-Modify-Write
DATIOB	Read-Modify-Write Byte

These operations are controlled by bus signals BSYNC L, BWTBT, BDAL0 L, BDIN L, and BDOUT L. See timing diagrams for further definition.

An additional mode, REFRESH, is necessary to prevent loss of data stored in the NMOS storage chips. NMOS Random Access Memory (RAM) devices store data on the gate capacitance of a field-effect transistor. A "1" is stored as the presence of charge and a "0" is stored as the absence of charge. The stored charge tends to deteriorate and must be renewed at least every two milliseconds. Therefore, one 1/128th of the memory (1/128th of each memory chip) is recharged (refreshed) every 15 microseconds.

Refresh circuitry is contained on the memory module. The Refresh cycle is transparent to the CPU. If a Refresh cycle is in progress and a Read or Write cycle is requested, a maximum of 450 nanoseconds will be added to the cycle.

STARTING ADDRESS	SWITCH SW1 1	2	3	4	5
0K	OFF	OFF	OFF	OFF	OFF
4K	ON	OFF	OFF	OFF	OFF
8K	OFF	ON	OFF	OFF	OFF
12K	ON	ON	OFF	OFF	OFF
16K	OFF	OFF	ON	OFF	OFF
20K	ON	OFF	ON	OFF	OFF
24K	OFF	ON	ON	OFF	OFF
28K	ON	ON	ON	OFF	OFF
32K	OFF	OFF	OFF	ON	OFF
36K	ON	OFF	OFF	ON	OFF
40K	OFF	ON	OFF	ON	OFF
44K	ON	ON	OFF	ON	OFF
48K	OFF	OFF	ON	ON	OFF
52K	ON	OFF	ON	ON	OFF
56K	OFF	ON	ON	ON	OFF
60K	ON	ON	ON	ON	OFF
64K	OFF	OFF	OFF	OFF	ON
68K	ON	OFF	OFF	OFF	ON
72K	OFF	ON	OFF	OFF	ON
76K	ON	ON	OFF	OFF	ON
80K	OFF	OFF	ON	OFF	ON
84K	ON	OFF	ON	OFF	ON
88K	OFF	ON	ON	OFF	ON
92K	ON	ON	ON	OFF	ON
96K	OFF	OFF	OFF	ON	ON
100K	ON	OFF	OFF	ON	ON
104K	OFF	ON	OFF	ON	ON
108K	ON	ON	OFF	ON	ON
112K	OFF	OFF	ON	ON	ON
116K	ON	OFF	ON	ON	ON
120K	OFF	ON	ON	ON	ON
124K	ON	ON	ON	ON	ON

For all other settings use equal increments of 128K plus the appropriate 4K increment from the above table.

	6	7	8	9
0-128K	OFF	OFF	OFF	OFF
128-256K	ON	OFF	OFF	OFF
256-384K	OFF	ON	OFF	OFF
384-512K	ON	ON	OFF	OFF
512-640K	OFF	OFF	ON	OFF
640-768K	ON	OFF	ON	OFF
768-896K	OFF	ON	ON	OFF
896-1024K	ON	ON	ON	OFF
1024-1152K	OFF	OFF	OFF	ON
1152-1280K	ON	OFF	OFF	ON
1280-1408K	OFF	ON	OFF	ON
1408-1536K	ON	ON	OFF	ON
1536-1664K	OFF	OFF	ON	ON
1664-1792K	ON	OFF	ON	ON
1792-1920K	OFF	ON	ON	ON
1920-2048K	ON	ON	ON	ON

ON = Closed
OFF = Open

TABLE 2.1

2.7 Control and Status Register

The control and status register may be read or written via the Q-BUS. The address of the CSR is switch selectable within the range of 172100-172136 for 16 bit address, 772100-772136 for 18 bit address, and 17772100-17772136 for 22 bit address systems. Switch SW2 positions 1-4 determine the CSR address (See Table 2.2).

The CSR allows program control of parity functions and contains diagnostic information if a parity error has occurred. The CSR bit assignments are shown below:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR ERR	ERR RTVL	NOT USED		A17 OR 0	A16 OR 0	A15 OR 0	A14 OR A21	A13 OR A20	A12 OR A19	A11 OR A18	NOT USED		WRT WRG PAR	NOT USED	PAR ENA

Parity Enable - Bit 0

This bit when set enables parity error detection. The DR-215 asserts BDAL17L during data time of a DATI or DATIO cycle and allows the CPU to trap to 114g. This bit may be read or written via the Q-BUS and is cleared by BINIT.

Write-Wrong Parity - Bit 2

This bit when set forces incorrect parity to be generated by the memory. This bit may be read or written via the Q-BUS and is cleared by BINIT.

Error Address - Bits 5-11

These bits contain the most significant address bits of the memory location where a parity error has occurred. The state of CSR bit 14 determines which addresses are read. Bits 5-11 may be read or written via the Q-BUS but are not cleared by BINIT.

Error Retrieval - Bit 14

This bit determines which error addresses are read onto the Q-BUS. When bit 14 is reset A11-A17 are read. When bit 14 is set A18-A21 are read. Bit 14 should be locked reset for operation in systems with 16 or 18 address lines (remove E11-E10 and install E11 to E12). This bit may be read or written from the Q-BUS and is cleared by BINIT.

SWITCH SW2

16 Bit Address	18 Bit Address	22 Bit Address	4	3	2	1
172100	772100	17772100	OFF	OFF	OFF	OFF
172102	772102	17772102	OFF	OFF	OFF	ON
172104	772104	17772104	OFF	OFF	ON	OFF
172106	772106	17772106	OFF	OFF	ON	ON
172110	772110	17772110	OFF	ON	OFF	OFF
172112	772112	17772112	OFF	ON	OFF	ON
172114	772114	17772114	OFF	ON	ON	OFF
172116	772116	17772116	OFF	ON	ON	ON
172120	772120	17772120	ON	OFF	OFF	OFF
172122	772122	17772122	ON	OFF	OFF	ON
172124	772124	17772124	ON	OFF	ON	OFF
172126	772126	17772126	ON	OFF	ON	ON
172130	772130	17772130	ON	ON	OFF	OFF
172132	772132	17772132	ON	ON	OFF	ON
172134	772134	17772134	ON	ON	ON	OFF
172136	772136	17772136	ON	ON	ON	ON

ON = Closed

OFF = Open

NOTE: E17 to E18 disables CSR selection.
E11 to E12 must be installed for 16 or 18 bit address operation.

CSR ADDRESS SELECT

TABLE 2.2

Parity Error - Bit 15

This bit is set when a parity error occurs. It does not cause a parity trap in the processor. Bit 15 may be read or written via the Q-BUS and is cleared by BINIT.

Unused Bits - Bits 1, 3, 4, 12 and 13

These bits are not used and are always read as a logical zero.

2.8 Power Requirements

The DR-215 Memory System requires the same DC voltages as the MSV11-L DEC memory. The necessary logic to operate with battery backup is provided on the memory module (+5B-AV1). The voltage-current requirements for each 128K x 18 memory assembly are as follows:

	Operating Amps	Standby Amps	Voltage Margin
+5V	1.85	1.45	±5%
+5V Battery	1.5	1.1	±5%
+5V Total (+5V & +5V Battery)	3.35	2.55	±5%

2.9 Bus Signals

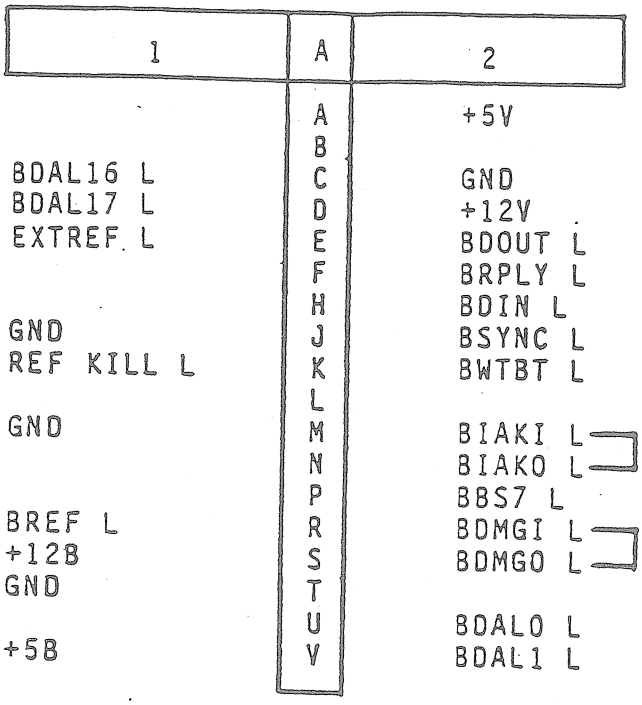
The memory interfaces with the processor, other memories and peripherals via connectors A and B. The bus signals and their appropriate pin numbers are shown in Table 2.3.

BDAL0 L through BDAL21 L — Data/Address Lines

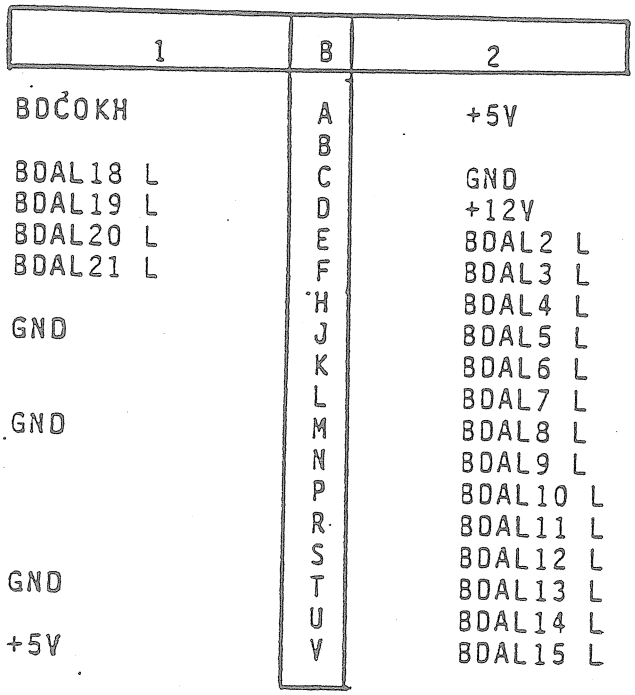
These 22 lines are used to communicate address and data information. The device requesting service from the memory first places address on these lines, then the same device either receives input data from or outputs data to the memory over the same bus lines. Extended addresses BDAL16-21 L are used to address up to 2M words of memory. BDAL16 L is also used for parity error signal propagation.

BSYNC L — Synchronize

Asserted by the bus master and used by the memory to accept address information on the BDAL bus.



1	A	2
	A	+5V
	B	
BDAL16 L	C	GND
BDAL17 L	D	+12V
EXTREF L	E	BDOUT L
	F	BRPLY L
	H	BDIN L
GND	J	BSYNC L
REF KILL L	K	BWTBT L
	L	
GND	M	BIAKI L
	N	BIAKO L
	P	BBS7 L
BREF L	R	BDMGI L
+12B	S	BDMGO L
GND	T	
	U	BDAL0 L
+5B	V	BDAL1 L



1	B	2
BDCOKH	A	+5V
	B	
BDAL18 L	C	GND
BDAL19 L	D	+12V
BDAL20 L	E	BDAL2 L
BDAL21 L	F	BDAL3 L
	H	BDAL4 L
GND	J	BDAL5 L
	K	BDAL6 L
	L	BDAL7 L
GND	M	BDAL8 L
	N	BDAL9 L
	P	BDAL10 L
	R	BDAL11 L
	S	BDAL12 L
GND	T	BDAL13 L
	U	BDAL14 L
+5V	V	BDAL15 L

TABLE 2.3

BWTBT — Write/Byte

Asserted by the bus master. When asserted prior to BSYNC L, it indicates to the memory that a DATO (Write) operation is to be performed. If BWTBT L is asserted during BDOUT L in a DATO operation, then the operation becomes DATOB (Write Byte).

BDCOK H — DC Power OK

Asserted by the power supply or the bus master. It inhibits all memory operation except Refresh cycles.

BDIN L — Data Input

Asserted by the bus master when it is ready to accept data from the memory. The memory must also respond with BRPLY L to complete the bus operations.

BDOUT L — Data Out

Asserted by the bus master to indicate that data to be stored in memory is valid on the BDAL bus lines. The memory must respond with BRPLY L to complete the bus operations.

BRPLY L — Reply

Asserted by the memory to indicate to the bus master that data is available on the BDAL bus or that the memory has accepted data from the bus.

BBS7 L — Bank 7 Select

Asserted by the bus master when the selected address is within the I/O map and is used by the memory to select the CSR and to disable normal memory operation.

2.10 Indicator Lamps

The DR-215 contains three indicator lamps which define the following conditions:

(See Figure 3.1 for physical location.)

LED1 (Red) - This LED when lit provides visual indication that a parity error has occurred on the memory assembly. This lamp is reset (turned off) with BINIT L or if a zero is written into bit 15 of the status register.

LED2 (Red) - This LED when lit provides a visual indication that a memory cycle, read or write, is in progress.

LED3 (Green) - This LED when lit indicates that +5 volts is available to the battery backup circuits of the memory. This lamp is normally lit and will remain on if +5 volts is removed from the system and the memory continues to receive +5 volts from the +5VB terminal (AV1).

2.11 Options

2.11.1 I/O Space

The I/O space size is strappable for 4K, 2K, 1K and .5K words according to the following table:

I/O Space	Jumpers		
	E1 to E2	E3 to E4	E5 to E6
4K (Normal)	OUT	OUT	OUT
2K	OUT	OUT	IN
1K	OUT	IN	IN
.5K	IN	IN	IN

2.11.2 Battery Backup

The DR-215 provides the necessary logic to operate with battery backup. The battery backup power requirements are shown in Section 2.8.

The battery backup option is jumper selectable. It is located on the front of the memory card near the connector fingers.

Jumper	Function
E8 to E9	No Battery Backup
E7 to E8	Battery Backup

2.11.3 External Refresh Option

The DR-215 has the capability of using an external refresh request signal generated by the user on Bus Pin AE1.

There are two options available:

(1) The user supplied request controls refresh timing during normal operation and during battery backup.

Jumper E36 to E37 and E38 to E39

(2) The user supplied request controls refresh during normal memory operation and internal requests control refresh during battery backup operation.

Jumper E33 to E36 and E33 to E34

NOTE: Remove jumpers E40 to E39 and E35 to E36 prior to the incorporation of either external refresh option.

The external refresh request must be a low true signal with a minimum pulse width of 80 nanoseconds, a maximum of 300 nanoseconds, and a maximum repetitive cycle of 14 microseconds.

2.11.4 External Parity Control

The DR-215 may be operated in systems where an external parity controller controls parity functions on all memories within the system. The DR-215 should be configured as follows in such systems:

Remove Jumpers:	E13 to E15
	E25 to E26
	E28 to E29
Install Jumpers:	E17 to E18
	E26 to E20
	E13 to E12

2.11.5 Parity Disable

Remove E23 to E24
Install E17 to E23

2.11.6 Upper or Lower Bank Removal

When a hard error occurs within one of the two banks that bank may be disabled. When the lower bank fails, the upper bank may be made to respond as the lower bank. Bank removal reduces available memory, but allows operation until repairs can be made.

Upper Bank Fails:	Install E16 to E15
Lower Bank Fails:	Remove E21-E22
	Install E16-E22
	E16-E15

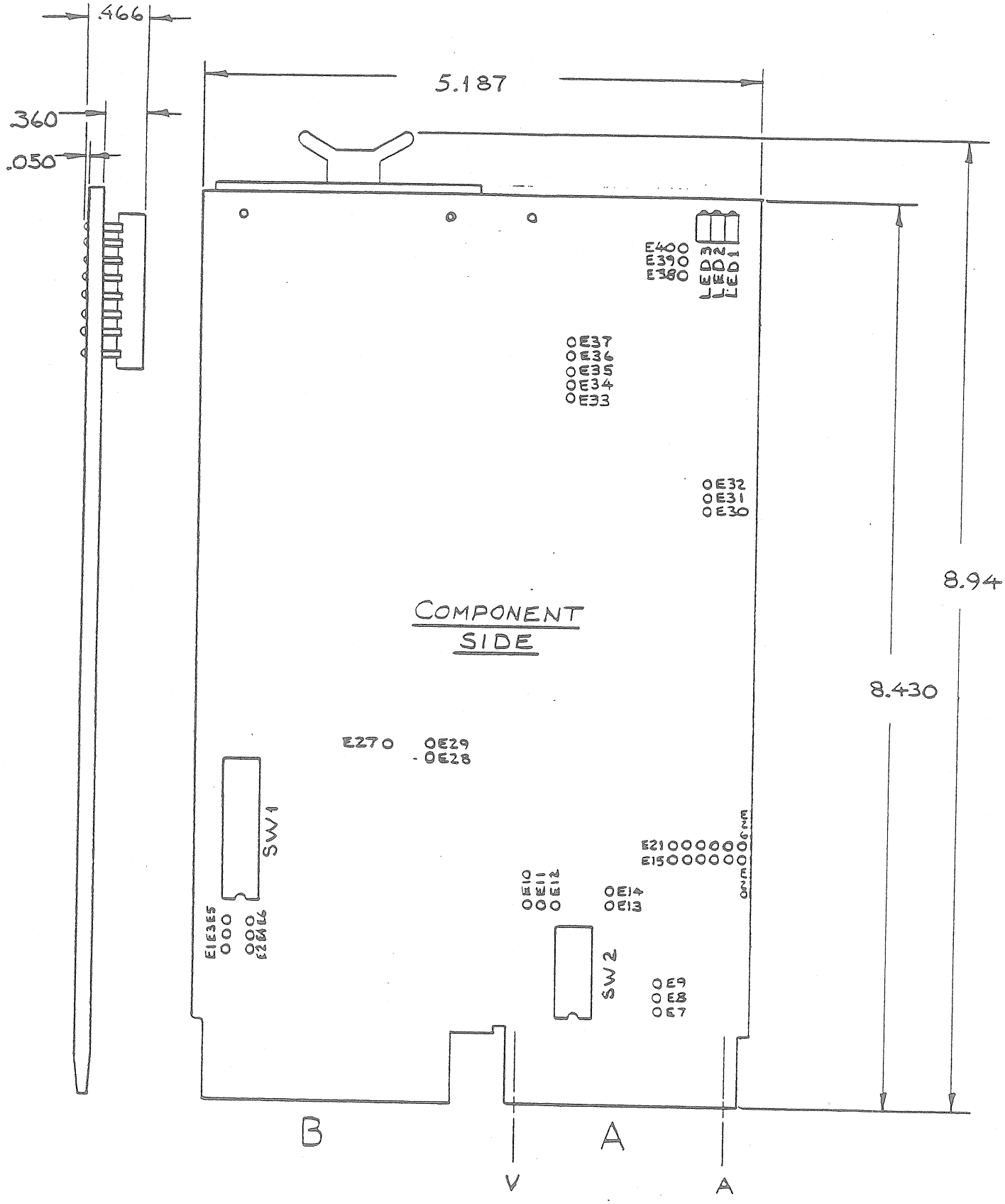
3.0 MECHANICAL SPECIFICATIONS

3.1 Dimensions

The DR-215 is designed to fit into the LSI-11 chassis or equivalent utilizing the space of a standard dual printed circuit board. The dimensions of the memory assembly are .466" (11.84mm) x 8.92" (226.57mm) x 5.186" (131.72mm). See Figure 3.1.

3.2 Weight

.5 pounds (.23 kg)



DR-215

FIGURE 3.1

4.0 ENVIRONMENTAL SPECIFICATIONS

4.1 Temperature

Operating: $0^{o}C$ to $+55^{o}C$

Storage: $-40^{o}C$ to $+80^{o}C$

4.2 Humidity

Operating: 0 to 90% (without condensation)

Non-Operating: 0 to 95% (without condensation)

4.3 Altitude

Operating: 1000 ft. below to 10,000 ft. above mean sea level

Non-Operating: 1000 ft. below to 20,000 ft. above mean sea level

4.4 Vibration

Will withstand normal stresses encountered in transportation.

5.0 INSTALLATION

5.1 Switch Settings

When installing the DR-215, the starting address shall be set according to Table 2.1 and the CSR address shall be set according to Table 2.2.

5.2 Jumper Options

Table 5.1 summarizes all jumper functions.

JUMPER FUNCTION SUMMARY

FUNCTION	JUMPERS IN	JUMPERS OUT
CSR Selection		
Disable CSR	17-18, 20-26	25-26
Enable CSR	25-26	17-18, 20-26
Parity Error Reporting		
Non-CSR	12-13	13-14
With CSR	13-14	12-13
Write Wrong Parity Enable		
Non-CSR	27-28	29-28
With CSR	29-28	27-28
Parity		
Disable	23-17	23-24
Enable	23-24	17-23
Memory Size		
128K	E21-E22	E15-E16
64K	E15-E16, E21-E22	
Bank Removal		
Upper Bank Fails	E16-E15	
Lower Bank Fails	E16-E22, E16-E15	E21-E22
Addressing		
16 or 18 Bit Address	E11-E12	E10-E11
22 Bit Address	E10-E11	E11-E12
Battery Backup	E7-E8	E8-E9
No Battery Backup	E8-E9	E7-E8
Refresh		
Internal	E35-E36, E40-E39	E36-E37, E38-E39 E33-E34, E33-E36
External	E36-E37, E38-E39	E35-E36, E40-E39 E33-E34, E33-E36
Internal Normal, External Backup	E33-E36, E33-E34	E36-E37, E38-E39 E35-E36, E40-E39
No Refresh (Test Only)	E36-E35, E39-E38	E40-E39, E36-E37 E33-E36, E33-E34

TABLE 5.1

I/O Space Size	IN	OUT
4KW		E1-E2, E3-E4, E5-E6
2KW	E5-E6	E1-E2, E3-E4
1KW	E3-E4, E5-E6	E1-E2
.5KW	E1-E2, E3-E4, E5-E6	

TABLE 5.1 (Continued)

6.0 THEORY OF OPERATION

In the following sections, all signal levels from 0.0 VDC to 0.8 VDC will be referred to as low or a logical "0" and all signal levels between +2.4 VDC and +5.2 VDC will be referred to as high or a logical "1".

6.1 Functional Definition of Terms

6.1.1 External

In this section, an "L" following the term indicates a low active state and an "H" a high active state.

BDAL0L-BDAL15L....time multiplexed address/bidirectional data lines, sufficient to select 1 of 32,768 locations by 16 bits.

BDAL0L....during address time in a write/byte mode, BDAL0L is used for data byte selection. (Byte 0 = H and Byte 1 = L)

BDAL16L thru BDAL21L....extended addresses used for expansion up to 2M words. During data time, BDAL16L is used for propagation of memory parity error signal and BDAL17L is used to indicate when parity is enabled.

BSYNCL....a synchronizing control signal from bus master to the memory. BSYNCL indicates address information is stable on the bus and starts a memory cycle.

BWTBTL....generated by the bus master, it informs the memory of the mode of operation for a given cycle.

BDINL....a request by the bus master for read data to be placed on the BDAL bus lines. The memory must reply with BRPLYL for completion of the memory cycle and termination of the command signal.

BDOUTL....a request by the bus master for the memory to accept write data from the bus and store the data. The memory must reply with BRPLYL to complete the memory cycle and terminate the command.

BRPLYL....a required response from the memory indicating read data is valid or write data has been accepted from the bus.

BDCOKH....a Power OK signal indicating DC power is at a sufficient level to sustain memory operation.

BREFL....in its active low state, BREFL indicates a processor controlled refresh cycle is in progress. The DR-215 will be shut down during this cycle.

BBS7L....a signal from the bus master indicating an I/O address has been placed on the bus. (See I/O Space option, Section 2.10.1.)

BINIT....used to initialize the memory to a known state.

REFKILL....Refresh Kill is used for maintenance purposes to disable internal memory refresh.

EXTREFL....used to control refresh cycles externally (option).

6.1.2 Internal

SYNCH....a buffered BSYNCL used as a clock in the address register section and a start command in the timing section.

RDRQH....Read Request is a high true signal which starts a DATI cycle or the Read portion of a DATIO cycle.

WRTRQH....Write Request is a high true signal which, in conjuction with DOUTH, starts a DATO cycle or the write portion of a DATIO cycle.

DINH....a high condition enables the data out drivers during a Read mode as long as RPLYH is present.

DOUTH....used to start a DATO cycle and the write portion of a DATIO cycle. DOUTH also generates WROAL and WR1AL.

RPLYH....in conjunction with DINH, enables the data out drivers and produces the bus signal BRPLYL.

CASTH....a high true signal used to generate column timing for the RAM devices.

RASTL....a low true signal used to generate row timing for the RAM devices.

CASAL....a low true signal used by the RAM devices to clock in column address information.

RASA-BL....2 low true signals used by the RAM devices to clock in row address information.

WRTL....a low true timing signal used to generate Read/Write controls for the RAM devices.

WROAL....in a low true state enables the lower byte RAM devices for a Write mode.

WR1AL....in a low true state enables the upper byte RAM devices for a Write mode.

ROWL....in a low true condition allows row addresses to be sent to the RAM devices on the AD0-AD7 address lines.

COLL....in a low true state allows column addresses to be sent to the RAM devices on the AD0-AD7 address lines.

PE0L....a parity error signal from the byte 0 parity generation circuitry (Data Bits BDAL0L-BDAL7L).

PE1L....a parity error signal from byte 1 parity generation circuitry (Data Bits BDAL8L-BDAL15L).

REFRQH....Refresh Request is a high true signal used to start a Refresh cycle.

REFRQL....Refresh Request is a low true signal used to lockout a bus cycle.

REFL....during a Refresh cycle, REFL is in a low true state which enables row addresses, row address strobes and disables column address strobes.

REFH....Refresh is a high true signal used to generate Refresh clear. The high to low transition is used to increment the refresh counter.

DO0O-DO15H....16 data bits out of the RAM devices or CSR.

DI0O-DI15H....16 data bits into the RAM devices or CSR multiplexed with address information.

DOPAH....parity data out of the RAM device for byte 0.

DOPBH....parity data out of the RAM device for byte 1.

DIPAH....parity data into the RAM device for byte 0.

DIPBH....parity data into the RAM device for byte 1.

ADOA-AL....8 buffered multiplexed address lines for the RAM's.

6.2 Modes of Operation

The text in Section 6.2 will be referenced to the Block Diagram and Bus Timing Diagrams (Figures 2.1-2.3). BBS7L, BREFL, and BDCOKH must be high 75 nanoseconds prior to the assertion of BSYNCL for any memory cycle to occur.

6.2.1 DATI (Read)

In this mode, the memory reads a full word of data at a location determined by the bus master and transfers this data onto the bus.

The address (BDAL1-21) of the memory location to be accessed is stable 75 nanoseconds prior to the low transition of BSYNCL. This address is received by the memory transceivers and is sent to the memory's address selection section. In conjunction with BREFL and BBS7L, this address is decoded in the memory selection circuitry. If BREFL and BBS7L are in a high level condition and the address falls within the memory's selected limit, the selection circuitry generates a valid memory select signal. The select signal is sent to the timing and control circuitry and allows a memory cycle to be performed upon receipt of the bus control signals.

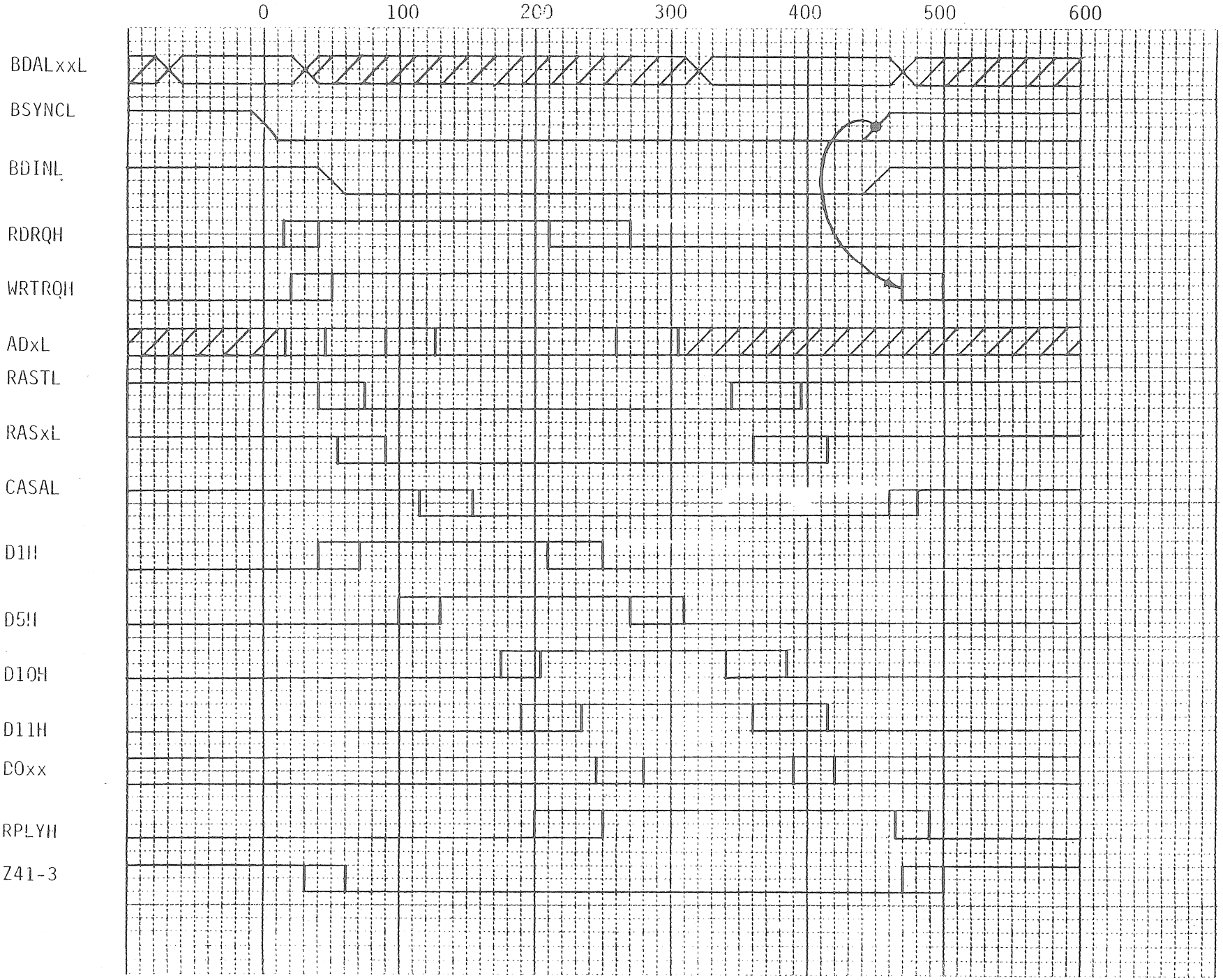
The bus master sets BWTBTL to a high level 75 nanoseconds before assertion of BSYNCL indicating a Read cycle will be performed.

BSYNCL is set low by the bus master, is received and sent to the timing and control section of the memory. Information on the BWTBTL bus line is stored in the control section of the memory by an internal memory clock (SYNCH). SYNCH is sent to the address register section and clocks the address present on the bus. This sequence allows the memory to store address and control commands for the rest of the memory cycle, even after valid address and control signals have been removed by the bus master.

RDRQH triggers the start of internal memory timing as long as internal memory refresh is not in control of the internal memory timing.

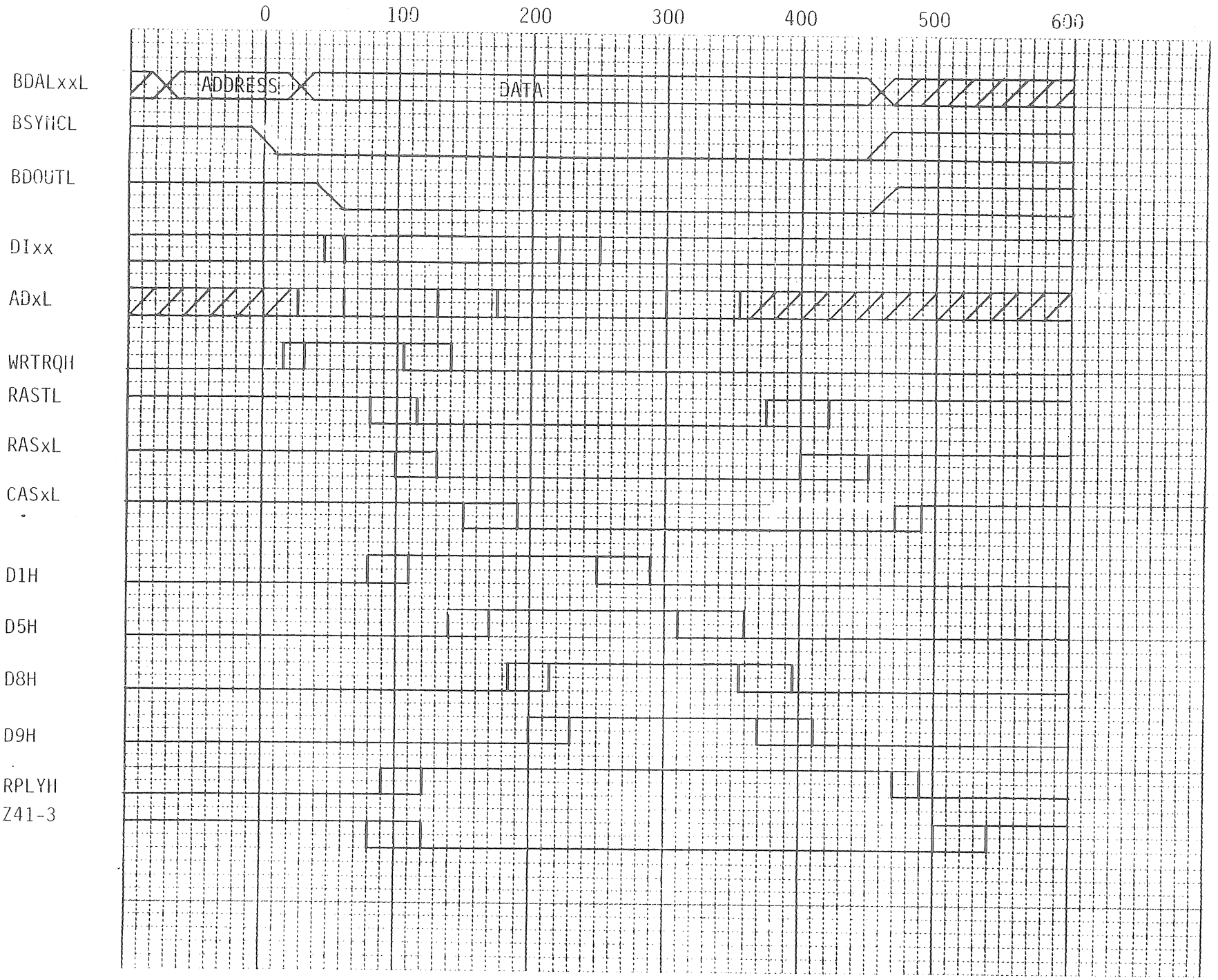
The memory timing is now in operation. Internal memory control signals RASxL, CASAL, and WRxAL are generated and routed to the RAM storage section. The row/column addresses are generated and forwarded to the RAM storage area. The aforementioned signals select a particular RAM device and a specific address (location) within the device.

The bus master requests read data by asserting BDINL. The DR-215 responds to BDINL by generating RPLYH in the control section of the memory and setting BRPLYL low on the bus.

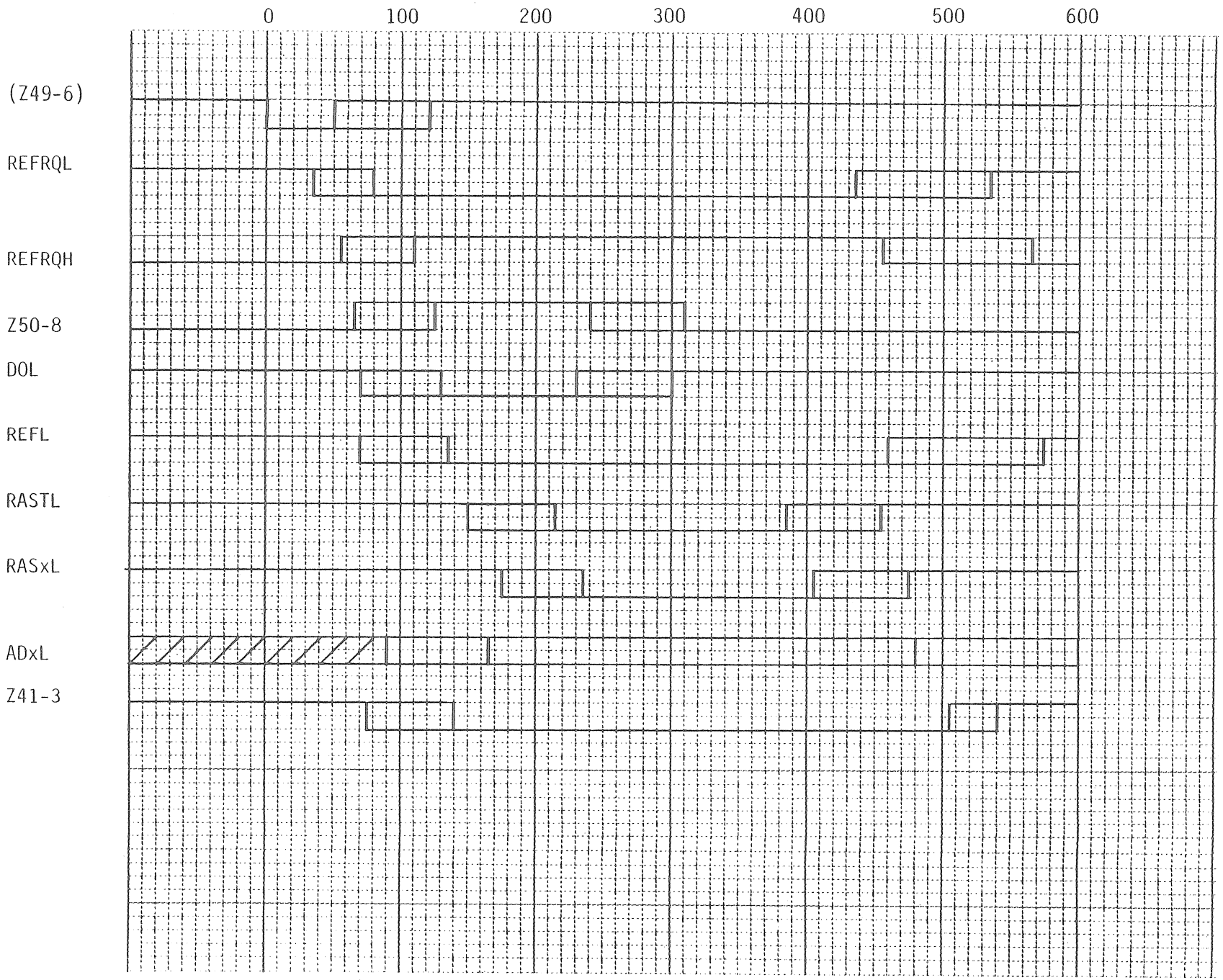


READ

Figure 3.1



WRITE
Figure 6.2



REFRESH
Figure 6.3

Data from RAM storage is sent to the data transceiver section 100 nanoseconds after CAS is received by the RAM device. BDINH and RPLYH are received by the transceivers and enable the driver portion of these gates. Valid data is placed on BDAL0-BDAL15 bus lines.

The bus master terminates BDINL after it has accepted data from the bus. The memory system sets BRPLYL high terminating the memory cycle. The bus master must wait 300 nanoseconds before starting the next memory cycle.

6.2.2 DATO (Write)

In this mode, the memory accepts and stores a full word of data from the bus master. Valid address information is placed on the bus 75 nanoseconds prior to BSYNCL. If the address falls within the limits of the memory, the memory is selected.

BSYNCL is asserted low and clocks address and control information into registers. The bus master asserts BDOUTL to indicate valid write data is available. DOUTH and WRTRQH start the memory timing. The memory timing section generates RASA-BL, CASAL, WROAL, and WR1AL and sends them to the RAM devices. The selected RAM device stores the data sent from the data transceiver section.

BRPLYL is asserted by the memory, indicating data has been stored in the memory. The bus master terminates BDOUTL which in turn allows the memory to terminate BRPLYL ending the memory cycle.

The bus master must wait 300 nanoseconds before asserting BSYNCL for the next memory cycle.

6.2.3 DATOB (Write/Byte)

This memory cycle is the same as a DATO cycle except a data byte (8 bits) is stored in memory. During normal address time, the bus master sets signal BDAL0L low for Byte 1 (BDAL8L-BDAL15L) or high for Byte 0 (BDAL0L-BDAL7L). This information allows the memory to write the correct byte of data. For a Byte Write operation, BWTBTL must be asserted low for the entire memory cycle.

6.2.4 DATIO (Read-Modify-Write)

In this mode, data is read from the memory, modified, and written into the same memory location.

BDAL1L-BDAL21L are asserted 75 nanoseconds prior to BSYNCL. BWTBTL is high during address time indicating a Read cycle. If the address is within the memory's boundaries, the memory is selected.

BSYNCL is asserted by the bus master. BSYNCL is buffered and used to latch address and mode control signals. RDRQH causes the memory to generate RASAL and CASAL.

The bus master asserts BDINL allowing the memory to access the selected RAM devices.

The memory asserts BRPLYL and sends DINH and RPLYH to the data transceiver section. DINH and RPLYH enable the driver portion of the transceiver, allowing the data to be placed on the BDALxxL lines.

The bus master accepts data from the bus and terminates BDINL. The DR-215 terminates BRPLYL, DINH, and RPLYH ending the Read portion of the memory cycle.

The bus master places Write data on the BDALxxL lines and asserts BDOUTL. DOUTH and WRTRQH start the Write portion of the memory cycle. The timing section generates RASxL, CASAL, WRxAL and sends the control signals to the RAM devices.

The data transceivers send data from the bus to the RAM devices. The selected RAM devices store the full word of data. The timing section asserts BRPLYL low allowing the bus master to terminate BDOUTL.

When BDOUTL is set to a high level, the memory terminates BRPLYL which ends the Write portion of the memory cycle. The bus master terminates BSYNCL and waits at least 300 nanoseconds before accessing the memory again.

6.2.5 DATIOB (Read-Modify-Write/Byte)

This mode of operation is the same as a DATIO cycle except a byte of data is stored during the Write portion of the cycle. BDAL0L is used to determine which byte is to be written. A high on the BDAL0L lines means byte 0 (BDAL1L-BDAL7L) will be written and a low means byte 1 (BDAL8L-BDAL15L) will be written.

BWTBTL is kept low during the entire Write portion of the memory cycle enabling the Write Byte cycle.

6.2.6 Refresh

Refresh is necessary to prevent loss of data stored in the NMOS storage chips. NMOS RAM devices store data on the gate capacitance of a field-effect transistor. A "1" is stored as teh absence of charge. The stored charge tends to deteriorate and must be renewed. Therefore, one row of each memory chip is recharged every 14 microseconds.

The Refresh cycle of the DR-215 is transparent to all bus master devices. If a memory cycle is in progress, refresh will occur immediately following the end of the memory cycle.

After a refresh cycle is requested within the memory, a delay of approximately 30 nanoseconds occurs before the refresh cycle starts. This delay allows for arbitration in case a memory cycle is also requested. If a memory cycle is requested within this time period, the memory cycle has priority.

Assuming no memory cycle has been requested, the refresh enable flip-flop is set. The refresh enable signal starts the refresh cycle.

The refresh counter address is sent to the RAM devices for row address selection. RAS is generated in the timing section and sent to the RAM devices. The selected row is refreshed allowing data to be retained.

The refresh cycle takes approximately 500 nanoseconds. If a memory cycle is requested during the refresh cycle, the memory cycle will start at the end of the refresh cycle. This allows the memory refresh cycle to be transparent to the bus master. A maximum of 500 nanoseconds may be added to the memory cycle.

6.3 General Description

A block diagram showing the interconnection of the major logic elements is contained on Sheet 1 of the schematic. The DR-215 contains semiconductor RAM storage, address selection logic, address registers, bi-directional data/address transceivers, timing and control logic, refresh circuitry, parity generation and checking, and a control and status register (CSR).

The semiconductor RAM storage array consists of 64K Dynamic RAM's. The RAM's are arranged in rows of 16 data bits and 2 parity bits. Modules may contain one or two rows of RAM's for capacities of 128K or 64K words.

Address selection logic determines if the bus address is within the module's address range. Switch 1 allows the memory to be offset in 4K word increments (See Table 2.1). The selection circuit also allows a failing bank (row) of RAM's to be disabled (See Section 2.10.6).

Address registers are needed on the DR-215 because address and data information are time-multiplexed on the Q-BUS. Addresses are set up 75 nanoseconds prior to BSYNCL. When BSYNCL is asserted, the addresses are latch in 74S374 octal

latches. The contents of these latches are then time multiplexed to the RAM array to supply the required row and column addresses.

The bi-directional data/address transceivers perform multiple functions. During address time the transceivers receive, buffer and invert the address bits. During data time they receive write data from the bus, drive read data onto the bus, and generate parity.

Timing and control logic determines the mode of operation and insures synchronization of the memory and bus master. Bus signals BDINL, BDOUTL, BWTBTL, and BBS7L determine the proper mode while BSYNCL and BRPLYL synchronize operation.

Refresh circuitry is required to insure data integrity. Dynamic RAM's store a charge on the gate capacitance of a field-effect transistor. The DR-215 performs a RAS only refresh. Every 14 microseconds, a refresh is performed on one row within all RAM devices. The refresh circuitry performs arbitration, supplies sequential row addresses, and generates all necessary timing and control.

The parity generation and checking logic helps to insure data integrity. When a word of data is written into the array tow parity bits (one per byte) are generated and stored. During a subsequent read cycle, the parity checking circuit compares newly generated parity bits to stored parity bits. If a discrepancy occurs, LED1 is turned on, bit 15 of the CSR is set, and BDAL16L is asserted.

The control and status register is used to control parity functions and store error address information. The CSR is addressed as an I/O device and has a switch selectable address (Table 2.2). The CSR bit assignment are discussed in Section 2.7.

6.4 Detailed Description

The text in this section is referenced to schematic 03334, bus timing diagrams (Figures 2.1-2.3), and internal timing diagrams (Figures 6.1-6.3).

6.4.1 Semiconductor RAM Storage

The semiconductor RAM storage array consists of one or two rows of 64K Dynamic RAM's shown on Sheet 7. Each row contains 18 RAM's, 16 data bits, and 2 parity bits. Data transfers to the RAM's are controlled by the WRxAL, RASxL, CASxL, and AD0A-AD7AL signals. Input data is presented on the DIØØ-15H and DIPA-BH (parity) lines. Output data appears on the DOØØ-15H and DOPA-BH (parity) lines.

The accessing of RAM locations requires the following sequence:

(1) 8 Row addresses valid on the ADØA-AD7AL pins.

(2) RASxL asserted to latch in the row address.

(3) Row addresses held for 10 nanoseconds, then column addresses multiplexed onto the AD0A-ADA7L pins.

(4) CASAL asserted, after 20 nanoseconds of column address set-up time, to latch in the address.

(5) If WRxAL is not asserted, read data will be valid 100 nanoseconds after assertion of CASAL.

(6) If WRxAL is asserted (early write cycle), the write data will be written into the RAM at the leading edge of CASAL.

(7) RASxL, CASAL, and WRxAL are negated and another RASxL cannot occur for 100 nanoseconds.

6.4.2 Address Selection

The address selection circuit consists of two 74S283 four bit adders, one 9 position dip switch, and associated gates shown on Sheet 4.

The address selection circuit allows the starting address of a module to be placed at any 4K word boundary between 0K and 2044K. Switch 1 controls the starting address (Table 2.1). The upper address limit is controlled by jumpers E16 and E15 (Table 2.4). If one row of RAM's is failing, it may be disabled according to Section 2.10.6.

During address time of a bus cycle, the nine most significant address bits, DI13-16H and A18-21H, are routed to the selection circuit. These lines are compared with the levels set at switch 1 using the two adders. The Σ4 output of Z20 chooses between the two rows of RAM's. This output must be stored at Z47 pin 5 due to the time-multiplexing of address and data on the Q-BUS.

In order for the system to be selected for a memory access, Z11 pin 8 must be low during address time. This occurs only when all four inputs are high. Pin 13 will always be high when DC power is within specification. Pin 9 is asserted low only when the current address is within the I/O space. Pin 12 is used on 64K word modules to set the upper address limit. Finally, Pin 10 will be high when BREFH and all four outputs (Σ1-Σ4) of Z21 are low.

6.4.3 Address Registers

The address registers are two 74S374 octal D-type flip-flops with three state outputs (Sheet 5). The registers are used to store 8 row and 8 column address bits during address time on the Q-BUS. Once a cycle has started, the contents are time-multiplexed to the RAM array.

At the beginning of a memory cycle Z37 pin 1 (Row L) is low. The contents of Z37 which were clocked in by SYNCH are enabled onto the ADØA-AD7AL lines. RASxL is asserted and the address is latched into the RAM chips. ROW L is negated and COL L (Z32 pin 1) is asserted. Eight new address bits are present at the RAM's. CASAL is asserted and these bits are stored in the RAM's. The RAM's now have 16 address bits stored internally. These bits are decoded and one location is accessed.

6.4.4 Data/Address Transceivers

Address and data information is time-multiplexed on the Q-BUS. In this section, the terms address time and data time will be used for ease of presentation.

6.4.4.1 Address Time

During address time address lines BDALØ-BDAL15L are received by four 2908 transceivers (Z1-Z4) on Sheet 5. Address lines BDAL16-21L are received by Z7 (8641) and Z5 (8640) on Sheet 4. These buffered inverted signals are internally referenced as DIØØ-17H and A18-21H.

The least significant address bit, DIØØH, is routed to a D-type flip-flop, Z47 (Page 4), and used to select between bytes during write byte cycles. The next 16 address bits DIØ1-16H are routed to the row and column address latches (Z37 and Z32) on Sheet 5. These addresses are decoded internally by the RAM's to choose one of 65,536 locations.

The nine most significant address bits DI13-16H and A18-21H are routed to the module selection adders Z20 and Z21 (Sheet 4). These addresses are compared to the levels set at switch 1 to determine if the address on the bus is within the module's range.

Address bits DI10-12H along with BBS7L are used to determine if an I/O address is on the bus. If I/O H is asserted, the memory is deselected and the CSR selection gate Z14 (Sheet 6) is enabled. Address bits DIØ1-DI11H and Switch 2 are used to select the CSR.

6.4.4.2 Data Time

During data time, the 2908 chips (Sheet 5) serve as transceivers, read data latches, and parity generators.

When a read cycle is performed, data from the RAM's is presented at the A0-A3 inputs of the 2908 chips. Odd parity is generated (Pin 10) and routed to the parity checking logic. Data is latched into the 2908 at the positive transition of DCLKH (Pin 19) and driven onto the Q-BUS (BØ-B3).

In the write mode, data is received at the BØ-B3 inputs. Pin 9 will be high so data is driven into the RAM array via the RØ-R3 outputs. In addition, odd parity will be generated (Pin 10) and routed to the parity circuit (Z35).

6.4.5 Timing and Control Logic

Timing and control logic determines the mode of operation and synchronizes memory timing and bus timing. Bus signals BDINL, BDOUTL, and BWTBTL determine the mode of operation while BSYNCL and BRPLYL synchronize timing. BBS7L and BDCOKH must be false for any memory cycle to occur. The timing and control logic is shown on Sheets 3 and 4.

All bus cycles are started when BSYNCL is asserted. The sequences which occur will be presented according to the mode of operation.

6.4.5.1 DATI Mode (Read)

The assertion of BSYNCL will initiate the following sequence:

(1) Z8 pin 2 will go high (SYNCH).

(2) The read request flip-flop (Z10 pin 11) and bank select flip-flop (Z47 pin 9) will be clocked and the reply flip-flop (Z30 pin 13) will be enabled.

(3) RDRQH (Z10 pin 9) and WRTRQH (Z10 pin 5) will be asserted. Assuming no refresh contention, the timing chain will be started at Z42 pin 8, the cycle latch will be set, and Z41 pin 3 will go low.

(4) BDINL will be asserted and Z7 will be enabled.

(5) RASTL will be generated at Z49 pin 8 and the row address will be latched into the RAM's.

(6) ROWL (Z43 pin 6) will be negated and COLL (Z43 pin 3) will be asserted.

(7) CASAL will be asserted (Z50 pin 3) and the column address will be latched.

(8) Z40 pin 10 will be pulsed to extend Z41 pin 3.

(9) DCLKH (Z22 pin 3) will go high to latch data into the 2908 transceivers (Sheet 5).

(10) Z30 pin 10 will go low and BRPLYL will be asserted (Z7 pin 12) indicating that data will be available in 125 nanoseconds.

(11) RPLYL (Z30 pin 3) will clock the parity flip-flop. If an error has occurred Z30 pin 5 will go high and BDAL16L (Z7 pin 15) will be asserted.

(12) BDINL will be negated by the bus master and the memory will negate BRPLYL. In return, the bus master will negate BSYNCL and the bus cycle will be completed.

(13) Z41 pin 3 will go high and the internal memory cycle will be complete.

6.4.5.2 DATO(B) Mode (Write)

DATO and DATOB cyles differ only in the number of bytes (2 or 1) written into memory and will be presented together. The assertion of BSYNCL will initiate the following sequence:

(1) Z8 pin 2 will go high (SYNCH).

(2) The write request flip-flop (Z10 pin 3) and bank select/byte select flip-flop (Z4 pin 9) will be clocked and the reply flip-flop (Z30 pin 3) will be enabled.

(3) WRTRQH will be asserted and Z42 pin 13 and Z44 pin 12 will be enabled.

(4) BDOUT will be asserted. Assuming no refresh contention, the timing chain will be started at Z42 pin 8, the cycle latch (Z50 pin 9) will be set, Z41 pin 3 will go low, and WRxAL will be asserted.

(5) RASTL (Z49 pin 8) will be asserted, the row address will be latched into the RAM's, and BRPLY will be asserted.

(6) ROWL (Z43 pin 6) will be negated and COLL (Z43 pin 3) will be asserted.

(7) CASAL (Z50 pin 3) will be asserted, the column address will be latched, and data will be written into the RAM's.

(8) Z40 pin 10 will be pulsed to extend Z41 pin 3.

(9) The bus master will negate BDOUT and the memory will then negate BRPLYL. In return, the bus master will negate BSYNCL and the bus cycle will be completed.

(10) Z41 pin 3 will go high and the internal cycle will be over.

6.4.5.3 DATIO(B) Mode (Read-Modify-Write)

DATO and DATOB cycles differ only in the number of bytes (2 or 1) written into memory and will be presented together. A DATO(B) cycle consists of a read cycle and a write cycle being performed during one BSYNCL assertion. Internally, the memory performs two separate operations which are presented in Sections 6.4.5.1 and 6.4.5.2.

6.4.6 Parity Generating and Checking

Parity generating and checking logic consists of four 2908 transceivers, one 74S86 quad exclusive-or gate (Z23) and one 74S135 quad exclusive-or/nor gate contained on Sheet 5.

During data time of a write cycle odd parity is generated at pin 10 of Z1-Z4 and routed to Z35 and Z23. The outputs of Z35 (pins 7 and 3) are stored in RAM along with data.

When data is read out of memory DOPØ-1H are input to Z23 (pins 9 and 5) where they are compared with newly generated parity (Z23 pins 11 and 3). If an error occurs in byte Ø DIØØ-DIØ7L) PEØL (Z23 pin 8) goes low. An error in byte 1 DIØ8-15L) causes PE1L (Z23 pin 6) to go low. A low on either of these lines at RPLYL time will cause PAREH (Z30 pin 5) and BDAL16L to be asserted, LED1 to be lit, the current address to be stored in the CSR, and bit 15 of the CSR to be set.

If parity is enabled, BDAL17L will be asserted and cause a parity trap to 114_8.

6.4.7 Refresh Circuitry

The refresh circuitry consists of a free-running oscillator (Z51), mode selector (Z49), request one shot (Z40), and refresh flip-flop (Z45), shown on Sheet 3.

The oscillator controls internal refresh requests. The refresh period is set to 14 microseconds using R11. An internal refresh is initiated when Z51 pin 3 goes high.

The mode selector (Z49) chooses between internal and external refresh modes. Three modes may be implemented, internal, external, and internal/external. Section 2.10.3 explains the proper jumper configurations.

All refresh cycles are initiated when Z49 pin 6 is asserted and REFKILL is negated. Z40 is fired and REFRQL is asserted to block a memory cycle from beginning. REFRQH is delayed 30 nanoseconds to allow cycle arbitration. If the refresh cycle wins the refresh flip-flop (Z45 pin 3) is clocked set and a refresh cycle occurs.

Any memory cycle requested during a refresh occurs upon completion of the refresh cycle (Z41 pin 3 going high).

6.4.8 Control and Status Register

The CSR is contained on Sheet 6. A detailed explanation of the CSR bit assignments is given in Section 2.7. The CSR is used to control parity functions and to allow testing of parity circuitry.

During normal memory operation, the CSR stores error address bits 11-21 and asserts BDAL17L during RPLYL time if bit Ø (Z26 pin 15) is set. When BSYNCL is asserted, the upper 11 bus address bits are stored in Z31 and Z24 and routed to Z34 and Z36. If an error occurs, Z34 pin 11 and Z36 pin 11 are clocked and the address is stored.

Error address information (22 address bit system) must be retrieved in three steps. First, the CSR must be read to retrieve A11-A17 from Z34. Second, bit 14 of the CSR must be set by writing into the CSR. Last, the CSR must be read again to retrieve A18-A21 from Z36.

The CSR can be used to force incorrect parity to be written. If bit 2 (Z26 pin 10) is set, WWPL (Z34 pin 4) will be asserted and DIPØ-1H will be inverted. This feature is for diagnostic purposes only.

7.0 PART NUMBERS/DOCUMENTATION

7.1 The following Dataram part numbers have been assigned to the DR-215 Memory System:

Part Number	Description
61541	DR-215, 128K x 18 with CSR
61542	DR-215, 64K x 18 with CSR

7.2 Documentation

61541	Bill of Materials, DR-215, 128K x 18 w/CSR
61541	Assembly, DR-215, 128K x 18, w/CSR
03334	Schematic, DR-215

REV. I

DWG. NO. 61541 SHEET 1 OF 4

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		RELEASED TO PRODUCTION	JM	11/25/82
B		ECN 2575 BRT	JM	11/26/82
C		ECN 2608	JM	5/5/82
D		ECN 2693	JM	5/5/82
E		ECN 2710	JM	5/5/82
F		ECN 2750	JM	5/5/82
G		ECN 2865	JHL	10-7-82
H		ECN 2925	JHL	10-7-82

DRAWN MAS	DATE 1-6-82
CHECKED RJE	DATE 1-6-82 25 JAN 83
ENGR JM	DATE 1/25/82
APPROVED RK	DATE 25 JAN 83

TITLE

BILL OF MATERIALS

DR-215 128K X 18 W/CSR

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 61541 REV H

SHEET 1 OF 4

TITLE: B/M DR-215 128K X 18 W/CSR

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	1	18408	LED GREEN PC MT W/INTL RES	LED ,3
2	2	18401	LED RED PC MT W/INTL RES	LED 1,2
3	18	18101	DIODE SILICON HIGH CONDUCTANCE	CR1-18
4	18	12331	CAP CER AXL .1µF +80/-20%	C15 - 32
5	5	12105	CAP TANT 4.7µF 10V	C1,2,6,7,10
6	3	12102	CAP TANT 15µF 20V	C3,9,14
7	1	12513	CAP SIL MICA 100PF 5%	C4
8	1	12318	CAP CER 3900PF 10%	C5
9	1	12518	CAP SIL MICA 33PF 5%	C8
10	1	12506	CAP SIL MICA 470PF 5%	C11
11	1	12523	CAP SIL MICA 820PF 5%	C13
12	1	12315	CAP CER .01µF 20%	C12
13	3	11105	RES MDL 10K OHMS 6 PIN	RM1,2,5
14	3	11103	RES MDL 1K OHMS 6 PIN	RM4,6,10
15	1	11953	RES MDL 1K OHMS	RM3
16	3	11412	RES MDL 33 OHMS 2%	RM7-9
17	5	10122	RES CC 1/4W 10K OHMS 5%	R1,5,6,8,13
18	1		RES S.A.T.	R2
19	1	10181	RES CC 1/4W 51K OHMS 5%	R3
20	1	10216	RES FLM 1/10W 5.11K OHMS 1%	R4
21	1	10117	RES CC 1/4W 2.0K OHMS 5%	R7
22	1	10151	RES CC 1/4W 33 OHMS 5%	R12
23	1	10145	RES CC 1/4W 22K OHMS 5%	R9
24	1	10113	RES CC 1/4W 1.0K OHMS 5%	R10
25	1		RES S.A.T.	R11
26	1	10109	RES CC 1/4W 270 OHMS 5%	R15

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 61541
SHEET 2 OF 4

REV. H

TITLE: B/M DR-215 128K X 18 W/CSR

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
27	1	10111	RES CC 1/4W 470 OHMS 5%	R14
28	4	16380	IC INTFC LINE XCVR 2908	Z1-4
29	3	16374	IC QUAD NOR BUS RX 8640	Z5,6,8
30	1	16345	IC QUAD UNI BUS XCVR 8641	Z7
31	1	16511	IC DUAL 5I/P NOR 74S260	Z12
32	1	16516	IC DUAL 4I/P NAND 74S20	Z11
33	1	16501	IC HEX INV 74S04	Z13
34	1	16537	IC 13I/P NAND 74S133	Z14
35	2	16505	IC QUAD EX OR 74S86	Z15,23
36	1	16237	IC HEX ST INV 74LS14	Z16
37	1	16202	IC DUAL D BIN FF 74LS74	Z17
38	3	16507	IC QUAD 2I/P NOR 74S02	Z9,18,53
39	4	16522	IC DUAL D BIN 74S74	Z10,30,45,48
40	2	16525	IC QUAD 2I/P AND 74S08	Z19,41
41	2	16535	IC 4B BIN FULL ADDER 74S283	Z20,21
42	3	16521	IC QUAD 2I/P OR 74S32	Z22,29,52
43	36	16940	IC DYNAMIC RAM 64K x 1	0A&B-15A&B,P0A&B-P1A&B
44	1	16558	IC QUAD EXCL OR 74S135	Z35
45	2	16513	IC QUAD 2I/P NAND 74S00	Z25,43
46	2	16207	IC QUAD D BIN 74LS175	Z26,47
47	1	16236	IC DUAL 4B BIN CNTR 74LS393	Z27
48	2	16234	IC OCT 3STAT BFR INV 74LS240	Z28,39
49	3	16260	IC OCT D FF 74LS374	Z31,34,36
50	2	16551	IC OCT D FF 74S374	Z32,37
51	2	16253	IC OCT 3STAT BFR 74LS244	Z33,38
52	1	16221	IC HEX D FF W/CLR 74LS174	Z24

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: B/M DR-215 128K X 18 W/CSR

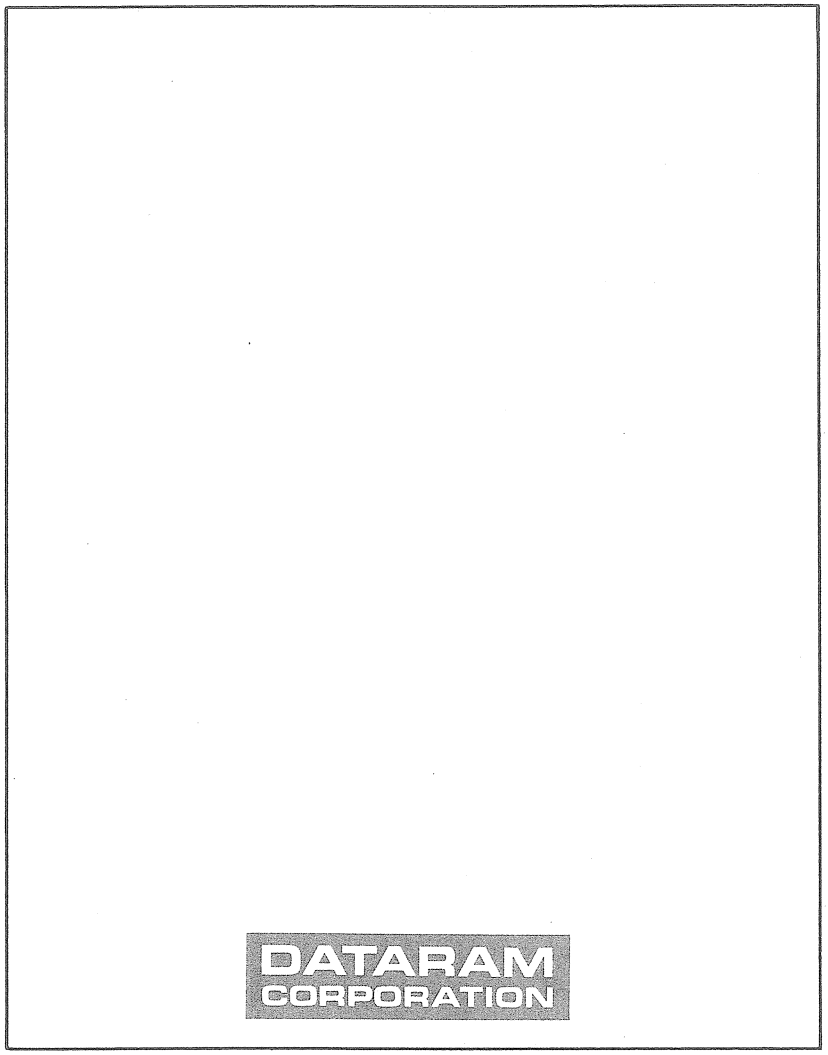
ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
53	1	16211	IC DUAL MONOSTABLE MV 74LS221	Z40
54	1	16553	IC AND/OR/INV 74S65	Z42
55	1	16519	IC AND/OR/INV 74S64	Z44
56	1	16206	IC QUAD 2I/P AND 74LS08	Z46
57	1	16512	IC DUAL AND/OR/INV 74S51	Z49
58	1	16529	IC QUAD 2I/P NAND ST 74S132	Z50
59	1	16356	IC TIMER 555	Z51
60	1	22916	SWITCH DIP 10 POS LOW PROF	SW1
61	1	22942	SWITCH DIP SPDT 4 POS	SW2
62	1	14108	DELAY LINE DIGITAL 150NS	DL1
63				
64	40	22601	CONT MALE	E1-40
65	1	40823	PCB DR-215	
66	1	27329	CARD HANDLE	
67	2	27323	RIVET BLIND STL EYE	
68	REF	03334	SCHEMATIC DR-215	
69	A/R	24504	WIRE SOL GRN 30 AWG WW	
70	A/R	30617	INK MARKING WHITE	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

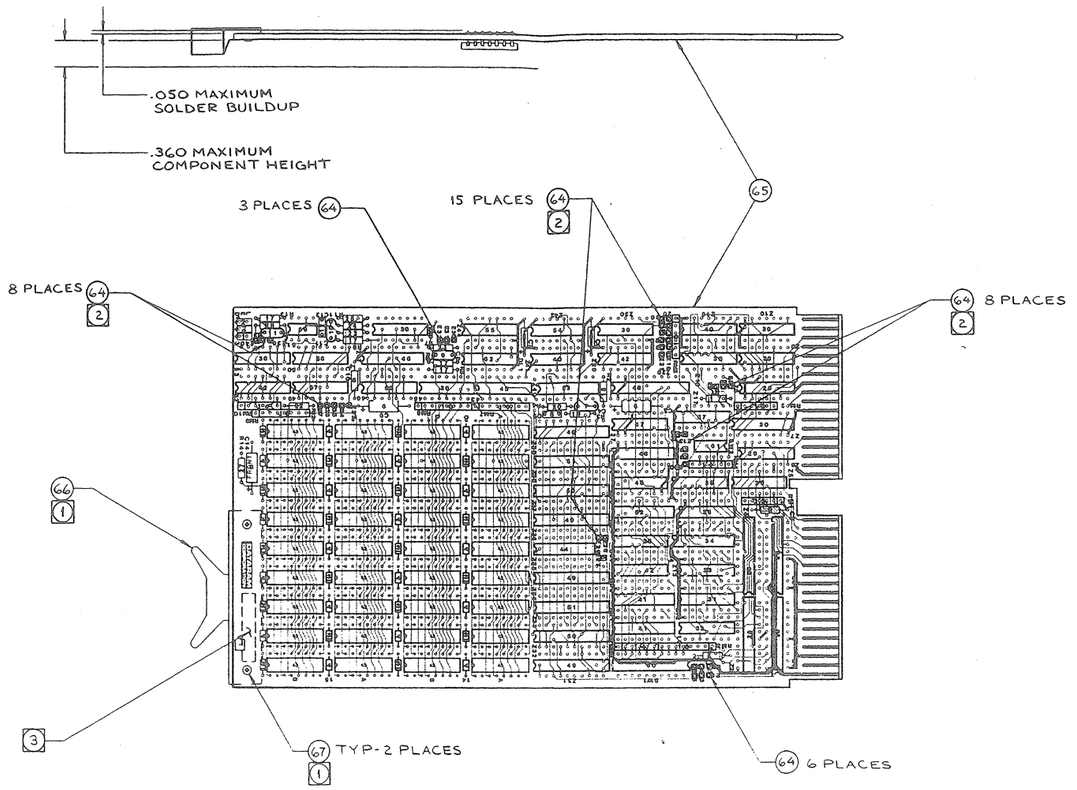
DWG. NO. B/M 61541
SHEET 4 OF 4

REV. H



Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	1/25/82	
	B	ECN 2575 BRT	1/26/82	
	C	ECN 2608	5/5/82	
	D	ECN 2693	5/5/82	
	E	ECN 2710	5/5/82	
	F	ECN 2750	5/5/82	
	G	ECN 2845	10-7-82	
	H	ECN 2925	10-7-82	



NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL AFTER FLOW SOLDER.
2. WIREWRAP E8 TO E9, E10 TO E11, E13 TO E14, E21 TO E22, E23 TO E24, E28 TO E29, E31 TO E32 E35 TO E36, E39 TO E40, E25 TO E26 AFTER TEST USING ITEM 69.
3. PERMANENTLY MARK PART NO., SERIAL NO. & DATE CODE WHERE SHOWN WITH ITEM NO. 70.

4 FOR SCHEMATIC DIAGRAM SEE DRAWING NO. 03334

61542	64K x 18 W/CSR
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE ... INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN B.TRUAX	12-29-81
CHECKED	25JAN82
ENGR	1/25/82
APPROVED RK	25JAN82

DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY,
DR-215 128K x 18 W/CSR

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	50473	61541	H

SCALE FULL SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	1/2/82	
	B	ECN 2675	5/5/82	
	C	ECN 2693	5/5/82	
	D	ECN 2710	5/5/82	
	E	ECN 2750	5/5/82	
	F	ECN 2751	5/5/82	
	G	ECN 2925	10-7-82	

A		
1		2
	A	+5V
	B	
BDAL16L	C	GND
BDAL17L	D	
EXTRFL	E	BDOUTL
	F	BRPLYL
	H	BDINL
GND	J	BSYNCL
REFKILL L	K	BWTBTL
	L	
GND	M	BIAK1 L
	N	BIAKØL
	P	BBS7L
BREFL	R	BDMG1L
	S	BDMGØL
	T	BINITL
	U	BDALØØL
+5VB	V	BDALØ1L

B		
1		2
BDCOK H	A	+5V
	B	
BDAL18L	C	GND
BDAL19L	D	
BDAL20L	E	BDALØ2L
BDAL21L	F	BDALØ3L
	H	BDALØ4L
GND	J	BDALØ5L
	K	BDALØ6L
	L	BDALØ7L
GND	M	BDALØ8L
	N	BDALØ9L
	F	BDAL10L
	R	BDAL11L
	S	BDAL12L
GND	T	BDAL13L
	U	BDAL14L
+5V	V	BDAL15L

REFKILL L

EXTRF L

REFRESH CLOCK SHT. 3

REFRESH COUNTER & ARBITRATION SHT. 5&3

BSYNC L

BDIN L

BDOUT L

BWTBT L

BDCOK H

BRPLY L

TIMING & CONTROL SHT. 3&4

PARITY GENERATION & CONTROL SHT. 5

DOPØH DIPØH DOP1H DIP1H

SEMICONDUCTOR RAM STORAGE 128K X 18 SHT. 7

+5V

DSTL

MEMORY BI DIRECTIONAL DATA & ADDRESS TRANSCEIVERS SHT 5

BDALØØLTHRU BDAL21L

DATA IN (16 BITS)

DATA OUT (16 BITS)

ROW/COLUMN ADDRESS GENERATION & ADDRESS REGISTERS SHT. 5

DOØØH-DO15H

DIØØH-DI15H

CSR SHT 6

MEMORY ADDRESS SELECTION SHT. 4

BREF L

BBS7 L

BINIT L

INTERNAL

EXTERNAL

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± ~ DECIMALS .XX ± ~ .XXX ± ~ ANGLES ± ~

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN B TRUAX	1-4-82
CHECKED	
ENG.	2/2/82
APPROVED RK	

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC, DR-215

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G

SCALE ~ SHEET 1 OF 7

STARTING ADDRESS SELECTION (SW 1)

STARTING ADDRESS	1	2	3	4	5
ØK	OFF	OFF	OFF	OFF	OFF
4K	ON	OFF	OFF	OFF	OFF
8K	OFF	ON	OFF	OFF	OFF
12K	ON	ON	OFF	OFF	OFF
16K	OFF	OFF	ON	OFF	OFF
20K	ON	OFF	ON	OFF	OFF
24K	OFF	ON	ON	OFF	OFF
28K	ON	ON	ON	OFF	OFF
32K	OFF	OFF	OFF	ON	OFF
36K	ON	OFF	OFF	ON	OFF
40K	OFF	ON	OFF	ON	OFF
44K	ON	ON	OFF	ON	OFF
48K	OFF	OFF	ON	ON	OFF
52K	ON	OFF	ON	ON	OFF
56K	OFF	ON	ON	ON	OFF
60K	ON	ON	ON	ON	OFF
64K	OFF	OFF	OFF	OFF	ON
68K	ON	OFF	OFF	OFF	ON
72K	OFF	ON	OFF	OFF	ON
76K	ON	ON	OFF	OFF	ON
80K	OFF	OFF	ON	OFF	ON
84K	ON	OFF	ON	OFF	ON
88K	OFF	ON	ON	OFF	ON
92K	ON	ON	ON	OFF	ON
96K	OFF	OFF	OFF	ON	ON
100K	ON	OFF	OFF	ON	ON
104K	OFF	ON	OFF	ON	ON
108K	ON	ON	OFF	ON	ON
112K	OFF	OFF	ON	ON	ON
116K	ON	OFF	ON	ON	ON
120K	OFF	ON	ON	ON	ON
124K	ON	ON	ON	ON	ON

FOR ALL OTHER SETTINGS USE EQUAL INCREMENTS OF 128K PLUS THE APPROPRIATE 4K INCREMENT FROM ABOVE TABLE.

	6	7	8	9	
0-128K	OFF	OFF	OFF	OFF	ON=CLOSED OFF=OPEN
128-256K	ON	OFF	OFF	OFF	
256-384K	OFF	ON	OFF	OFF	
384-512K	ON	ON	OFF	OFF	
512-640K	OFF	OFF	ON	OFF	
640-768K	ON	OFF	ON	OFF	
768-896K	OFF	ON	ON	OFF	
896-1024K	ON	ON	ON	OFF	
1024-1152K	OFF	OFF	OFF	ON	
1152-1280K	ON	OFF	OFF	ON	
1280-1408K	OFF	ON	OFF	ON	
1408-1536K	ON	ON	OFF	ON	
1536-1664K	OFF	OFF	ON	ON	
1664-1792K	ON	OFF	ON	ON	
1792-1920K	OFF	ON	ON	ON	
1920-2048K	ON	ON	ON	ON	

CSR ADDRESS SELECTION

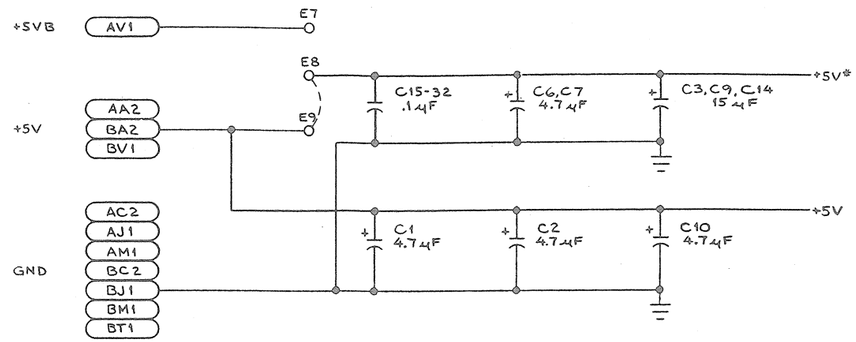
CSR ADDRESS			SWITCH 2 POSITION			
16 BIT ADDRESS	18 BIT ADDRESS	22 BIT ADDRESS	4	3	2	1
172100	772100	17772100	OFF	OFF	OFF	OFF
172102	772102	17772102	OFF	OFF	OFF	ON
172104	772104	17772104	OFF	OFF	ON	OFF
172106	772106	17772106	OFF	OFF	ON	ON
172110	772110	17772110	OFF	ON	OFF	OFF
172112	772112	17772112	OFF	ON	OFF	ON
172114	772114	17772114	OFF	ON	ON	OFF
172116	772116	17772116	OFF	ON	ON	ON
172120	772120	17772120	ON	OFF	OFF	OFF
172122	772122	17772122	ON	OFF	OFF	ON
172124	772124	17772124	ON	OFF	ON	OFF
172126	772126	17772126	ON	OFF	ON	ON
172130	772130	17772130	ON	ON	OFF	OFF
172132	772132	17772132	ON	ON	OFF	ON
172134	772134	17772134	ON	ON	ON	OFF
172136	772136	17772136	ON	ON	ON	ON

NOTE: E17 TO E18 DISABLES CSR SELECTION.
E11 TO E12 MUST BE INSTALLED FOR 16 OR 18 BIT ADDRESS OPERATION.

ON=CLOSED
OFF=OPEN

LAST DESIGNATION USED	
INTEGRATED CIRCUIT	Z52
CAPACITOR	C31
RESISTOR	R15
RESISTOR MODULE	RM10
DIODE	CR18
SWITCH	SW2
DELAY LINE	DL1
WIRE WRAP POST	E40
LED	LED3

REF. DESIG	GATES USED / TOTAL GATES	TYPE
Z16	5 / 6	74LS14



JUMPER FUNCTION SUMMARY

FUNCTION	JUMPERS IN	JUMPERS OUT
CSR SELECTION		
DISABLE CSR	E17-E18, E20-E26	E25-E26
ENABLE CSR	E25-E26	E17-E18, E20-E26
PARITY ERROR REPORTING		
NON-CSR	E12-E13	E13-E14
WITH CSR	E13-E14	E12-E13
WRITE WRONG PARITY ENABLE		
NON-CSR	E27-E28	E29-E28
WITH CSR	E28-E29	E27-E28
PARITY		
DISABLE	E23-E17	E24-E23
ENABLE	E24-E23	E23-E17
MEMORY SIZE		
128K	E21-E22	E15-E16
64K	E15-E16, E21-E22	
BANK REMOVAL		
UPPER BANK FAILS	E15-E16, E16-E22	
LOWER BANK FAILS	E21-E22, E15-E16	
ADDRESSING		
16 OR 18 BIT ADDRESS	E11-E12	E10-E11
22 BIT ADDRESS	E10-E11	E11-E12
BATTERY BACKUP	E7-E8	E8-E9
NO BATTERY BACKUP	E8-E9	E7-E8

FUNCTION	JUMPERS IN	JUMPERS OUT
REFRESH		
INTERNAL	E35-E36, E39-E40	E36-E37, E38-E39 E33-E34, E33-E36
EXTERNAL	E36-E37, E38-E39	E35-E36, E39-E40 E33-E34, E33-E36
INTERNAL NORMAL, EXTERNAL BACKUP	E33-E36, E33-E34	E36-E37, E38-E39 E35-E36, E39-E40
NO REFRESH (TEST ONLY)	E35-E36, E38-E39	E39-E40, E36-E37 E33-E36, E33-E34
I/O SPACE SIZE		
4KW		E1-E2, E3-E4, E5-E6
2KW	E5-E6	E1-E2, E3-E4
1KW	E3-E4, E5-E6	E1-E2
.5KW	E1-E2, E3-E4, E5-E6	

5 AFTER FINAL TEST, WIREWRAP E8 TO E9, E10 TO E11, E13 TO E14 E21 TO E22, E23 TO E24, E28 TO E29, E31 TO E32, E25 TO E26 E35 TO E36, E39 TO E40.

4 * INDICATES BATTERY BACK-UP

3. ALL DIODES ARE DATARAM P/N 18101

2. ALL CAPACITOR ARE IN μF, ±10%.

1. ALL RESISTORS ARE IN OHMS, CARBON COMPOSITION, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED.

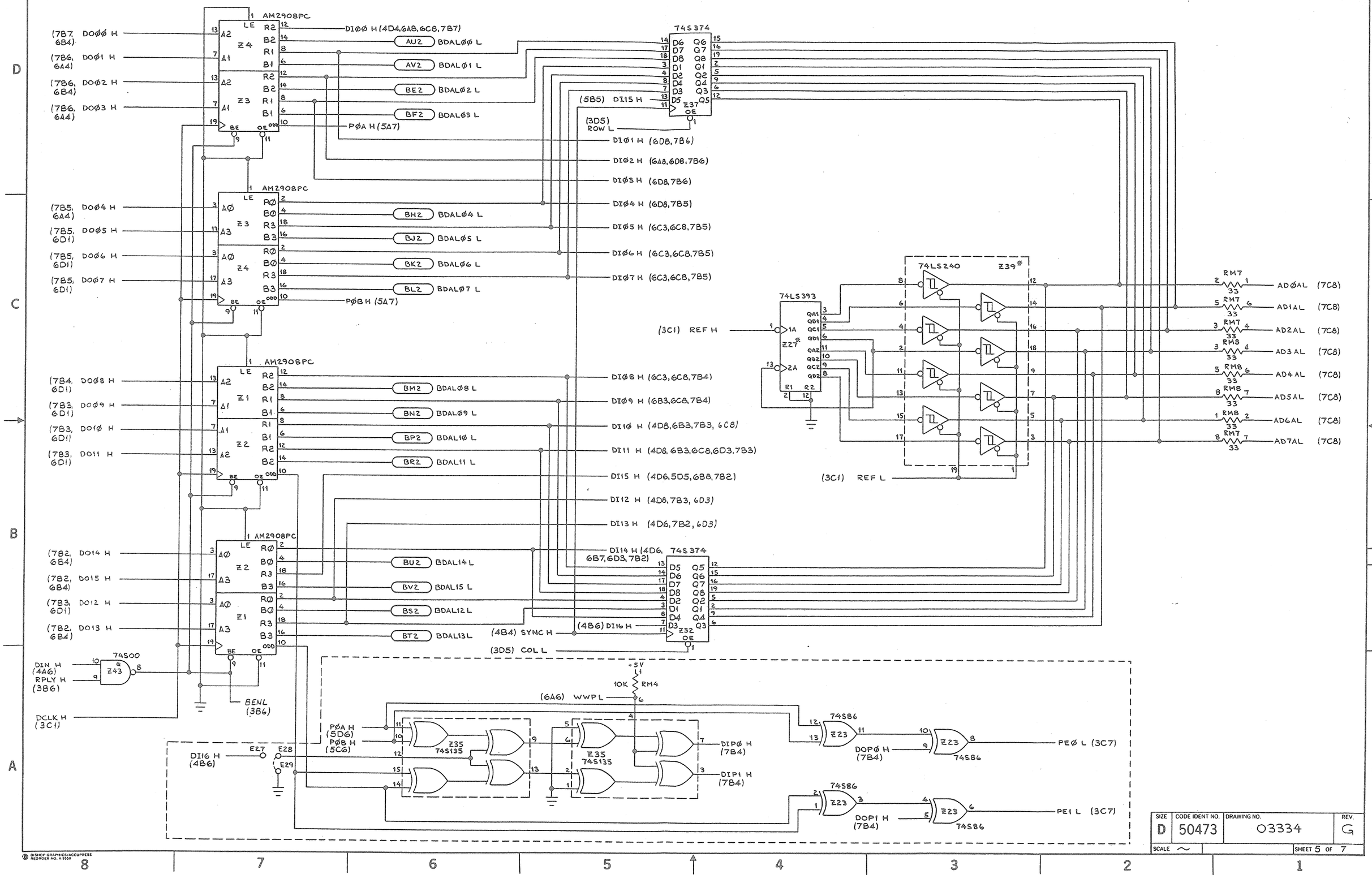
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~		SHEET 2 OF 7	

DOUT H (4A3)
WRTRQ H (4B5)
REFRQ L (3B1)
DCOK H (4A5)
(4B5) RDRQH
REFRQ H (3B1)
CASTL (4A3)
Z41 74S08
Z42 74S65
WRITE
READ
REFRESH
R7 2K
R6 10K
C8 33PF
R4 5.1K
R2 S.A.T.
C4 100PF
Z40 74LS221
Z43 74S00
ROW L (5D5)
COL L (5B5)
Z50 74S132
Z53 74S02
DL1
D1OH (4B4, 4A4)
D1H (4B4)
Z28 74LS240
D11H (3C8)
Z16 74LS14
(3B7) CSR DLK L
Z29 74S32
DSH (4B4, 4A4)
DCLK H (5A8)
Z22 74S32
(4B2) RASTL
Z46 74LS08
R5 10K
Z45 74S74
REF H (4C3,5C4)
REF L (4B4,5B3,4A4)
D11 H (3D2)
REF L (3C1)
E30 E31 E32
Z44 74S64
CSR
CSR RPY H (6C4)
E25 E26 E20
CSR DLK L (3D3)
(5A2) PEØ L
(5A2) PE1 L
Z25 74S00
Z19 74S08
BPERH (4B8)
E23 E24 E17
(6C4) CSRSEL H
BENL (5A7)
Z18 74S02
Z30
PAREH (6A3)
PAREL (6B8)
SYNCH (4B4)
R3 51K
C5 .1000PF
Z40 74LS221
REFRQ H (3D8)
REFRQ L (3D8)
AK1 REFKILL
R1 10K
Z16 74LS14
Z30 74S74
RPLY H (4A8,4B5, 5A8,6A5)
RPLYL (4A3)
RPYCK H (4A6)
SYNC H (4B4)
AE1 EXTRFL
Z8 8640
(4A5) DCOK H
E37 E33 E36 E34 E35
Z49 74S51
R15 270
C13 820PF ±5%
Z53 74S02
E39 E40 E38
R13 10K
R10 1K
R11 S.A.T.
R9 22K
Z51 555
RES VCC DIS TRIG THLD CON VOL OUT GND
C11 470PF ±5%
C12 .01 ±20%

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~		SHEET 3 OF 7	

BBS7L
AP2
Z6 8640
Z11 74S20
Z16 74LS14
I/O H (6C8)
RM6
RM3
+5V
1K
(5B5) DI10 H
(5B5) DI11 H
(5B5) DI12 H
DI13 H (5B5)
Z22 74S32
SW1
74S283
(5B5) DI14 H
(5B5) DI15 H
E22
E21
Z16 74LS14
RM5 10K
Z47 74LS175
(5D7)DIØØ H
(3C1) REF H
R8 10K
Z53 74S02
Z52 74S32
RM10 1K
RM9 33
RASB L (7C8)
RASA L (7B8)
WRØAL (7C8)
WRIAL (7C8)
Z46 74LS08
Z12 74S260
Z11 74S20
Z18 74S02
Z19 74S08
RM1
BDAL18L
BC1
BDAL19L
BD1
BDAL20L
BE1
BDAL21L
BF1
BREF L
AR1
Z5 8640
A18H (6B3)
A19H (6B3)
A20H (6B3)
A21H (6B3)
BREF H
BSYNC L
AJ2
Z8 8640
RM5 10K
SYNCH (3B8,6C6, 3B5, 5B5)
Z10 74S74
RDRQ H (3D8)
Z48 74S74
Z50 74S132
(3C3) D5 H
(3D4) D10 H
Z29 74S32
RM2 10K
DS8641N
BDAL16L
AC1
BDAL17L
AD1
BPERH (3C6)
BWTBT L
AK2
EREBH (6A4)
BRPLY
AF2
RPLY H (3B6)
Z7
DI16 H (5B5, 5A7, 6D3)
DI17H (6D3)
WTBT H
WRTRQ H (3D8)
Z9 74S02
(3B6) RPLY H
Z9 74S08
(3C1) REF L
(3C5) D1 H
Z49 74S51
RAST L (3C3)
R12 33
CASA L (7C8)
LED2
LED3
DOUT H (3D8, 6C6)
(3D4) D10H
D5H (3C3)
Z16 74LS14
Z29 74S32
Z45 74S74
RPLYL (3B6)
CASTL (3D8)
(3C1) REFL
(6A6) PCINITL
Z41 74S08
BDIN L
AH2
BDOUT L
AE2
BDCOK H
BA1
DIN H (5A8, 6C5)
RPYCK H (3B8)
DCOK L (6A8)
Z28 74LS240
DCOK H (3B5, 3D8)

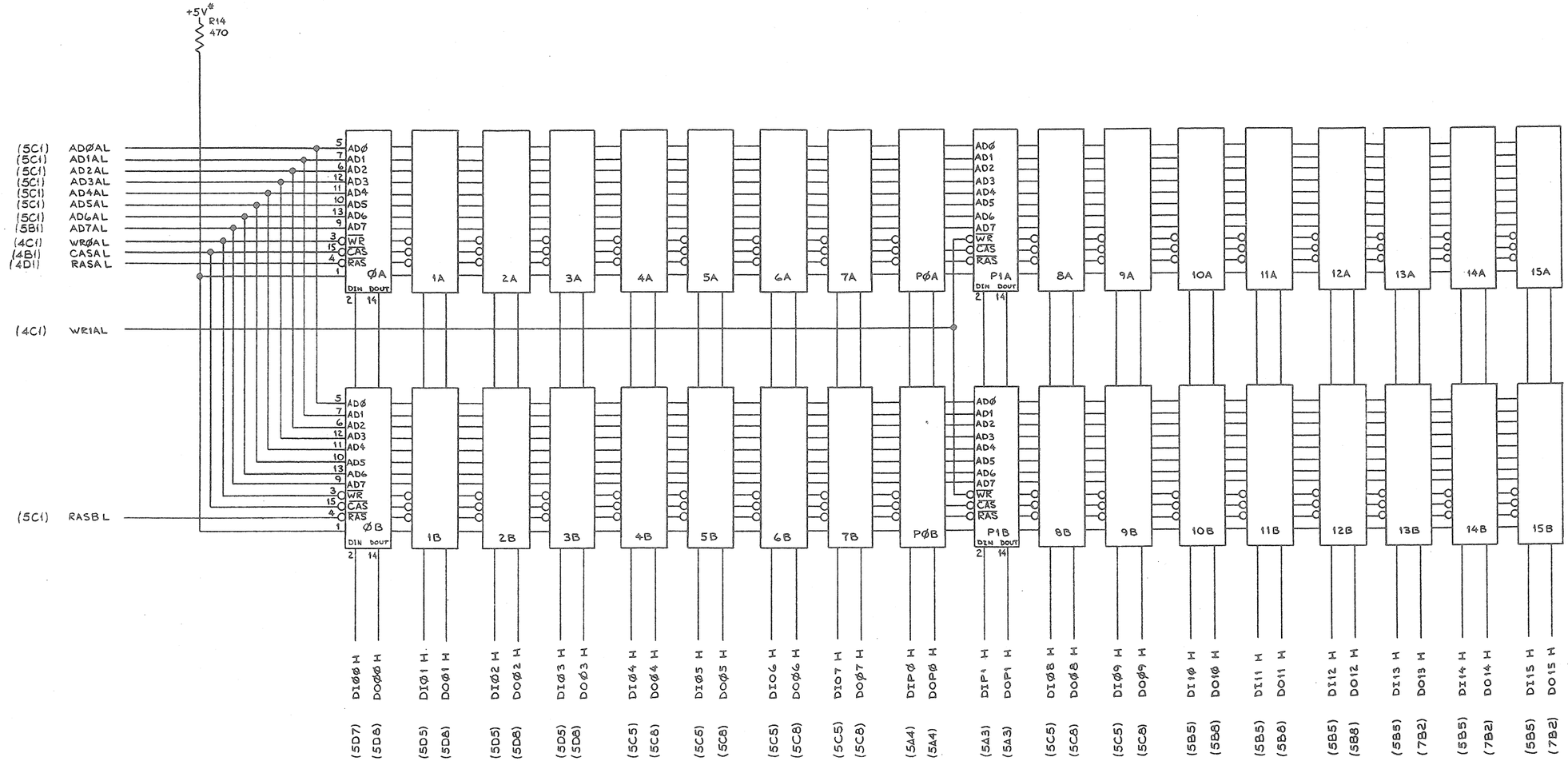
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~		SHEET 4 OF 7	



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~			SHEET 5 OF 7

SW2
RM4 1K
+5V
74S86
Z15
DIØ1 H (5D5)
DIØ2 H (5D5)
DIØ3 H (5D5)
(5C5) DIØ4 H
74S04
Z13
(5D7) DIØØ H
(5C5) DIØ5 H
(5C5) DIØ7 H
(5C5) DIØ8 H
(5C5) DIØ9 H
(5B5) DI11 H
(5C5) DIØ6 H
(5B5) DI1Ø H
74S133
Z14
(6A6) PCINTL
74LS74
Z17
(4B4) SYNC H
RM5 10K
CSRSEL H (3B6)
74S00
Z25
(4A6) DIN H
(4A3) DOUT H
CSRRPY H (3B8)
WRCSR H (6A8,6B3)
74LS374
Z31
Z34
(5B5) DI11 H
(5B5) DI12 H
(5B5) DI13 H
(5B5) DI14 H
(5B5) DI15 H
(4B6) DI16 H
(4B6) DI17 H
DOØ5 H (5C8)
DOØ6 H (5C8)
DOØ7 H (5C8)
DOØ8 H (5C8)
DOØ9 H (5C8)
DO1Ø H (5B8)
DO11 H (5B8)
DO12 H (5B8)
Z33
74LS244
(5C5) DIØ5 H
(5C5) DIØ6 H
(5C5) DIØ7 H
(5C5) DIØ8 H
(5C5) DIØ9 H
(5B5) DI1Ø H
(5B5) DI11 H
(6C4) WRCSR H
Z19
74S08
Z22
74S32
(3B5) PARE H
74LS174
Z24
(4C7) A18 H
(4C7) A19 H
(4B7) A20 H
(4B7) A21 H
RM1 10K
Z36
(4D5) I/O H
(3B4) PARE L
E17
E18
Z19
LED1
(5B5) DI15 H
Z17
ERR H
74LS74
DO15 H (5B8)
DO14 H (5B8)
DOØ2 H (5D8)
DOØØ H (5D8)
DO13 H (5B8)
DOØ4 H (5C8)
DOØ3 H (5D8)
DOØ1 H (5D8)
Z38
74LS244
(5B5) DI14 H
E10
E11
E12
74LS175
Z26
LWAD L
(5D5) DIØ2 H
WWP H
WWP L (5A5)
(5D7) DIØØ H
(6C4) WRCSR H
BINIT L
AT2
8640
Z6
74S260
Z12
(4A6) DCOK L
PCINT L (6D6, 4A4)
(3B6) RPLY H
Z41
EREB H (4B8)

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~		SHEET 6 OF 7	



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03334	G
SCALE ~		SHEET 7 OF 7	