TECHNICAL MANUAL

DR-275

DATARAM CORPORATION

TECHNICAL MANUAL

DR-275

06139

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1.0 GENERAL

The Dataram Model DR-275 Semiconductor Memory Array Board is designed to operate in Digital Equipment Corporation's (DEC's*) VAX*-11/730 and VAX*-11/750 Model computers. It will operate with or in place of DEC's Model MS730 in the VAX 11/730 and with or in place of DEC's Model M8750 in the VAX 11/750.

The Dataram Model DR-275, at full capacity, consists of 1 MByte of memory with 7 ECC bits using NMOS 64K semiconductor technology. The array and logic is organized on a signal height hex width card utilizing the space of one standard card slot. The DR-275 features 1 MByte of data storage with 7 ECC bits, interface logic to the Bus, a red L.E.D. which indicates board selection, a green L.E.D. which indicates +5V battery backup is present and a module enable/disable switch.

2.0 ELECTRICAL SPECIFICATIONS

2.1 Description

The DR-275 consists of 156 dynamic NMOS RAM devices arranged in a 256K x 39 Bit Array. The DR-275 also contains the necessary word addresses, multiplexed addresses (row & column) and write drivers to select the array. Tri-state receivers and drivers are used to transfer data between the memory control boards and the DR-275 array. All timing and data control for the DR-275 is generated by the DEC VAX-11/730, 740 compatible Memory Controller.

2.2 Cycle and Access Times

The DR-275 is governed by the VAX-11/750 and VAX-11/730 memory controllers, thus the following table shows typical cycle and access times for the array module:

Mode	Cycle Time	Access Time
Read	500ns	270ns
Write	500ns	100ns
Read-Modify-Write	850ns	270/630ns
Initialize	500ns	---
Refresh	500ns	---
Exchange	1150ns	270/830ns

2.3 Interface

The DR-275 interfaces directly with the DEC MC730 (VAX-11/730) and DEC (VAX-11/750) memory control boards. Signals required by the memory array boards are listed below.

INT BUS AOH-A7H	Multiplexed Row/Column Address Lines
INT BUS MA14H, MA15H	Row Address Selects
INT BUS RAS TIM L	Row Address Strobe Timing
INT BUS CAS TIM L	Column Address Strobe Timing
INT BUS WR TIM L	Write Timing
INT BUS AD MEM SEL L	Array Board Selection

INT BUS DB00-31 RD L	32 Bit Bi-directional Data Lines
INT BUS CB1,2,4,8,16, 32, T RD L	7 Bit ECC Bi-directional Data Lines
INT BUS DR EN L	Array Data Driver

See Table I for pin assignments.

2.4 Power Requirements

The DR-275 must be operated from +5VDC. Proper power sequencing is provided by the VAX-11/750 and VAX-11/730 memory subsystem power supplies. Voltage-current requirements at a cycle time of 500 nanoseconds plus a 14 microsecond refresh interval are as follows:

	Operating Amps	Standby Amps	Battery Amps
+5V ± 5%	.700	.700	----
+5VB ± 5%	1.900	1.000	1.000

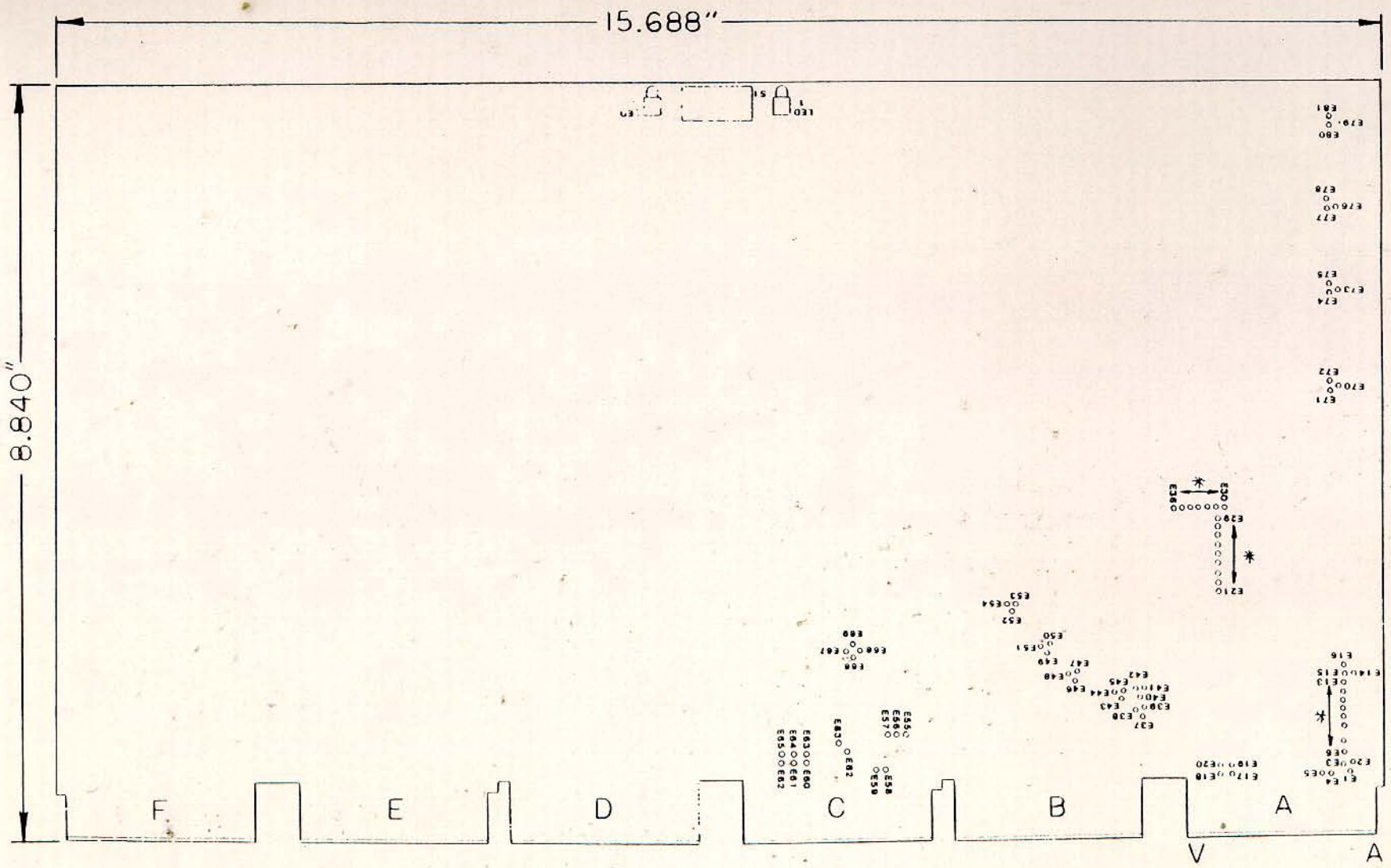
3.0 MECHANICAL SPECIFICATIONS

3.1 Dimensions

The DR-275 Semiconductor Array Board is designed to fit mechanically into the VAX-11/750 and VAX-11/730 chassis. The DR-275 requires the space of one DEC Hex printed circuit board. (See Figure 1).

3.2 Weight

1.25 pounds (.567 kg)



MECHANICAL OUTLINE

Figure 1

* = SEQUENCED NUMBERS

4.0 ENVIRONMENTAL SPECIFICATIONS

4.1 Temperature

Operating: $0^{o}C$ to $+55^{o}C$
Storage: $-40^{o}C$ to $+80^{o}C$

4.2 Humidity

Operating: 0 to 90% (without condensation)
Non-Operating: 0 to 95% (without condensation)

4.3 Altitude

Operating: 1000 ft. below to 10,000 ft. above mean sea level.
Non-Operating: 1000 ft. below to 20,000 ft. above mean sea level.

4.4 Vibration

Will withstand normal stresses encountered in transportation.

A

	1		2
A	INT BUS DB11 RD L	A	+5
B	INT BUS DB10 RD L	B	MEM PRESS
C	INT BUS MA15 H	C	GND
D	INT BUS DB09 RD L	D	INT BUS MA14 H
E	INT BUS REFCYC (2) L	E	INT BUS ADD MEM SEL L
F	INT BUS DB08 RD L	F	INT BUS A02 H
H	INT BUS A01 H	H	INT BUS DB27 RD L
J	INT BUS DB26 RD L	J	INT BUS A03 H
K	INT BUS A00 H	K	INT BUS DB25 RD L
L	INT BUS DB24 RD L	L	INT BUS A06 H
M	INT BUS CAS TIM L	M	INT BUS DR EN L
N	INT BUS DB15 RD L	N	INT BUS WR TIM L
P	INT BUS A05 H	P	INT BUS DB31 RD L
R	+12 BATT	R	INT BUS DB14 RD L
S	-12V	S	INT BUS RAS TIM L
T	GND	T	INT BUS DB13 RD L
U	+12 BATT	U	INT BUS DB12 RD L
V	FNGP 7L	V	INT BUS 04 H

B

	1		2
A	FNGP 3L	A	
B	FNGP 5L	B	INT BUS DB29 RD L
C	INT BUS DB30 RD L	C	INT BUS GND RD L
D	+5 BATT	D	INT BUS DB28 RD L
E	FNGP 4L	E	INT BUS DB19 RD L
F	INT BUS DB18 RD L	F	INT BUS DB03 RD L
H	INT BUS DB17 RD L	H	INT BUS DB16 RD L
J	INT BUS DB02 RD L	J	INT BUS DB00 RD L
K	INT BUS CB8 RD L	K	INT BUS DB01 RD L
L	INT BUS CB2 RD L	L	INT BUS CB4 RD L
M	FNGP 6L	M	INT BUS CB1 RD L
N	T.P. 5	N	INT BUS A07H
P	INT BUS DB07 RD L	P	INT BUS CB6 RD L
S	INT BUS DB23 RD L	S	INT BUS DB22 RD L
T	GND	T	INT BUS DB21 RD L
U	INT BUS DB20 RD L	U	INT BUS CBT RD L
V	INT BUS CB32 RD L	V	INT BUS CB16 RD L

TABLE I

C

1		2
NP6 SO	A	
NP6 OUT	B	
	C	GND (-5)
	D	
T.P. -5	E	
	F	
	H	
	J	
FNGP1 L	K	
	L	
FNGP2 L	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	

D

1		2
	A	+5
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	B6 7 SO
	L	B6 7 OUT
	M	B6 6 SO
	N	B6 6 OUT
	P	B6 5 SO
	R	B6 5 OUT
	S	B6 4 SO
GND	T	B6 4 OUT
	U	
	V	

Conn. E EL2 T.P. Term.
Conn. F No Connections

TABLE I-B

TABLE I
(cont.)

5.0 INSTALLATION

The DR-275 has been designed to utilize one standard hex card slot of the VAX 11/750 or VAX 11/730.

5.1 Switch Settings and Jumper Options

5.1.1 Switch Settings

Switch 1-1 located on the rear of the card must be in the ON position (switch up) for the DR-275 to be enabled. When the switch is in the ON position, the green L.E.D. will be ON to indicate that correct +5V battery backup is applied to the board and the board is enabled.

5.1.2 Jumper Settings

All jumpers are factory installed, there are no selectable options.

5.2 Computer Installation

The DR-275 may be installed in the VAX 750 or VAX 730 as follows:

5.2.1 VAX 11/750

The DR-275 may be installed in any current VAX 11/750 computer or in any earlier version to which appropriate modifications have been made to the backplane, as described in the VAX 11/750 upgrade kit. These modifications enable the VAX 11/750 to accommodate a maximum of 8 MBytes of memory, or accommodate a mixture of memory boards utilizing 16 K MOS and 64K MOS RAM technology.

The following slots of the VAX 11/750 have been specified for memory.

	Memory	Memory	Memory	Memory	Memory	Memory	DR-275	DR-275	LØØ11						LØØ5	LØØ4	LØØ3	LØØ2	
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

MEMORY ARRAY SLOTS

UNIBUS EXPANSION SLOT

COMET BACKPLANE

5.2.2 VAX 11/730

The VAX 11/730 consists of from 1 to 5 memory array modules that use 64K MOS RAM chips for data storage. Up to five 1 MByte array modules may be installed to give a maximum memory capacity of 5 MBytes. The minimum memory configuration is 1MB.

Card slots for the VAX 11/730 backplane have been specified as follows:

1	Disk Controller	
2		
3		
4	Memory Controller	
5	Writable Control Store	
6	DR-275 Memory Array	
7	Memory Array	
8	Memory Array	
9	Memory Array	
10	Memory Array	
11		
12	Terminator	Quad Slot

VAX 11/730 CPU BACKPLANE

5.3 Diagnostics

The DR-275 is completely compatible with all Digital Equipment Corporation's memory diagnostics. No software patches are needed. The diagnostics will run as if DEC's original equipment is installed.

5.3.1 The RAM array of the DR-275 has been layed out in 4 rows (Rows A-D) of 39 columns (0-38) as marked on the silk screen of the DR-275. The following table shows the correlation between DEC's chip numbers and Dataram's row and column numbers for the RAM storage array.

DEC COMPONENT NUMBER	DATARAM ROW/COLUMN #	DEC COMPONENT NUMBER	DATARAM ROW/COLUMN #
E100	A-27	E130	A-24
E101	A-11	E131	A-8
E103	D-27	E132	A-36
E104	D-11	E133	D-24
E105	B-27	E134	D-8
E106	B-11	E135	B-24
E108	C-27	E136	B-8
E109	C-11	E137	B-36
E110	A-26	E138	C-24
E111	A-10	E139	C-8
E112	A-38	E140	A-31
E113	D-26	E141	A-15
E114	D-10	E142	A-35
E115	B-26	E143	D-31
E116	B-10	E144	D-15
E117	B-38	E145	B-31
E118	C-26	E146	B-15
E119	C-10	E147	B-35
E120	A-25	E148	C-31
E121	A-9	E149	C-15
E122	A-37	E150	A-30
E123	D-25	E151	A-14
E124	D-9	E152	A-34
E125	B-25	E153	D-30
E126	B-9	E154	D-14
E127	B-37	E155	B-30
E128	C-25	E156	B-14
E129	C-9	E157	B-34

DEC COMPONENT NUMBER	DATARAM ROW/COLUMN #
E158	C-30
E159	C-14
E160	A-29
E161	A-13
E162	A-33
E163	D-29
E164	D-13
E165	B-29
E166	B-13
E167	B-33
E168	C-29
E169	C-13
E170	A-28
E171	A-12
E172	A-32
E173	D-28
E174	D-12
E175	B-28
E176	B-12
E177	B-32
E178	C-28
E179	C-12
E180	A-19
E181	A-3
E182	D-35
E183	D-19
E184	D-3
E185	B-19
E186	B-3
E187	C-35
E188	C-19
E189	C-3
E190	A-18
E191	A-2
E192	D-34
E193	D-18
E194	D-2
E195	B-18
E196	B-2
E197	C-34
E198	C-18
E199	C-2
E200	A-17
E201	A-1
E202	D-33
E203	D-17
E204	D-1
E205	B-17
E206	B-1
E207	C-33
E208	C-17
E209	C-1
E210	A-16
E211	A-Ø
E212	D-32
E213	D-16
E214	D-Ø
E215	B-16
E216	B-Ø
E217	C-32
E218	C-16
E219	C-Ø
E220	A-23
E221	A-7
E222	D-38
E223	D-23
E224	D-7
E225	B-23
E226	B-7
E227	C-38
E228	C-23
E229	C-7
E230	A-22
E231	A-6
E232	D-37
E233	D-22
E234	D-6
E235	B-22
E236	B-6
E237	C-37
E238	C-22
E239	C-6
E240	A-21
E241	A-5
E242	D-36
E243	D-21
E244	D-5
E245	B-21
E246	B-5
E247	C-36
E248	C-21
E249	C-5
E250	A-20
E251	A-4
E253	D-20
E254	D-4
E255	B-20
E256	B-4
E258	C-20
E259	C-4

TABLE 5.1

5.3.2 If the diagnostics being used refer to a bad RAM by address and bit number, the bad RAM may be located as follows:

1. Subtract starting address of board from the error address.
2. If difference between the starting address and error address is between:

OCTAL	
0 - 177777	0 - 64K - Bad RAM is located in Row A.
200000 - 377777	64K - 128K - Bad RAM is located in Row B.
400000 - 577777	128K - 192K - Bad RAM is located in Row C.
600000 - 777777	192K - 256K - Bad RAM is located in Row D.

The bit number (0-31) will correspond to the column number as labeled on the silk screen of the DR-275. For the check bits the following applies:

CHECK BIT NUMBER	DR-275 COLUMN NUMBER
CBO 1	32
CBO 2	33
CBO 4	34
CBO 8	35
CBO 16	36
CBO 32	37
CBO T	38

6.0 THEORY OF OPERATIONS

6.1 Hardware

This section contains the theory of operation of the DR-275 Semiconductor Memory Array. This material makes reference to the schematic 03364 and the block diagram on sheet one of the same. Reference is also made to timing diagrams Figure 2, and Figure 3.

6.1.1 Functional Description

The DR-275 consists of 4 major parts (see block diagram), a memory array, address drivers, data bus transceiver, and a control section. All timing, memory module selection, and relative address selection is performed by the memory control boards.

6.1.1.1 Memory Array

The memory array of the DR-275 consists of 156 NMOS Dynamic RAMs arranged in a 64K x 39 bit x 4 row configuration. Each row has a separate row address strobe (RAS), which is needed to initiate the RAM device cycle. Each RAM is dimensioned in a 256 x 256 array and accessed through 8 multiplexed address lines (AØ-A7). This configuration enables selection of one of 256K double length words (1 MByte), by using 8 address lines and the appropriate timing.

The memory array receives the following signals:

1. AØØ-AØ7 - 8 multiplexed address lines, enables selection of one location from a 256 x 256 bit array.
2. RAS (A-D) - Row address strobe, indicates the first 8 bits are valid on address lines, and initiates the RAM device cycle.

3. CAS - Column address strobe, indicates the second 8 bits of the address are valid on address lines.
4. WR 0-3, CB - Write, simultaneously initiates a write cycle on all 4 bytes and ECC bits of the selected double length word.
5. IN, OUT - Data path for one bit to be written to or read from a specified location.

6.1.1.2 Data Bus Transceivers

There are 39 data bus transceivers on the DR-275 (Z13-Z22). Each transceiver interfaces the backplane data lines to the memory array. During a write cycle, (DATO), the data is transmitted from the backplane to the IN line of the RAM device. During a read cycle, (DATI), the data is retrieved from a specified location, placed on the OUT line of the RAM device and transferred to the backplane through the 39 bus transceivers. The bus transceivers consist of two 74LS240, the input side of the transceiver is always enabled, the output side (data to backplane) is enabled through DOEN L.

6.1.1.3 Address Drivers

The address drivers of the DR-275 (Z3-Z6) interface the memory array multiplexed address lines to the backplane. In order for the address drivers to become active, they must receive a SEL signal from the control section.

6.1.1.4 Control Section

The DR-275 control section receives the following signals from the memory controller.

1. AD MEM SEL - Asserted low, indicates memory module selected by controller, enables address drivers.
2. MA14, MA15 - Row address select lines, enables selection of one of four - 64K x 39 bit rows.

3. RAS TIM - Row address strobe time line, indicates that the first 8 bits of the address are valid on AØ-A7.

4. CAS TIM L - Column address strobe time, indicates that the second 8 bits of the address are valid on AØ-A7.

5. WR TIM L - Write time line when asserted indicates that valid data to be stored in a selected location of the memory array is present at the data bus transceivers.

6. DREN L - Array data driver enable when asserted enables output to the bus through the data bus transceivers.

7. REFCYC - Refresh cycle when asserted initiates 1/256 of the refresh cycle. The controller supervises the timing and address selection of the sections of memory to be refreshed.

6.1.2 Modes of Operation (Refer to Figures 2 and 3)

The DR-275 is capable of operating in five modes: read, write, read-modify-write, refresh, and initialize. All timing and arbitration of modes is generated by the memory control boards. The following is the sequence which each mode follows. The exact timing is dependent on the memory controller.

6.1.2.1 Read

In this mode, the memory module reads a double word (32 bits + 7 ECC bits) from a specified location and transfers the bits to the data bus transceivers.

It is assumed that REFCYC is in its inactive state and ADD MEM SEL is in its active state.

With ADD MEM SEL in its active state, the address drivers are enabled. The memory controller now asserts MA14, MA15 so that the proper 64K 39 bit row may be selected (Z10-Z11).

Then the memory controller asserts AØØ-AØ7 with the appropriate RAM row address. Upon the receipt of the RAS TIM L, the appropriate RAS (A-D) is asserted (Z10-Z11). This signal is transferred to the memory array and the RAM row address is strobed in. The eight bit row address must be asserted for a minimum of 20 ns after the receipt of RAS, where upon the RAM column address may be asserted.

CAS TIM L is now asserted by the memory controller. Upon receipt of this signal, all RAM devices in the array receive the column address and strobe, however, only the 64K x 39 bit row which received RAS (A-D) will respond. The column address must remain asserted for at least 45ns after CAS is received. After a maximum delay of 75ns, valid data will be available on the output transceivers, if DREN L had been asserted (Z13-Z22). The data is now transferred to the memory control board (DOØ-DO38). The memory controller checks the data for errors and if none are found negates ADD MEM SEL which completes the cycle.

6.1.2.2 Write Cycle (DATO)

As with the read cycle, the write cycle depends upon the memory controller for cycle arbitration and timing. The cycles start out the same; the memory selected, MA14 and MA15 asserted, the RAM row address asserted and strobed, however, prior to the assertion of CAS TIM L, WR TIM L and the data (DBØ-DB38) which is to be stored, must be asserted. The assertion of WR TIM L is transmitted through (Z8 and Z9) to all the RAM devices. This signal indicates that a write cycle is about to commence.

The data to be written to the selected cells is latched into an on chip register by the combination of WR TIM L and CAS, while RAS is still active. The data must remain a minimum of 45ns after the assertion of CAS. The write signal must remain 30ns after the assertion of CAS, after the appropriate wait, the cycle is ended.

6.1.2.3 Read-Modify-Write

This cycle is a combination of the read cycle and write cycle. It is initiated as a read cycle then the word read is transferred to the memory controller and checked for errors. If no errors are found, the controller combines the new data bytes to be written with the existing bytes of data, generates 7 new syndrome code bits and initiates a write cycle.

The write cycle is initiated by asserting WR TIM L while CAS and RAS are still asserted. The memory module then follows the format of a write cycle.

6.1.2.4 Refresh

In this mode, the memory controller sends the appropriate refresh addresses, REFCYC L and RAS to all memory modules. The controller goes through a refresh cycle approximately every 12us. 64K RAMs require 256 refresh cycles every 2 ms.

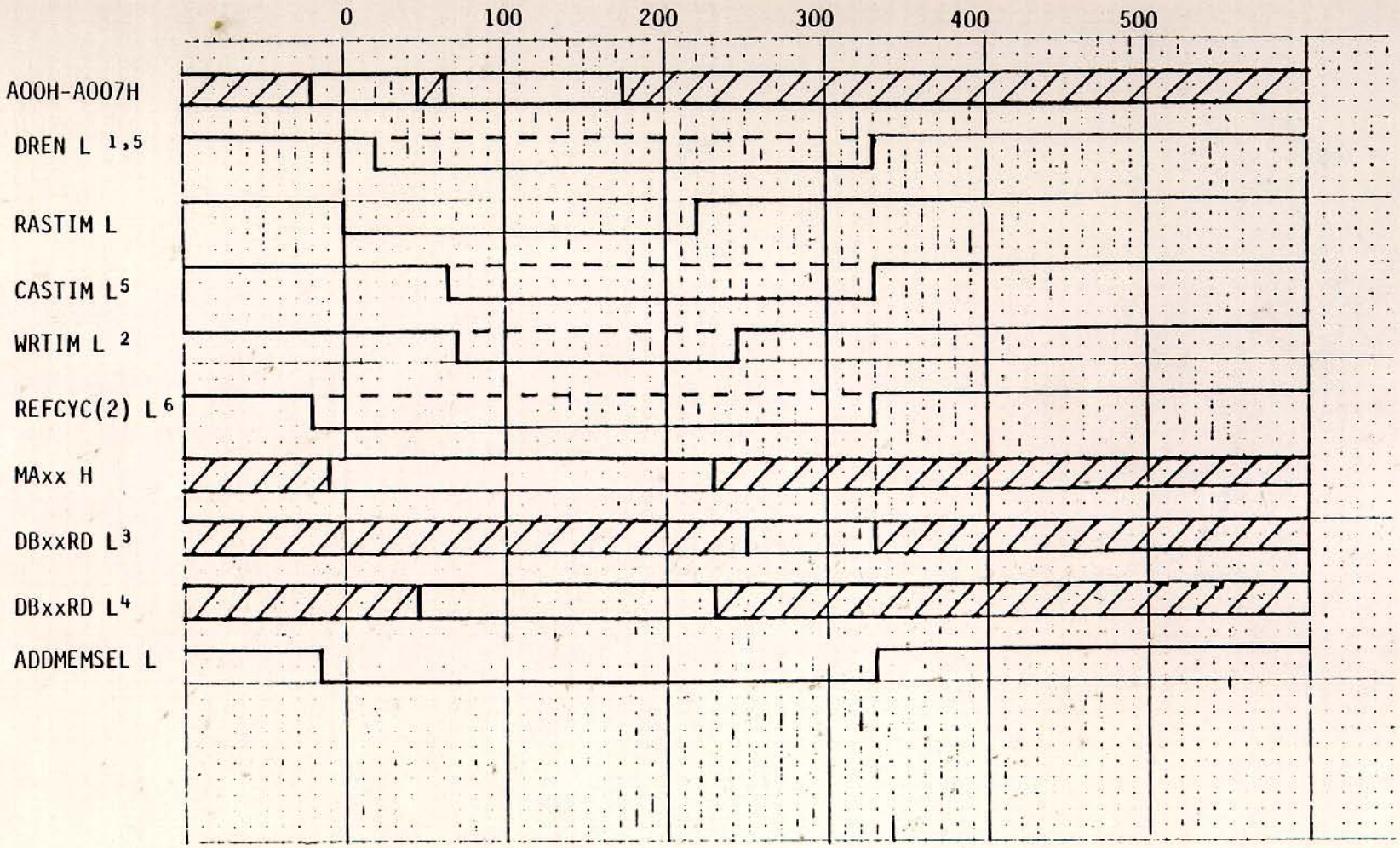
The memory controller selects all memory modules, sends REFCYC, which enables all rows of the memory module, and then sends the appropriate row address.

RAS L is asserted by the memory controller and received by the control section of the memory array. RAS is used to generate row address strokes for all RAM devices in the NMOS memory array section.

CAS L is not asserted during refresh cycle therefore, the cycle is completed after the negation of RAS L.

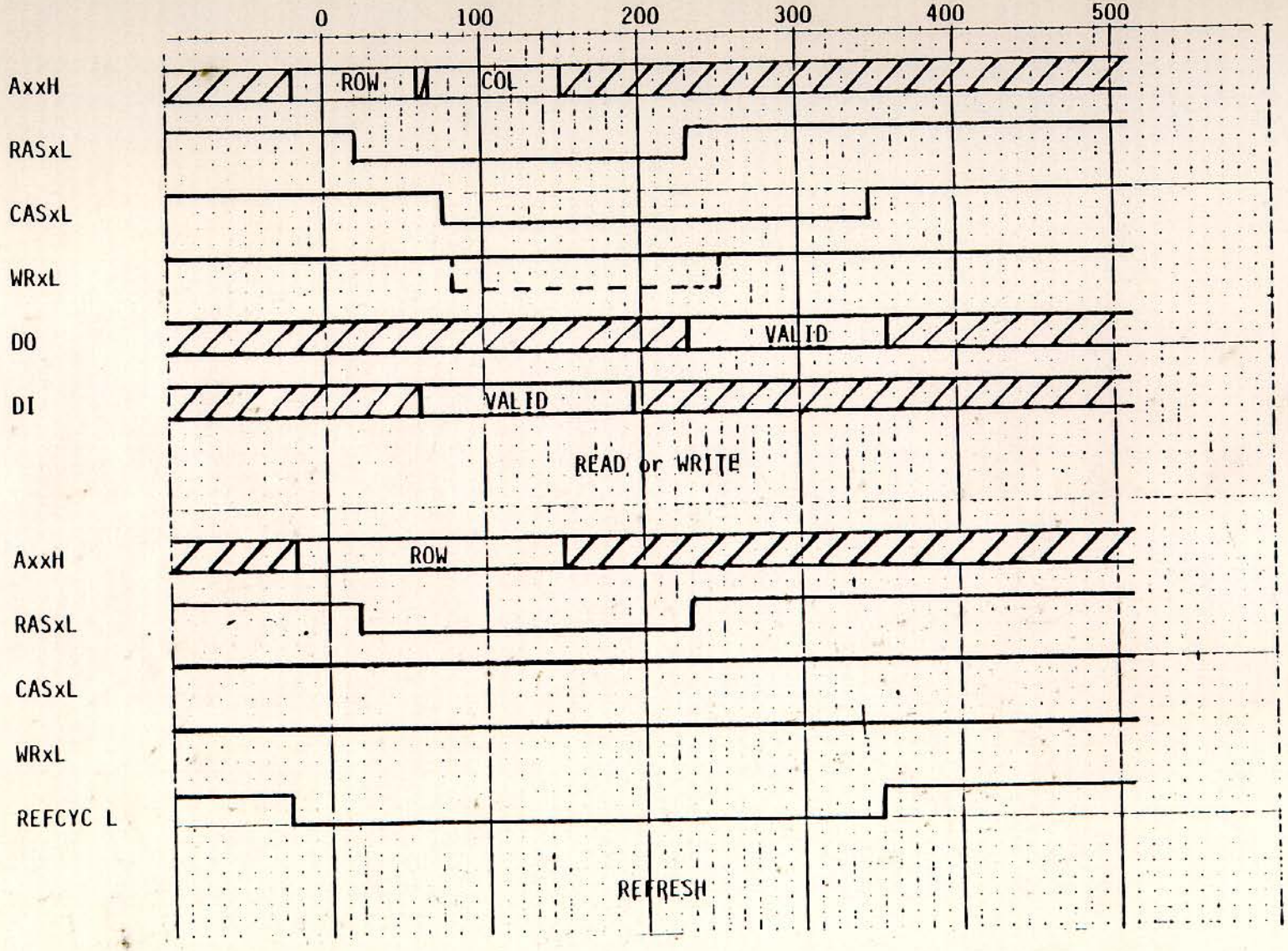
6.1.2.5 Initialize

This mode only occurs on power up. After a cold start, a power up sequence is initiated and the memory controller writes correct syndrome bits to all memory locations.



1. Dotted during Write cycle.
2. Dotted During Read cycle.
3. Read only.
4. Write only.
5. Dotted during Refresh cycle.
6. Dotted during Read or Write.

EXTERNAL BUS TIMING - FIGURE 2



DR-275

INTERNAL TIMING - FIGURE 3

7.0 PART NUMBERS/DOCUMENTATION

7.1 Part Numbers

The following part numbers have been assigned to the DR-275.

Part Number	Description
67503	DR-275 Semiconductor Memory Array 512KW + ECC

7.2 Documentation

The following documentation numbers have been assigned to the DR-275.

Schematic Drawings	-	03364
Bill of Material	-	67503
Assembly Drawing	-	67503

REV. H

DWG. NO. 67503 SHEET OF

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
XØ		PRELIMINARY RELEASE		
A		Release to Production	E.M.O.	8/27/82
B		ECN 2942	E.M.O.	10/6/82
C		ECN 2949	E.M.O.	10/6/82
D		ECN 2972A	E.M.O.	11/5/82
E		ECN 2989	E.M.O.	11/5/82
F		ECN 3002	E.M.O.	11/11/82
G		ECN 3035	E.M.O.	1/3/83
H		ECN 3076	E.M.O.	3/1/83

DRAWN	DLL
DATE	7-16-82
CHECKED	[signature]
DATE	9-8-82
ENGR.	E.M.O.
DATE	7-19-82
APPROVED	RK
DATE	9 SEP 82

TITLE

BILL OF MATERIALS

DR-275 MEMORY ARRAY 512KW + ECC (1024KB)

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 67503

SHEET 1 OF 3

REV. H

TITLE: B/M DR-275 MEMORY ARRAY 512KW + ECC (1024KB)

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	1	40803	PCB DR-175S	
2	1	18407	DIODE LED GREEN	LED1
3	1	18406	DIODE LED RED	LED2
4	13	11411	RES MDL 22 OHMS 2%	RM6,10,11,13-22
5	2	11105	RES MDL 10K OHMS 6 PIN	RM1,8
6	4	11988	RES MDL 1K OHMS 2%	RM2-5
7	2	11103	RES MDL 1K OHMS 6 PIN	RM7,9
8	1	10135	RES CC 1/4W 300 OHMS 5%	R9
9	1	10110	RES CC 1/4W 390 OHMS 5%	R13
10	2	10196	RES CC 1/4W 10 OHMS 5%	R11,12
11	1	10113	RES CC 1/4W 1K OHMS	R10
12	2	10111	RES CC 1/4W 470 OHMS 5%	R2,8
13	2	10122	RES CC 1/4W 10K OHMS 5%	R5,6
14	2	10113	RES CC 1/4W 1K OHMS 5%	R1,3
15	1	10601	RES CC 1/4W 5.1K OHMS 5%	R7
16	1	10151	RES CC 1/4W 33 OHMS 5%	R4
17	14	12102	CAP TANT 15uF 20V	C11,15-17,19-21,23,24,26-29,31
18	8	12105	CAP TANT 4.7uF 10V	C1,4,7 10,13 32,33,34
19	97	12331	CAP CER AXL .1uF -20/80%	C2,3,5,6,9,12,ROW A,B,C&D
20	1	12339	CAP CER, .47uF±20%	C14
21				NOT USED
22	1	20401	TRANSISTOR QUAD DIP	Q1
23	1	22919	SWITCH DIP SIDE ACTUATED SPST 8 ROCKERS	S1
24	1	16526	IC QUAD 2I/P NAND GATE 74503	Z1
25	156	16940	DYNAMIC RAM 64K x 1	ROW A,B,C&D
26	10	16234	IC OCTAL BUFFER/LD/LR TRI STATE 74LS240	Z13-22

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: B/M DR-275 MEMORY ARRAY 512KW + ECC (1024KB)

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
27	1	16531	IC OCTAL BUFFER/LINE DRIVER/LINE RECEIVER 74S240	Z9
28	5	16528	IC BUS DRVR/BFR 74S241	Z3-6,8
29	2	16516	IC DUAL 4I/P NAND GATE 74S20	Z10,11
30	1	16507	IC QUAD 2I/P NOR 74S02	Z2
31	1	16529	IC QUAD 2I/P NAND ST 74S132	Z7
32	1	16316	IC MONOSTABLE MV 74121	Z12
33				NOT USED
34				NOT USED
35	1	42649	STIFFENER CIRCUIT CARD DR-111	
36	4	22214	BEAD PIN	
37	2	42651	SPACER HANDLE MOUNT DR-111	
38	2	42650	HANDLE INSERTER EXTRACTOR DR-111	
39	7	26304	SCREW PNH PHL STEEL 2-56 x 5/16	
40	2	26107	NUT HEX SELF-LOCKING STEEL 2-56	
41	2	26212	WASHER BELLEVILLE SPRING 5/32	
42	A/R	30602	INK MARKING BLK	
43	REF	03364	SCHEMATIC DR-275	
44				NOT USED
45	A/R	24404	WIRE SOL GRN KYNAR #24 AWG	
46	8	11414	RES MDL 39 OHMS 2%	RM 23-30
47	1	12107	CAP TANT 2.2uf 20V	C8

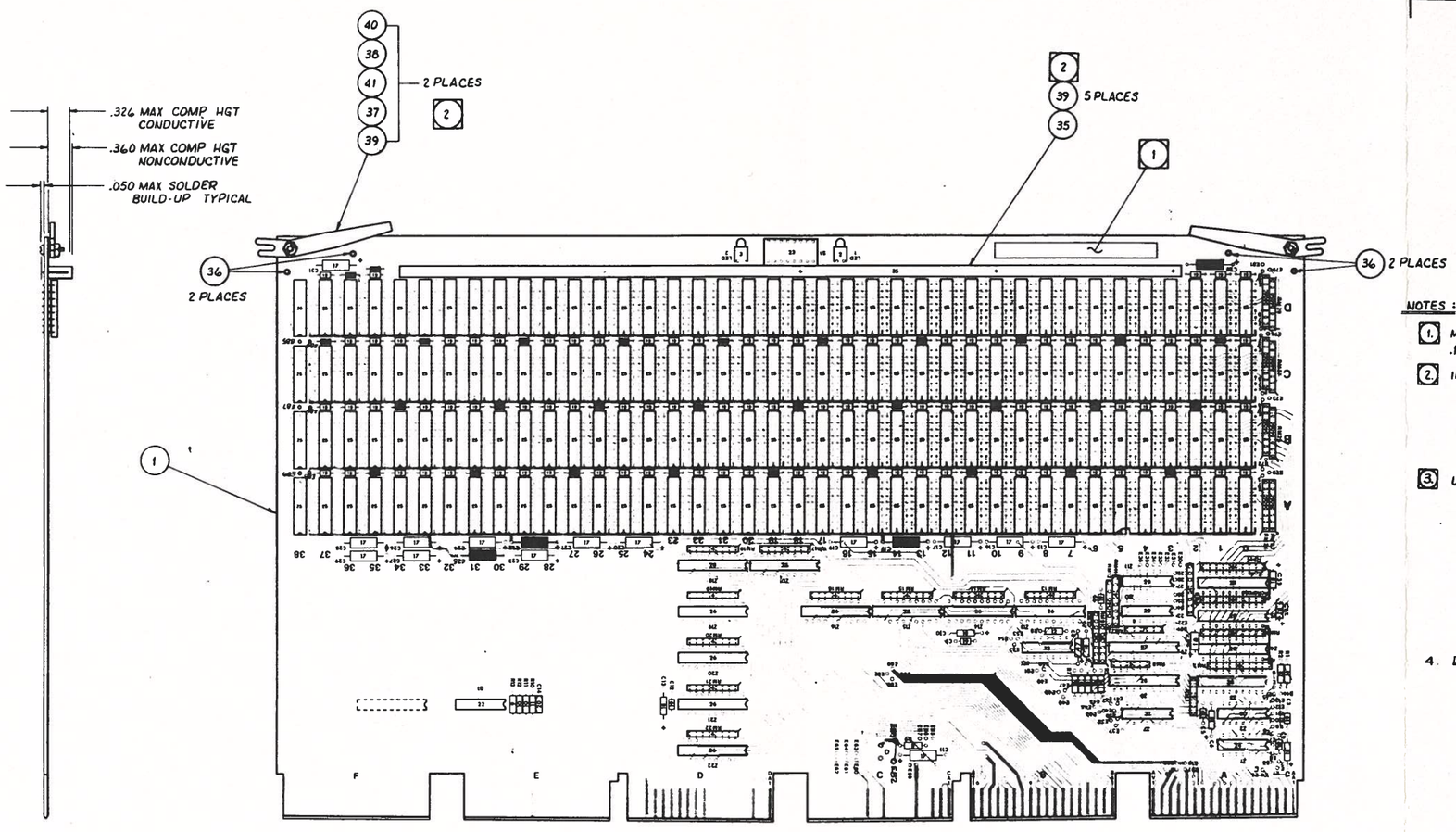
*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 67503
SHEET 3 OF 3

REV H

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION	9-9-82	E.M.O
	B	ECN 2942	10/6/82	E.M.O
	C	ECN 2949	10/6/82	E.M.O
	D	ECN 2972 A	11/5/82	E.M.O
	E	ECN 2989	11/22/82	E.M.O
	F	ECN 3002	11/12/82	E.M.O
	G	ECN 3035	1/31/83	E.M.O
	H	ECN 3076	3/11/83	E.M.O



NOTES :

1. MARK ASSY NO., REV. LEVEL, SERIAL NO. & DATE CODE WITH .12 HIGH CHARACTERS USING ITEM 42.
2. INSTALL AFTER FLOW SOLDER.
3. USING ITEM 45 INSTALL THE FOLLOWING JUMPERS

	E4 TO E5	E6 TO E7
E14 TO E15	E31 TO E32	E24 TO E25
E43 TO E45	E46 TO E48	E27 TO E28
E52 TO E54	E56 TO E57	E60 TO E63
E61 TO E64	E62 TO E65	E21 TO E22
E82 TO E83	E71 TO E72	E74 TO E75
E77 TO E78	E80 TO E79	E90 TO E92
E91 TO E93	E94 TO E96	

4. DO NOT INSTALL SHADED IN COMPONENTS.

	DR-275
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± —— DECIMALS .XX ± —— .XXX ± —— ANGLES ± ——
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. GELTCH	8-13-82
CHECKED	9-8-82
ENGR. E.M.O.	9-9-82
APPROVED R.K.	9/9/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

DR-275 MEMORY ARRAY
(256 × 39)

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	67503	H

SCALE 1/1 SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	XO	PRELIMINARY RELEASE	6/10/82	R.M.
	A	RELEASE TO PRODUCTION	9/20/82	E.R.D.
	B	ECN 2962	10/6/82	E.R.D.
	C	ECN 2989	11/5/82	E.M.D.
	D	ECN E9782	11/5/82	E.M.D.

1	A	2
INT BUS DB11 RDL	A	+5
INT BUS DB10 RDL	B	MEM PRES
INT BUS MA15 H	C	GND
INT BUS DB09 RDL	D	INT BUS MA14 H
INT BUS REFCYC(2) L	E	INT BUS ADD MEM SEL L
INT BUS DB08 RDL	F	INT BUS A02 H
INT BUS A01 H	H	INT BUS DB27 RDL
INT BUS DB26 RDL	J	INT BUS A03 H
INT BUS A00 H	K	INT BUS DB25 RDL
INT BUS DB24 RDL	L	INT BUS A06 H
INT BUS CASTIM L	M	INT BUS DREN L
INT BUS DB15 RDL	N	INT BUS WRTIM L
INT BUS A05 H	P	INT BUS DB31 RDL
+12 BATT	R	INT BUS DB14 RDL
-12 V	S	INT BUS RASTIM L
GND	T	INT BUS DB13 RDL
+12 BATT	U	INT BUS DB12 RDL
FNGP7H	V	INT BUS A04 H

1	B	2
FNGP3L	A	
FNGP5L	B	INT BUS DB29 RDL
INT BUS DB30 RDL	C	GND
+5 BATT	D	INT BUS DB28 RDL
FNGP4L	E	INT BUS DB19 RDL
INT BUS DB18 RDL	F	INT BUS DB03 RDL
INT BUS DB17 RDL	H	INT BUS DB16 RDL
INT BUS DB02 RDL	J	INT BUS DB00 RDL
INT BUS CB8 RDL	K	INT BUS DB01 RDL
INT BUS CB2 RDL	L	INT BUS CB4 RDL
FNGP6H	M	INT BUS CB1 RDL
T.P. -5	N	INT BUS A07 H
INT BUS DB07 RDL	P	INT BUS DB06 RDL
INT BUS DB05 RDL	R	INT BUS DB04 RDL
INT BUS DB23 RDL	S	INT BUS DB22 RDL
GND	T	INT BUS DB21 RDL
INT BUS DB20 RDL	U	INT BUS CBT RDL
INT BUS CB32 RDL	V	INT BUS CB16 RDL

1	C	2
NP6 SO	A	
NP6 OUT	B	
	C	GND (-5)
	D	
T.P. -5	E	
	F	
	H	
	J	
FNGP1L	K	
	L	
FNGP2L	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	

1	D	2
	A	+5
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	B6 7 SO
	L	B6 7 OUT
	M	B6 6 SO
	N	B6 6 OUT
	P	B6 5 SO
	R	B6 5 OUT
	S	B6 4 SO
	T	B6 4 OUT
	U	
	V	
GND		

1	E	2
	A	
	B	
	C	
	D	
	E	
	F	
	H	
	J	
	K	
	L	T.P. TERM
	M	
	N	
	P	
	R	
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	U	
	V	

1	F	2
	A	
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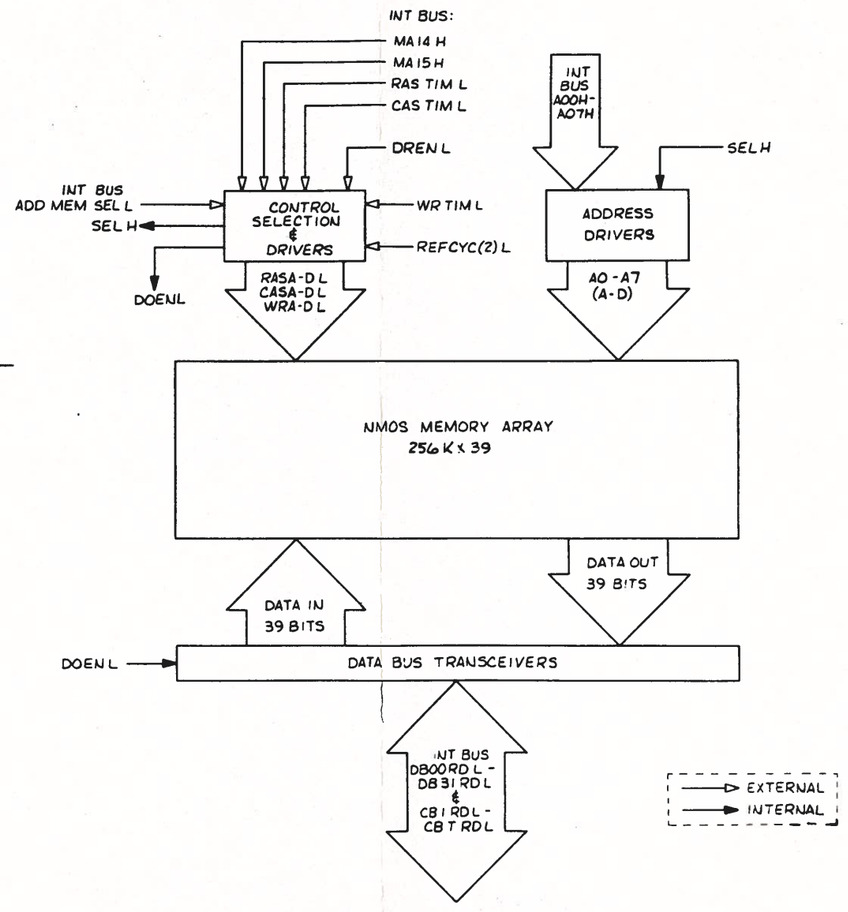


LAST REFERANCE USED	
INTEGRATED CIRCUIT	Z22
RESISTOR MODULE	RM30
RESISTOR	R13
CAPACITOR	C31
TRANSISTOR	Q1
LED	LED2
SWITCH	S1
JUMPER PIN	E89

REF.	USED GATES/TOTAL	TYPE
Z1	2/4	74S03
Z2	3/4	74S02
Z7	3/4	74S132
Z8	7/8	74S241
Z22	6/8	74LS240

1. ALL RESISTORS ARE CARBON COMPOSITION, 1/4 WATT ± 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

	DR-275
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

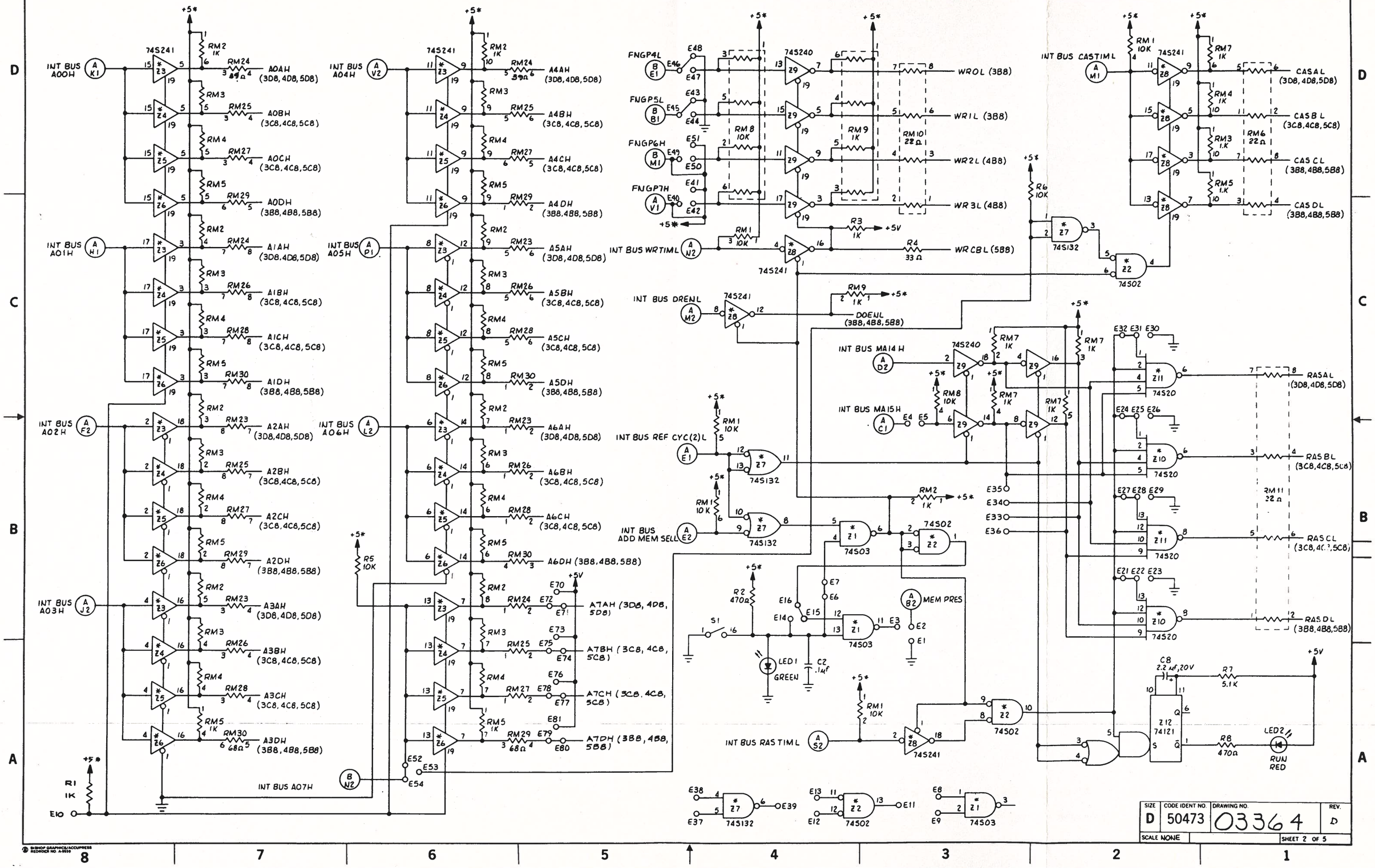
APPROVALS	DATE
DRAWN R. MENDOZA	7-19-82
CHECKED	9-20-82
ENG	9-14-82
APPROVED	10/5/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

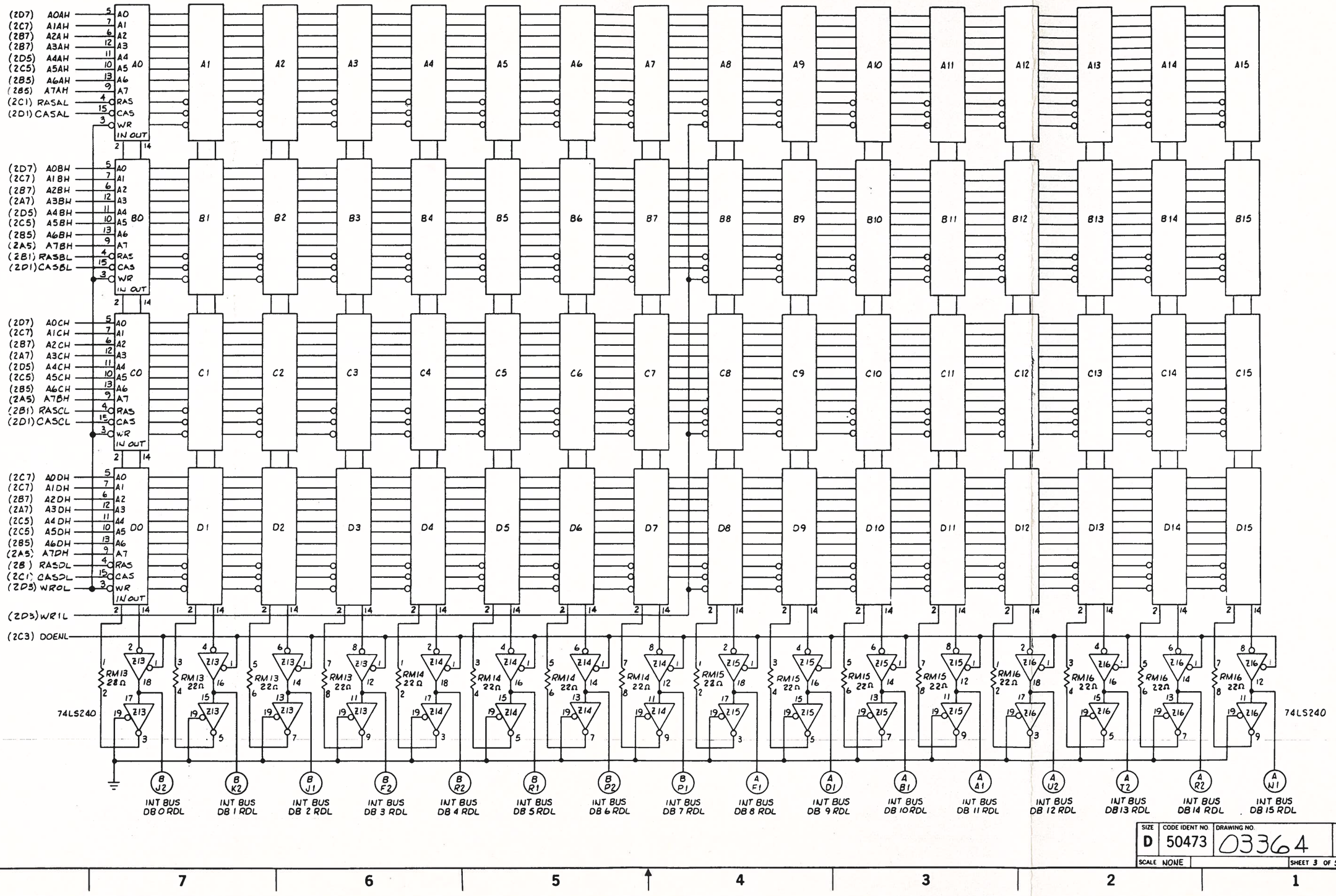
SCHEMATIC DR-275
MEMORY ARRAY
512KW + ECC (1MB)

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03364	D

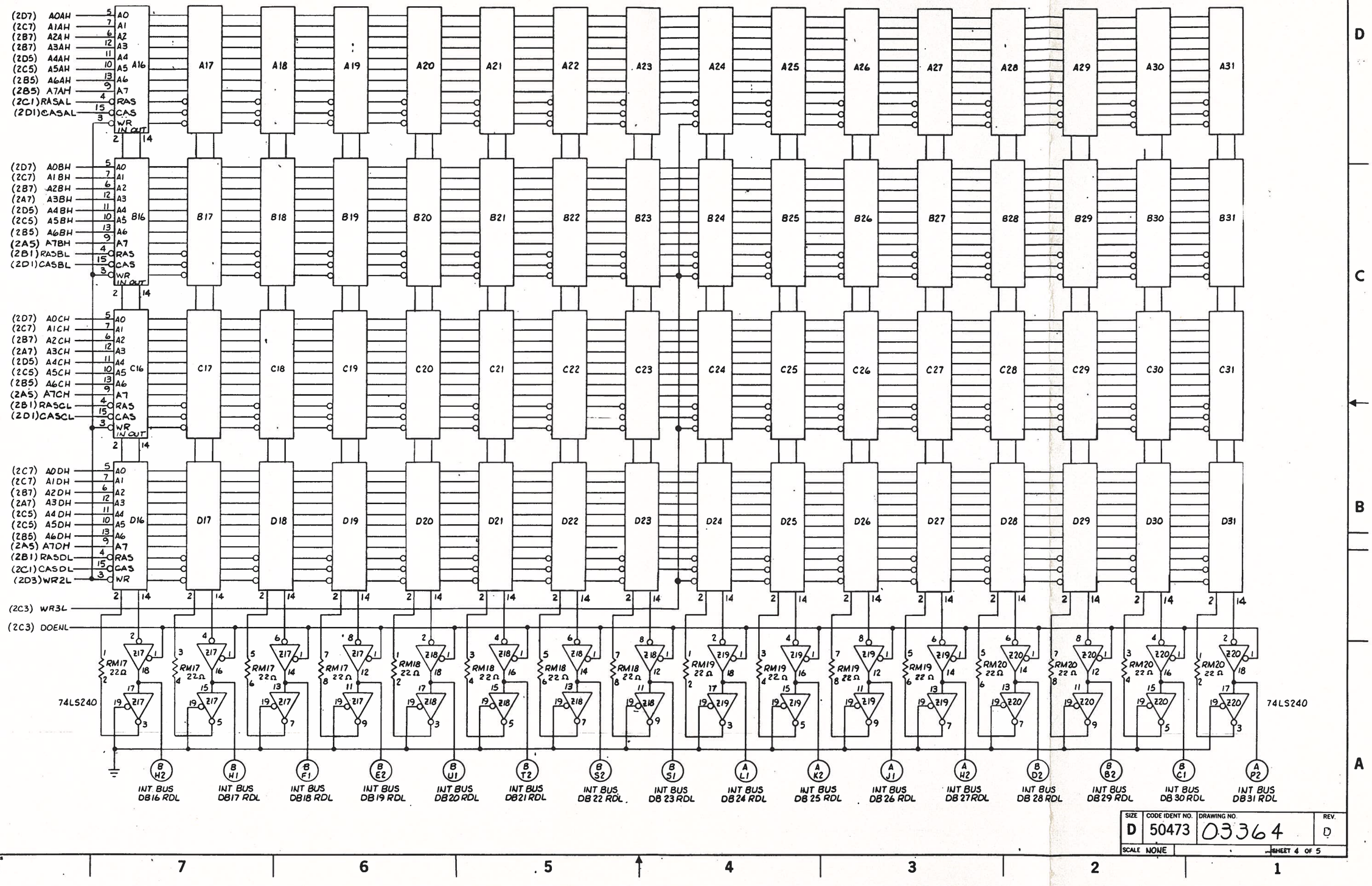
SCALE NONE SHEET 1 OF 5



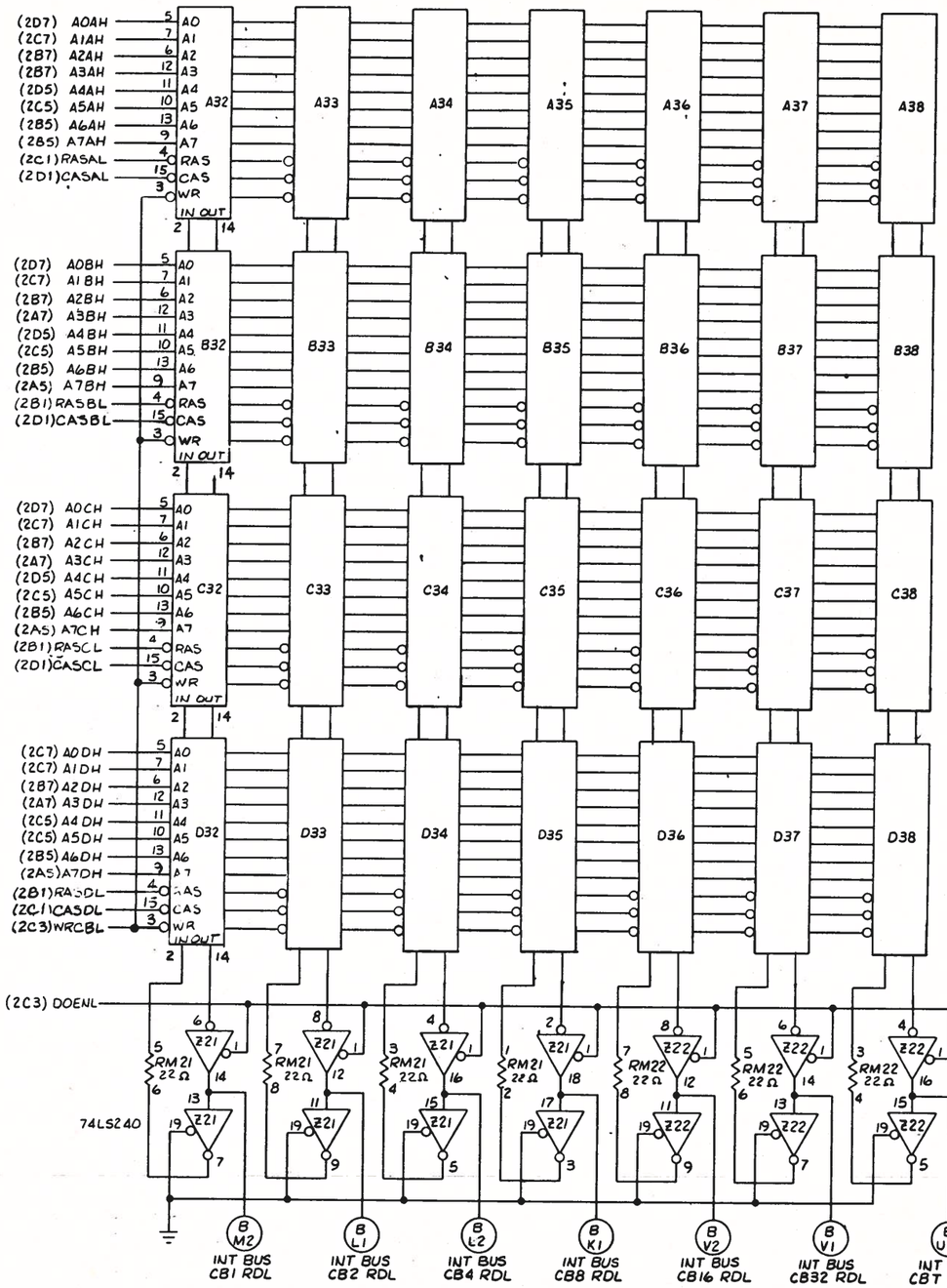
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03364	D
SCALE NONE		SHEET 2 OF 5	

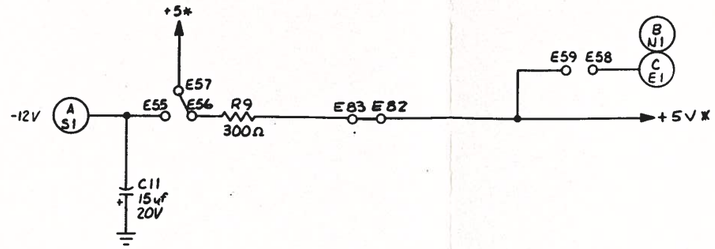


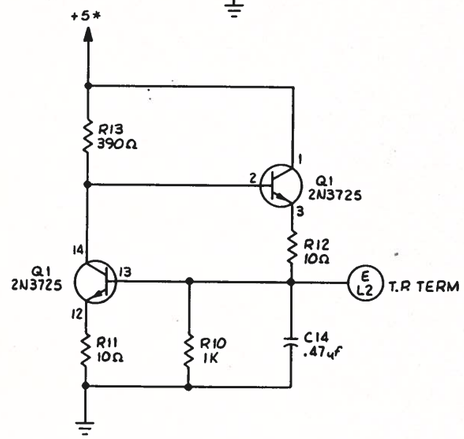
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03364	D
SCALE NONE		SHEET 3 OF 5	

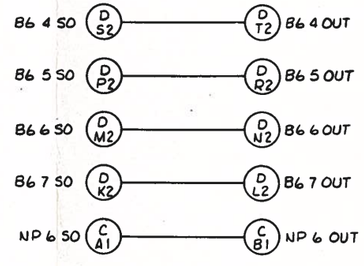


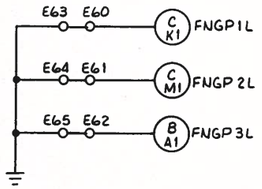
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03364	D
SCALE NONE		SHEET 4 OF 5	



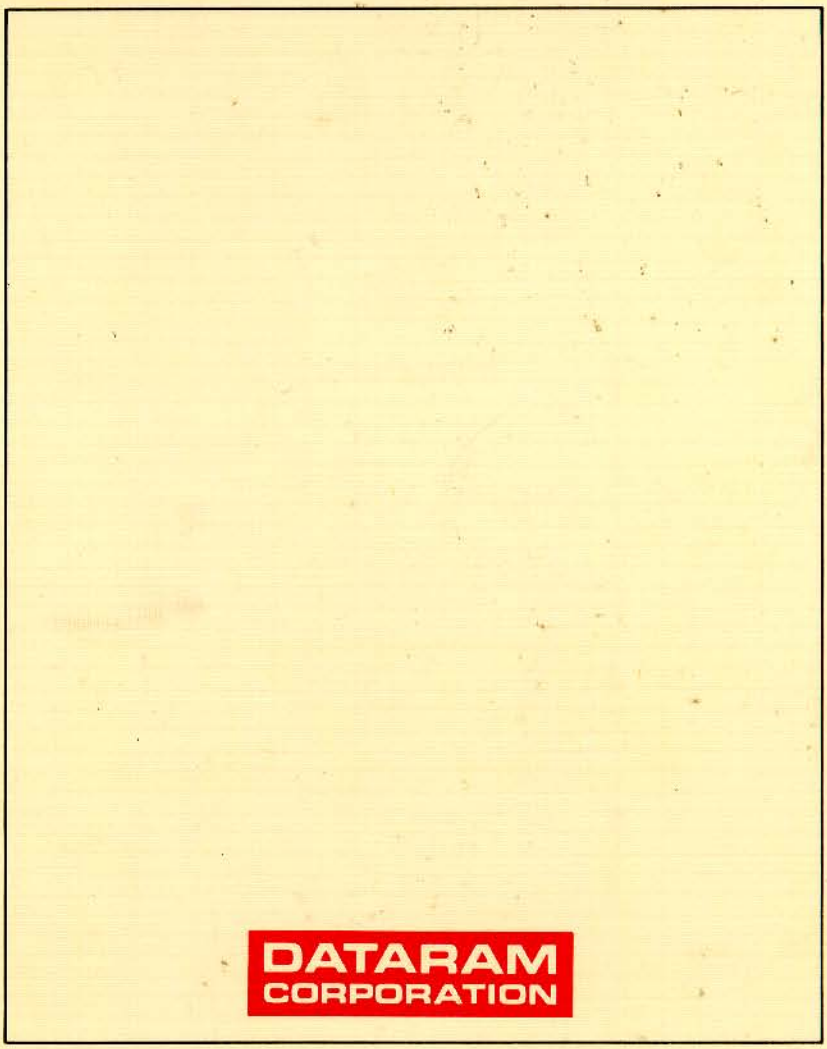








SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03364	D
SCALE NONE			SHEET 5 OF 5



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