BULK SEMI MEMORY SYSTEM

MODEL DR-129/229S

DATARAM
CORPORATION

BULK SEMI MEMORY SYSTEM

MODEL DR-129/229S

06067

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1.0 GENERAL

The DR-129/229S consists of a Bulk Semiconductor Control (BSC) board and from 1 to 16 Bulk Semiconductor Array (BSA) boards. The DR-129S memory system uses 16K dynamic RAM devices, while the DR-229S uses 64K dynamic RAM's. Each DR-129S Bulk Semiconductor Array (BSA) board contains 512K bytes of storage using 16K NMOS semiconductor memory chips. The maximum system capacity is 8 megabytes (16 BSA boards). Each DR-229S Bulk Semiconductor Array (BSA) board contains 2 megabytes of storage using 64K NMOS semiconductor memory chips. The maximum system capacity is 32 megabytes (16 BSA boards). The identical Bulk Semiconductor Controller is used for 16K or 64K RAM's and is strapped accordingly.

DR-129S BSA (16K RAM) boards and DR-229S BSA (64K RAM) boards may not be intermixed in the same system.

Each DR-129/229S BSA board contains Error Correcting Code (ECC) storage and the BSC board contains ECC circuitry to correct all single bit errors and detect all double bit errors which may occur during operation of the system. In addition, error logging circuitry to record up to 64 memory error locations is contained on the BSC board. The error log may be directly examined from the memory bus and when used in conjunction with a Dataram BULK SEMI chassis provides information for an error log display.

The DR-129/229S may be configured as either an 18-bit word or a 36-bit word memory system by installation of wirewrap jumpers on the BSC board.

The DR-129/229S memory system is electrically compatible to the Dataram BULK CORE (DR-128) memory system and will work with all Dataram BULK CORE Interface (BI) modules. The DR-129/229S interface is via a handshake asynchronous bus through an exchange of request and status signals. This allows convenient access to the memory for a variety of users, both fast and slow.

1.1 Bulk Semiconductor Control (BSC) Board

The BSC contains all necessary logic to drive up to 16 BSA boards. This logic consists of the following circuitry:

1. Timing and Control
2. Data Registers
3. Address Registers
4. ECC Generating & Checking Logic
5. Error Logging Storage & Display Control Logic
6. Refresh Circuits

The data input/output circuitry can be configured to provide either an 18 or 36 bit interface.

1.2 Bulk Semiconductor Array (BSA) Board

The DR-129S BSA Board is configured as a 128K x 43 bit memory array and the DR-229S BSA Board is configured as 512K x 43 bits. The 43-bit word length consists of 36 bits of data and 7 bits of ECC storage. A 39-bit version (32 data and 7 ECC) is also available. The BSA consists of 344 16K or 64K NMOS semiconductor memory chips, row/column address drivers and data buffers. Also included is inverter circuitry to generate -5 volts for the 16K semiconductor chips.

2.0 ELECTRICAL SPECIFICATIONS

2.1 System Characteristics

2.1.1 Size

DR-129S: 512K bytes expandable to 8 megabytes in 512K byte increments. A 512K byte system may be configured as 128K x 36 or 256K x 18 bits with maximum capacity of either 2048K x 36 or 4096K x 18.

DR-229S: 2 megabytes expandable to 32 megabytes in 2 megabyte increments. A 2 megabyte system may be configured as 512K x 36 or 1024K x 18 bits with maximum capacity of either 8192K x 36 or 16,384K x 18.

Multiple Systems:

With the 25 bit addressing capability of the DR-129/229S, multiple systems may be daisychained to obtain maximum capacities of 128 megabytes using a 36 bit word or 64 megabytes using an 18 bit word.

2.1.2 Modes and Cycle Time

Cycle time differs for various modes of operation.

2.1.2.1 18 Bit Configuration

*Includes 75 nanoseconds Read-Modify-Time

Mode	Minimum Cycle Time (nsec)
Read Word	550
Read Even Number of Sequential Words	400 (avg)
Write Word	700
Write Either Byte	700
Read Word/Modify/Write Word	900*
Read Word/Modify/Write Either Byte	900*

2.1.2.2 36 Bit (Double Word) Configuration

Mode	Minimum Cycle Time (nsec)
Read Double Word	550
Write Double Word	550
Write Any Byte or Bytes	700
Read Double Word/Modify/Write Double Word	900*
Read Double Word/Modify/Write Any Byte(s)	900*

*Includes 75 nanoseconds Read/Modify Time

2.1.2.3 Refresh

An additional mode, Refresh, is necessary to prevent loss of data stored in the NMOS storage chips. NMOS Random Access Memory (RAM) devices store data on the gate capacitance of a field-effect transistor. A "1" is stored as the presence of a charge and a "0" is stored as the absence of a charge. The stored charge tends to deteriorate and must be renewed at least every two milliseconds.

Refresh cycle time is 700 nanoseconds. When ADRAVN is sent to the memory during a Refresh cycle, the memory cycle and access times may be extended by up to 700 nanoseconds.

2.1.3 Access Time

For an even number of sequential words (18 bit), access time is 260 nanoseconds average. For all other modes, access time is 400 nanoseconds maximum.

2.1.4 Voltage and Current Requirements

The BSC board uses +5 volts and +15 volts. The DR-129S BSA board uses +5 volts and +15 volts while the DR-229S BSA board only uses +5 volts. Separate inputs for battery backup to support memory refresh at reduced current during primary power failure are provided.

DR-129S

Voltage ±5%	Current Max. Amps Operating	Standby
BSC +5V Total	10.1	9.8
BSC +5V BBU	.95	.9
BSC +15V	.1	.1
BSC +15V BBU	.1	.1
BSA +5V Total	1.2	.86
BSA +5V BBU	.55	.41
BSA +15V	.95	.45
BSA +15V BBU	.95	.45

DR-229S

Voltage ±5%	Current Max. Amps Operating	Standby
BSC +5V Total	10.1	9.8
BSC +5V BBU	.95	.9
BSC +15V	.1	.1
BSC +15V BBU	.1	.1
BSA +5V Total	3.5	2.4
BSA +5V BBU	2.8	1.9

2.2 Input/Output Signal Lines

MNEMONIC	DESCRIPTION	NO. OF LINES	INPUT/ OUTPUT	LOAD/ DRIVE
ADRAVN	Address Available	1	IN	1 S
ADRACN	Address Accepted	1	OUT	74S38
ADROON-ADR24N	Memory Address	25	IN	1 LS
RADVLDN	Response Address Valid (Data Clock)	1	IN	1 S
DTAOON-DTA35N	Memory Data (Bidirectional)	36	IN/OUT	1 LS/1 74S38
ODAVN	Output Data Available	1	OUT	74S38
IDACN	Input Data Accepted	1	OUT	74S38
MRDRN	Memory Read	1	IN	1 LS
MWRLBN	Memory Write Lower Byte, Lower Word	1	IN	1 LS
MWRUBN	Memory Write Upper Byte, Lower Word	1	IN	1 LS
MWRLBAN	Memory Write Lower Byte, Upper Word	1	IN	1 LS
MWRUBAN	Memory Write Upper Byte, Upper Word	1	IN	1 LS
MEMSIZO-MEMSIZ6	Memory Size	7	OUT	74S38
PWRINTN	Power Interrupt	1	IN	1 S
NORMN	Normalize	1	IN	1 TTL
CRERN	Correctable Error	1	OUT	74S38
UCERN	Uncorrectable Error	1	OUT	74S38
STATN	Status	1	IN	1 S
STAVN	Status Available	1	OUT	74S38
MBYN	Memory Busy	1	OUT	74S38
CLRBYN	Clear Busy	1	OUT	74S38
LGFUL	Logful	1	OUT	74S74
ERR	Error	1	OUT	74121
BGN	Begin Log	1	IN	1 S
CLRN	Clear Log	1	IN	1 TTL
EXAMN	Examine Log	1	IN	1 S

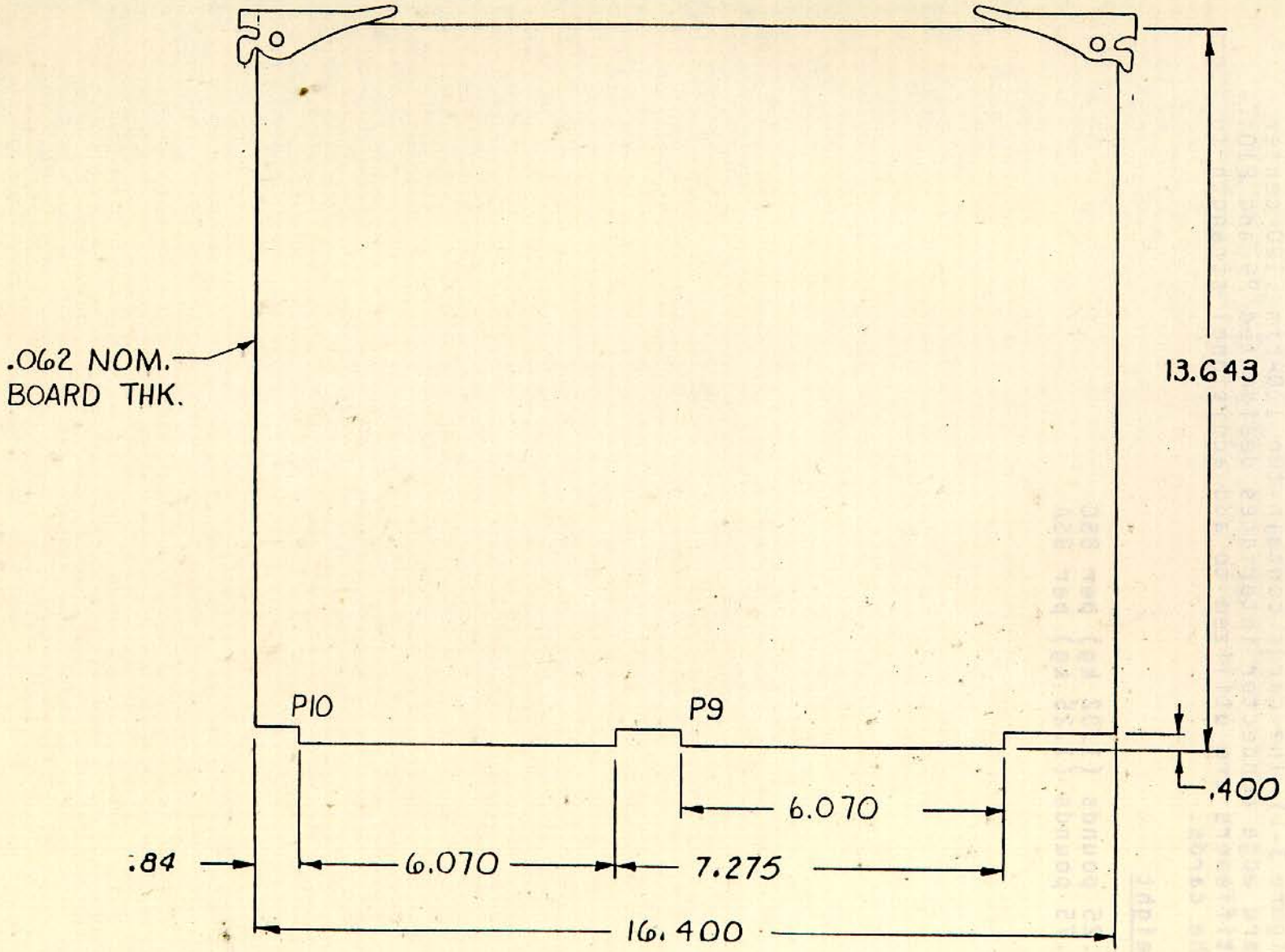
3.0 MECHANICAL SPECIFICATIONS

3.1 Dimensions

The BSA and BSC cards measure 13.64" x 16.4" and are designed to fit on a minimum of 0.75 inch centers. (See Figure 3-1). The cards contain two 120-pin .100 center card edge connector interfaces designated P9 and P10. Stiffeners are utilized to add additional strength to the cards.

3.2 Weight

2.25 pounds (1.02 kg) per BSC
2.75 pounds (1.25 kg) per BSA



MECHANICAL OUTLINE
BULK SEMICONDUCTOR MODULE
FIGURE 3.1

4.0 ENVIRONMENTAL SPECIFICATIONS

4.1 Cooling

BSC	50cfm
BSA (each)	15cfm

4.2 Storage Temperature

-40°C to +80°C

4.3 Operating Temperature

0°C to +55°C

4.4 Relative Humidity

Up to 95% without condensation

4.5 Altitude

Up to 10,000 feet above mean sea level - operating
Up to 40,000 feet above mean sea level - storage

4.6 Vibration

Will withstand normal stresses encountered in transport.

5.0 ORDERING INFORMATION

The following part numbers have been assigned to the DR-129/229S:

62904	DR-129/229S BULK SEMI Controller (BSC)	36 Bit
62901	DR-129/229S BULK SEMI Controller (BSC)	18 Bit
62902	DR-129S BULK SEMI Array (BSA)	128K x 43
62907	DR-129S BULK SEMI Array (BSA)	128K x 39
62981	DR-229S BULK SEMI Array (BSA)	512K x 43
62982	DR-229S BULK SEMI Array (BSA)	512K x 39

6.0 INSTALLATION AND OPERATION

The DR-129/229S is installed in the Dataram 7" or 15-3/4" BULK SEMI chassis for operation with Dataram or user designed memory interfaces. The appropriate BULK SEMI chassis manuals cover installation instructions. Careful review of the theory of operation and the schematics in this manual will aid in troubleshooting the memory.

The DR-129/229S BSC has many configurations and option jumpers. These are listed on Sheet 2 of Schematic 03191. These jumpers should be checked carefully to ensure that the BSC is configured properly for the application.

7.0 THEORY OF OPERATION

In the following sections, all signal levels from 0.0VDC to +0.8VDC will be referred to as a low and all signal levels from +2.4VDC to +5.2VDC will be referred to as a high. If the last letter of a signal mnemonic is the letter "N", this signal is low true asserting. If the last letter is not an "N", the signal is high true asserting. Discussion of operation will refer to schematics 03191 and 03333 contained in the rear of this manual.

7.1 General Description

Refer to Block Diagrams Sheet 1 of 03191 and Sheet 1 of 03333.

7.1.1 Memory Bus

The DR-129/229S consists of a BULK SEMI Controller and up to 16 BULK SEMI Array (BSA) boards. All boards are identical in size and contain two card edge printed circuit connectors identified as P9 and P10. All interface between the memory system and the outside world occurs on connector P9 of the BSC. This interface is defined as the memory bus and consists of all data, address, control and command signals to the memory. The BSC, acting on command and control signals from the memory bus temporarily stores data and address signals and forwards data for storage at the appropriate location in the dynamic RAM's on the BSA board. All communication between the BSC and the BSA boards occurs between connector P10 of the BSC and connectors P9 and P10 of the BSA boards. This path is defined as the array bus. Figure 7.1 depicts the paths of communication for the memory bus and the array bus. The signals on the memory bus at connector P9 of the BSC are defined as follows:

Address Available (ADRAVN)

ADRAVN initiates the start of a Read, Write or Read/Modify/Write cycle. The command must be a low and remain low until the assertion of ADRACN.

Address Accepted (ADRACN)

ADRACN is asserted to indicate that the addressed memory modules have accepted the address and cycle control information which is validated by ADRAVN. This information may go invalid when ADRAVN goes false. If there is no Refresh contention, ADRACN will go true within 780 nanoseconds of the receipt of ADRAVN. The ADRACN output is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

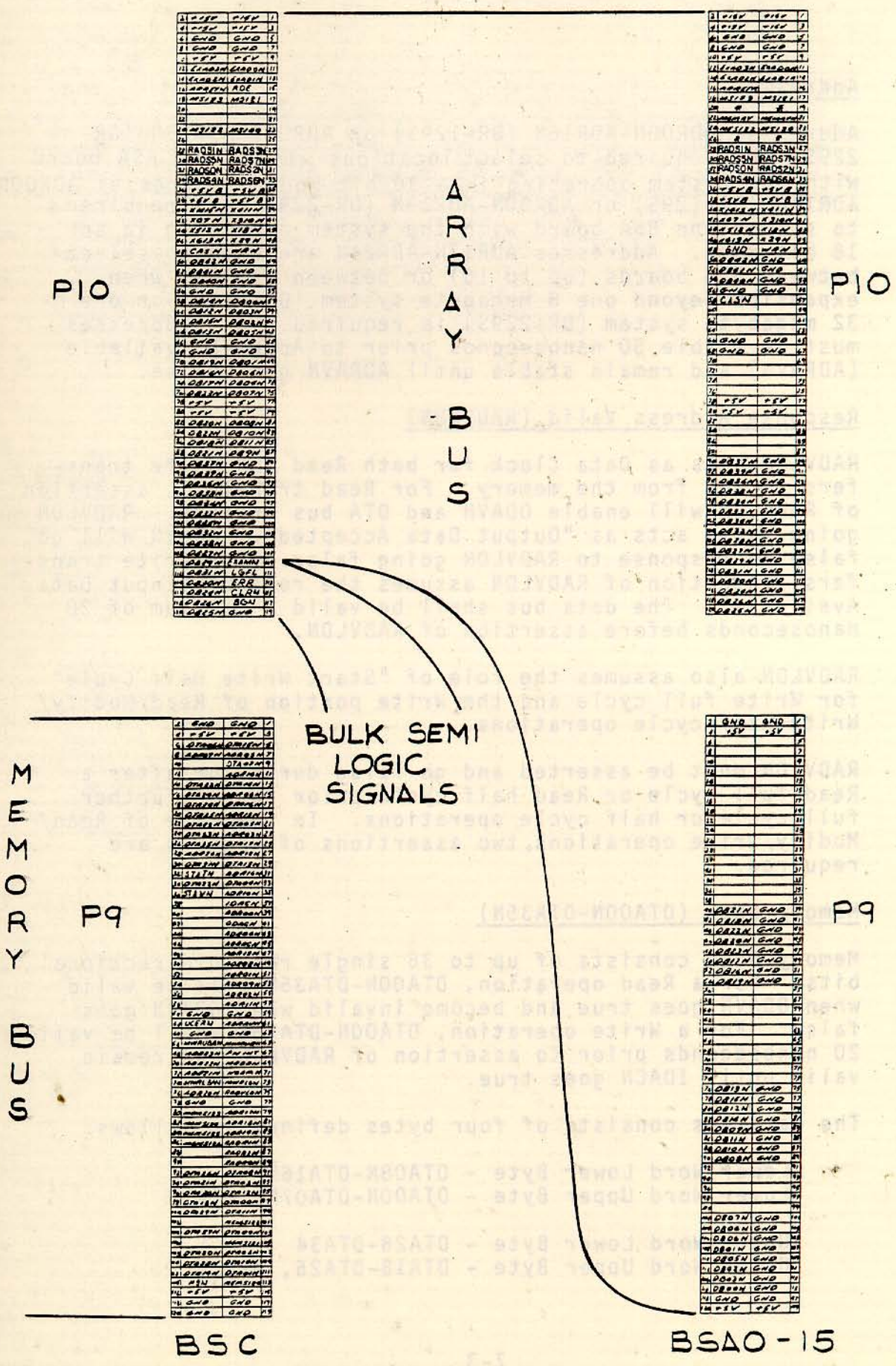

P10
ARRAY BUS
P10
MEMORY BUS
P9
BULK SEMI LOGIC SIGNALS
P9
BSC
BSA0-15

FIG 7.1

Addresses

Addresses ADR00N-ADR16N (DR-129S) or ADR00N-ADR18N (DR-229S) are required to select locations within one BSA board with the system operating in a 36 bit mode. Addresses ADR00N-ADR17N (DR-129S) or ADR00N-ADR19N (DR-229S) are required to select one BSA board with the system operating in an 18 bit mode. Addresses ADR17N-ADR24N are used to select between BSA boards (up to 16) or between systems when expansion beyond one 8 megabyte system (DR-129S) or one 32 megabyte system (DR-229S) is required. All addresses must be stable 50 nanoseconds prior to Address Available (ADRAVN) and remain stable until ADRAVN goes false.

Response Address Valid (RADVLDN)

RADVLDN acts as Data Clock for both Read and Write transfers to and from the memory. For Read transfers, assertion of RADVLDN will enable ODAVN and DTA bus drivers. RADVLDN going false acts as "Output Data Accepted". ODAVN will go false in response to RADVLDN going false. For Write transfers, assertion of RADVLDN assumes the role of "Input Data Available". The data bus shall be valid a minimum of 20 nanoseconds before assertion of RADVLDN.

RADVLDN also assumes the role of "Start Write Half Cycle" for Write full cycle and the Write portion of Read/Modify/Write half cycle operations.

RADVLDN must be asserted and go false during or after a Read full cycle or Read half cycle prior to any further full cycle or half cycle operations. In the case of Read/Modify/Write operations, two assertions of RADVLDN are required.

Memory Data (DTA00N-DTA35N)

Memory Data consists of up to 36 single rail bidirectional bits. For a Read operation, DTA00N-DTA35N will be valid when ODAVN goes true and become invalid when ODAVN goes false. For a Write operation, DTA00N-DTA35N shall be valid 20 nanoseconds prior to assertion of RADVLDN and remain valid until IDACN goes true.

The data bus consists of four bytes defined as follows:

Lower Word Lower Byte - DTA08N-DTA16N
Lower Word Upper Byte - DTA00N-DTA07N, DTA17

Upper Word Lower Byte - DTA26-DTA34
Upper Word Upper Byte - DTA18-DTA25, DTA35

Data bus is non-inverting (a low written into memory results in a low read from memory) and is low-true. Data outputs are derived from 74S38 open collector gates and shall be pulled-up at the receiving end.

For an 18 bit configuration, upper word data bits are internally wired in parallel with the lower data bits. Address ADR00N is then used to control selection of upper or lower words.

Data bits DTA00N-DTA15N are also used to provide error log information when enabled by the signal STATN or EXAMN. The memory chip in error is defined as follows:

BSA Board Number	DTA03N-DAT06N
Chip Row Number	DTA00N-DTA02N
Exact Bit in Error	DTA07N-DTA12N
Uncorrectable Error	DTA13N
Log Location Empty	DTA14N
Correctable Error	DTA15N

Output Data Available (ODAVN)

Assertion of ODAVN indicates that output data is valid and will remain valid until RADVLDN goes false. During a Read operation when RADVLDN is true, ODAVN will go true no later than 400 nonoseconds from ADRAVN and will go false after RADVLDN goes false. (See Figures 7.2, 7.3, and 7.6.) ODAVN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

Input Data Accepted (IDACN)

Assertion of IDACN by the memory module indicates that input data validated by RADVLDN has been accepted. IDACN will go true after RADVLDN goes true and will go false after RADVLDN goes false. (See Figures 7.4, 7.5 and 7.6.)

IDACN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

Cycle Control Lines
(MRDRN, MWRLBN, MWRUBN, MWRLBAN, MWRUBAN)

The cycle control lines, Memory Read (MRDRN), Memory Write Lower Byte (MWRLBN), Memory Write Upper Byte (MWRUBN), Memory Write Lower Byte Upper Word (MWRLBAN) and Memory Write Upper Byte Upper Word (MWRUBAN) are used to control the various Read/Write modes of operation. MRDRN, MWRLBN and MWRUBN shall be valid 50 nanoseconds prior to ADRAVN and remain valid until ADRAVN goes false. Tables 7.1 and 7.2 define the various modes of operation for all combinations of MRDRN, MWRLBN, MWRUBN, MWRLBAN and MWRUBAN.

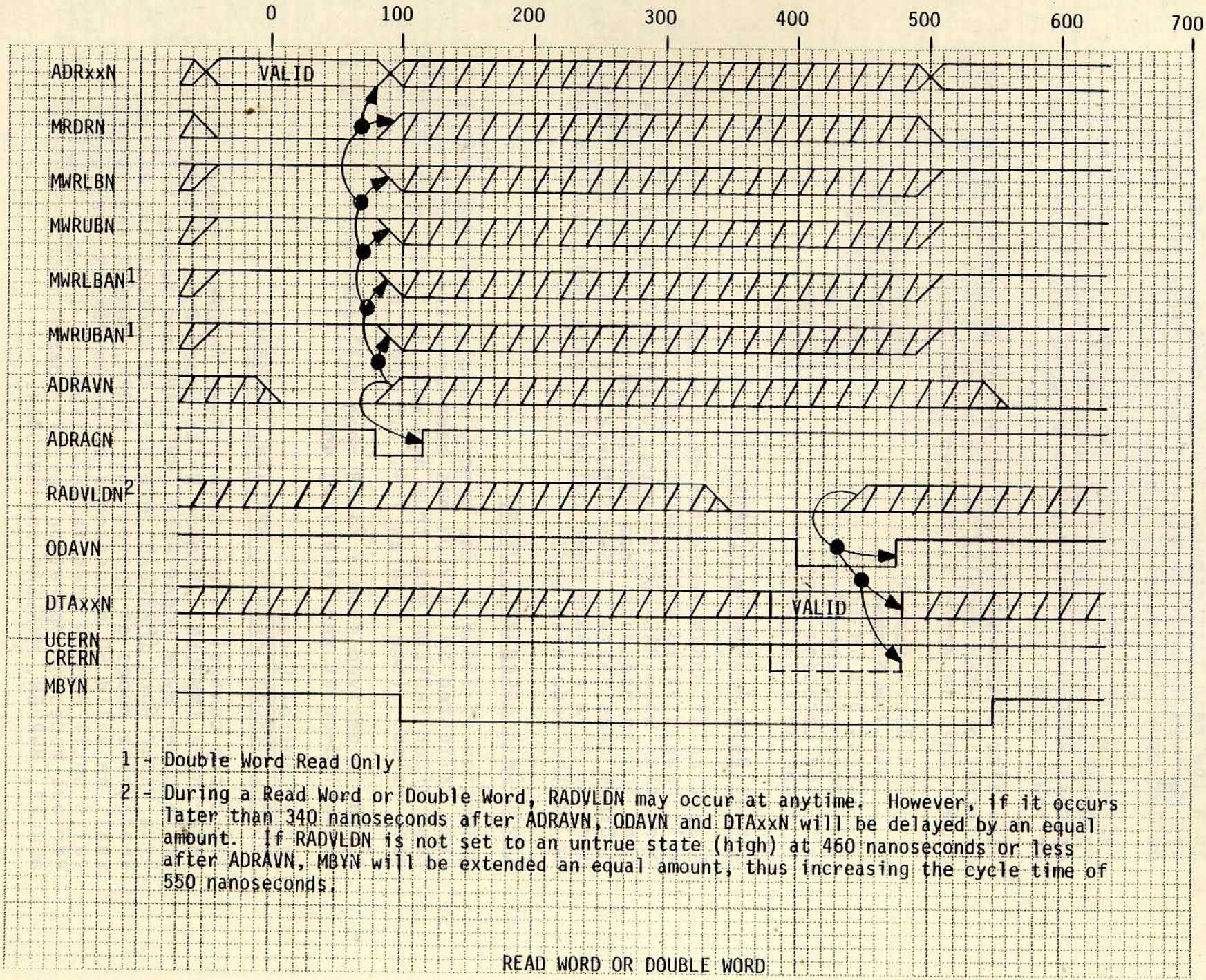
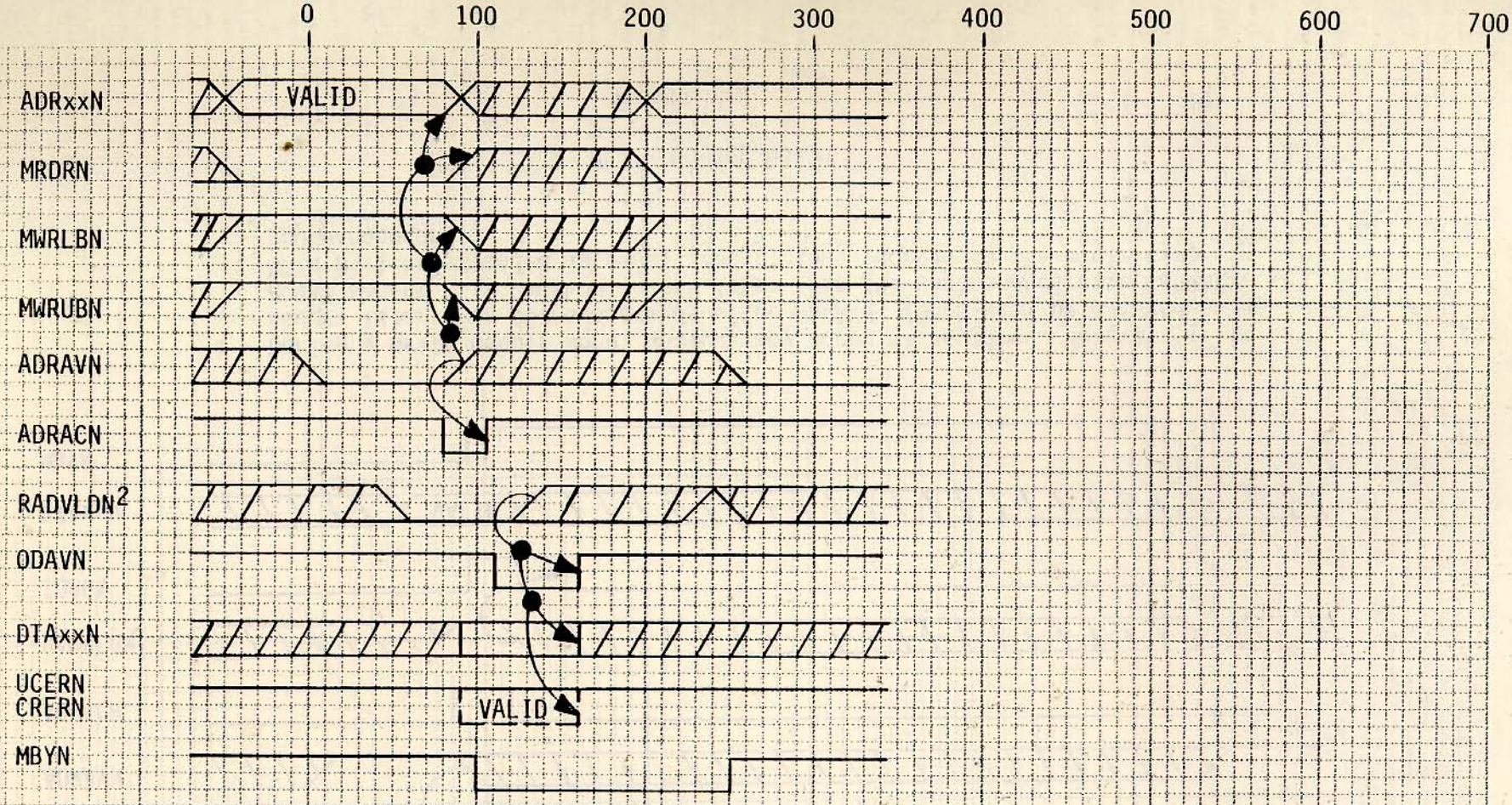

0
100
200
300
400
500
600
700
ADRxxN
VALID
MRDRN
MWRLBN
MWRUBN
MWRLBAN1
MWRUBAN1
ADRAVN
ADRACN
RADVLDN2
ODAVN
DTAxxN
VALID
UCERN
CRERN
MBYN
1 - Double Word Read Only
2 - During a Read Word or Double Word, RADVLDN may occur at anytime. However, if it occurs later than 340 nanoseconds after ADRAVN, ODAVN and DTAxxN will be delayed by an equal amount. If RADVLDN is not set to an untrue state (high) at 460 nanoseconds or less after ADRAVN, MBYN will be extended an equal amount, thus increasing the cycle time of 550 nanoseconds.
READ WORD OR DOUBLE WORD

FIGURE 7.2

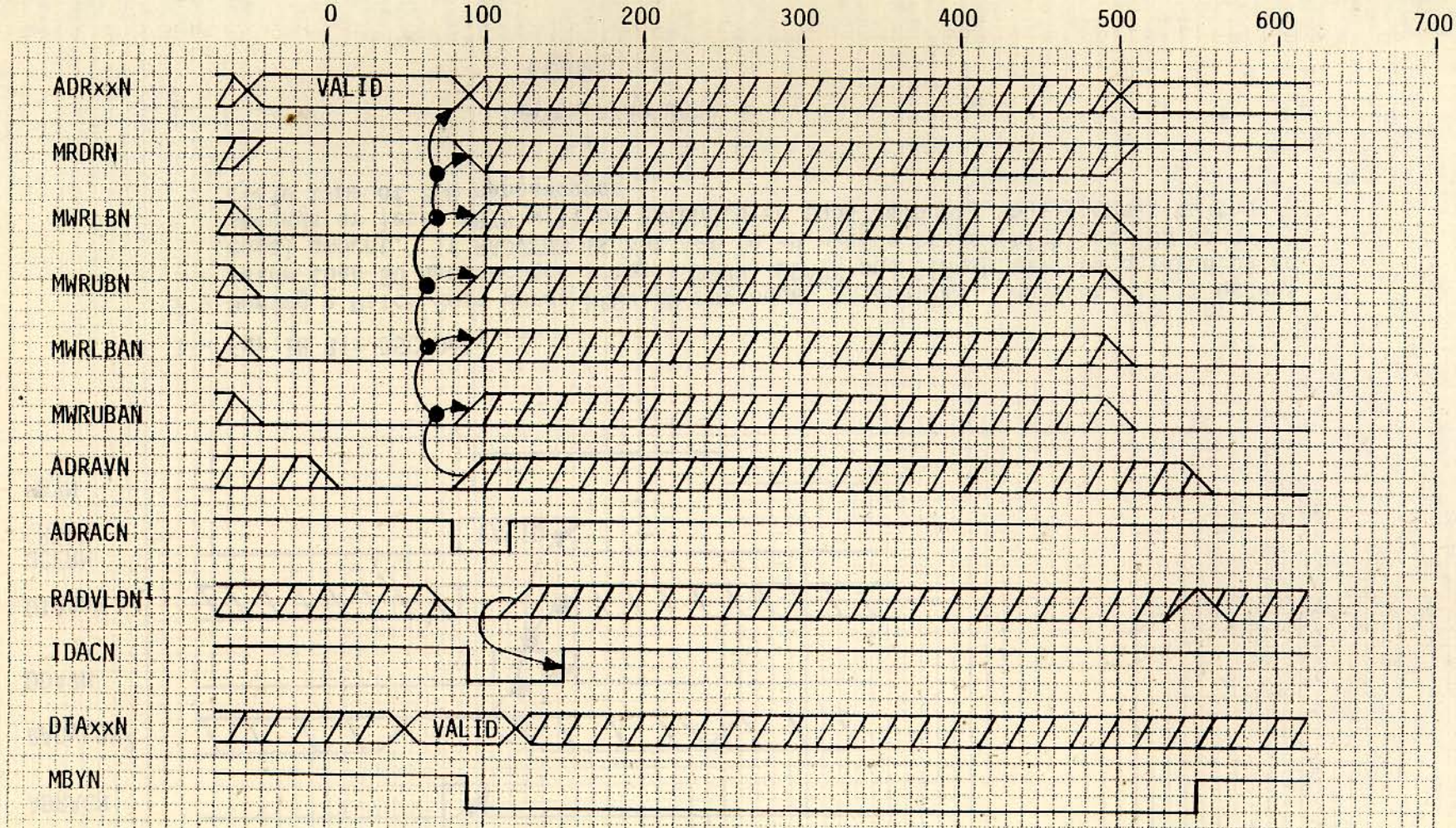


1 - For 18 Bit BSC Only

2 - During a Match Read Word, RADVLDN may occur at anytime. However, if it occurs later than 50 nanoseconds after ADRAVN, ODAVN and DTAxxN will be delayed by an equal amount. If RADVLDN is not set to an untrue state (high) at 130 nanoseconds or less, MBYN will be extended an equal amount, thus increasing the cycle time of 250 nanoseconds.

MATCH READ WORD

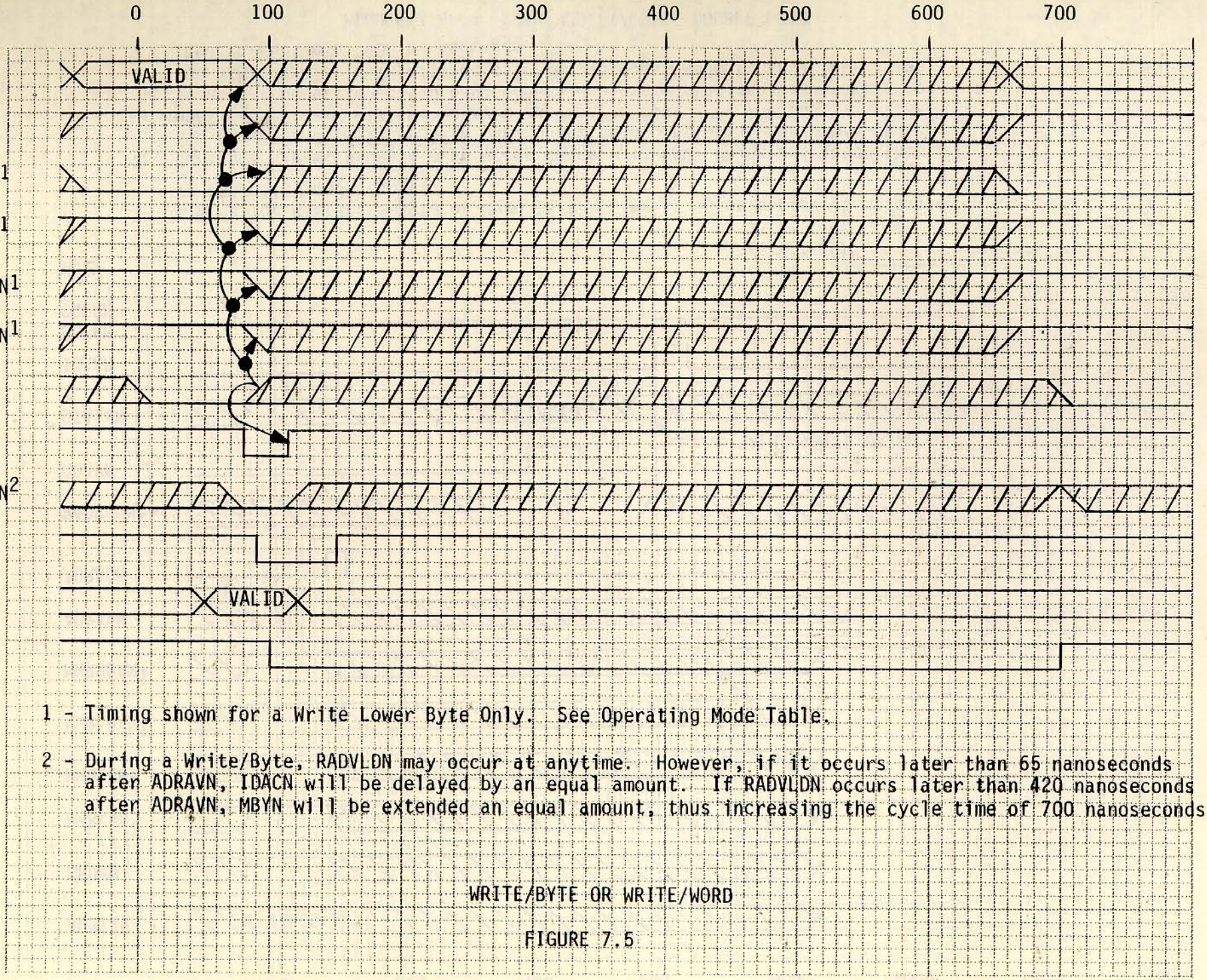
FIGURE 7.3



1 - During a Write Double Word, RADVLDN may occur at anytime. However, if it occurs later than 65 nanoseconds after ADRAVN, IDACN will be delayed by an equal amount. If RADVLDN occurs later than 195 nanoseconds after ADRAVN, MBYN will be extended an equal amount, thus increasing the cycle time of 550 nanoseconds.

WRITE DOUBLE WORD

FIGURE 7.4

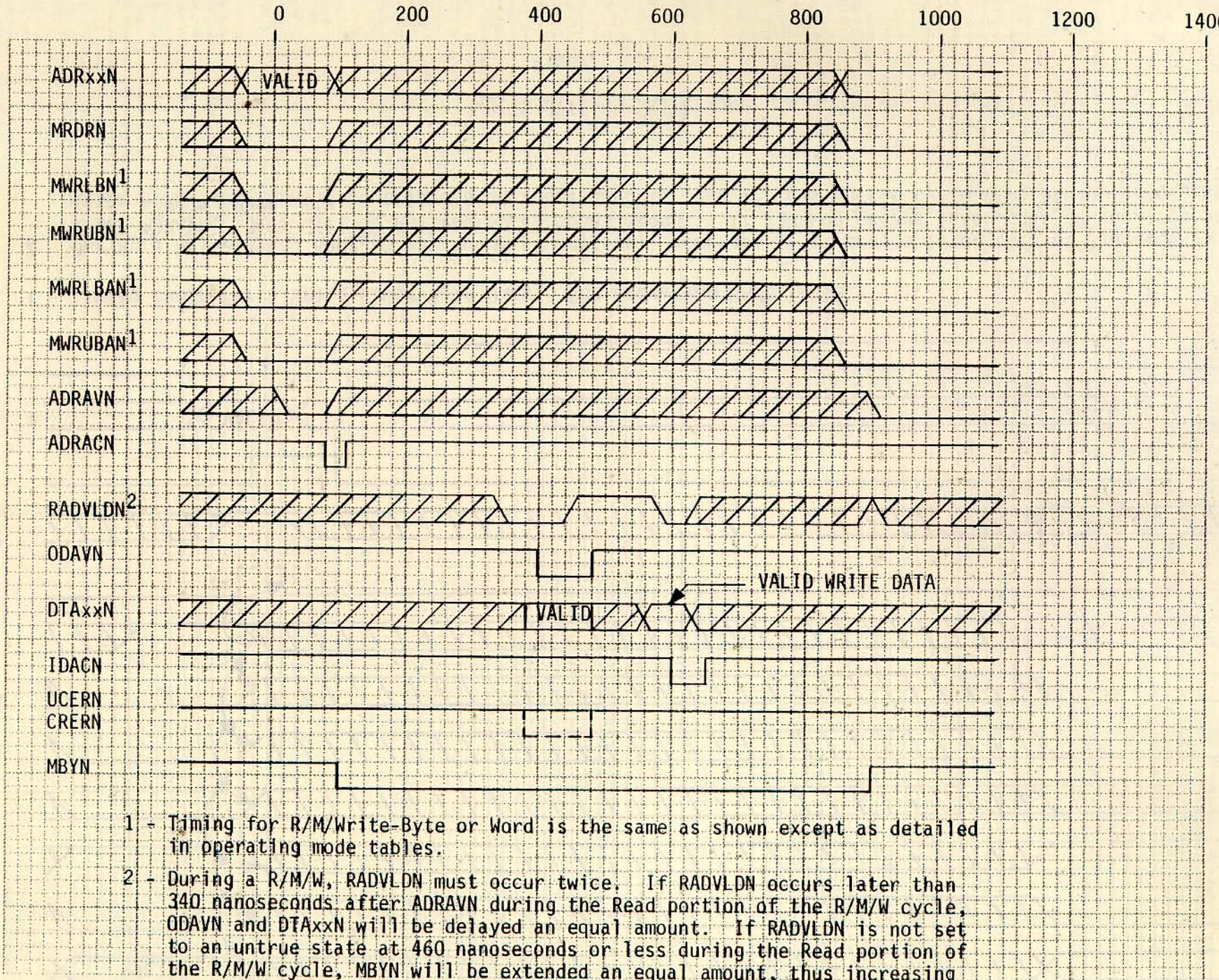


1 - Timing shown for a Write Lower Byte Only. See Operating Mode Table.

2 - During a Write/Byte, RADVLDN may occur at anytime. However, if it occurs later than 65 nanoseconds after ADRAVN, IDACN will be delayed by an equal amount. If RADVLDN occurs later than 420 nanoseconds after ADRAVN, MBYN will be extended an equal amount, thus increasing the cycle time of 700 nanoseconds.

WRITE/BYTE OR WRITE/WORD

FIGURE 7.5



1 - Timing for R/M/Write-Byte or Word is the same as shown except as detailed in operating mode tables.

2 - During a R/M/W, RADVLDN must occur twice. If RADVLDN occurs later than 340 nanoseconds after ADRAVN during the Read portion of the R/M/W cycle, ODAVN and DTAxxN will be delayed an equal amount. If RADVLDN is not set to an untrue state at 460 nanoseconds or less during the Read portion of the R/M/W cycle, MBYN will be extended an equal amount, thus increasing the cycle time of 900 nanoseconds.

FIGURE 7.6 - READ/MODIFY/WRITE DOUBLE WORD

36 BIT CONFIGURATION

	Lower Word		Upper Word		
MRDRN	MWRLBN	MWRUBN	MWRLBAN	MWRUBAN	Cycle
LOW	HIGH	HIGH	HIGH	HIGH	READ DBL WORD
HIGH	LOW	HIGH	HIGH	HIGH	WRITE LOWER BYTE LOWER WORD
HIGH	HIGH	LOW	HIGH	HIGH	WRITE UPPER BYTE LOWER WORD
HIGH	HIGH	HIGH	LOW	HIGH	WRITE LOWER BYTE UPPER WORD
HIGH	HIGH	HIGH	HIGH	LOW	WRITE UPPER BYTE UPPER WORD
HIGH	LOW	LOW	HIGH	HIGH	WRITE LOWER WORD
HIGH	HIGH	HIGH	LOW	LOW	WRITE UPPER WORD
HIGH	LOW	LOW	LOW	LOW	WRITE DBL WORD
LOW	LOW	LOW	LOW	LOW	*READ DBL WORD MODIFY WRITE DBL WORD
LOW	LOW	HIGH	HIGH	HIGH	*READ DBL WORD MODIFY WRITE LOWER BYTE LOWER WORD
LOW	HIGH	LOW	HIGH	HIGH	*READ DBL WORD MODIFY WRITE UPPER BYTE LOWER WORD
LOW	HIGH	HIGH	LOW	HIGH	*READ DBL WORD MODIFY WRITE LOWER BYTE UPPER WORD
LOW	HIGH	HIGH	HIGH	LOW	*READ DBL WORD MODIFY WRITE UPPER BYTE UPPER WORD
LOW	LOW	LOW	HIGH	HIGH	*READ DBL WORD MODIFY WRITE LOWER WORD
LOW	HIGH	HIGH	LOW	LOW	*READ DBL WORD MODIFY WRITE UPPER WORD

*The processor must accept read data from memory prior to transmitting the write data.

TABLE 7.1

18 BIT CONFIGURATION

MRDRN	MWRLBN	MWRUBN	Cycle
LOW	HIGH	HIGH	READ WORD
HIGH	LOW	HIGH	WRITE LOWER BYTE
HIGH	HIGH	LOW	WRITE UPPER BYTE
HIGH	LOW	LOW	WRITE WORD
LOW	LOW	HIGH	*READ WORD MODIFY WRITE LOWER BYTE
LOW	HIGH	LOW	*READ WORD MODIFY WRITE UPPER BYTE
LOW	LOW	LOW	*READ WORD MODIFY WRITE WORD

*The processor must accept read data from memory prior to transmitting the write data.

TABLE 7.2

Memory Size (MEMSIZ0-MEMSIZ6)

The MEMSIZ0-MEMSIZ6 outputs are sent to the processor to indicate total memory capacity of expanded systems. The use of MEMSIZ0-MEMSIZ6 will prevent addressing of non-present memory modules to avoid hang-up conditions from failure to receive ADRACN from non-present memory modules. The MEMSIZ0-MEMSIZ6 signals are derived from 74S38 open collector gates and shall be pulled-up at the receiving end.

Power Interrupt (PWRINTN)

The power system shall drive PWRINTN when loss of logic or storage power is detected. PWRINTN shall be asserted as early as possible after power failure is detected, but in no case so late as to allow malfunction of a busy memory board. The busy memory will complete the cycle requested and will inhibit any further cycles from being initiated. A not busy memory will not initiate any cycles when PWRINTN is asserted.

Normalize (NORMN)

The NORMN signal acts as a general reset. The NORMN will clear all internal memory control registers, cause all memory modules to go "unbusy" and abort any outstanding data transfers. This may cause a Write cycle to store erroneous data. No further cycles may be initiated until NORMN goes false. NORMN must be asserted for at least 150 nanoseconds.

Correctable Error (CRERN)

The correctable error signal is asserted during valid data time in a Read cycle when a correctable error has occurred in the memory. If a correctable error has occurred, CRERN shall be true when ODAVN goes true and shall remain true until ODAVN goes false. CRERN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

Uncorrectable Error (UCERN)

The uncorrectable error signal is asserted during valid data time in a Read cycle when an uncorrectable error has occurred in the memory. If an uncorrectable error has occurred, UCERN shall be true when ODAVN goes true and shall remain true until ODAVN goes false. UCERN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

Status (STATN)

Status is asserted when the error log is to be examined from the memory bus. Assertion of STATN disables memory data and steers error log information to Data Bits DTA0ON-DTA15N on the memory data bus. The command must be low and remain low until the assertion of STAVN. When STATN is asserted in direct response to receipt of an error signal, the log will present that error information. (See Figure 7.7.) Repetitive assertions of status will sequentially examine the 64 log locations.

Status Available (STAVN)

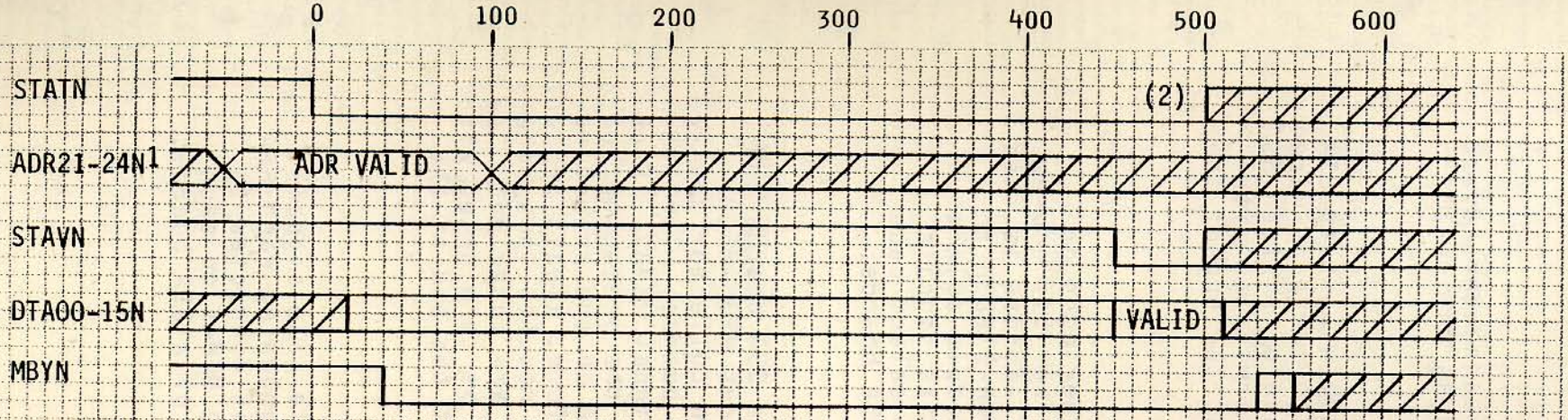
Status Available is asserted by the memory to indicate that the error log information is available. Status Available will go low 450 nanoseconds after receipt of status and remain low until status goes false. STAVN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

Memory Busy (MBYN)

Memory Busy is asserted when ADRAVN is accepted by the memory and shall remain asserted until the memory has completed its cycle. MBYN is also asserted upon power up while the memory is performing an internal clear. MBYN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end. MBYN is not asserted during a Refresh cycle.

Clear Busy (CLRBYN)

Clear Busy is asserted by the memory upon power up to indicate that the memory is performing an internal clear operation. An internal memory clear is necessary to establish proper parity in the ECC circuitry and to clear the error log. CLRBYN will go low at power up and remain low for 4 seconds. CLRBYN will not be asserted and the memory will not be internally cleared if BBU is utilized and main power fails. CLRBYN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.



1 - During an EXAMINE cycle, ADR21-24N are not used.

2 - If STATN does not go untrue at 500 nanoseconds, STAVN DTAxxN, and MBYN will be extended an equal amount.

LOG STATUS (EXAMINE) READ CYCLE

FIGURE 7.7

7.1.2 Array Bus

The signals on the array bus between BSC connector P9 and the BSA connectors P9 and P10 are defined as follows:

Extended Addresses (EXADON-EXAD3N)

The four signals EXADON-EXAD3N select between sixteen BSA boards. The four signals are compared with the hard-wired module select codes MSON-MS3N to enable one of sixteen BSA boards. The extended addresses must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Module Select Codes (MSON-MS3N)

The module select codes MSON-MS3N are either open or grounded at each BSA to provide a unique four bit address for each of sixteen BSA's. This four bit address is then compared with the extended addresses EXADON-EXAD3N to provide appropriate BSA selection. The module select codes are also used to derive the array size signals MSIZ0-MSIZ3. Figure 7.8 shows the module select code arrangement for sequential selection of BSA boards.

Module Size (MSIZ0-MSIZ3)

The module size signals are derived on the BSA boards and are the inversion of the module select codes MSON-MS3N. The module size signals are driven by open collector devices and are wired in parallel between all BSA boards. The module size lines from each BSA are gated with signal MEMAV. Each BSA board, when inserted, forces MEMAV of the preceding board false, thus disabling the module size line on the preceding board. The highest board inserted, therefore, always presents its module size signals to the BSC. This results in a binary board count as from one to sixteen boards are inserted. See Figure 7.8. The module size signals must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Memory Available (MEMAV, MEMAVN)

Memory Available (MEMAV) enables the module size signals MSIZON-MSIZ3N on each BSA. MEMAVN is grounded on each BSA. BSA slots must be wired such that MEMAVN is connected to MEMAV of each preceding slot, thus causing MEMAV on each preceding slot to go false upon insertion of a BSA board.

BULK SEMI ARRAY SLOT	MS 0	MS 1	MS 2	MS 3	MSIZ 0	MSIZ 1	MSIZ 2	MSIZ 3	NUMBER OF BSA's
0	L	L	L	L	H	H	H	H	1
1	H	L	L	L	L	H	H	H	2
2	L	H	L	L	H	L	H	H	3
3	H	H	L	L	L	L	H	H	4
4	L	L	H	L	H	H	L	H	5
5	H	L	H	L	L	H	L	H	6
6	L	H	H	L	H	L	L	H	7
7	H	H	H	L	L	L	L	H	8
8	L	L	L	H	H	H	H	L	9
9	H	L	L	H	L	H	H	L	10
10	L	H	L	H	H	L	H	L	11
11	H	H	L	H	L	L	H	L	12
12	L	L	H	H	H	H	L	L	13
13	H	L	H	H	L	H	L	L	14
14	L	H	H	H	H	L	L	L	15
15	H	H	H	H	L	L	L	L	16

Signals MS0N-Pin 25, MS1N-Pin 19, MS2N-Pin 26 and MS3N-Pin 20 on 16 BULK SEMI Array slots are either open (H) or ground (L).

FIGURE 7.8

RAS Addresses (RADS0N-RADS7N)

Low true assertion of one of the eight lines RADS0N-RADS7N enables one of eight rows of dynamic RAM's on the selected BSA board and provides the row strobe for the multiplexed row addresses of that row. During a refresh operation, all eight lines are asserted low simultaneously to provide a row address strobe to all RAM's on the BSA. The RAS address lines must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Column Address Strobe (CASN)

The column address strobe signal when asserted provides a column strobe for the multiplexed column addresses of the dynamic RAM's. The column address strobe line must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Multiplexed Addresses (X07N-X613N, X1415N)

The eight multiplexed addresses (X07N-X613N, X1415N) when demultiplexed by the row and column address strobes provide sixteen addresses to decode one of 65,536 locations in each 64K RAM. For BSA's using 16K RAM's multiplexed address X1415N is not used. The multiplexed address lines must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Array Refresh (ARREFN)

The array refresh signal ARREFN is asserted when it is necessary to refresh the dynamic RAM's. ARREFN enables all BSA boards at the same time thus causing all dynamic RAM's to be refreshed at the same time. The array refresh line must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Write (WRN)

The write signal (WRN) provides a strobe for input data to the dynamic RAM's. The write line must be terminated with 220/330 ohm pull-up/pull-down resistors at the end of the array bus.

Array Data Bus (DB00N-DB42N)

The bidirectional array data bus DB00N-DB42N carries read and write data between the BSA's and the BSC. The data lines must be terminated with 330 ohm pull-down resistors at the end of the array bus.

Read Bus Enable (RBE)

The Read Bus Enable (RBE) signal determines the direction of data flow through the data bus drivers and receivers at the BSA. When RBE is asserted high, data is read from the BSA. The Read Bus Enable line must be terminated with a 220/330 ohm pull-up/pull-down resistor at the end of the array bus.

The following signals emanate from P10 of the BSC and are used for error logging functions:

Logfull (LGFUL)

Logfull is high true asserted by the memory when the maximum address of the 64 word error log has been reached. LGFUL is driven by a 74S74 and is used in conjunction with a BULK SEMI chassis to drive Logfull indicator light circuitry. After the LGFUL signal is asserted, the log will wrap around and continue to log errors beginning again at the lowest log address.

Error (ERR)

Error is a high true signal of approximately one second duration asserted by the memory each time a correctable or uncorrectable error has occurred. ERR is driven by a 74121 and is used in conjunction with a BULK SEMI chassis to drive error indicator light circuitry.

Begin Log (BGN)

Begin Log is low true asserted when the error log is to be returned to the lowest log address. BGN must be low for a minimum of 150 nanoseconds and is normally used in conjunction with a BULK SEMI chassis.

Clear Log (CLRN)

Clear Log is asserted when all 64 locations of the error log are to be cleared. CLRN must be low for a minimum of 150 nanoseconds. A log clear operation takes 72 microseconds. Completion of a log clear results in assertion of Logfull from the memory. CLRN is normally used in conjunction with a BULK SEMI chassis.

Examine Log (EXAMN)

Examine Log is used in conjunction with a BULK SEMI chassis. Assertion of EXAMN performs the same operation as STATN. In the BULK SEMI chassis, error information will be displayed as long as EXAMN is asserted.

7.1.3 BULK SEMI Array (BSA)

The DR-129/229S uses as its storage element 16K or 64K NMOS dynamic RAM's in 16 pin dual-in-line packages. To achieve the packing density, the sixteen binary addresses required to select one of 65,536 locations for a 64K RAM are presented as eight multiplexed signals at the device. The eight signals are demultiplexed inside the package by a row and column strobe. The proper application of the row address strobe (RAS), the column address strobe (CAS), and the multiplexed addresses provides data out of the RAM. The proper application of the RAS, CAS multiplexed address and a write strobe allows data to be written into the device.

The storage mechanism within the dynamic RAM is the gate capacitance of a field-effect transistor. A "1" is the presence of a charge and a "0" is stored as the absence of a charge. The stored charge tends to deteriorate and must be renewed at least every two milliseconds. This is accomplished by selecting each row address once within the two millisecond period.

The DR-129/229S BSA consists of an array of 344 dynamic RAM's configured as 128K (16K RAM's) or 512K (64K RAM's) by 43 bits. The 43 bits of storage consist of 36 data bits plus 7 bits of error checking and correcting code (ECC) created on the BSC to enable single bit error correction and double bit error detection. The BSA board contains the necessary circuitry to receive the address, RAS, CAS, and write strobe information from the BSC and drive the RAM array. (There is no timing generated on the BSA.) The BSA also contains the necessary drivers and receivers to transmit data and receive data from the BSC. All data transfers between the BSC and the BSA consist of 43 bits.

Sheet 1 of schematic 03333 is the block diagram of the BSA. To reduce drive loading, the 344 RAM array is divided into three groups of 15, 14 and 14 bits with each group driven by separate RAS, CAS, Address and WR drivers. The RAS, CAS, Address and WR signals to the drivers are received at the array bus by buffers which are enabled when the appropriate BSA address has been selected. Data to and from the RAM array is buffered at the array bus and enabled in either the read or write direction by the signal Read Bus Enable (RBE).

The BSA also contains regulator circuitry to generate +12 volts and -5 volts from the +15 volt supply when 16K RAM's are used. The 64K RAM's operate from +5 volts only and consequently do not use this circuitry.

7.1.4 BULK SEMI Controller (BSC)

Sheet 1 of schematic 03191 is the block diagram for the BSC. During a normal memory operation, addresses and cycle control signals from the memory bus establish the location and type of cycle to be performed. The addresses are compared to the module size signals from the BSA to ensure memory exists at the location requested. If memory exists, a select signal is issued and upon receipt of ADRAVN a cycle is begun. The cycle control signals and the addresses are latched and the addresses are appropriately translated for 18 bit or 36 bit operation or for 16K or 64K RAM's. The lower order addresses are multiplexed to provide RAM addresses; the middle order addresses are decoded to provide row addresses; the higher order addresses provide BSA extended addresses.

During a power up clear cycle, clear addresses override memory bus addresses to provide sequential address selection.

Data on the memory bus is handled as 18 or 36 bits. Data inside the BSC is always handled as 36 bits. Data buffers at the memory bus steer the data to or form the proper 36 bit registers. Data written into memory is stored in registers and then passed to the array bus and to error code generation circuits. The data and the ECC codes are then stored in dynamic RAM's on a BSA. Data and ECC codes read from a BSA are fed to error code check and correction circuitry where single bit errors are corrected. The data is then latched and fed to the memory bus. If an error has occurred, the bit and address information is stored in an error log which may be interrogated via the memory data bus.

The timing and control section provides RAS, CAS, and WR timing and mode controls to manipulate data for Byte operations.

7.2 Modes of Operation

The DR-129/229S has eight major modes of operation. They are:

READ
MATCH READ
WRITE 36 BITS
WRITE BYTE OR 18 BIT WORD
READ/MODIFY/WRITE
POWER CLEAR
STATUS OR EXAMINE
REFRESH

The modes are described as follows:

7.2.1 Read (See Figure 7.2)

ADRAVN in conjunction with the appropriate address and cycle control signals begins a read cycle. Upon receipt of ADRAVN the BSC responds with ADRACN, asserts a memory busy signal, latches address and cycle control signals and starts delay line timing to create RAS and CAS signals. The RAS and CAS signals are of a fixed preset duration. The RAS, CAS, and address signals are steered to the appropriate BSA from which 36 bits of data plus 7 ECC Bits are read. The data and ECC Bits are received on the BSC where the data bits are corrected if necessary and stored in a 36 bit register. Data is taken from the BSC by assertion of RADVLDN. The BSC responds to RADVLDN with ODAVN which is asserted at the memory access time or immediately upon receipt of RADVLDN if RADVLDN is later than the access time. ODAVN signals that data has been enabled on the memory bus. The data and ODAVN will remain valid until RADVLDN goes false. The memory will remain busy until ODAVN goes false. A BSC strapped for 18 bits operates exactly as a 36 bit BSC except that data from the appropriate half of the 36 bit BSC data register is steered to the 18 bit memory bus by the address A0.

7.2.2 Match Read (see Figure 7.3)

A match read cycle occurs automatically in an 18 bit BSC when sequential address reads are being done. Since data from the BSA is always stored as 36 bits on the BSC, two adjacent 18 bit words are actually stored. Upon receipt of ADRAVN, the cycle control lines and addresses ADR01N-ADR24N are compared with those of the previous cycle. If they agree no access to the BSA is required. The data is simply steered immediately to the memory bus from the appropriate data registers upon receipt of RADVLDN. To take advantage of the match read access time, RADVLDN must be asserted very early in the cycle.

7.2.3 Write 36 Bits (See Figure 7.4)

The write cycle begins with ADRAVN in conjunction with the address and cycle control signals. The BSC responds with ADRACN, asserts a memory busy signal, latches address and cycle control signals and starts delay line timing to create RAS and CAS signals. The RAS and CAS signals, however, are not of a fixed duration as in a read cycle. The RAS and CAS signals must be latched so they remain until data to be written is presented by RADVLDN. Upon receipt of RADVLDN the BSC clocks the data into registers, responds with IDACN and creates write timing to generate error checking codes and store the data and the ECC code on the BSA. When internal write timing is complete, the RAS and CAS signals are unlatched and memory busy is negated. Cycle time will be delayed by late presentation of RADVLDN.

7.2.4 Write Byte or 18 Bit Word (See Figure 7.5)

The write byte operation begins exactly as a 36 bit write operation. However, since only a portion of a 36 bit word is to be written into memory, the 36 bit word already in memory must be read so that the portion which will not change may be combined with the new data, thus enabling correct ECC to be generated for the new word. The BSC therefore performs an internal read operation, corrects the data if necessary and stores it in a 36 bit register. New data received at RADVLDN is clocked into registers and IDACN is asserted. The write timing, however, is not begun until the old 36 bit word has been corrected and stored. The latched cycle control lines establish which old data and which new data is to be combined in a new word. Write timing is then begun as in a 36 bit write operation to store the new word and its ECC codes on the BSA.

The write byte minimum cycle time is increased due to time allowed for the read portion.

A BSC strapped for 18 bits always operates as described above.

7.2.5 Read/Modify/Write (See Figure 7.6)

The Read/Modify/Write cycle operates in a similar manner to the Write Byte cycle. Upon receipt of ADRAVN, the addresses and the cycle control signals, the timing is begun and RAS and CAS signals are latched. The BSC then responds to two sequential RADVLDN signals. On the first RADVLDN, ODAVN is asserted and corrected data is presented to the memory bus. RADVLDN is then removed and

the data and ODAVN are negated. Upon receipt of the second RADVLDN, new data is clocked into the BSC, IDACN is asserted, and the data is combined with the old data as dictated by the latched cycle control lines. Write timing is then begun to store the new word and its ECC on the BSA and complete the cycle.

7.2.6 Power Up Clear

The Power Up Clear cycle automatically establishes proper ECC in the memory at power up by performing 36 bit writes at all locations. Upon power up the signal CLBYN is asserted by the BSC and a sequential address count is begun. The array bus data lines are all forced high thus writing "ones" to the memory. CLBYN prevents all other operations until power up clear is complete. The error log is also cleared at this time. The power up clear cycle is independant of +5 volts and will only respond to loss of +5B and +15 volts.

7.2.7 Status or Examine (See Figure 7.7)

The status cycle is used to examine the error log from the memory bus. The cycle is begun by assertion of STATN and the upper addresses ADR21N-ADR24N. Upon assertion of STATN, all other accesses to the memory will be blocked and data from the error log will be steered to memory bus data bits DTA00N-DTA15N. The signal STAVN is asserted when the log information is available. The log information will remain as long as STATN is asserted. Figures 7.9A and B provide the error decode information for the data bits DTA00N-DTA15N.

The examine cycle is identical to the status cycle except that addresses ADR21N-ADR24N need not be decoded to examine the error log.

7.2.8 Refresh

The refresh cycle is internally generated by a free-running clock on the BSC to provide periodic refresh to the dynamic RAM's. With the exception of status, examine, or power up clear, the refresh cycle periodically enters into contention with the other cycles. If a refresh cycle has been requested just prior to the assertion of ADRAVN, the memory cycle may be delayed up to 700 nanoseconds at which time ADRACN will be asserted. In a Read cycle if a refresh cycle has been requested after ADRACN has been asserted, the refresh cycle will occur directly after the Read cycle. In a Write cycle if a refresh has been requested after ADRACN has been asserted but before RADVLDN has been asserted, the refresh cycle will shut down the cycle and commence to refresh. Upon receipt of RADVLDN, data will be immediately clocked in and IDACN will be asserted. The Write cycle will automatically restart upon completion of the refresh cycle.

7.3 BSA Detailed Description

Refer to Schematic 03333.

7.3.1 Internal Signals

The internal signals on the BSA are defined as follows:

AOAN-AOMN thru A7AN-A7MN - The buffered multiplexed address lines X07N-X63N, X1415N which drive the dynamic RAM's.

CASAN-CASMN - The buffered CASH signal which drives the dynamic RAM's.

CASSL (CAS Select) - The inverted CASN signal gated by SELN.

RASOAN-RAS7AN, RASOBN-RAS7BN, RASOCN-RAS7CN - The buffered RADSON-RADS7N lines which drive the dynamic RAM's.

RWON-RW4N - The buffered RBE signal which enables the data transceivers.

SELN (Select) - SELN is asserted low when the array board has fallen within the appropriate address range. SELN enables CASN, WRN, and RBE. SELN is not asserted during a refresh.

SELRN (Select RAS) - SELRN is asserted low when the array board has fallen within the appropriate extended address range or when the array refresh (ARREFN) signal has been asserted. SELRN enables the RAS address lines RADSON-RADS7N.

WRAN-WRMN - The buffered WRN signals which drive the dynamic RAM's.

DTAxxN BUS LOG DECODE (ROW & BOARD)

	Data Bit			
Board	03	04	05	06
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

	Data Bit		
Row	00	01	02
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

0 = Low
1 = High

FIGURE 7.9A

DTAxxN BUS LOG DECODE (BIT)

Data Error Bit	Type of Error	DTAxxN Bit 07	08	09	10	11	12	13	14	15
--	NO ERR	1	1	1	1	1	1	1	0	1
00	CRE	0	1	1	0	1	1	1	1	0
01	CRE	1	0	1	0	1	1	1	1	0
02	CRE	0	0	1	0	1	1	1	1	0
03	CRE	1	1	0	0	1	1	1	1	0
04	CRE	0	1	0	0	1	1	1	1	0
05	CRE	1	0	0	0	1	1	1	1	0
06	CRE	0	1	1	1	0	1	1	1	0
07	CRE	1	0	1	1	0	1	1	1	0
08	CRE	0	0	1	1	0	1	1	1	0
09	CRE	1	1	0	1	0	1	1	1	0
10	CRE	0	1	0	1	0	1	1	1	0
11	CRE	1	0	0	1	0	1	1	1	0
12	CRE	0	1	1	0	0	1	1	1	0
13	CRE	1	0	1	0	0	1	1	1	0
14	CRE	0	0	1	0	0	1	1	1	0
15	CRE	1	1	0	0	0	1	1	1	0
16	CRE	0	1	0	0	0	1	1	1	0
17	CRE	1	0	0	0	0	1	1	1	0
18	CRE	0	1	1	1	1	0	1	1	0
19	CRE	1	0	1	1	1	0	1	1	0
20	CRE	0	0	1	1	1	0	1	1	0
21	CRE	1	1	0	1	1	0	1	1	0
22	CRE	0	1	0	1	1	0	1	1	0
23	CRE	1	0	0	1	1	0	1	1	0
24	CRE	0	1	1	0	1	0	1	1	0
25	CRE	1	0	1	0	1	0	1	1	0
26	CRE	0	0	1	0	1	0	1	1	0
27	CRE	1	1	0	0	1	0	1	1	0
28	CRE	0	1	0	0	1	0	1	1	0
29	CRE	1	0	0	0	1	0	1	1	0
30	CRE	0	1	1	1	0	0	1	1	0
31	CRE	1	0	1	1	0	0	1	1	0
32	CRE	0	0	1	1	0	0	1	1	0
33	CRE	1	1	0	1	0	0	1	1	0
34	CRE	0	1	0	1	0	0	1	1	0
35	CRE	1	0	0	1	0	0	1	1	0
36	CRE	1	1	1	1	1	1	1	1	0
37	CRE	1	1	1	1	1	0	1	1	0
38	CRE	1	1	1	1	0	1	1	1	0
39	CRE	1	1	1	0	1	1	1	1	0
40	CRE	1	1	0	1	1	1	1	1	0
41	CRE	1	0	1	1	1	1	1	1	0
42	CRE	0	1	1	1	1	1	1	1	0
	UCE	X	X	X	X	X	X	0	1	X

0 = Low
1 = High
X = Don't Care

FIGURE 7.9B

7.3.2 BSA Selection

Sheet 2 of the schematic depicts BSA selection. Extended addresses EXADON-EXAD3N from the array bus are buffered by Z44 and compared with hard-wired module select codes MSON-MS3N at Exclusive-OR Z41. If the select codes and the extended addresses agree, the inputs Z42-1, 2, 3, 12, and 13 go low, resulting in a high at Z42-5. Z42-5 is inverted to create SELRN at Z42-6 and SELRN at Z44-6. SELRN at Z42-6 may also be asserted low by array bus signal ARREFN which is buffered by Z44. The ARREFN signal allows SELRN to be asserted during a refresh cycle. SELRN enables the array bus signals RADSON-RADS7N at Z45 and Z46 (Sheet 3). During memory read or write only one of the signals RADSON-RADS7N is asserted low. During refresh all of the signals are asserted low. The array bus signals CASN, WRN, and RBE are enabled at Z18 by SELRN. Multiplexed addresses XO7N-X613N, X1415N are buffered at Z19 (Sheet 4) and drive the array via inverters Z20-Z37.

7.3.3 Data (Sheets 4-6)

The data into the array is received by 74LS240's. The data from the array is driven by 74S38 open collector devices. The data out is enabled by signals RWON-RW4N which are the expanded buffered array bus signal RBE.

7.4 BSC Detailed Description

Refer to schematic 03191.

7.4.1 Internal Signals

The internal signals on the BSC are defined as follows:

ADOON-AD24N (Latched Addresses) - Addresses ADROON-ADR24N which have been received at the memory bus and latched on the BSC.

BO-B10, BON-B10N (Write Delay Line Timing Signals) - These signals provide timing for the write operation during a write cycle.

BWRN (Blanking Write) - BWRN is asserted low at the end of a write operation to prevent a refresh cycle beginning before the write cycle is complete.

CC1N, CC2N, CC4N, CC10N, CC20N, CC40N, CCPN - The ECC code bits which are read from the array bus as DB36N-DB43N and sent to the ECC parity generators.

CINTN (Clear Initialize) - CINTN is held low upon power up until +5B and +15 volts have stabilized. CINTN initiates a power up clear cycle. CINTN is not asserted during power failure when battery backup is used.

CIP (Cycle in Progress) - CIP in asserted high upon the acceptance of an ADRAVN signal from the memory bus.

CLAD01N-CLAD16N (Clear Addresses) - Addresses generated during the power up clear mode to allow writing proper error checking code in all memory locations.

CLBY, CLBYN (Clear Busy) - CLBY is generated by the BSC to indicate it is in the power up clear mode. CLBY disables memory bus generated addresses and enables clear addresses CLAD01N-CLAD16N and forces the memory into the write mode. CLBYN forces a set data pattern on the array bus to allow proper ECC to be written.

CLSTR (Clear Start) - CLSTR is generated during a power up clear and begins internal write cycles to provide proper ECC to the memory.

CLWN (Clear Write) - CLWN is asserted low if a write cycle has been interrupted by a refresh. CLWN clears the byte write timing register which is reset from the major delay line timing upon restart.

CRD0-CRD35A (Corrected Data) - Data from the array bus which has been corrected and latched. This data is fed to the memory bus read drivers.

CREN (Correctable Error) - This signal is asserted high when a single bit error has occurred.

DIOON-DIO35N - Data from the array bus which is fed to the ECC parity generators for ECC code generation.

DO-D20, DON-D20N (Delay Line Timing Signals) - These signals provide the major timing for the operation of the BSC.

D27-D33 - Latched data from the memory bus which is multiplexed with the ECC code bits to manipulate ECC syndrome generation. These signals are used for diagnostic purposes only.

ECC1, ECC2, ECC4, ECC10, ECC20, ECC40, ECCP (Error Check and Correction Bits) - The outputs of the ECC parity tree which are used during read as syndrome bits and during write to create checking code bits.

EC0-EC35 (Error Correction) - The EC0-EC35 signals are the decoded error syndrome bits which correct a single bit error from the array bus. The signals are normally low. One of the signals will be asserted high for single bit correction.

EXSEL (Extended Select) - The EXSEL signal is used to enable the BSC when multiple memory systems are daisychained. The EXSEL signal is jumper enabled as a function of addresses ADR21N-ADR24N and gates ADRAVN.

INCASN (Internal CAS) - INCASN is an internal CAS timing signal which gates the WRSN to ensure proper write restart timing.

INTN (Initialize) - INTN is held low upon power up until +5 volts and +15 volts have stabilized. INTN clears all registers and prevents spurious timing signals. INTN is wire-ORED with NORMN.

IWUBAN, IWLBAN, IWUBBN, IWLBBN (Internal Byte Write Data Enable Lines) - These lines enable internal corrected array bus data to be combined with latched memory bus data to create new 36 bit words during byte write operations.

LKOUTN (Lockout) - LKOUTN is an extended memory busy signal used to prevent the start of a memory cycle until the previous cycle has been completed and address and control signals have been unlatched, thus enabling proper setup time for new address and control signals. LKOUTN gates ADRAVN.

LUCE (Latched Uncorrectable Error) - LUCE is the UCE signal which has been stored in a register.

MATCHN (Match) - The MATCHN signal is low true asserted when the memory is strapped for 18 bits is in the read mode and has just previously done a read at the same address or at the same address plus or minus one if the second least significant address ADR1N has not toggled. MATCHN is disabled high for a 36 bit BSC. The MATCH signal enables data to be read directly from the 36 bit data register, thus shortening the memory cycle dramatically.

MB, MBN (Memory Busy) - The MB, MBN signal is a portion of the memory busy sginal MBYN. MBN is used to latch memory bus addresses and cycle control signals on the BSC.

MSEL (Memory Select) - MSEL is high true asserted when the memory falls within the bounds of the asserted memory bus addresses. MSEL gates ADRAVN.

ODACN (Output Data Accepted) - ODACN internally gates data to the memory bus, clears the CIP register during a read cycle and extends MBYN during a MATCH cycle. ODACN generates ODAVN.

RAS (Row Address Strobe) - The RAS signal gates the appropriate latched and decoded memory bus addresses to create the RAS addresses (RADSON-RADS7N) on the array bus.

RDALBN (Read All Bytes) - The RDALBN signal is generated by the latch cycle control lines (WRUBAN, WRLAN, WRUBN, WRLBN) and is asserted low when all bytes are being read.

RDEN1-RDEN3 (Read Enable) - RDEN1-RDEN3 enable the memory bus read data drivers and steer data from the 36 bit array bus data registers to the eighteen bit memory data bus when the BSC is strapped for eighteen bits. RDEN1-RDEN3 are gated by ODACN.

RDLAN (Read Latch) - RDLAN is asserted low to latch data from the array bus which has been corrected. RDLAN also generates array bus signal RBE.

RDSN (Read Start) - RDSN is asserted low to begin the major delay timing during a normal memory access. RDSN is initiated by CIP when the memory is not in a MATCH cycle.

READN - READN is the buffered and latched cycle control signal MRDRN.

RFHCLK (Refresh Clock) - RFHCLK is derived from a free-running 14 microsecond timer and signals the need for a refresh cycle. RFHCLK initiates RFHRQN.

RFHCLN (Refresh Clear) - RFHCLN is asserted low at the end of a refresh cycle to clear refresh timing registers.

RFHE, RFHEN (Refresh Enable) - This signal indicates that a refresh cycle has been enabled and prevents any read or write operations in the memory.

RFHRQN (Refresh Request) - RFHRQN is asserted when a refresh cycle is required. RFHRQN gates ADRAVN.

RFRSN (Refresh Set) - RFRSN is asserted low when refresh contention has been resolved and refresh has won. RFRSN initiates RFHEN.

RM00-RM015 - RM00-RM015 are the outputs of the error log which contains failed RAM error information.

RWADON-RWAD2N (Row Addresses) - RWADON-RWAD2N are the higher order latched memory bus addresses which are decoded to create the RAS addresses (RADSON-RADS7N).

STBYN (Status Busy) - STBYN is low true asserted when a Status cycle has been initiated from the memory bus or when an Examine has been initiated from a BULK SEMI chassis. STBYN gates ADRAVN and prevents normal RAM memory access.

UCE (Uncorrectable Error) - This signal is asserted high when a multiple bit error has occurred.

WIPN (Write In Progress) - WIPN is asserted low upon the beginning of the write portion of a memory cycle.

WORD, WORDN - This signal allows data from the 36 bit array bus to be steered to the 18 bit memory bus when in the 18 bit mode. When in the 18 bit mode, this signal is controlled by ADROON. In the 36 bit mode, this signal steers data directly to the 36 bit memory bus from the 36 bit array bus.

WRALB (Write All Bytes) - WRALB is asserted high in a double word write operation and enables an earlier write with a shorter cycle time. WRALB is disabled low in an eighteen bit BSC.

WRCLK (Write Clock) - WRCLK is initiated by RADVLDN during a write or a read/modify/write cycle and clocks memory bus data into registers on the BSC.

WRINTN (Write Initialize) - During a write cycle, WRINTN clears the memory busy register, the RAS and CAS registers, and the byte write timing register.

WRLAN (Write Lower Byte A) - WRLAN is a buffered and latched MWRLBN.

WRLBN (Write Lower Byte B) - WRLBN is a buffered and latched MWRLBAN.

WRUAN (Write Upper Byte A) - WRUAN is a buffered and latched MWRUBN.

WRUBN (Write Upper Byte B) - WRUBN is a buffered and latched MWRUBAN.

WRSN (Write Restart) - WRSN is asserted low to restart the major timing delay line if it has been shut down due to a refresh interruption of a write cycle.

WUBAN, WLBAN, WUBBN, WLBBN (Byte Write Data Enable Lines) - These lines enable latched memory bus data to be combined with corrected array bus data to create new 36 bit words during byte write operations.

7.4.2 Address and Selection (Sheets 3 and 4)

The memory bus addresses ADROON-ADR24N are buffered on the BSC by 74LS241's Z202, 203, 205, 207 and if a cycle is begun are latched by MBN in 74S373 octal registers, Z201, 204, 206, 208. The latched addresses then pass to 74S257 tri-state 2 to 1 multiplexers Z173-177 and 74S253 tri-state multiplexers Z149, 151, 179, and 180 where they are translated to accommodate 18 or 36 bit operation or 16K or 64K RAM's. For 18 bit operation, the B input of multiplexers Z174-4 is passed and ADROON determines WORD or WORDN. For 64K RAM's, the addresses at multiplexers Z149, 151, 179, and 180 are shifted up by two to accommodate the increased BSA capacity. The addresses 0 thru 15 (Sheet 3) are multiplexed at tri-state octal buffers Z192 and Z193 to provide the multiplexed addresses to the array bus. The timing signal D2N at Z197-2 and Z154-9 enables addresses 7 thru 13 and 15 during RAS time and addresses 0 thru 6 and 14 during CAS time. The timing signal D2N is gated with RFHEN to disable these addresses during refresh and enable refresh addresses which are generated at refresh counter Z195 and buffered onto the array bus via Z194. The Row addresses RWADON-RWAD2N from multiplexers Z179 and Z149 are decoded at octal decoder Z189 and buffered to the array bus via Z190. Tri-state buffer Z190 is enabled by RAS at Z196-1 to provide proper timing for the RAS address signals RADSON-RADS7N. During normal memory operation, only one RAS address at a time is asserted low. During refresh all RAS addresses are asserted low by enabling tri-state buffer Z191 with RFHEN and passing the RAS signal to the array bus. Extended address from Z151 and Z180 (Sheet 4) are buffered to the array bus by octal buffer Z186.

The BSC is selected when inverted module size lines from the array bus (Sheet 4) are presented to the adder Z187 and summed with the extended addresses from multiplexers Z151 and Z180. If the extended addresses are equal to or less than the inverted module size lines, a carry is generated and MSEL is asserted high. MSEL gates ADRAVN thus enabling a cycle to begin.

Multiple memory systems may be bussed together and selected separately by the signal EXSEL which is enabled at Z211-6 by the inverted or non-inverted addresses AD21N-AD24N at Z211-3, 4, and 5. EXSEL gates ADRAVN thus enabling a cycle to begin.

7.4.3 Data (Sheets 8-12)

Data to be written into memory is received from the memory bus by 74S240's Z100 - Z107 and clocked into octal registers Z113, Z117, Z121, Z130 and Z136 by WR CLK upon receipt of RADVLDN. In the 18 bit mode, buffers Z102, Z106 and Z107 are disabled. Data is alternately steered to registers Z113, Z117, Z121-13, Z121-14 or registers Z126, Z130, Z121-7, Z121-8 by enabling the buffers Z100, Z103-13, Z103-11, Z104 or Z100, Z103-6, Z103-8, Z105 with the signals WORD or WORDN. The signals WORD, WORDN are toggled by the least significant address A0. In the 36 bit mode, WORD is forced low and WORDN is forced high disabling Z100, Z103-6, Z103-8, Z105. Z102, Z106, Z107 are enabled and 36 bits of data pass directly to the registers. Data from the registers is passed to the array bus via buffers Z122, Z156, Z159, Z163, Z166, Z169 where it is passed to the BSA's. The data is also passed back to the BSC via buffers Z158, Z161, Z165, Z171 and thence to error checking code circuitry (Sheet 11) as signals DI000N-DI035N. The error checking code circuitry uses extended parity generation to create a modified Hamming code. The code bits ECC1, ECC2, ECC4, ECC10, ECC20, ECC40, and ECCP are buffered to the array bus check bit via Z200 (Sheet 12) as signals DB36N-DB42N for storage on the BSA along with the data bits.

Data read from the BSA is passed to the BSC via buffers Z158, Z161, Z165, Z171 (Sheet 8) and thence to the error checking code circuitry (Sheet 11) as signals DI000N-DI035N and to Exclusive-OR gates (Sheet 18) where the data awaits correction if necessary. The signals DI000N-DI035N at the error checking circuitry are combined with the check bits received from the BSA to determine if errors have occurred. The parity generated code bits ECC1, ECC2, ECC4, ECC10, ECC20, ECC40, and ECCP define a unique code to correct single bit errors and detect double bit errors if they have occurred. (See Figure 7.10) The code bits at parity chip Z67 and nand gate Z66 determine if a correctable or uncorrectable error has occurred. The correctable error signal enables the error decoders (Sheet 12). When a single bit error has occurred, the code bits at decoders Z58, Z61, Z62, Z63, Z65, Z68, Z71 assert one error correction signal EC0-EC35 low for the bit in error. The error correction signals EC0-EC35 proceed to Exclusive-OR's (Sheet 8) where the data from the array bus has been awaiting correction. Bits not requiring correction are inverted at the Exclusive-OR by the high true correction signals. The bit in error is not inverted by the low correction signal, thus providing corrected data. After sufficient time for correction, the corrected data is latched by RDLAN at octal registers Z114, Z118, Z123, Z127, Z131. The data remains latched until the beginning of another memory cycle. The latched corrected data

ECC ERROR DECODE

BIT	CODE BIT ECC1	ECC2	ECC4	ECC10	ECC20	ECC40	ECCP
00	1	0	0	1	0	0	1
01	0	1	0	1	0	0	1
02	1	1	0	1	0	0	0
03	0	0	1	1	0	0	1
04	1	0	1	1	0	0	0
05	0	1	1	1	0	0	0
06	1	0	0	0	1	0	1
07	0	1	0	0	1	0	1
08	1	1	0	0	1	0	0
09	0	0	1	0	1	0	1
10	1	0	1	0	1	0	0
11	0	1	1	0	1	0	0
12	1	0	0	1	1	0	0
13	0	1	0	1	1	0	0
14	1	1	0	1	1	0	1
15	0	0	1	1	1	0	0
16	1	0	1	1	1	0	1
17	0	1	1	1	1	0	1
18	1	0	0	0	0	1	1
19	0	1	0	0	0	1	1
20	1	1	0	0	0	1	0
21	0	0	1	0	0	1	1
22	1	0	1	0	0	1	0
23	0	1	1	0	0	1	0
24	1	0	0	1	0	1	0
25	0	1	0	1	0	1	0
26	1	1	0	1	0	1	1
27	0	0	1	1	0	1	0
28	1	0	1	1	0	1	1
29	0	1	1	1	0	1	1
30	1	0	0	0	1	1	0
31	0	1	0	0	1	1	0
32	1	1	0	0	1	1	1
33	0	0	1	0	1	1	0
34	1	0	1	0	1	1	1
35	0	1	1	0	1	1	1
36	0	0	0	0	0	0	1
37	0	0	0	0	0	1	0
38	0	0	0	0	1	0	0
39	0	0	0	1	0	0	0
40	0	0	1	0	0	0	0
41	0	1	0	0	0	0	0
42	1	0	0	0	0	0	0
No Errors	0	0	0	0	0	0	0

1 = High
0 = Low

FIGURE 7.10

CRD0-CRD35 is buffered to the memory bus via 74S38 open collector devices (Sheet 10). CRD0-CRD15 are first passed through 2 to 1 multiplexers to allow selection between memory data CRD0-CRD15 and error log data RM00-RM015. The 74S38 data output gates are enabled by signals RDEN1, RDEN2, RDEN3. In the 18 bit mode, RDEN1 is permanently low while RDEN2 and RDEN3 are toggled by address A0. In the 36 bit mode, RDEN1 and RDEN3 are enabled while RDEN2 is disabled low.

For write operations in the 18 bit mode or for byte writes, data is first read from the BSA, corrected and latched as described in the read operations. Data to be written is clocked into registers as indicated in the write operation. The portion of the corrected data from the BSA which is to be retained is merged on the array bus with the newly clocked data and sent to the BSA and to the error checking code circuitry. The write operation then proceeds as described earlier. The merging of data is accomplished via tri-state buffers Z122, Z157, Z160, Z162, Z164, Z167 (Sheet 8) which steer the latched corrected data back to the array bus and via tri-state buffers Z122, Z156, Z159, Z162, Z163, Z169 (Sheet 9) which steer the newly clocked data to the array bus. The internal data buffers are enabled by signals IWLBAN, IWUBAN, IWLBBN, and IWUBBN while the newly clocked data buffers are enabled by WLBAN, WUBAN, WLBBN, and WUBBN. These signals are derived from the mode control lines.

7.4.4 Timing and Control

Figure 7.11 thru 7.15 depict the timing for the BSC in various modes of operation. The major delay line timing is identical for all modes.

7.4.4.1 Read (No Match)

The read cycle timing proceeds as follows:

1) Addresses and cycle control signals are presented on the memory bus.

2) ADRAVN is asserted low at Z209-3. If the memory is not busy from a log interrogate (STATUS) or from a previous cycle and if RFHRQN has not been asserted, Z39-8 will go low. A low at Z39-8 sets cross coupled latch Z11, Z212 and C1P is asserted. R12, R13 and C6 at Z11-10 form a pulse stretching network to ensure sufficient width to set the Schmitt triggered gate.

3) CIP clocks a high into the memory busy flip-flop Z14-12 and MBYN and MBN are asserted.

4) The assertion of MBN latches the address and cycle control lines.

5) CIP at Z35-3 enables RDSN at Z35-6 which sets cross coupled latch Z34, Z35 and propogates a high thru delay line Z7 and Z5. The latch is reset by delay line signal D14N which results in a timing pulse 220 nanoseconds long.

6) RDSN at cross coupled latch Z57, Z60 (Sheet 6) asserts the RAS timing signal. The latch is held reset or in the flow thru state by the previously asserted signal RDALBN at Z97-8. RDALBN is established by the cycle control lines. The RAS signal width at Z57-6 is determined by RDSN and the timing signal D8N. WRSN at Z57-2 is high for this mode of operation.

7) At time delay D4N CASN is asserted at cross coupled latch Z56 (Sheet 6). The latch is also held in the flow thru state by RDALBN low.

8) At the trailing edge of D2N the data available flip-flop Z9 (Sheet 5) is preset thus asserting nand input Z13-1 high in anticipation of a RADVLDN signal. The preset to data available flip-flop Z9 is gated by the cycle control signal READ at Z55-10. The data available flip-flop also extends memory busy at OR gate Z12-2 until RADVLDN has arrived.

9) At the trailing edge of D6N the cross coupled latch Z16, Z15 (Sheet 6) is set This asserts RDLAN which latches the corrected data registers.

10) At the leading edge of D8N the CIP latch Z11, Z212 is reset.

11) At D16 the memory busy flip-flop is cleared by nand gate output Z39-6 (Sheet 5). Memory busy may be extended by the data available flip-flop if RADVLDN has not yet arrived.

12) Upon receipt of RADVLDN which is enabled by MB at Z182-4, the signal ODACN is asserted at Z13-3. ODACN enables the data out gates and after a short delay enables ODAVN.

13) Upon negation of RADVLDN, ODACN is negated. This clocks a low into the data available flip-flop which negates MBYN. The cycle is complete.

7.4.4.2 Match Read

The Match Read cycle proceeds exactly as Steps 1 thru 4 in a Read cycle. However, if a match has occurred MATCHN is asserted low blocking CIP at Z35 and thus preventing the start of delay line timing. The cycle proceeds as follows:

1) MATCH at Z8-10 presets the data available flip-flop.

2) Upon receipt of RADVLDN and the assertion of ODACN the CIP latch is reset and the memory busy flip-flop is cleared.

3) Upon negation of RADVLDN, ODACN is negated. This clocks a low into the data available flip-flop which negates MBYN. The cycle is complete.

7.4.4.3 Write 36 Bits

The write cycle proceeds exactly as steps 1 thru 5 in a Read cycle. However, since the signal RDALBN is high during a write cycle, the RAS and CAS latches are set. The remainder of the cycle follows:

1) The latch Z57, Z60 is set by RDSN thus generating RAS.

2) At D4N the CASN latch Z56 is set.

3) RADVLDN is enabled at Z182 by memory busy and by presetting of flip-flop Z1. Z1 is preset by nand Z2 with inputs CIP and RDALBN.

   RADVLDN is further gated at Z29-9 by cycle control lines READN and RDALBN both high at nand Z32-1, 2.

   The assertion of RADVLDN at Z29-8 generates WRCLK which clocks a high into flip-flop Z31-2 and which enables IDACN.

   The Q side of Z31 enables nand Z110 which sets cross coupled write latch Z59, Z2. The write timing delay line is now ready to begin.

4) RDLAN is enabled when latch Z15, Z16 is set by nand Z16-8 at major delay line time D8.

5) The output of write latch Z59-6 is gated at Z56-3 by major delay line timing signal D12 at Z32-9 or by the $\overline{Q}$ of flip-flop Z1-8 clocked at the trailing edge of D8N. Write delay line timing begins. The write latch is reset after 110 nanoseconds.

6) The signal WRN is generated by the write delay line.

7) At the end of write delay line timing WRINTN is generated. The RAS and CAS latches are reset. The memory busy flip-flop is cleared. The cycle is complete.

7.4.4.4 Write Byte or 18 Bit Word

The byte write or 18 bit write timing is exactly the same as the 36 bit write timing except that in Step 5 the write delay line timing is not enabled at D12 but only at the trailing edge of D8N. This ensures time for a read operation before new data is written. The RDLAN signal is also generated later via nand Z16-3, 4, 5 at the trailing edge of D6N. Nand Z16-9, 10, 11 is disabled by the cycle control lines.

7.4.4.5 Read/Modify/ Write

The Read/Modify/Write cycle proceeds exactly as a byte write cycle except that two RADVLDN's are issued. The sequence of responses to RADVLDN is as follows:

1) At D2N the data available flip-flop Z9 is preset. D2N is enabled by READ at Z55-10 and by the Q output of Z31-9 at Z55-9. Z31-10 has been preset at initialization or by a previous cycle.

2) RADVLDN is enabled at Z182-6 and enables ODACN at Z13-3 thus providing the read response to the cycle. RADVLDN, however, is blocked from the write circuitry by Z29-10 which is low due to the cycle control lines READN being low at Z32-1 and the Q of Z31-9 being high.

3) Upon negation of the first RADVLDN, ODACN is negated. The trailing edge of ODACN clocks a low into Z31-2 sending the Q output Z31-9 low. This enables Z29-10 preparing the memory for a write response to the next RADVLDN.

7.4.4.6 Refresh

A Refresh cycle proceeds as follows:

1) Free running timer Z3 and one shot Z10 create 150 nanosecond low going pulse RFHCLK.

2) RFHCLK presets Z9 and issues RFHRQ at Z9-5.

3) RFHRQ and RFHCLK at Z35-1 and Z36-4 start delay line timing with RFRSN if the memory is not busy from a previous cycle as indicated by BWRN at Z36-5 and the delay line timing at Z35-2.

4) RFSRN presets Z42-4 issuing RFHE and RFHEN which disable CAS, enable ARREFN and enable all RAS address lines simultaneously.

Contention between a refresh cycle and the start of a memory cycle is resolved at nand gate Z39-8 and at nand gate Z35-12. If a RFHRQ occurs at Z39-13 before an ADRAVN, the memory cycle is delayed. If the ADRAVN occurs just before a RFHRQ the pulse stretching network R12, R13, C6 insures the setting of the CIP latch. Delay line time is begun and the refresh is blocked at Z35-2 before RFHCLK goes high.

During a write cycle, if refresh has been blocked at the beginning or occurs after the beginning, the cycle may be interrupted if RADVLDN has not yet clocked flip-flop Z31-5. Contention is resolved at Z110-1, 2, 3 (Sheet 5) and at Z30-8, 9, 10. If a write cycle is not yet in progress, RFHQN will be passed at Z30-8 thus resetting the RAS and CAS latches. After appropriate delays at Z35-2, the refresh cycle will occur. Upon receipt of RADVLDN flip-flop Z31-5 will be clocked high and upon negation of RFHRON at Z110-1 will set the write latch. The signal WRSN at Z2-8 begins major delay line timing allowing the RAS and CAS latches to again be set. The write cycle then proceeds as normal.

7.4.4.7 Power Up Clear (Sheet 12)

The Power Up Clear cycle proceeds as follows: (See Figure 7.16)

1) Upon power up transistor Q1 is on (CINTN asserted) and remains on until the +5B and +15 volts have exceeded preset values. Counters Z46, Z47, Z48 are reset. Flip-flop Z42-13, Z44-14 are cleared. CINTN and CLBY are asserted. And gate Z41 is disabled.

2) On power up CINTN is negated enabling and gate Z41-11. The delayed signal at Z41-8 becomes CLSTR which creates an internal write cycle. CLBY remains high disabling memory bus addresses. CLBYN enables power up clear address drivers Z73, Z74, Z75.

3) The timing signal BION via and Z43-11, 12, 13 advances the address counters and clocks the current address into flip-flop Z44-12. BION delayed via one shot Z64 clocks the newly advanced address into flip-flop Z44-2. Flip-flops Z44-6 and Z44-9 along with and gate Z43-8, 9, 10 form a comparison circuit to determine if maximum counter address has been reached. If max address has not been reached, Z43-8 remains low allowing CLBYN to be reclocked low at Z42-12. CLBY continues to enable and gate Z41-9 thus allowing another CLSTR signal.

4) The process of step three continues until maximum address count has been reached. Z43-8 goes high allowing CLBYN to be negated at flip-flop Z42-9. The cycle is complete.

7.4.4.8 Error Log (Sheet 7)

The error log is written as follows:

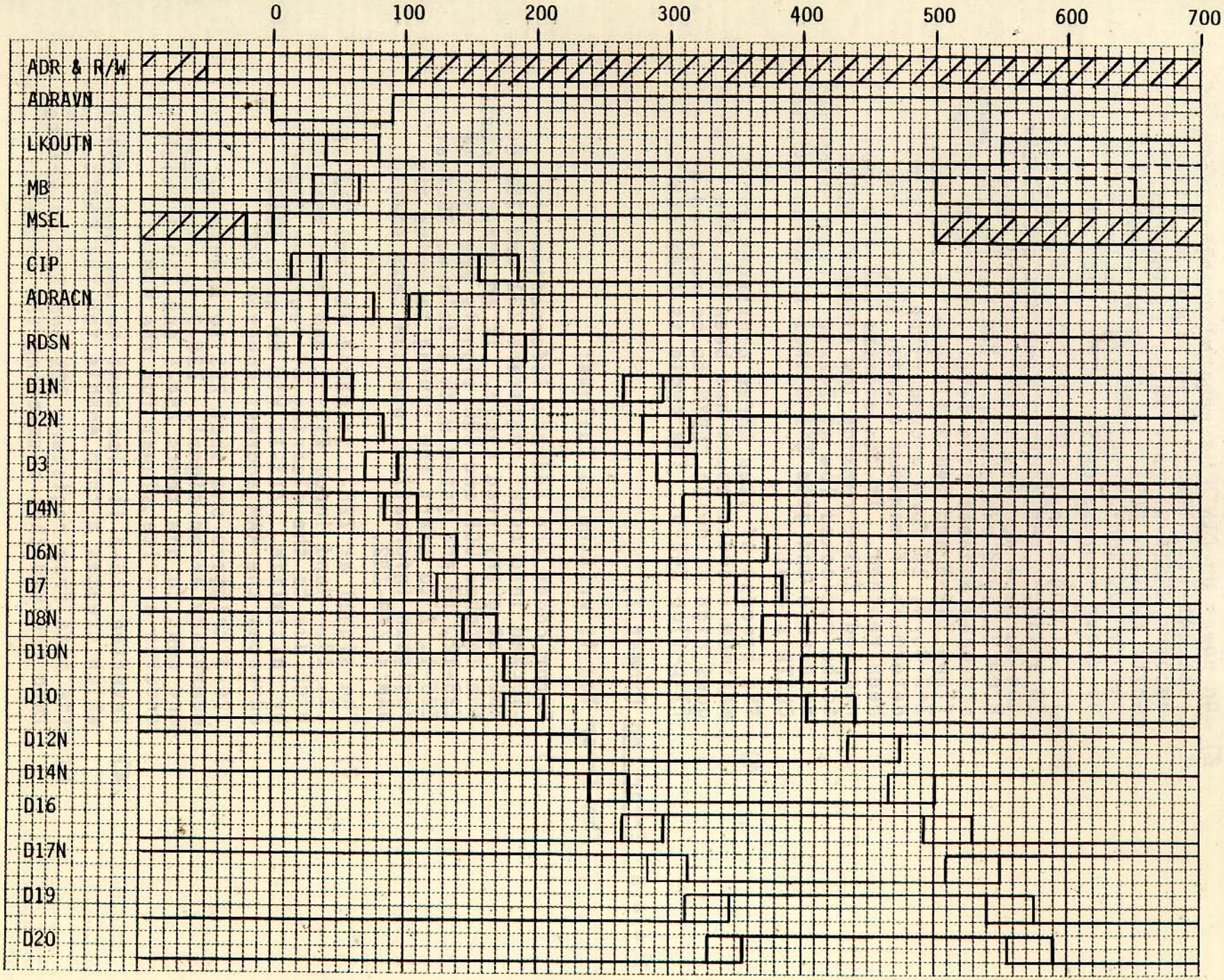
1) Error codes and address information are clocked into octal registers Z21 and Z22 by RDLA at every read cycle. If an error occurs, the latched UCE and CRE signals are ORed at Z25-12, 13 and gated with a delayed RDLA at Z26-1, 2 to start the timing to write the register information into the CMOS static RAM's Z49-Z52.

2) The signal at Z26-3 is gated at nand Z13-11, 12, 13. Nand input Z13-12 has been enabled high due to the clearing of register Z70-6 by initialize. Z13-11 via or gate Z24-4 advances the RAM address counter Z23.

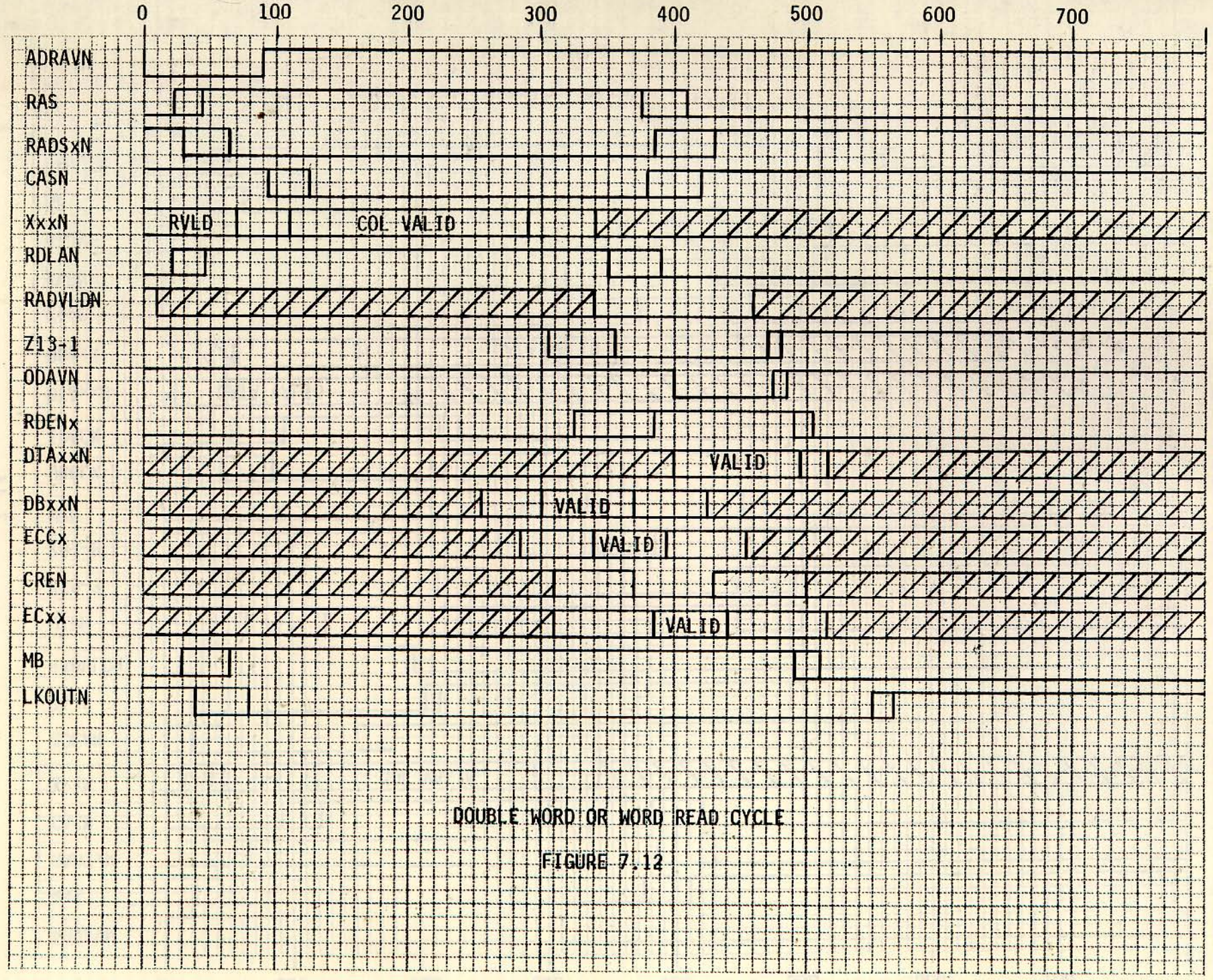
3) Z26-3 triggers one shot Z53 to create a momentary error signal. Z26-3 is inverted and sent to one shots Z54-5 and Z19-4 which creates a write signal for the RAM's.

4) Inverted Z26-3 is also sent to one shot Z54-11 which creates a chip enable for the RAM's.

5) The data from registers Z21 and Z22 is written into the RAM thus completing the write.



DELAY LINE TIMING
FIGURE 7.11



DOUBLE WORD OR WORD READ CYCLE

FIGURE 7.12

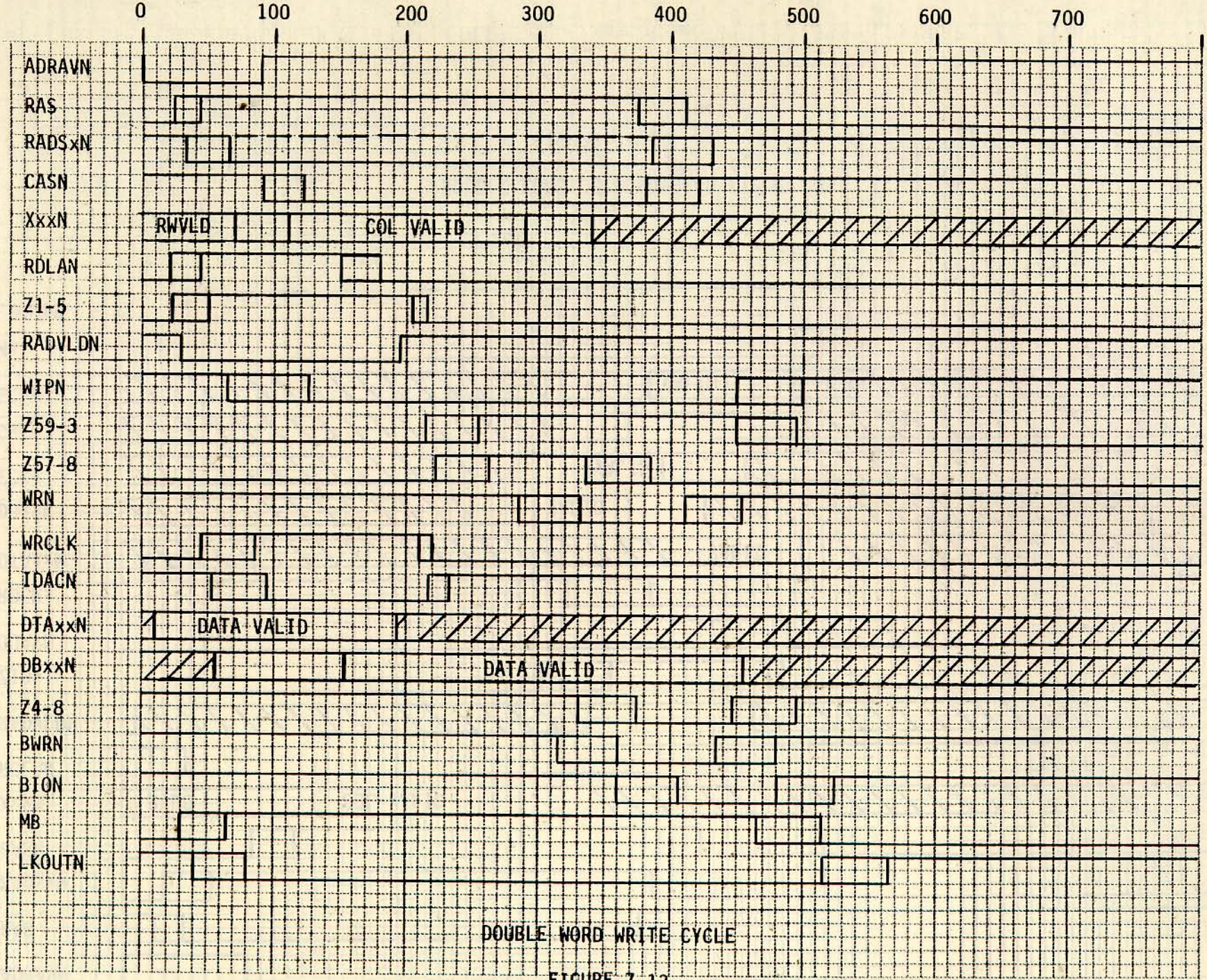
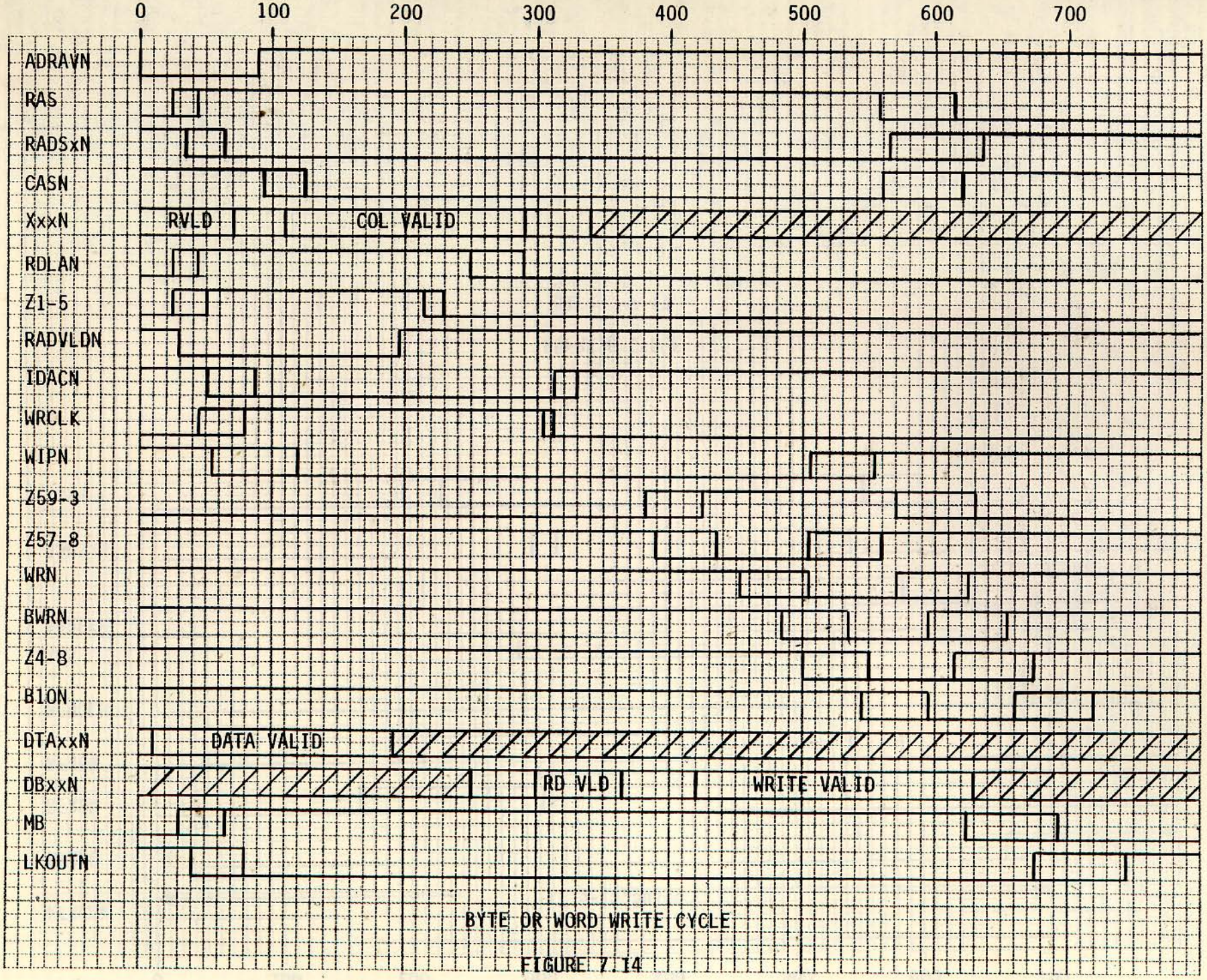
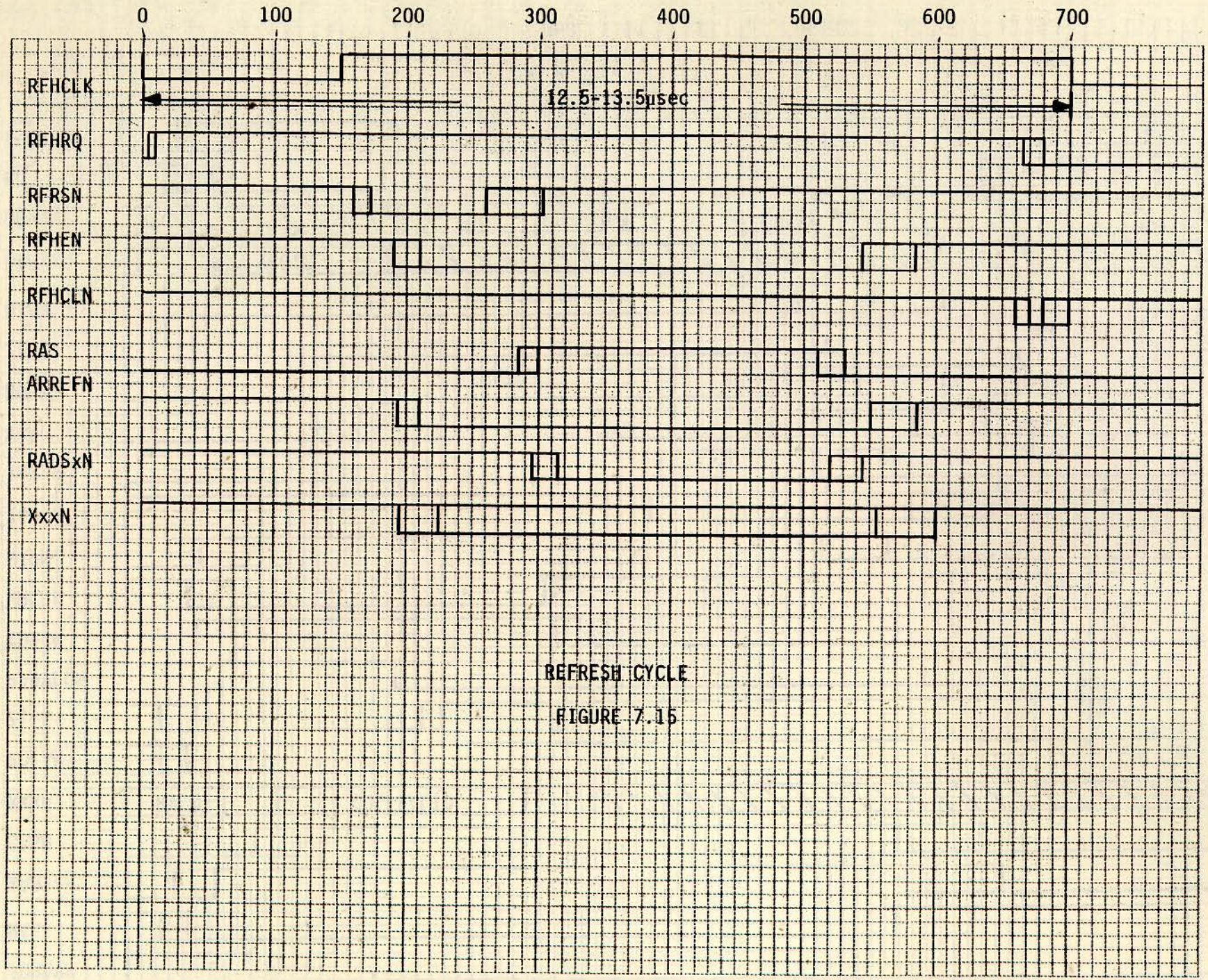

0
100
200
300
400
500
600
700
ADRAVN
RAS
RADSxN
CASN
XxxN
RWVLD
COL VALID
RDLAN
Z1-5
RADVLDN
WIPN
Z59-3
Z57-8
WRN
WRCLK
IDACN
DTAxxN
DATA VALID
DBxxN
DATA VALID
Z4-8
BWRN
BION
MB
LKOUTN
DOUBLE WORD WRITE CYCLE

FIGURE 7.13



BYTE OR WORD WRITE CYCLE

FIGURE 7.14



REFRESH CYCLE

FIGURE 7.15

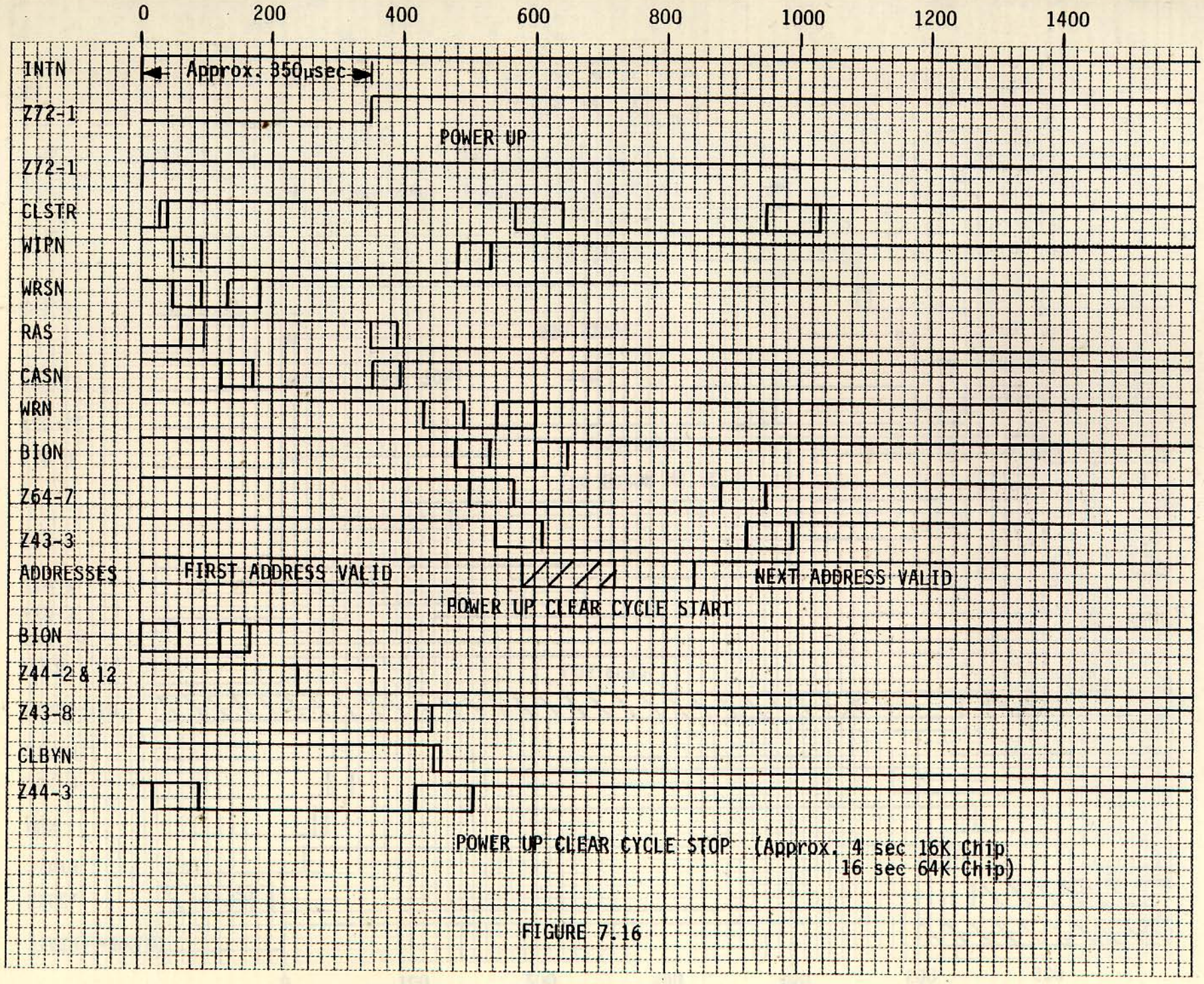

0
200
400
600
800
1000
1200
1400
INTN
Approx. 350μsec
Z72-1
POWER UP
Z72-1
CLSTR
WIPN
WRSN
RAS
CASN
WRN
BION
Z64-7
Z43-3
ADDRESSES
FIRST ADDRESS VALID
NEXT ADDRESS VALID
POWER UP CLEAR CYCLE START
BION
Z44-2 & 12
Z43-8
CLBYN
Z44-3
POWER UP CLEAR CYCLE STOP (Approx. 4 sec 16K Chip
16 sec 64K Chip)

FIGURE 7.16

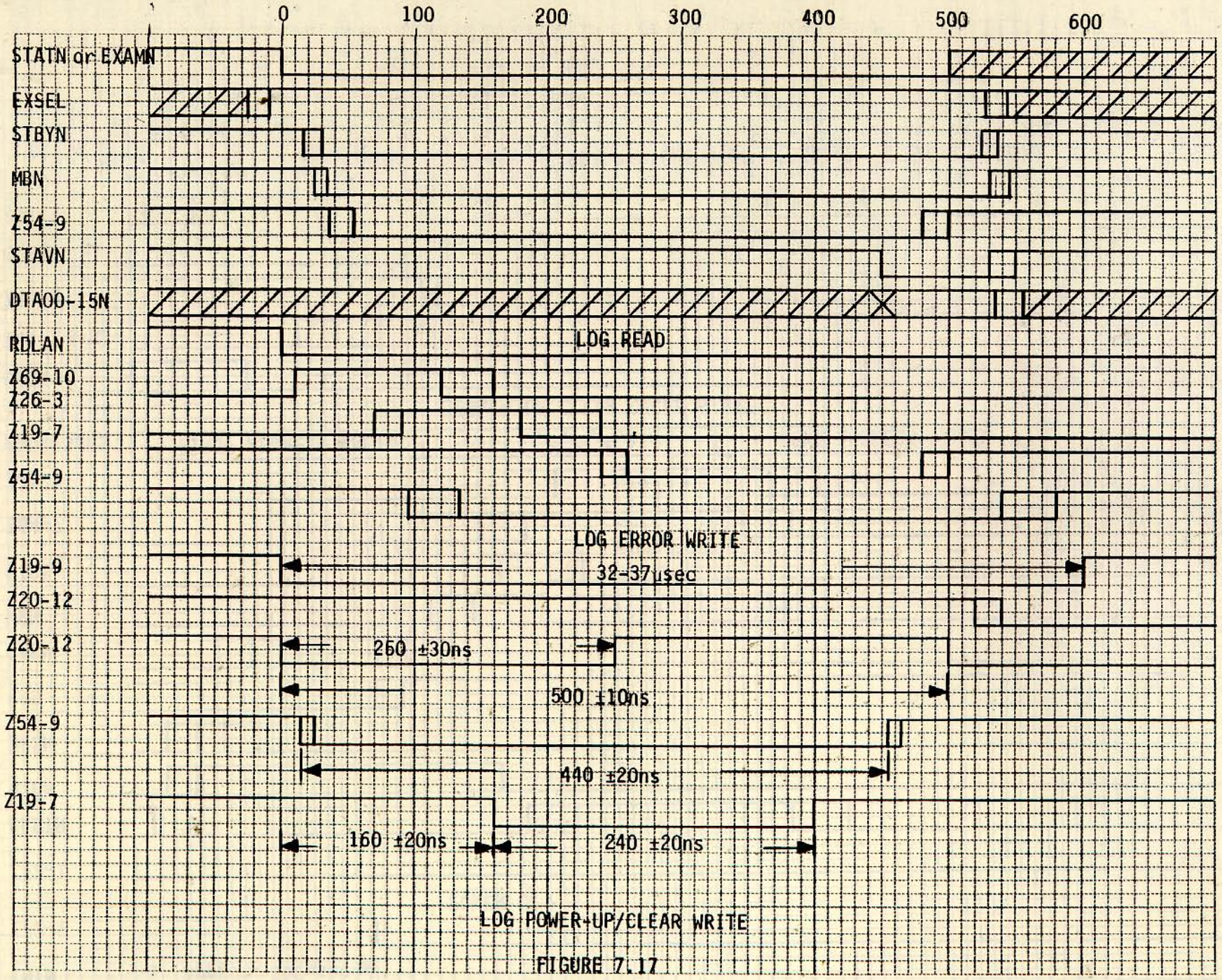

0
100
200
300
400
500
600
STATN or EXAMN
EXSEL
STBYN
MBN
Z54-9
STAVN
DTA00-15N
RDLAN
LOG READ
Z69-10
Z26-3
Z19-7
Z54-9
LOG ERROR WRITE
Z19-9
32-37 µsec
Z20-12
Z20-12
250 ±30ns
500 ±10ns
Z54-9
440 ±20ns
Z19-7
160 ±20ns
240 ±20ns
LOG POWER-UP/CLEAR WRITE

FIGURE 7.17

The error log is read as follows:

1) STATN or EXAMN is asserted low presetting flip-flop at Z27-10 to assert STBY and STBYN. One shot Z45-4, 5 is also triggered.

2) After a 400 nanosecond time out the one shot Z45-7 enables STAVN on the memory bus.

3) The assertion of STBYN at Z6-13 triggers one shot Z54-11 to create the chip enable signal to read the RAM's.

4) The assertion of STBY clocks a low to Z70-6 which prevents the address counter from advancing the next time the error log is written.

5) Upon negation of STATN or EXAMN Z81-8 goes high clocking a low to Z27-9 and disabling STATN gate Z108-11. The negation of STBY and STBYN creates a pulse at Z25-4, 5, 6, which advances the address counter.

An error log clear cycle proceeds as follows:

1) The assertion of CINT or CLRBN triggers one shot Z19-11, 12. The one shot delay is set for greater than 32 microseconds.

2) The one shot $\overline{Q}$ output Z19-9 is inverted at Z72-3, 4 and tristates the registers Z21 and Z22 which have pullups on their outputs.

3) The low going edge of one shot Z19-9 triggers the multivibrator pair Z20. The multivibrator oscillates with a 500 nanosecond period and triggers one shots Z54-12 and Z54-4 which create chip enable and write enable signals to the RAM's. The address counter is advanced via OR gate Z24-3 at the end of each period. All highs are written into the static RAM's.

4) Step 3 continues until the address counter reaches its maximum count when the maximum address is inverted at Z80-3, 4 and used to reset one shot Z19-9. This disables multivibrator pair Z20.

5) At the resetting of Z19-9 a low going pulse is created at Z25-3 to reset the log full register and reset the address counter.

7.4.5 Match (Sheet 4)

The match circuitry compares last used addresses and mode information to determine if data is already stored in registers on the BSC.

At the end of each cycle the addresses and the mode signal RDALBN are clocked into registers Z137, Z141, Z145 by the trailing edge of MBN. At the start of the next cycle, the stored addresses and mode are compared with the current addresses and mode at comparators Z135, Z139, Z143, Z147. If the old and new addresses and mode agree, the A=B outputs of the comparators are asserted high. The resultant highs at nand gate Z178 inputs assert MATCHN low at Z178-8.

8.0 DOCUMENTATION

Schematic Diagram

Document No. 03191, BSC
03183, BSA

System Assembly Drawing

Document No. 62901, BSC
62902, BSA

System Bill of Materials

Document No. 62901, BSC
62902, BSA

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED & REDRAWN PER ECN 1878 & 1879	5-20-80	
	B	ECN 1906	5-20-80	
	C	ECN 1919	5-20-80	
	D	ECN 1920	5-20-80	
	E	ECN 1940	24 JUL 80	RK
	F	ECN 1975	24 JUL 80	RK
	G	ECN 1998	24 JUL 80	RK
	H	ECN 2000	24 JUL 80	RK
	J	ECN 2049	15 SEP 80	RK
	K	ECN 2058	15 SEP 80	RK
	L	ECN 2341	16 FEB 82	RK
	M	ECN 2360	16 FEB 82	RK
	N	ECN 2412	16 FEB 82	RK
	P	ECN 2527	16 FEB 82	RK
	R	ECN 2562 BRT	16 FEB 82	RK

CLRBYN

CLEAR SHT 7

RFSH ADD CNTR SHT 3

ADROON-ADR24N

ADDRESS LATCH SHT 3&4

AD00-AD20

AD21-AD24

ADDRESS TRANSLATION SHT 3&4

MUX ADD DRVRS SHT 3

X07N-X14,15N

RWA0ON-RWA02N

ROW DRVRS SHT 3

RA0SON-RA07N

EX ADD DRVRS SHT 4

EXA0ON-EXA03N

MEMSIZE & SELECT SHT 4

MEMSIZE0-6

MSIZ0-MSIZ3

RFHEN

RFSH TIMING SHT 5

MODE LATCH SHT 6

MRD2N, MWRLBN, MWRUBN, MWRLBAN, MWRUBAN

SEL

EXSEL

ARREFN

RBEN

P10

ARRAY BUS

P9

MEMORY BUS

ADRAVN

ADRACN

RADVLDN

ODAVN

IDACN

MBYN

PWRINTN

NORMN

TIMING & CONTROL SHT 5&6

WXBXN

IWXBXN

WR CLK

RDLAN

DATA RCVRS SHT 9

DTA18N - DTA35N

DATA RCVRS 18 BIT ONLY SHT 9

DATA RCVRS SHT 9

DTA0ON-DTA17N

DATA REGISTERS SHT 9

DATA DRVRS SHT 9

DATA DRVRS SHT 8

DB0ON THRU DB35N

DATA DRVRS SHT 10

DATA DRVRS 18 BIT ONLY SHT 10

DATA DRVRS SHT 10

READ LATCH SHT 8

ERROR CORRECTION SHT 8&12

DI0ON THRU DI35N

DATA RCVR SHT 8

ECC

ERROR CODE GENERATION SHT 11

CODE RCVR SHT 12

DB36N-DB42N

CC

ERROR LOG DATA MUX SHT 10

RM00-RM15

ERROR LOG SHT 7

CODE DRVR SHT 12

RWA0ON-RWA03N

EXA0ON-EXA03N

LGFUL

ERR

CRERN

UCERN

STATN

EXAMN

STAVN

CLRN

BGN

62901/62904	BULK SEMI
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN JOHNSON	MAY 5 80
CHECKED	5-20-80
ENG	5-20-80
APPROVED RK	20 MAY 80

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
BULK SEMI CONTROLLER

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R

SCALE NONE SHEET 1 OF 12

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

P9

2	GND	GND	1
4	+5V	+5V	3
6	DTA06N	DTA15N	5
8	ADR07N	ADR05N	7
10		DAT07N	9
12		ADR19N	11
14	DTA32N	DTA14N	13
16	DTA24N	ADR06N	15
18	DTA34N	DTA16N	17
20	DTA25N	ADR13N	19
22	DTA23N	DTA05N	21
24	DTA33N	ADR03N	23
26	DTA35N	DTA17N	25
28	ADR24N	ADR15N	27
30	DTA31N	DTA13N	29
32	STATN	ADR16N	31
34	DTA22N	DTA04N	33
36	STAVN	ADR10N	35
38	UCERN	IDACN	37
40	CRERN	ADR00N	39
42	CLRBYN	ODAVN	41
44	MEMSIZE3	ADR04N	43
46	MEMSIZE4	ADRACN	45
48	MEMSIZE5	ADR12N	47
50	MEMSIZE6	ADR08N	49
52		ADR01N	51
54	ADR20N	ADR09N	53
56	ADR21N	ADR02N	55
58	ADR22N	ADR11N	57
60	GND	GND	59
62	ADR23N	ADRAVN	61
64	GND	GND	63
66	MWRUBAN	MWRUBN	65
68		PWINTN	67
70		MRDRN	69
72		NORMN	71
74	MWRLBAN	MWRLBN	73
76		RADVLDN	75
78	GND	GND	77
80		ADR17N	79
82		ADR18N	81
84		ADR19N	83
86			85
88			87
90			89
92	DTA26N	DTA08N	91
94	DTA21N	DTA03N	93
96	DTA30N	DTA12N	95
98	DTA18N	DTA00N	97
100	DTA29N	DTA11N	99
102		MEMSIZ2	101
104	DTA27N	DTA09N	103
106		MEMSIZ1	105
108	DTA20N	DTA02N	107
110	DTA28N	DTA10N	109
112	DTA19N	DTA01N	111
114	MBYN	MEMSIZ0	113
116	+5V	+5V	115
118	GND	GND	117
120	GND	GND	119

P10

2	+15V	+15V	1
4	+15V	+15V	3
6	GND	GND	5
8	GND	GND	7
10	+5V	+5V	9
12	EXAD3N	EXADON	11
14	EXAD2N	EXADIN	13
16	ARREFN	RBEN	15
18	MSIZ3	MSIZ1	17
20			19
22			21
24	MSIZ2	MSIZ0	23
26			25
28	RADS1	RADS3	27
30	RADS5	RADS7	29
32	RADS0	RADS2	31
34	RADS4	RADS6	33
36	+5B	+5B	35
38	+5B	+5B	37
40	X1415N	X411N	39
42	Y07N	X310N	41
44	X512N	X18N	43
46	X613N	X29N	45
48	CASN	WRN	47
50	DB42N	GND	49
52	DB41N	GND	51
54	DB40N	GND	53
56	GND	GND	55
58	DB14N	DB00N	57
60	DB12N	DB03N	59
62	DB15N	DB02N	61
64	DB13N	DB05N	63
66	GND	GND	65
68	GND	GND	67
70	DB19N	DB01N	69
72	DB16N	DB06N	71
74	DB17N	DB04N	73
76	DB23N	DB07N	75
78	+5V	+5V	77
80	+5V	+5V	79
82	DB20N	DB08N	81
84	DB22N	DB10N	83
86	DB18N	DB11N	85
88	DB21N	DB09N	87
90	DB37N	GND	89
92	DB39N	GND	91
94	DB36N	GND	93
96	DB38N	GND	95
98	DB34N	GND	97
100	DB33N	GND	99
102	DB35N	GND	101
104	DB32N	GND	103
106	DB28N	GND	105
108	DB27N	GND	107
110	DB29N	EXAMN	109
112	DB31N	LGFL	111
114	DB30N	ERR	113
116	DB24N	CLR	115
118	DB26N	BGN	117
120	DB25N	GND	119

NOTE 5

"E" POINT	LOCATION	"E" POINT	LOCATION
1	12C3	61	7C4
2	12C3	62	7C4
3	4B1	63	7C4
4	4B1	64	7C4
5	9D3	65	7C4
6	9D3	66	7C4
7	3A6	67	5C4
8	3A6	68	5C4
9	12B7	69	12A3
10	12B7	70	12A3
11	4A6	71	12A3
12	4A6	72	7C4
13	4D2	73	10B3
14	4D2	74	10B3
15	4D2	75	12A6
16	4D2	76	12A6
17	4D2	77	12C3
18	4D2	78	12C3
19	4D2	79	7C8
20	4D2	80	7C8
21	4D2	81	7C8
22	4D2	82	NOT USED
23	4D2	83	NOT USED
24	4D3	84	5D8
25	4D3	85	5D8
26	4B1	86	5B7
27	4B1	87	5B7
28	4B1		
29	4A1		
30	4A1		
31	4A1		
32	4A1		
33	4A1		
34	4A1		
35	4A1		
36	4B1		
37	4A1		
38	4A1		
39	4A1		
40	4A1		
41	4A1		
42	4A1		
43	4D3		
44	4D4		
45	4A2		
46	4A2		
47	6D7		
48	6C7		
49	6C7		
50	6C7		
51	4B2		
52	4B2		
53	6C7		
54	6C7		
55	6C5		
56	6C5		
57	4A2		
58	4A2		
59	6B8		
60	6B8		

LAST DESIGNATION USED	
INTEGRATED CIRCUIT	Z218
JUMPER	E87
RESISTOR	R116
CAPACITOR	C99
RESISTOR MODULE	RM22
TRANSISTOR	Q6
DIODE	CR6
INDUCTOR	L4

REFERENCE DESIGNATION	GATES USED PER TOTAL	PART NUMBER
Z11	1/4	74S132
Z15	3/3	74S10
Z26	3/4	74LS08
Z36	3/4	74S08
Z38	5/6	74S04
Z40	2/3	74S10
Z25	3/4	74LS32
Z45	1/2	26S02
Z59	3/4	74S132
Z60	1/3	74S10
Z64	1/2	26S02
Z70	1/2	74LS74
Z80	5/6	74LS04
Z81	3/4	74132
Z89	2/4	74S86
Z103	4/8	74S240
Z107	2/8	74S240
Z110	2/4	74S38
Z121	4/8	74S374
Z122	2/8	74S240
Z123	4/8	74S373
Z154	5/6	74S04
Z162	2/8	74S240
Z163	2/8	74S240
Z164	2/8	74S240
Z165	4/8	74S241
Z173	1/4	74S257
Z181	3/4	74LS32
Z183	1/2	75453
Z185	4/8	74S240
Z186	4/8	74S241
Z197	3/4	74S08
Z199	3/4	74S257
ZZ01	5/8	74S373
ZZ02	1/6	74LS241
ZZ11	1/3	74S11
ZZ12	1/2	74S20
ZZ13		SPARE
ZZ14		SPARE
ZZ15	1/4	74S32
ZZ17	3/4	74S38
ZZ18	2/4	74S38

OPTIONS	
JUMPER	FUNCTION
E1 TO E2	ODD/EVEN PARITY
E73 TO E74	JUMPER TO DISABLE PARITY ERROR

JUMPER	FUNCTION
E43 TO E44	JUMPER FOR 16K CHIPS-ADDR MUX
E51 TO E52	JUMPER TO DISABLE MEMSIZ
E69 TO E71	CUT FOR 64K CHIPS - CLRBY
E69 TO E70	JUMPER FOR 64K CHIPS - CLRBY
E79 TO E80	JUMPER FOR NORMAL LOG OPERATION

JUMPER FOR 36 BIT OPERATION	
JUMPER	FUNCTION
E5 TO E6	WORD DISABLE
E7 TO E8	ADDR MUX
E11 TO E12	DISABLE MATCH
E24 TO E25	ADDR MUX
E49 TO E53	MODE CONTR
E50 TO E54	MODE CONTR
E59 TO E60	WORD DISABLE

TEST PURPOSES ONLY	
JUMPER	FUNCTION
E9 TO E10	REMOVE JUMPER TO DISABLE ECC INTO PTREE
E67 TO E68	JUMPER TO DISABLE REFRESH
E75 TO E76	JUMPER TO DISABLE ECC CORRECTION
E77 TO E78	JUMPER TO DISABLE CLEAR
E80 TO E81	JUMPER TO SET UP LOG TIMING
E84 TO E85	OPEN FOR TEST (MBN BYPASS) JUMPER FOR NORMAL OPERATION
E86 TO E87	OPEN FOR TIMEOUT CHECK JUMPER FOR NORMAL OPERATION

JUMPER FOR 18 BIT OPERATION	
JUMPER	FUNCTION
E47 TO E53	MODE CONTR
E48 TO E54	MODE CONTR
E55 TO E56	WRALB DISABLE

MEMSIZ CONFIGURATION WIRING

CONFIGURATION	JUMPERS	CONFIGURATION	JUMPERS
18 BIT BSC 16K RAM CHIPS	E3-E33, E4-E34, E29-E37, E30-E38, E31-E39, E32-E40, E41-E57, E42-E58	36 BIT BSC 16K RAM CHIPS	E29-E36, E30-E37, E31-E38, E32-E39, E4-E40, E41-E57, E42-E58
CHASSIS 1	E26-E45, E27-E46	CHASSIS 1	E26-E3, E27-E45, E28-E46
CHASSIS 2	E34-E45, E27-E46	CHASSIS 2	E33-E3, E27-E45, E28-E46
CHASSIS 3	E26-E45, E35-E46	CHASSIS 3	E26-E3, E34-E45, E28-E46
CHASSIS 4	E34-E45, E35-E46	CHASSIS 4	E33-E3, E34-E45, E28-E46
		CHASSIS 5	E26-E3, E27-E45, E35-E46
18 BIT BSC 64K RAM CHIPS CHASSIS 1	E4-E34, E57-E37, E58-E38, E29-E39, E30-E40, E31-E41, E32-E42, E3-E33, E45-E34, E46-E35	CHASSIS 6	E33-E3, E27-E45, E35-E46
		CHASSIS 7	E26-E3, E34-E45, E35-E46
		CHASSIS 8	E33-E3, E34-E45, E35-E46
		BIT BSC 64K RAM CHIPS	E4-E36, E57-E37, E29-E38, E30-E39, E31-E40, E32-E41, E58-E42, E3-E33, E45-E34
		CHASSIS 1	E46-E26
		CHASSIS 2	E46-E35

EXTERNAL SELECT STRAPPING

8MBYTES PER CHASSIS 36 BIT BSC 16K CHIPS

CHASSIS 1	E14-E21, E16-E22, E18-E23
CHASSIS 2	E13-E21, E16-E22, E18-E23
CHASSIS 3	E14-E21, E15-E22, E18-E23
CHASSIS 4	E13-E21, E15-E22, E18-E23
CHASSIS 5	E14-E21, E16-E22, E17-E23
CHASSIS 6	E13-E21, E16-E22, E17-E23
CHASSIS 7	E14-E21, E15-E22, E17-E23
CHASSIS 8	E13-E21, E15-E22, E17-E23

8MBYTES PER CHASSIS 18 BIT BSC 16K CHIPS

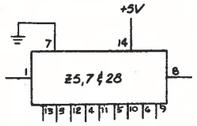
CHASSIS 1	E16-E21, E18-E22, E20-E23
CHASSIS 2	E15-E21, E18-E22, E20-E23
CHASSIS 3	E16-E21, E17-E22, E20-E23
CHASSIS 4	E15-E21, E17-E22, E20-E23
CHASSIS 5	E16-E21, E18-E22, E19-E23
CHASSIS 6	E15-E21, E18-E22, E19-E23
CHASSIS 7	E16-E21, E17-E22, E19-E23
CHASSIS 8	E15-E21, E17-E22, E19-E23

32MBYTES PER CHASSIS 36 BIT BSC 64K CHIPS

CHASSIS 1	E18-E22, E20-E23
CHASSIS 2	E17-E22, E20-E23
CHASSIS 3	E18-E22, E19-E23
CHASSIS 4	E17-E22, E19-E23

32MBYTES PER CHASSIS 18 BIT BSC 64K CHIPS

CHASSIS 1	E20-E23
CHASSIS 2	E19-E23



FOR REV H & LATER P.C. BOARDS (NOTE 4)

DETAIL A-

5. COMPONENTS USING +5B ARE BE INDICATED BY AN ASTERISK, *.
4. THE PINOUTS SHOWN IN DETAIL-A- SHALL APPLY TO REV H AND LATER P.C. BOARDS USING 150ns DIGITAL DELAY LINE DATARAM P/N 14108.
3. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W
2. CAPACITANCE VALUES ARE IN MICROFARADS
1. CAPACITANCE TOLERANCES AND VOLTAGES ARE AS FOLLOWS; PICOFARADS - ±5%, 100V; 4.7 MICROFARADS - ±20%, 10V; 15 MICROFARADS - ±20% 20V

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	8-21-79
CHECKED	5-20-80
ENG.	5-20-80
APPROVED	

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM, BULK SEMI CONTROLLER

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R

SCALE | SHEET 2 OF 12

03191

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9958

(6C3) RFHE

Z195 74LS393

+5V

R93 10K

WORDN (6A3,9A8)

Z172 74S04

WORD (6C2,9A8)

ADR00N P9-39
ADR01N P9-51
ADR02N P9-55
ADR03N P9-23

Z203 Z204 74S373

AD00N (4D8)
AD01N (4D8)
AD02N (4D8)
AD03N (4D8)

CLAD00N (12D1)
CLAD01N (12D1)
CLAD02N (12D1)
CLAD03N (12D1)

Z174 74S257

+5V

R98 10K

PU1 (4D5)

74LS241 Z203

ADR04N P9-43
ADR05N P9-7
ADR06N P9-15
ADR07N P9-8

AD04N (4C8)
AD05N (4C8)
AD06N (4C8)
AD07N (4C8)

CLAD04N (12D1)
CLAD05N (12D1)
CLAD06N (12C1)
CLAD07N (12C1)

Z175 74S257

Z205 Z206 74S373

ADR08N P9-49
ADR09N P9-53
ADR10N P9-35
ADR11N P9-57

AD08N (4C8)
AD09N (4C8)
AD10N (4C8)
AD11N (4C8)

CLAD08N (12C1)
CLAD09N (12C1)
CLAD10N (12C1)
CLAD11N (12C1)

Z176 74S257

74LS241 Z205

ADR12N P9-47
ADR13N P9-19
ADR14N P9-11
ADR15N P9-27

AD12N (4B8)
AD13N (4B8)
AD14N (4B8,4D4)
AD15N (4B8,4D4)

CLAD12N (12C1)
CLAD13N (12B1)
CLAD14N (12B1)
CLAD15N (12B1)

Z177 74S257

(5C3) MBN

(4D4) AD16N

Z173 74S257

CLAD16N (12B1)

+5V R94 10K

E7 JUMPER FOR 36 BITS

E8

(12C3) CLBY

Z194 74S240

Z192 Z193 74S241

RM9 +5V*

X07N P10-42
X18N P10-43
X29N P10-45
X310N P10-41
X411N P10-39
X512N P10-44
X613N P10-46
X1415N P10-40

(6C3) RFHEN
(5B2) D2N

Z197 74S08

Z154 74S04

Z196 74S00

(4D1) RWADON
(4D1) RWADIN
(4D1) RWAD2N

Z189 74S138

R101 10K +5V

(6C3) RFHEN
(6B6) RAS

Z197 74S08

Z197 74S08

74S240 Z191

74S241 Z190

RM5 +5V*

RADS7N P10-29
RADS6N P10-33
RADS5N P10-30
RADS4N P10-34
RADS3N P10-27
RADS2N P10-31
RADS1N P10-28
RM7
RADS0N P10-32

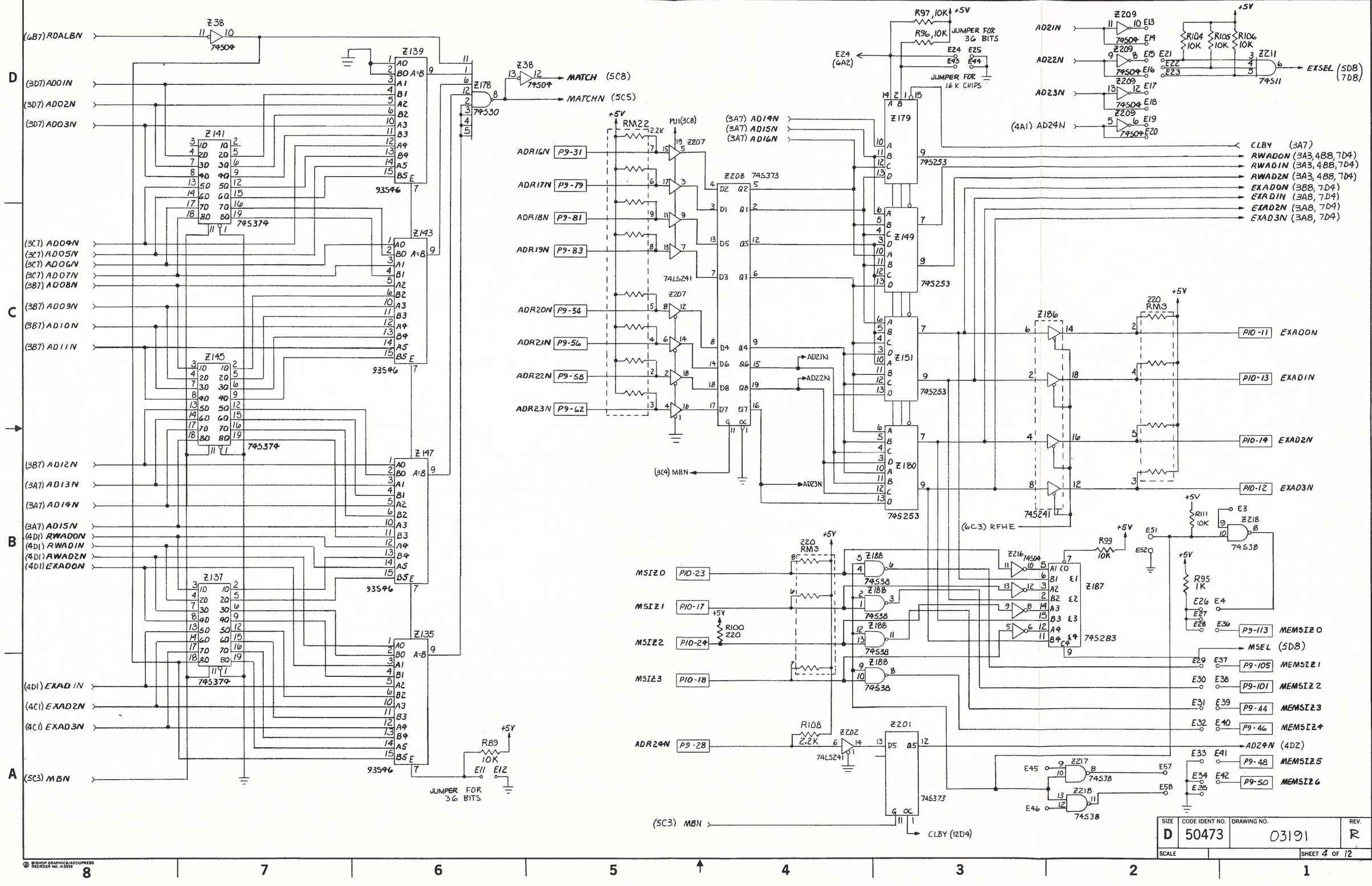
(6B6) RAS
(6C3) RFHEN

Z196 74S00

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE			SHEET 3 OF 12

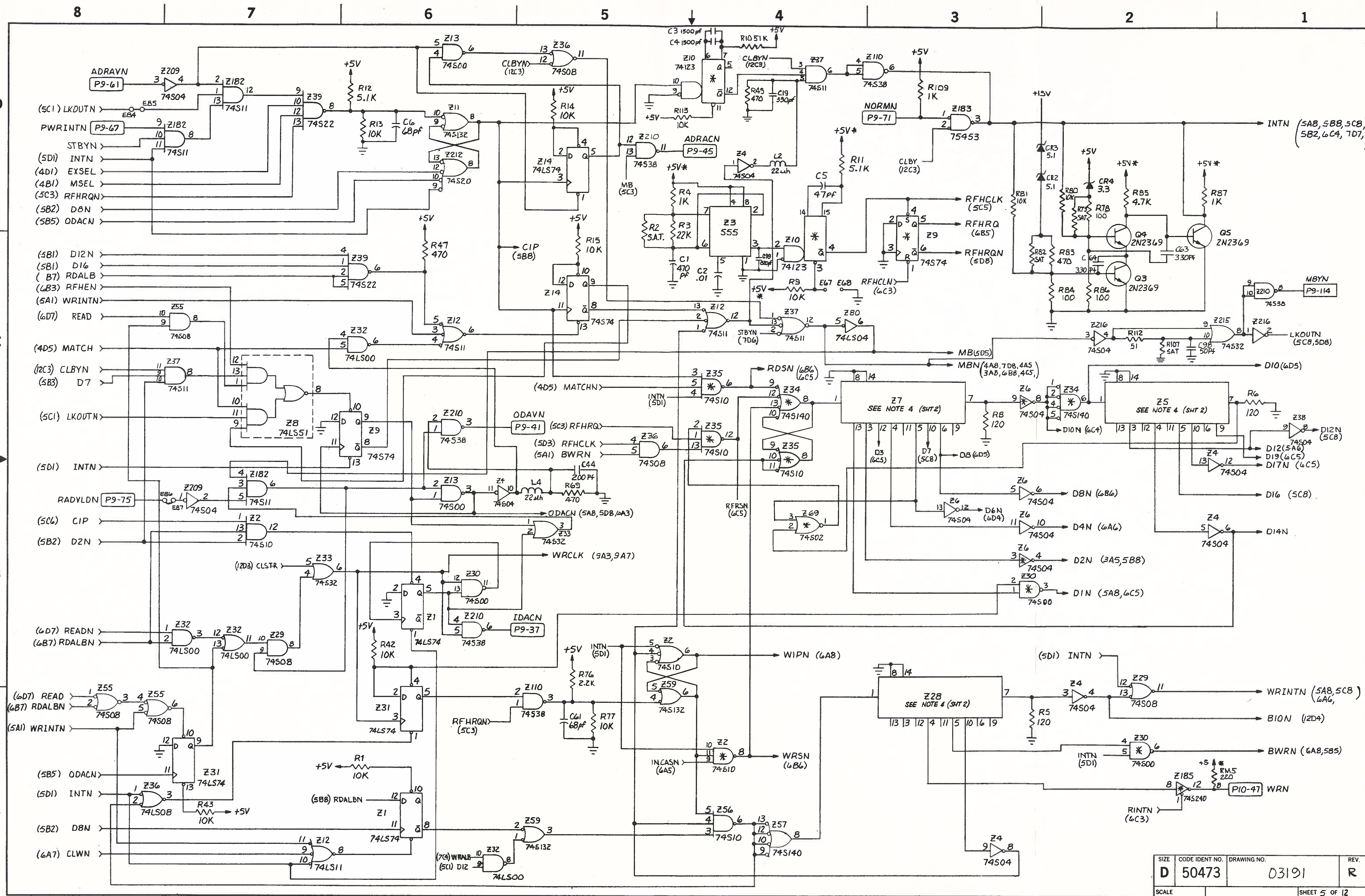
03191

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9559



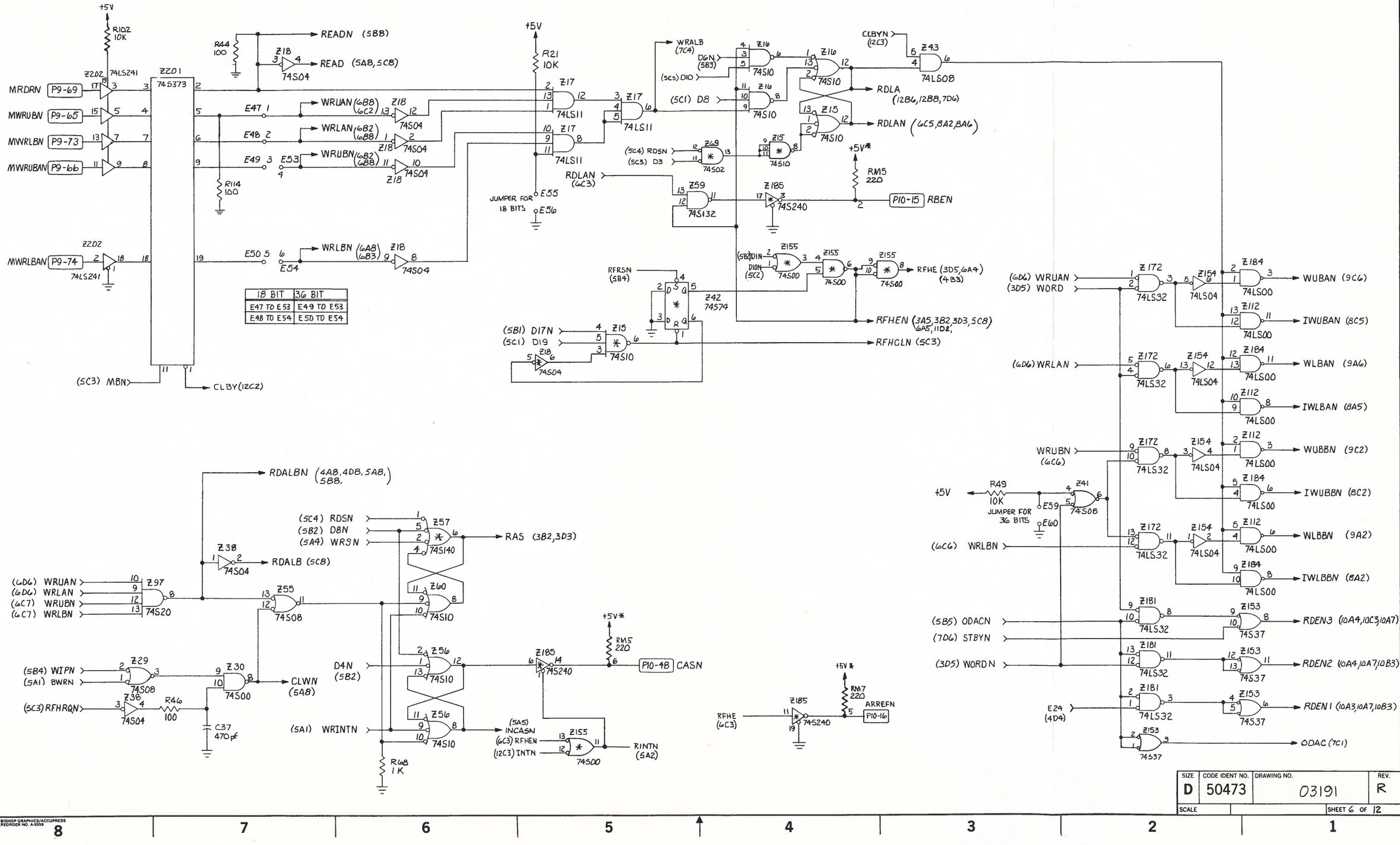
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 4 OF 12	

03191



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R

SCALE — SHEET 5 OF 12

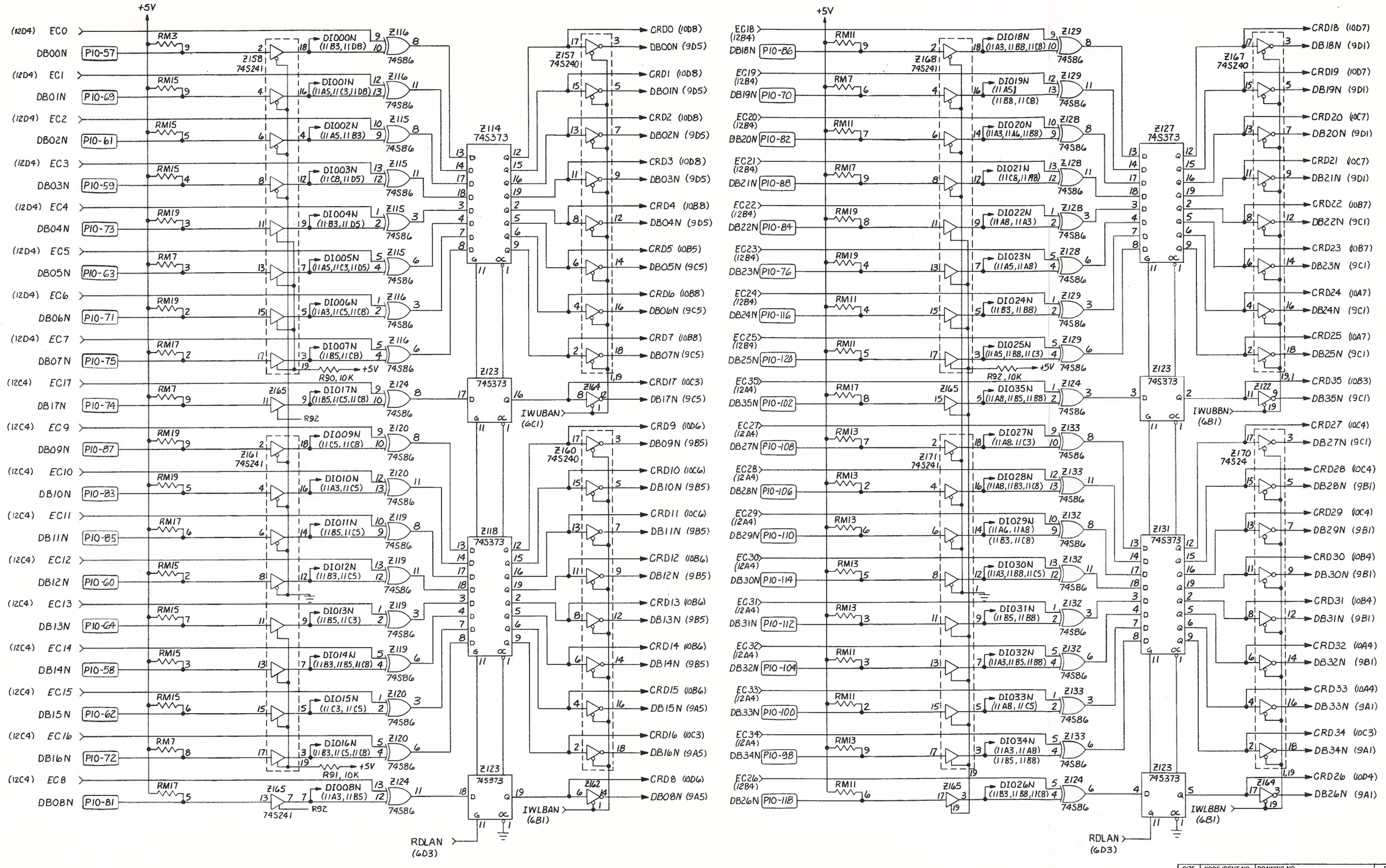


SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 6 OF 12	

03191

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9559

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 7 OF 12	



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
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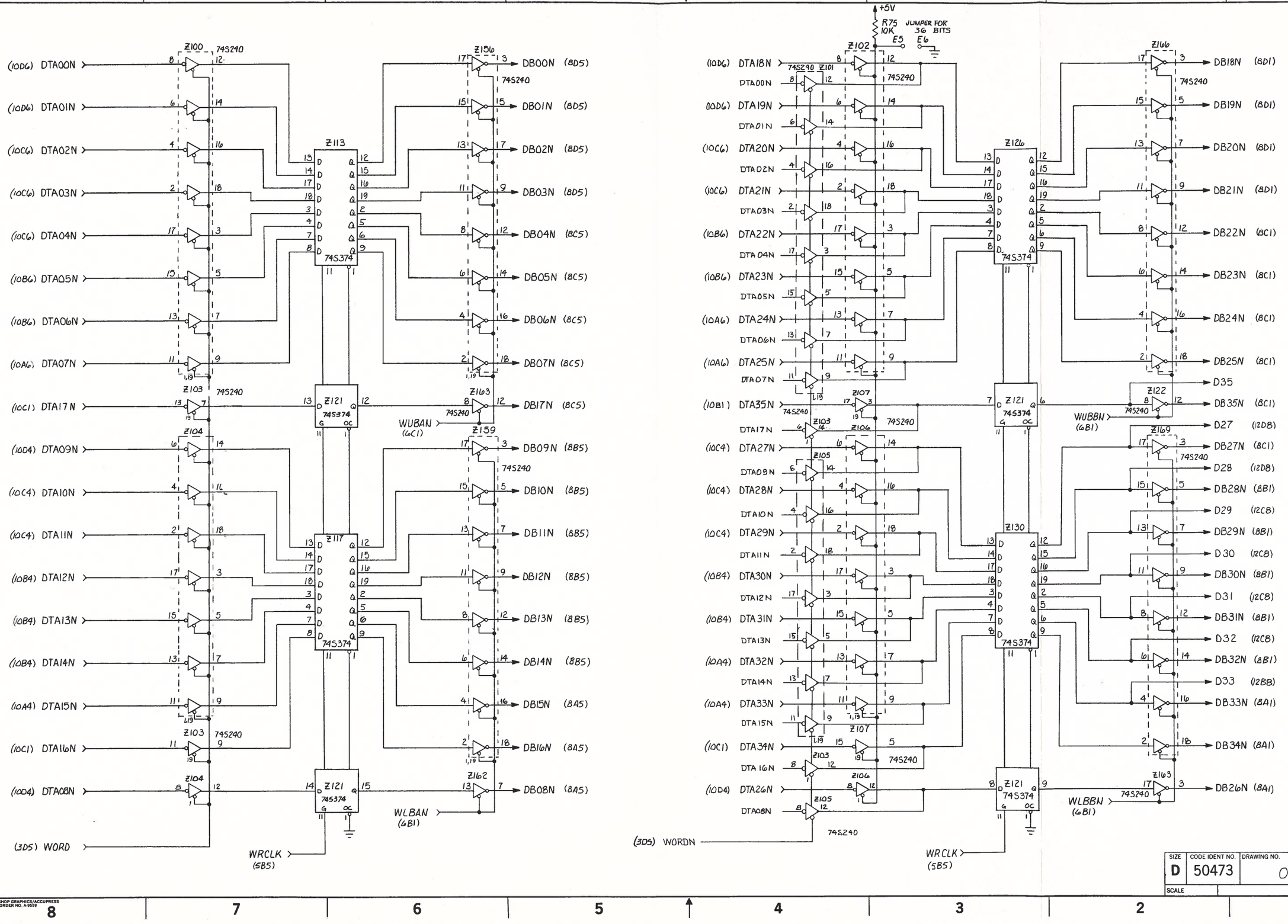
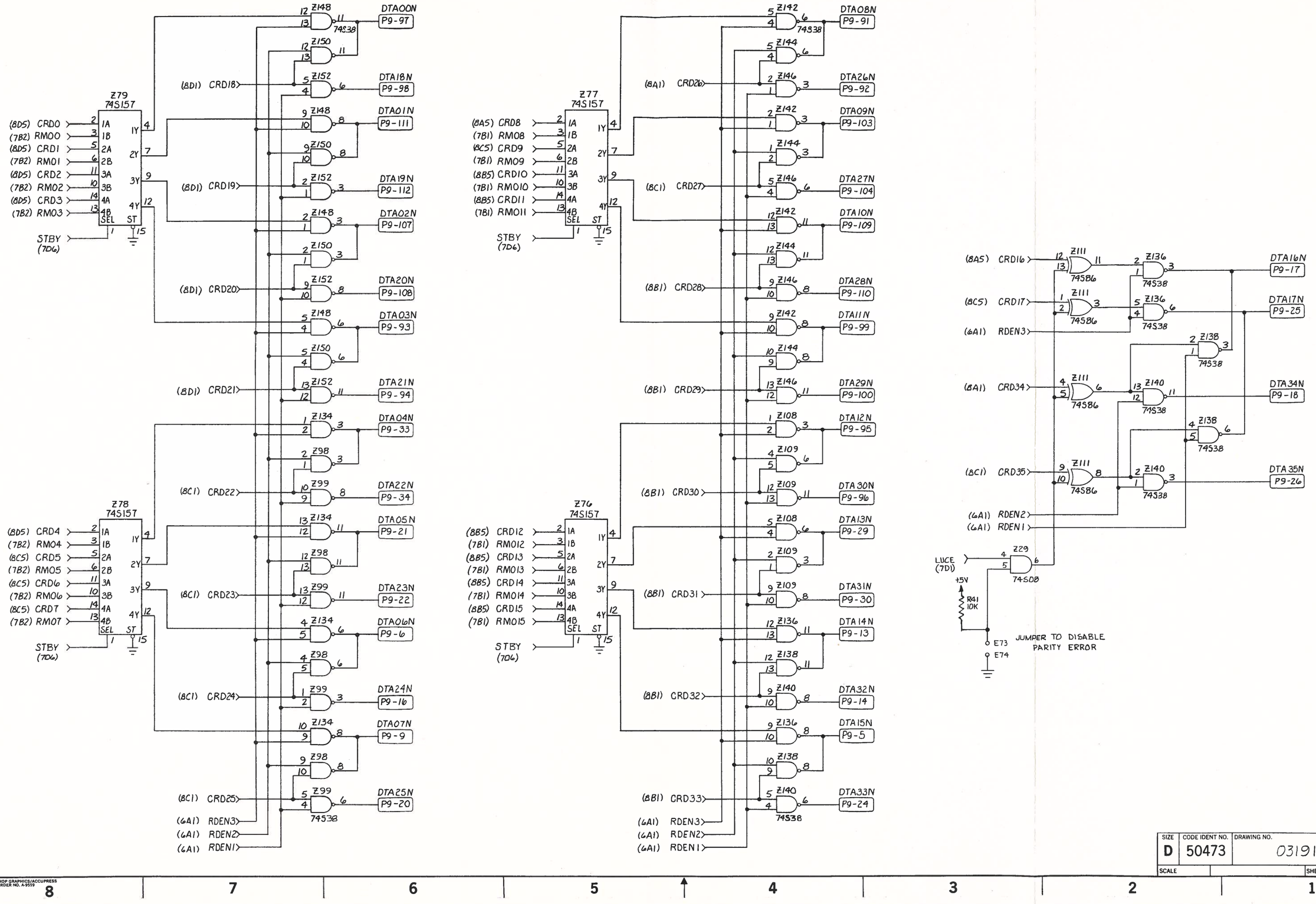
SCALE		SHEET 8 OF 12	

03191



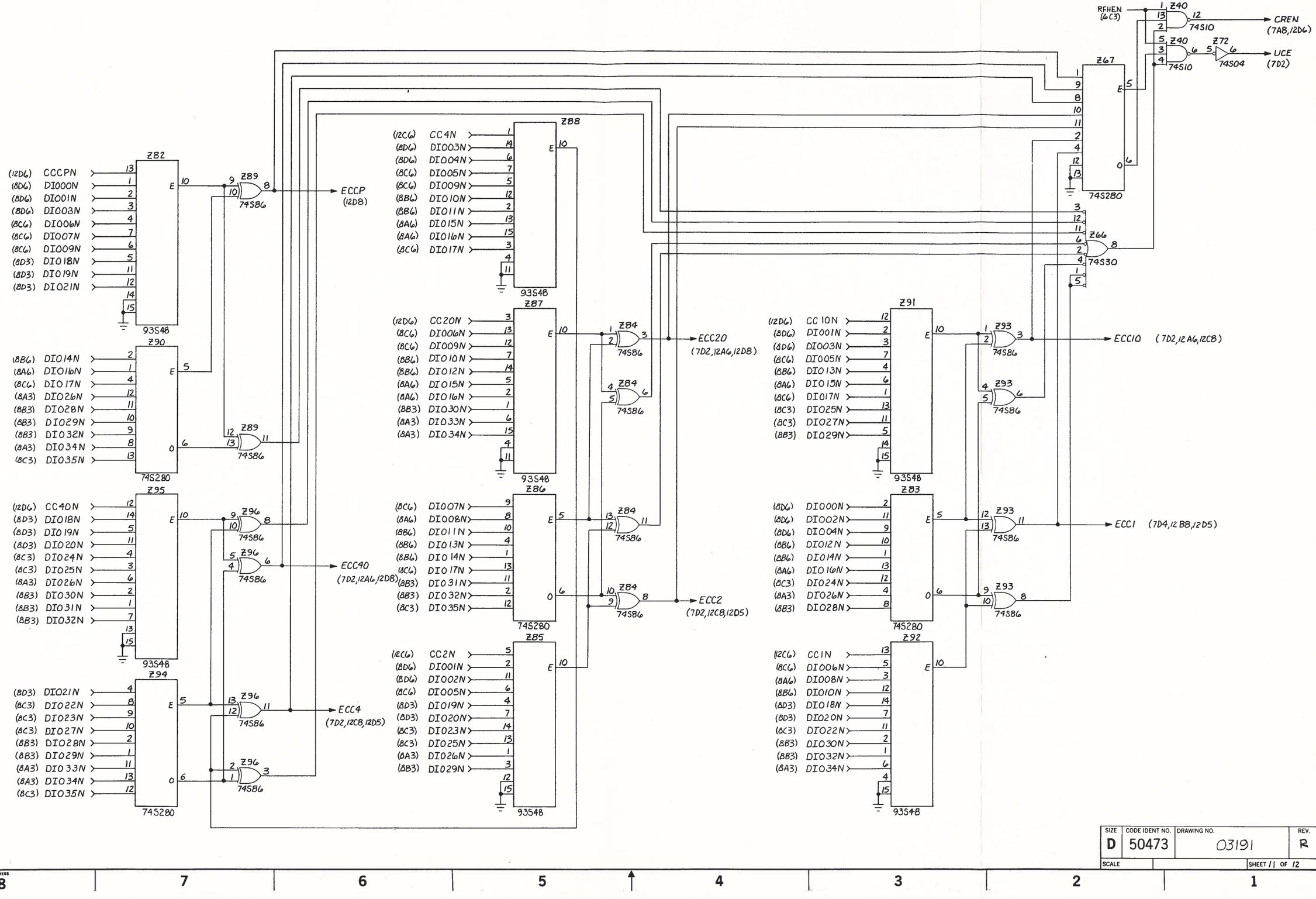
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 9 OF 12	

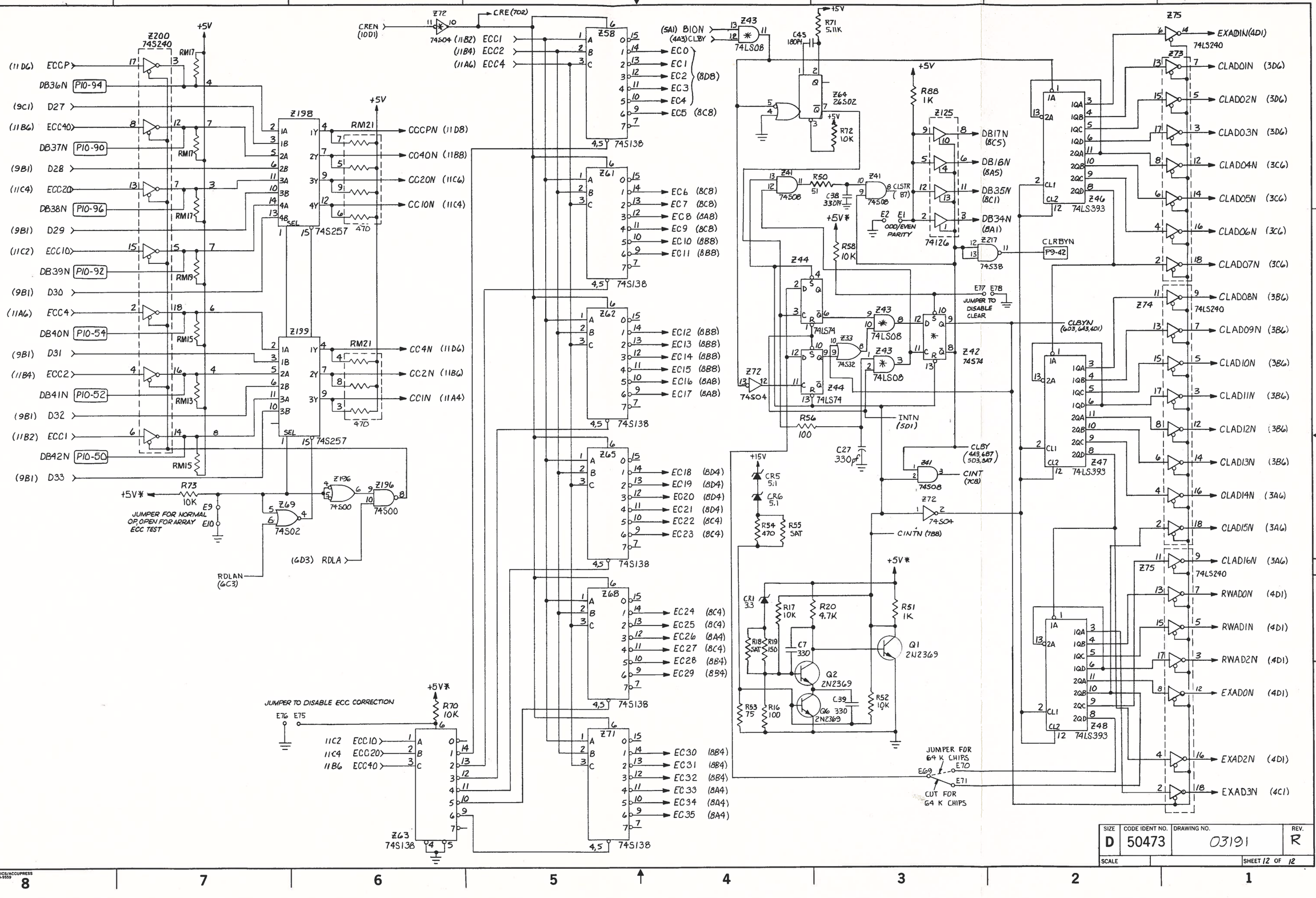
03191



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 10 OF 12	

03191


Z82
(12D6) CCCPN
(8D6) DI000N
(8D6) DI001N
(8D6) DI003N
(8C6) DI006N
(8C6) DI007N
(8C6) DI009N
(8D3) DI018N
(8D3) DI019N
(8D3) DI021N
93S48
Z90
(8B6) DI014N
(8A6) DI016N
(8C6) DI017N
(8A3) DI026N
(8B3) DI028N
(8B3) DI029N
(8B3) DI032N
(8A3) DI034N
(8C3) DI035N
74S280
Z95
(12D6) CC40N
(8D3) DI018N
(8D3) DI019N
(8D3) DI020N
(8C3) DI024N
(8C3) DI025N
(8A3) DI026N
(8B3) DI030N
(8B3) DI031N
(8B3) DI032N
93S48
Z94
(8D3) DI021N
(8C3) DI022N
(8C3) DI023N
(8C3) DI027N
(8B3) DI028N
(8B3) DI029N
(8A3) DI033N
(8A3) DI034N
(8C3) DI035N
74S280
Z89
74S86
Z89
74S86
Z96
74S86
Z96
74S86
Z96
74S86
ECCP
(12D8)
ECC40
(7D2,12A6,12D8)
ECC4
(7D2,12C8,12D5)
Z88
(12C6) CC4N
(8D6) DI003N
(8D6) DI004N
(8C6) DI005N
(8C6) DI009N
(8B6) DI010N
(8B6) DI011N
(8A6) DI015N
(8A6) DI016N
(8C6) DI017N
93S48
Z87
(12D6) CC20N
(8C6) DI006N
(8C6) DI009N
(8B6) DI010N
(8B6) DI012N
(8A6) DI015N
(8A6) DI016N
(8B3) DI030N
(8A3) DI033N
(8A3) DI034N
93S48
Z86
(8C6) DI007N
(8A6) DI008N
(8B6) DI011N
(8B6) DI013N
(8B6) DI014N
(8C6) DI017N
(8B3) DI031N
(8B3) DI032N
(8C3) DI035N
74S280
Z85
(12C6) CC2N
(8D6) DI001N
(8D6) DI002N
(8C6) DI005N
(8D3) DI019N
(8D3) DI020N
(8C3) DI023N
(8C3) DI025N
(8A3) DI026N
(8B3) DI029N
93S48
Z84
74S86
Z84
74S86
Z84
74S86
ECC20
(7D2,12A6,12D8)
ECC2
(7D2,12C8,12D5)
Z91
(12D6) CC10N
(8D6) DI001N
(8D6) DI003N
(8C6) DI005N
(8B6) DI013N
(8A6) DI015N
(8C6) DI017N
(8C3) DI025N
(8C3) DI027N
(8B3) DI029N
93S48
Z83
(8D6) DI000N
(8D6) DI002N
(8D6) DI004N
(8B6) DI012N
(8B6) DI014N
(8A6) DI016N
(8C3) DI024N
(8A3) DI026N
(8B3) DI028N
74S280
Z92
(12C6) CC1N
(8C6) DI006N
(8A6) DI008N
(8B6) DI010N
(8D3) DI018N
(8D3) DI020N
(8C3) DI022N
(8B3) DI030N
(8B3) DI032N
(8A3) DI034N
93S48
Z93
74S86
Z93
74S86
Z93
74S86
ECC10 (7D2,12A6,12C8)
ECC1 (7D4,12B8,12D5)
Z67
74S280
Z66
74S30
RFHEN (6C3)
Z40
74S10
CREN (7AB,12D6)
Z40
74S10
Z72
74S04
UCE (7D2)
03191
SIZE D
CODE IDENT NO. 50473
DRAWING NO. 03191
REV. R
SCALE
SHEET 11 OF 12
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9555



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03191	R
SCALE		SHEET 12 OF 12	

03191

LAST DESIGNATION USED	
INTEGRATED CIRCUIT	Z44
RESISTER	R165
CAPACITOR	C431
DIODE	CR48
RESISTER MODULE	RM1
VOLTAGE REGULATOR	VR2
TRANSISTOR	Q3

REF. DESIG.	GATES USED PER TOTAL	PART NUMBER
Z16	7/8	74LS240
Z17	3/4	74S38
Z18	4/8	74LS240
Z40	NOT USED	–
Z44	6/8	74S240

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X1	ECN 1678	16OCT79	RK
	X2	ECN 1679	16OCT79	RK
	A	ECN 1680 REL. TO PRODUCTION	16OCT79	RK
	B	ECN 1740	16OCT79	RK
	C	ECN 1741	16OCT79	RK
	D	ECN 1755	6NOV79	RK
	E	ECN 1820	10-9-80	RK

ARREFN
EXAD0N
EXAD1N
EXAD2N
EXAD3N
MS3N
MS2N
MS1N
MS0N
MEMAV
MEMAVN
SELN(2B8)
SELN (2D2,2B4,2A4)
CASSL (2D2)
LED 1
MS1Z3
MS1Z2
MS1Z1
MS1Z0
+15V
+12V
+5V
-5V
+5VB
P1

NOTE:
1. * INDICATES +5V BACKUP.

P10

+15V	2	1	+15V
+15V	4	3	+15V
GND	6	5	GND
GND	8	7	GND
+5V	10	9	+5V
EXAD3N	12	11	EXAD0N
EXAD2N	14	13	EXAD1N
ARREFN	16	15	
MS1Z3	18	17	MS1Z1
MS3N	20	19	MS1N
MEMAV	22	21	MEMAVN
MES1Z2	24	23	MS1Z0
MS2N	26	25	MS0N
RADS1	28	27	RADS3
RADS5	30	29	RADS7
RADS0	32	31	RADS2
RADS4	34	33	RADS6
+5VB	36	35	+5VB
+5VB	38	37	+5VB
X1415N	40	39	X411N
X07N	42	41	X310N
X512N	44	43	X18N
X613N	46	45	X29N
CASN	48	47	WRN
DB42N	50	49	GND
DB41N	52	51	GND
DB40N	54	53	GND
GND	56	55	GND
	58	57	
	60	59	
	62	61	
	64	63	
GND	66	65	GND
GND	68	67	GND
	70	69	
	72	71	
	74	73	
	76	75	
+5V	78	77	+5V
+5V	80	79	+5V
	82	81	
	84	83	
	86	85	
	88	87	
DB37N	90	89	GND
DB35N	92	91	GND
DB36N	94	93	GND
DB38N	96	95	GND
DB34N	98	97	GND
DB33N	100	99	GND
DB35N	102	101	GND
DB32N	104	103	GND
DB28N	106	105	GND
DB27N	108	107	GND
DB29N	110	109	GND
DB31N	112	111	GND
DB30N	114	113	GND
DB24N	116	115	GND
DB26N	118	117	GND
DB25N	120	119	GND

P9

GND	2	1	GND
+5V	4	3	+5V
	6	5	
	8	7	
	10	9	
	12	11	
	14	13	
	16	15	
	18	17	
	20	19	
	22	21	
	24	23	
	26	25	
	28	27	
	30	29	
	32	31	
	34	33	
	36	35	
	38	37	
DB21N	40	39	GND
DB18N	42	41	GND
DB22N	44	43	GND
DB20N	46	45	GND
DB23N	48	47	GND
DB17N	50	49	GND
DB16N	52	51	GND
DB19N	54	53	GND
	56	55	
	58	57	
	60	59	
	62	61	
	64	63	
	66	65	
	68	67	
	70	69	
	72	71	
	74	73	
DB13N	76	75	GND
DB15N	78	77	GND
DB12N	80	79	GND
DB14N	82	81	GND
DB09N	84	83	GND
DB11N	86	85	GND
DB10N	88	87	GND
DB08N	90	89	GND
	92	91	
	94	93	
	96	95	
	98	97	
	100	99	
DB07N	102	101	GND
DB04N	104	103	GND
DB06N	106	105	GND
DB01N	108	107	GND
DB05N	110	109	GND
DB02N	112	111	GND
DB03N	114	113	GND
DB00N	116	115	GND
GND	118	117	GND
+5V	120	119	+5V

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED	
APPLICATION		DIMENSIONS ARE IN INCHES	
		TOLERANCES ON:	
		FRACTIONS ±	DECIMALS .XX ± .XXX ±
		ANGLES ±	
		MATERIAL:	

DRAWN	J.L. WEITZ	DATE 5/22/79
CHECKED	RK	
ENGR.	RK	16 OCT 79
APPROVED	[signature]	10/16/79

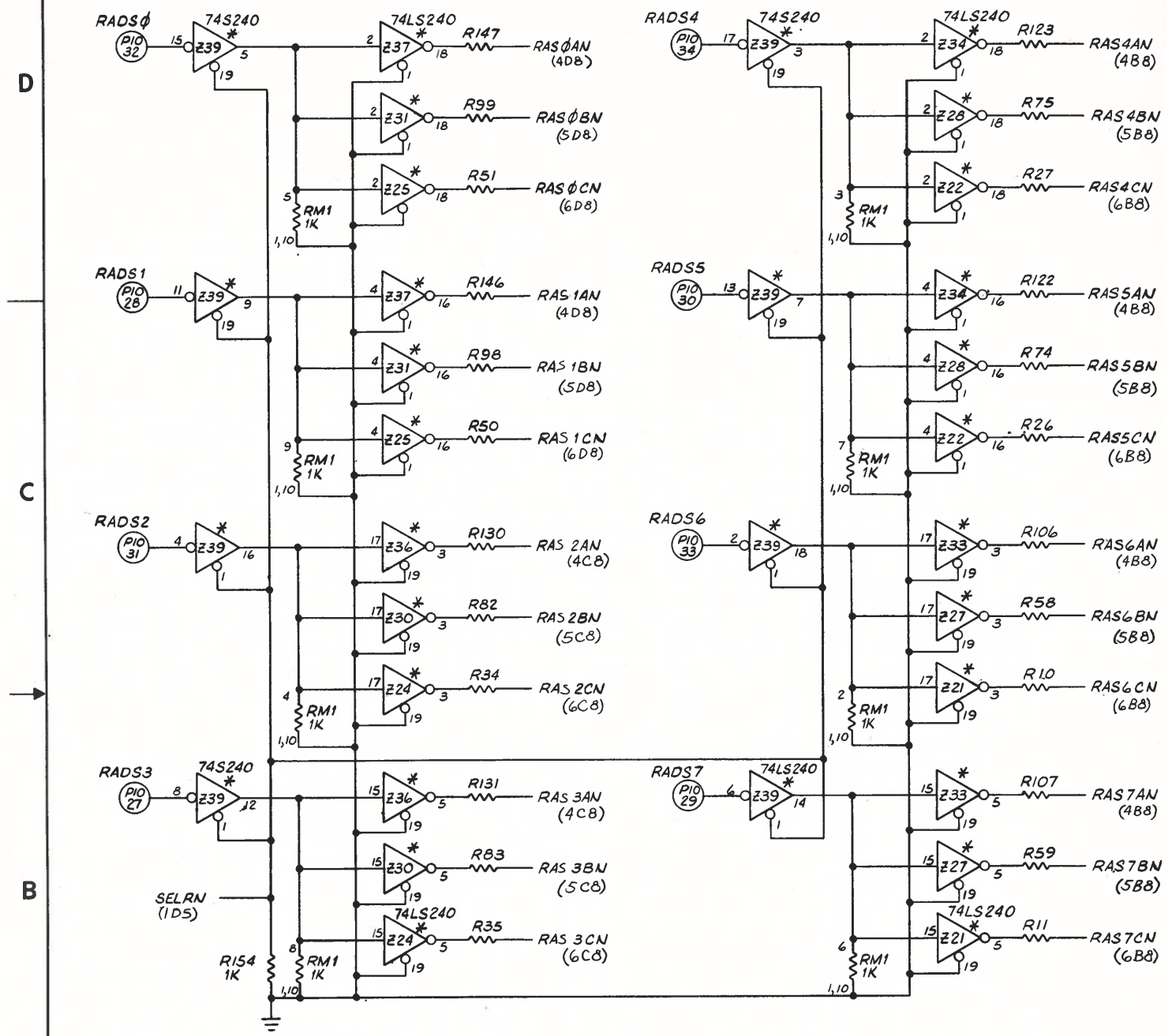
DATARAM CORPORATION
CRANBURY NEW JERSEY

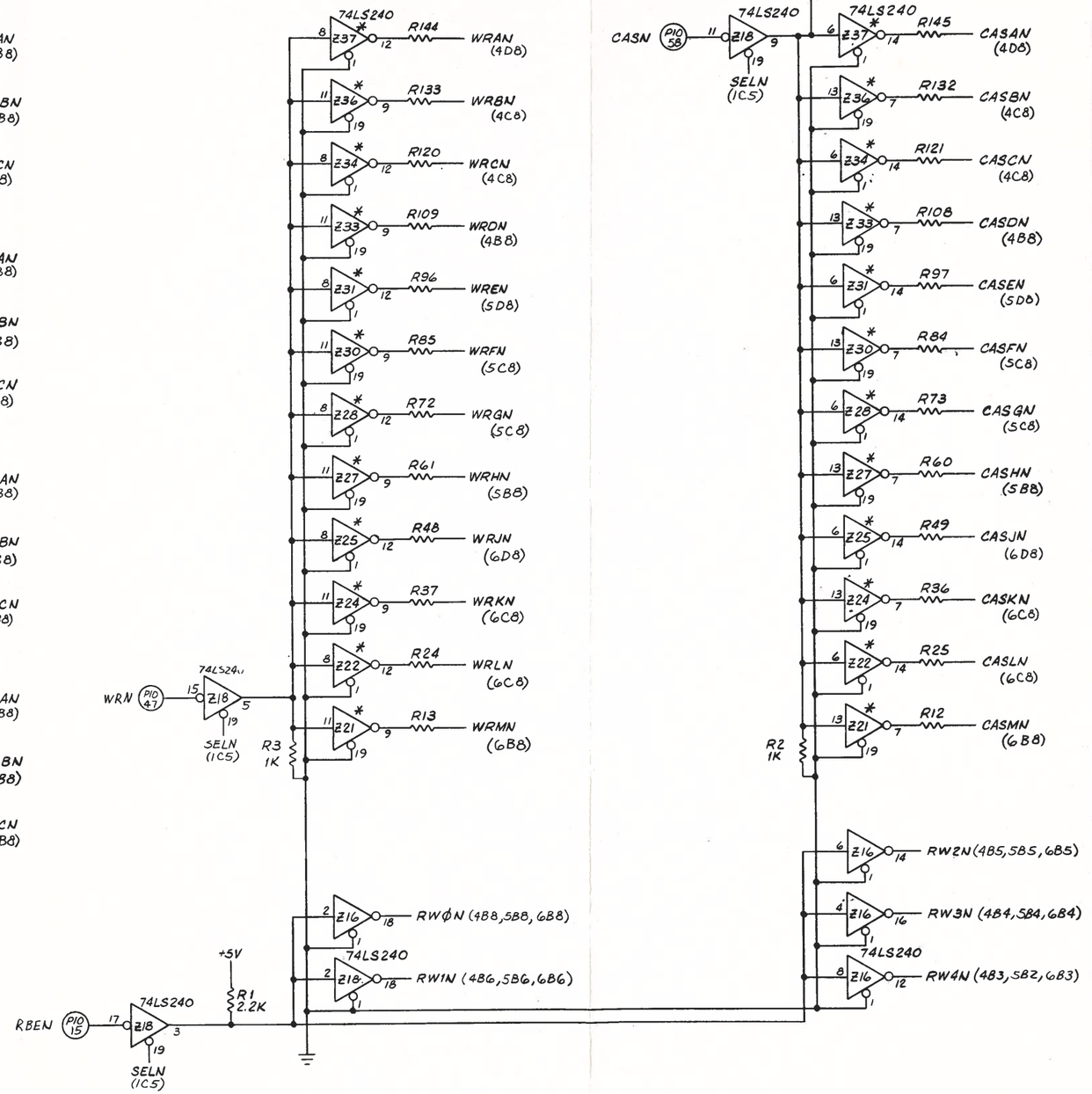
SCHEMATIC
DR-129S
BULK SEMI ARRAY 128K x 43

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	50473	03183	E

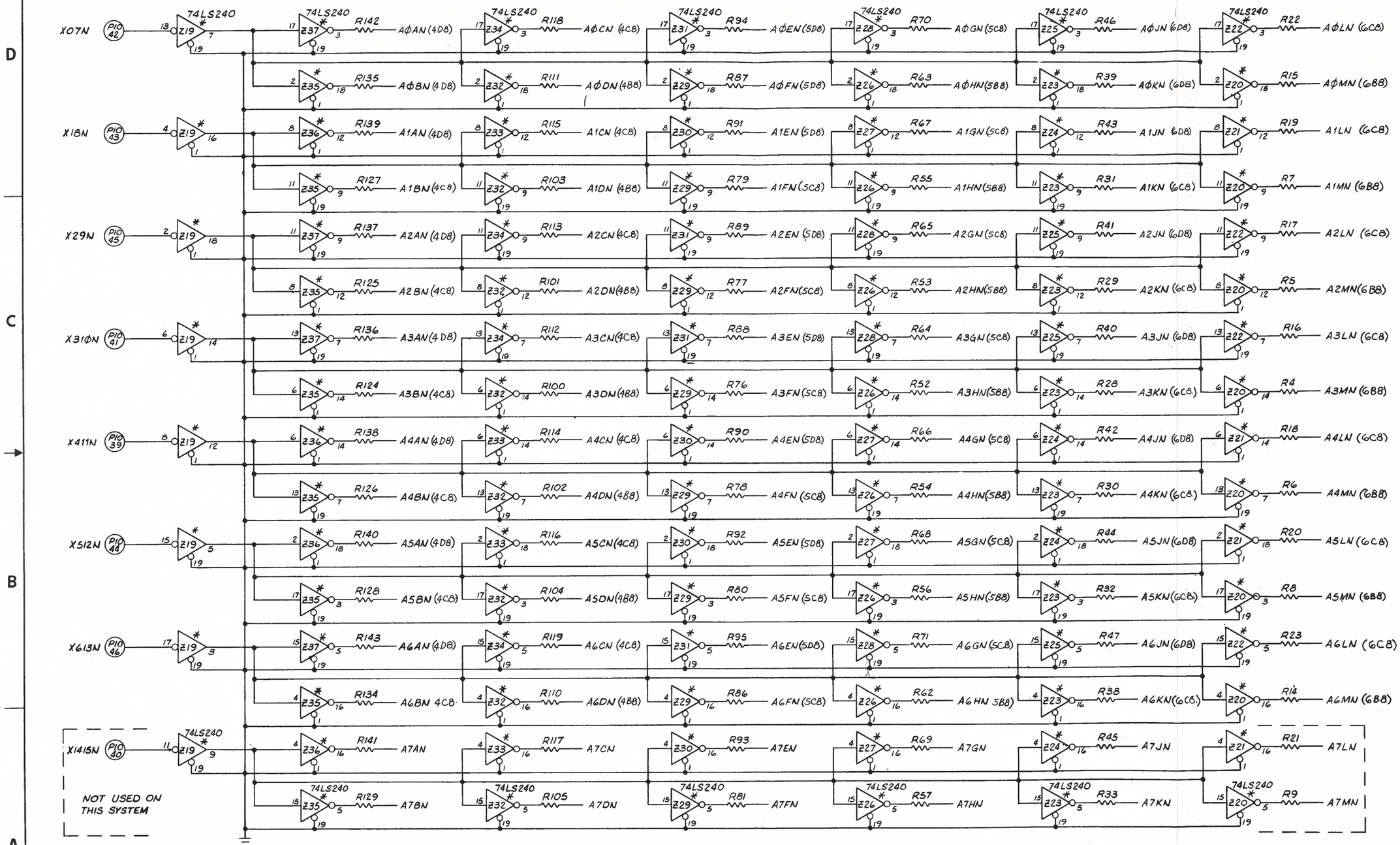
SCALE | SHEET 1 OF 6

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

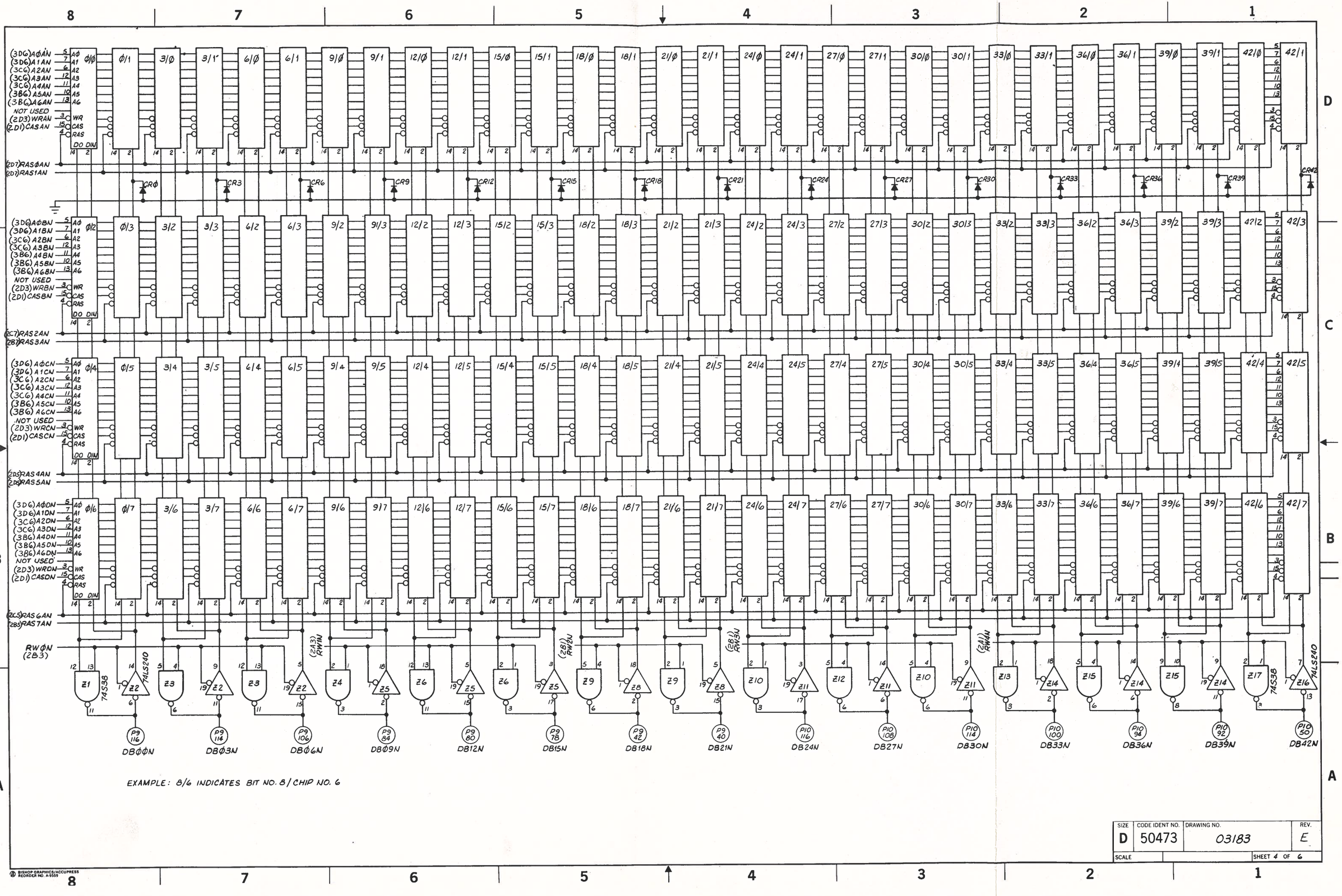




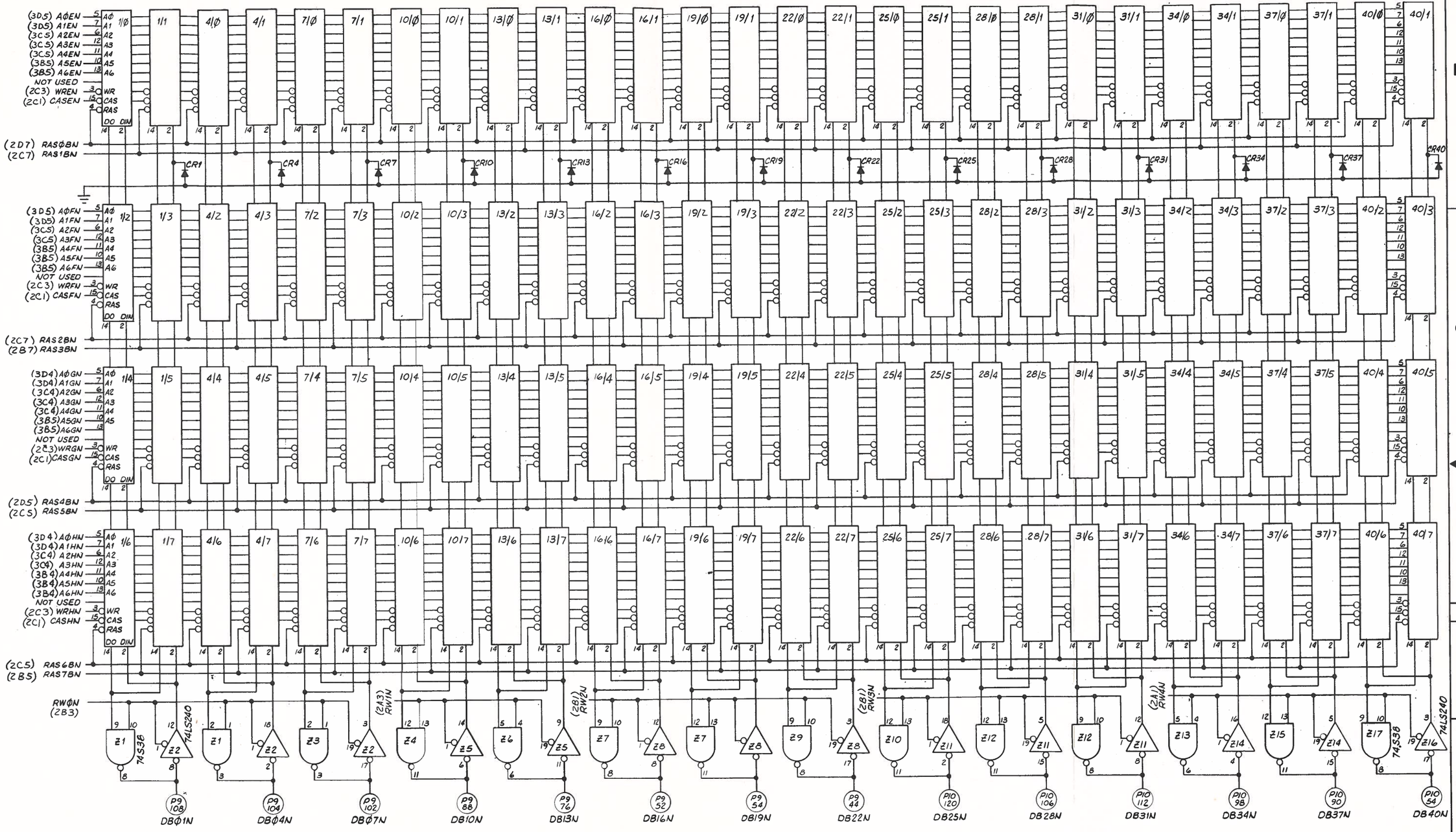
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03183	E
SCALE		SHEET 2 OF 6	



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03183	E
SCALE		SHEET 3 OF 6	

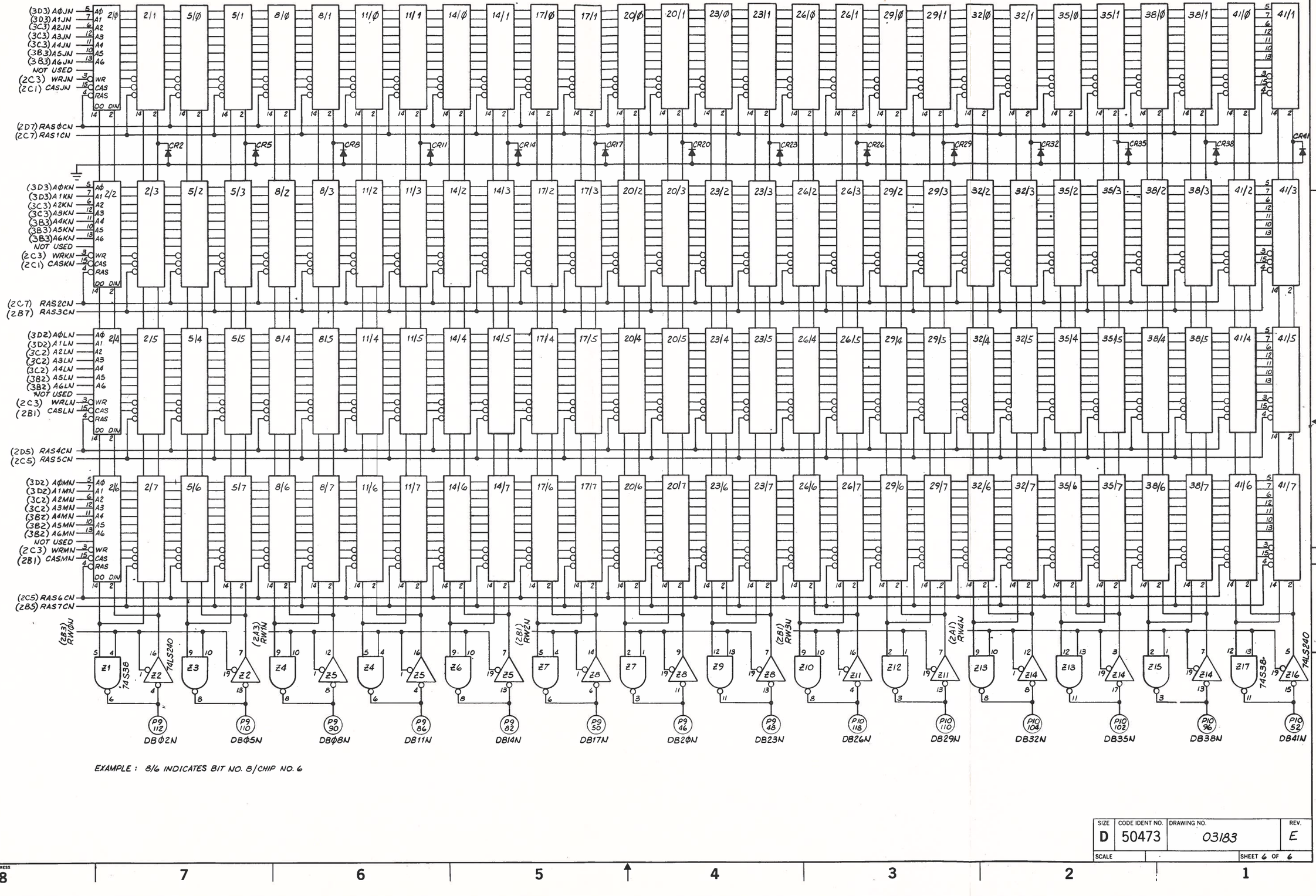


SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03183	E
SCALE			SHEET 4 OF 6



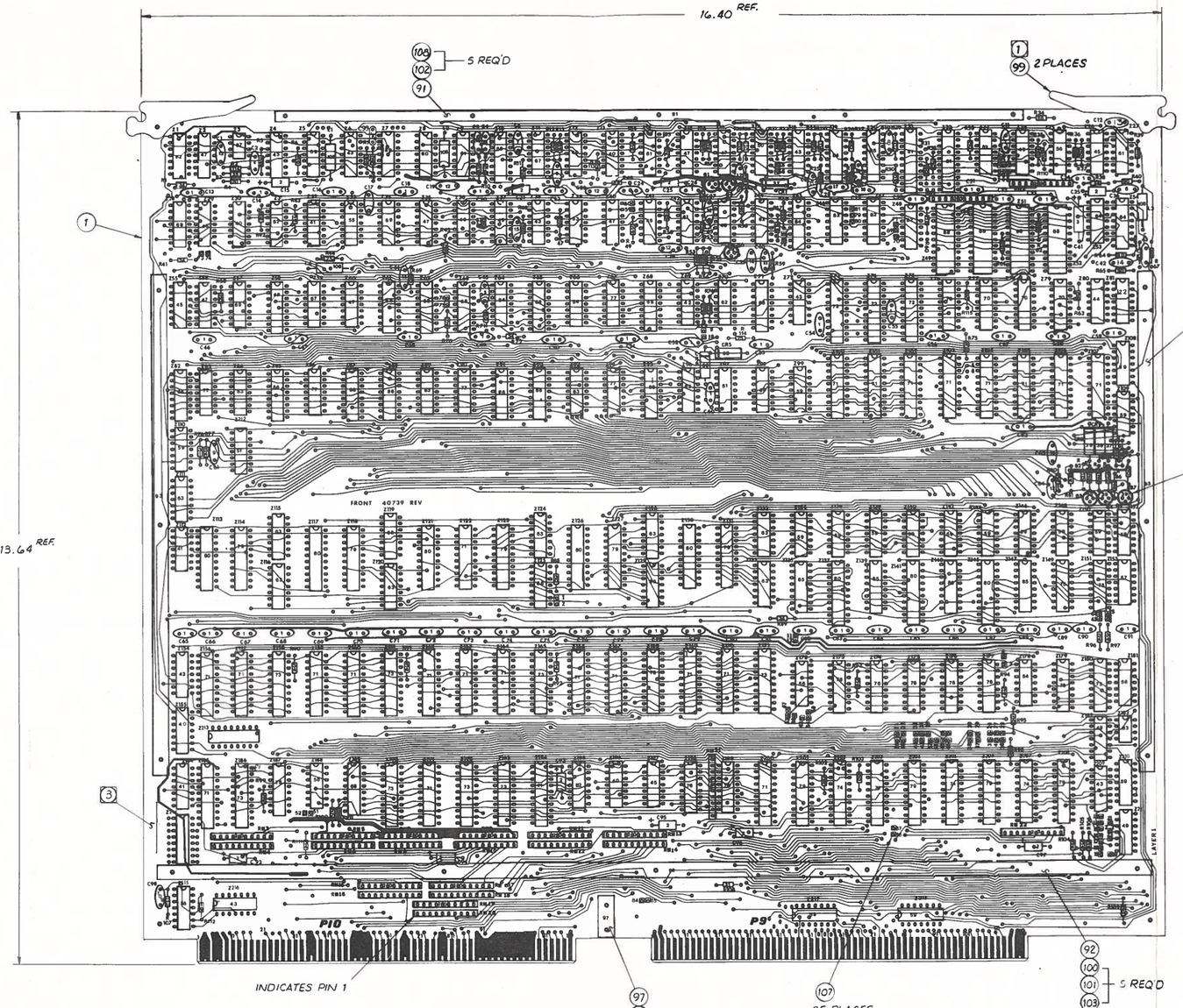
EXAMPLE: 8/6 INDICATES BIT NO. 8/ CHIP NO. 6

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03183	E
SCALE		SHEET 5 OF 6	



SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03183	E
SCALE		SHEET 6 OF 6	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	3-17-80	J DUNCAN
	B	ECN 1878	29 May 80	RK
	C	ECN 1879 REDRAWN		
	D	ECN 1884		
	E	ECN 1906		
	F	ECN 1919		
	G	ECN 1920		
	H	ECN 1922		
	J	ECN 1940		
	K	ECN 1951A		
	L	ECN 1970		
	M	ECN 1975		
	N	ECN 1998		
	P	ECN 2000	24 JULY 80	RK
	R	ECN 2044 cms	15 SEP 80	RK

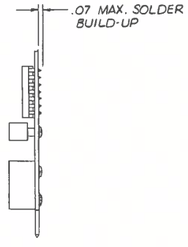


5

TABLE I			
62901 18 BIT, 16K RAM		62904 18 BIT, 16K RAM	
FROM	TO	FROM	TO
E9	E10	E5	E6
E43	E44	E7	E8
E47	E53	E9	E10
E48	E54	E11	E12
E55	E56	E24	E25
		E43	E44
		E49	E53
		E50	E54
		E59	E60

NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL AFTER FLOW SOLDER.
2. INSTALL TRANSISTOR PADS ITEM 96 TO TRANSISTORS ITEM 39 6 PLACES PRIOR TO PC. BOARD MOUNTING.
3. MARK PART NO., LATEST REV., SERIAL NO. & DATE CODE APPROX. WHERE SHOWN.
4. FOR SCHEMATIC DIAGRAM SEE DWG NO. 03191.
5. ADD JUMPER WIRES FOR 62901 OR 62904 PER TABLE I. SEE SCHEMATIC 03191 FOR OPTIONAL JUMPERING INFORMATION.



NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN JOHNSON	5-23-80
CHECKED	
ENGR.	
APPROVED RK	25 JULY 80

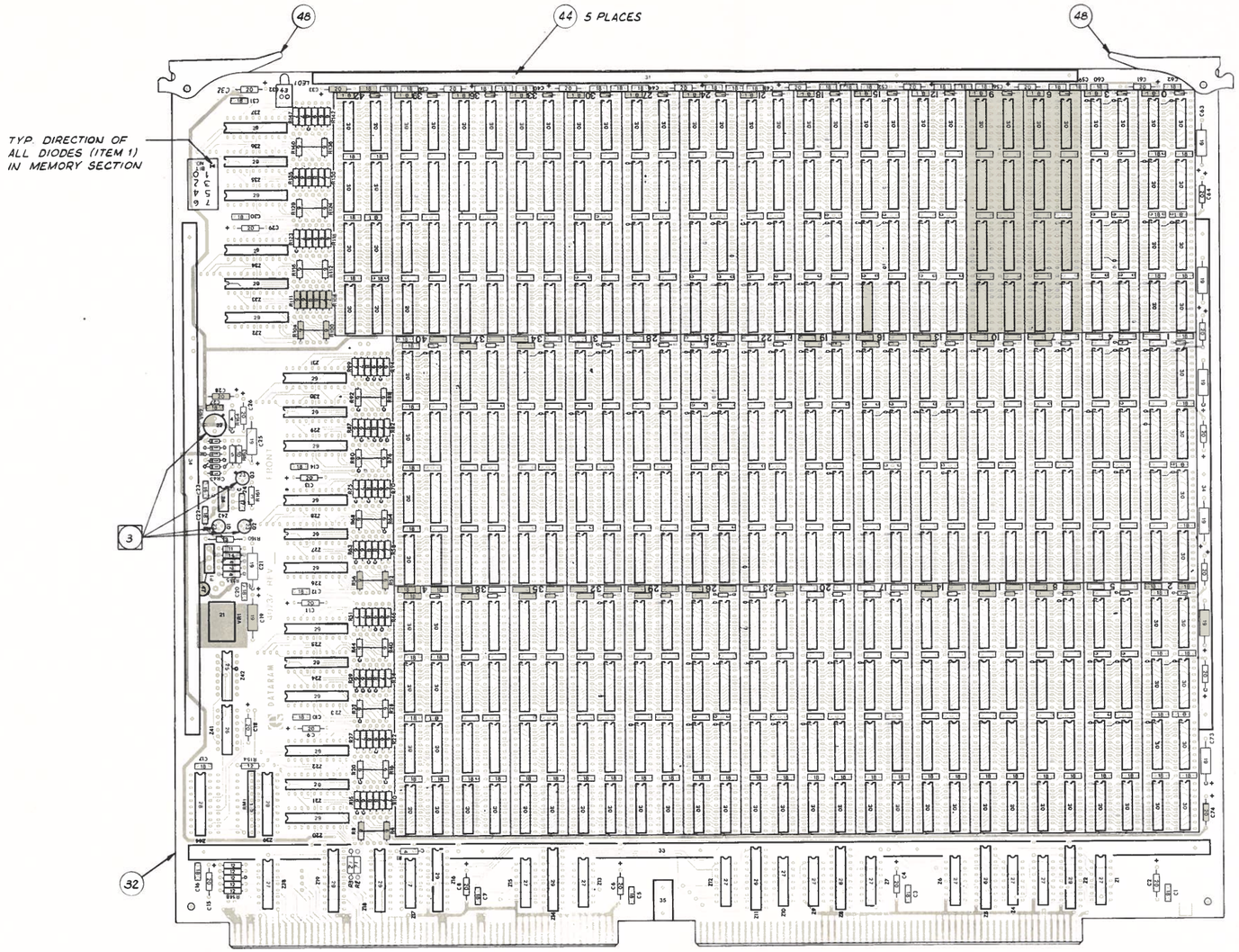
DATARAM CORPORATION
CRANBURY NEW JERSEY

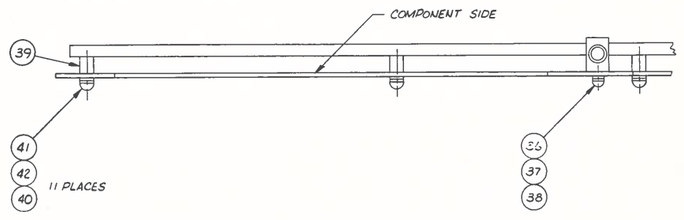
ASSEMBLY DR-129S BSC
18 BIT / 36 BIT

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	50473	62901/62904	R

SCALE FULL SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X1	ECN 1678	18 JULY 79	RK
	X2	ECN 1679	18 JULY 79	RK
	A	ECN 1680 RELEASE TO PRODUCTION	18 JULY 79	RK
	B	ECN 1740	16 OCT 79	RK
	C	ECN 1741	16 OCT 79	RK
	D	ECN 1755	6 NOV 79	RK
	E	ECN 1820	10-9-80	[illegible]
	F	ECN 1951A	10-9-80	[illegible]





NOTES:

1. MAXIMUM COMPONENT HEIGHT IS .400 EXCLUDING GUIDE BLOCK (ITEM 35).
2. MAXIMUM LEAD LENGTH IS .050.
3. PRIOR TO INSERTION IN P.C. BOARD, INSTALL ITEM 46 ON ITEM 22 & ITEM 45 ON ITEM 23.

		UNLESS OTHERWISE SPECIFIED		DATARAM CORPORATION		
		DIMENSIONS ARE IN INCHES		CRANBURY NEW JERSEY		
		TOLERANCES ON:		ASSEMBLY		
		FRACTIONS DECIMALS ANGLES		DR-1295		
		± XX ± ±	DRAWN J. L. WEITZ 5-22-79	BULK SEMI ARRAY 128K x 43		
		XXX ±	CHECKED			
		MATERIAL:	ENGR. RK 18 JULY 79	SIZE D	CODE IDENT. NO. 50473	DRAWING NO. 62902 REV. F
			APPROVED [illegible] 7/27/79	SCALE FULL		SHEET 1 OF 1
NEXT ASSY	USED ON					
APPLICATION						

DUNNING 44-567 18156

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE REVISION LETTER IF ANY, AND DATE

REV. AC

DWG. NO. 62901 62904 SHEET 1 OF 7

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		Released to Production		3-17-80
B		ECN 1878 JAY	RK	24 JUL 80
C		ECN 1879 JAY		
D		ECN 1884 JAY		
E		ECN 1906 JAY		
F		ECN 1919 JAY		
G		ECN 1920 JAY		
H		ECN 1922 JAY		
J		ECN 1940 JAY		
K		ECN 1951A JAY		
L		ECN 1970 JAY		
M		ECN 1975 JAY		
N		ECN 1998 JAY		
P		ECN 2000 JAY	RK	24JUL80
R		ECN 2044 (cons	RK	15 SEPT 8
S		ECN 2347	RK	19 MAR 8
T		ECN 2341		
U		ECN 2360		
V		ECN 2464		
W		ECN 2527		
Y		ECN 2562		
Z		ECN 2568		
AA		ECN 2617		
AB		ECN 2618 BRT		
AC		ECN 2638 BRT 3-17-82	RK	19MAR82

DRAWN MAS	DATE 1-24-80
CHECKED RK	DATE 17MAR80
ENGR JAY	DATE 3-17-80
APPROVED RK	DATE 17MAR80

TITLE

BILL OF MATERIALS

ASSY DR-129S BSC 18 BIT, 36 BIT

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 62901 62904 SHEET 1 OF 7

REV. AC

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	56	12316	CAP CER .1uf 20%	C13,14,16,18,20,22,24,26,
				30-34,46-60,62,65-91
2	10	12105	CAP TANT 4.7uf 10V	C15,21,25,35,92-97
3	1	12102	CAP TANT 15uf 20V	C41
4	1	12315	CAP CER .01uf 20%	C2
5	1	12608	CAP SIL MICA 180pf 5%	C45
6	1	12513	CAP SIL MICA 100pf 5%	C36
7	1	12516	CAP SIL MICA 47pf 5%	C5
8	2	12509	CAP SIL MICA 150pf 5%	C8, 10
9	2	12519	CAP SIL MICA 68pf 5%	C6,61
10	1	12513	CAP SIL MICA 100pf 5%	C9
11	1	12504	CAP SIL MICA 200pf 5%	C40
12	8	12505	CAP SIL MICA 330pf 5%	C7, 19,23,27,38-39
				63,64
13	3	12506	CAP SIL MICA 470pf 5%	C1,C37,C12
14	1	12609	CAP SIL MICA 240pf 5%	C42
15	1	12311	CAP CER 1500 pf 20%	C3
16	1	12311	CAP CER 1500 pf 20%	C4
17	1	12306	CAP CER 220 pf 20%	C28
18	1	12319	CAP CER 5600pf 20%	C29
19	2	10103	RES CC 1/4W 51 OHMS 5%	R50,112
20	9	11907	RES MDL 220 OHMS 5%	RM3,5,7,9,11,13,15,17,19,
21				
22	1	11903	RES MDL 470 OHMS	RM21
23	3	11904	RES MDL 2.2K OHMS 5%	RM1,2,22

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
24	1	10159	RES CC 1/4W 75 OHMS 5%	R53
25	13	10105	RES CC 1/4W 100 OHMS 5%	R16,18,34,39,44,46,48,56,84,86,110,114,115
26	3	10602	RES CC 1/4W 120 OHMS 5%	R5,6,8
27	1	10108	RES CC 1/4W 220 OHMS 5%	R100
28	2	10111	RES CC 1/4W 470 OHMS 5%	R54,83
29	5	10111	RES CC 1/4W 470 OHMS 5%	R7,45,47,67,69
30	15	10113	RES CC 1/4W 1K OHMS 5%	R4,32,33,35,37, 51,60,
				61,65,68,87,88,95,103,
				109
31	2	10118	RES CC 1/4W 2.2K OHMS 5%	R76,108
32	2	10121	RES CC 1/4W 4.7K OHMS 5%	R20,85
33	2	10601	RES CC 1/4W 5.1K OHMS 5%	R11,12
34	43	10122	RES CC 1/4W 10K OHMS 5%	R1,9,13-15,17,21,22,
				30,38,41,42,43,49,52,
				57,58,62,70,72-75,77,80,
				81,89-94,96-99,101,102,
				105,106,111,113,104
35	1	10145	RES CC 1/4W 22K OHMS	R3
36	3	10181	RES CC 1/4W 51K OHMS 5%	R10,25,63
37	2	18202	DIODE ZENER 3.3V 1N746	CR1,4
38	4	18205	DIODE ZENER 5.1V 1N751A	CR2,3,5,6
39	6	20104	XSTR NPN SWG 2N2369A	Q1-6
40	4	16513	IC QUAD 2I/P NAND 74S00	Z13,30, 155,196
41	3	16205	IC QUAD 2I/P NAND 74LS00	Z112,184,32
42	1	16507	IC QUAD 2I/P NOR 74S02	Z69
43	8	16501	IC HEX INV 74S04	Z4,6,18,38,72,154,209,216

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 62901
B/M 62904
SHEET 3 OF 7

REV. AC

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
44	1	16210	IC HEX INV 74LS04	Z80
45	6	16525	IC QUAD 2I/P AND 74S08	Z29,36,41,55,197,26
46	1	16206	IC QUAD 2I/P AND 74LS08	Z43
47	7	16515	IC TPL 3I/P NAND 74S10	Z2,15,16,35,40,56,60
48				
49	5	16503	IC TPL 3I/P AND 74S11	Z12,24,37,182,211
50	1	16212	IC TPL 3I/P AND 74LS11	Z17
51	2	16516	IC DUAL 4I/P NAND 74S20	Z97,212
53	1	16541	IC DUAL 4I/P NAND 74S22	Z39
54	2	16542	IC 8I/P NAND 74S30	Z66,178
55	2	16521	IC QUAD 2I/P POS OR 74S32	Z33,215
56	3	16220	IC QUAD 2I/P POS OR 74LS32	Z25,172,181
57	1	16518	IC QUAD 2I/P NAND 74S37	Z153
58	1	16309	IC QUAD 2I/P NAND 7438	Z188
59	18	16514	IC QUAD 2I/P NAND 74S38	Z98,99,108-110,134,136,138,
				140,142,144,146,148,150,
				152,210,217,218
60	1	16209	IC DUAL AND/OR/INV 74LS51	Z8
61	4	16522	IC DUAL D BINARY 74S74	Z9,14,27,42
62	4	16202	IC DUAL D BINARY 74LS74	Z44,70,1,31
63	14	16505	IC QUAD EXCL OR 74S86	Z84,89,93,96,111,115,116,
				119,120,124,128,129,132,
				133
64	1	16316	IC MONSTABLE MV 74121	Z53
65	2	16326	IC DUAL MONOSTABLE MV 74123	Z10,20
66	1	16317	IC TRI-STATE AND BUFFER 8094	Z125

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

TITLE: B/M ASSY DR-129 BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
67	2	16529	IC QUAD 2I/P NAND ST 74S132	Z11,59
68	8	16520	IC 3 TO 8 DCDR/MUX 74S138	Z58,61-63,65,68,71,189
69	2	16543	IC 4I/P NAND 50 OHM DRVR 74S140	Z34,57
70	4	16506	IC QUAD 2 TO 1 MUX 74S157	Z76-79
71	24	16531	IC BUS DRVR/BFR 74S240	Z100-107,122,156,157,159,
				160,162-164,166,167,169,
				170,185,191,194,200
72	3	16234	IC 3STAT BFR/DRVR/RCVR 74LS240	Z73-75
73	9	16528	IC BUS DRVR/BFR/INV 74S241	Z158,161,165,168,171,186,
				190,192,193
74	4	16254	IC 3STAT BFR/DRVR/RCVR 74LS241	Z202,203,205,207
75	4	16538	IC DUAL 4 TO 1 MUX 74S253	Z149,151,179,180
76	7	16539	IC QUAD 2 TO 1 MUX 74S257	Z173-177,198,199
77	5	16544	IC 9B PARITY GEN/CHKR 74S280	Z67,83,86,90,94
78	1	16535	IC 4B BINARY FULL ADDER 74S283	Z187
79	9	16536	IC OCTAL D LATCH 74S373	Z114,118,123,127,131,201,
				204,206,208
80	8	16551	IC OCTAL D FLIP FLOP 74S374	Z113,117,121,126,130,137,
				141,145
81	2	16551	IC OCTAL D FLIP FLOP 74S374	Z21,22
82	5	16236	IC DUAL 4B BIN CNTR 74LS393	Z23,46,47,48,195
83	1	16607	IC PRPHL POS-OR DRIVER 75453	Z183
84	4	16532	IC RESET MONOSTABLE MV 26S02	Z45,54,64,19
85	4	16555	IC 6B IDENT COMPTR 93S46	Z135,139,143,147
86	7	16556	IC 12B PARITY GEN/CHKR 93S48	Z82,85,87,88,91,92,95
87	1	16356	IC TIMER 555	Z3

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DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 62901
B/M 62904
SHEET 5 OF 7

REV. AC

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
88	4	16746	IC STATIC RAM 256 x 4	Z49,50,51,52
89	3	14108	DELAY LINE, DIGITAL 150ns	Z5,7,28
90	7	10216	RES FLM 1/10W 5.11K OHMS 1%	R23,26,31,40,59,64,71
91	1	42649	STIFFENER CIRCUIT CARD	
92	1	42648	STIFFENER LONG	
93	2	42647	STIFFENER SHORT	
94	1	40835	PC BOARD DR-129S/229S CONTROLLER	
95	---	03191	SCHEMATIC BS CONTROLLER	
96	6	27316	PAD, TRANSISTOR TO-18	
97	1	42944	GUIDE BLOCK	
98	2	26321	SCR PNH PHL STL 4-40 x 3/16	
99	2	27334	CARD EJECTOR (WITH PIN)	
100	11	27204	SPACER RND THD NYL WHT 2-56 x .10 LG	
101	16	26304	SCR PNH PHL STL 2-56 x 3/8	
102	16	26205	WASHER INT TOOTH STL #2	
103	16	26210	WASHER FLAT NYL WHT #2	
104	2	26206	WASHER INT TOOTH STL #4	
105	2	26204	WASHER FLAT STL #4	
106	4	14502	INDUCTOR 22mH	L1-4
107	85	22601	CONTACT MALE	
108	A/R	30401	TAPE POLYEST 1/4W	
109	1	12506	CAP SIL MICA 470 pf 5%	C98
110	1	-	RES CC 1/4W S.A.T.	R107
111	1	12313	CAP CER 2700 pf 10%	C11
112	1	-	RES CC 1/4W S.A.T.	R29
113	1	-	RES CC 1/4W S.A.T.	R66

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 62901
B/M 62904
SHEET 6 OF 7

REV. AC

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
114	1	-	RES CC 1/4W S.A.T.	R116
115	1	-	RES CC 1/4W S.A.T.	R82
116	1	-	RES CC 1/4W S.A.T.	R79
117	1	-	RES CC 1/4W S.A.T.	R55
118	1	-	RES CC 1/4W S.A.T.	R18
119	1	-	RES CC 1/4W S.A.T.	R2
120	1	10106	RES CC 1/4W 150 OHMS 5%	R19
121	1	12310	CAP CER 820pf 20%	C99
122	1	16324	IC QUAD 2 I/P NANDSCHM 74132	Z81
123	16	26203	WASHER FLAT STL #2	

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DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 62901
B/M 62904
SHEET 7 OF 7

REV. AC

REV. AA

DWG. NO. 62902 SHEET 1 OF 4

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
X1		ECN 1678	RK	18JUN79
X2		ECN 1679	RK	18JUN79
A		ECN 1680 Release to Production	RK	18JUN79
B		ECN 1740	RK	16OCT79
C		ECN 1741	RK	16OCT79
D		ECN 1755	RK	6NOV79
E		ECN 1820	[illegible]	10-9-80
F		ECN 1951A	[illegible]	10-9-80
G		ECN 2452	RK	18FEB82
AA		ECN 2596	RK	18FEB82
AB		ECN 2602	RK	18MAR82

DRAWN	MAS
DATE	5-1-79
CHECKED	[illegible]
DATE	5/7/79
ENGR.	RK
DATE	18JUN79
APPROVED	[illegible]
DATE	7/16/79

TITLE

BILL OF MATERIAL

DR-129S BULK SEMI ARRAY, 128K x 43

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 62902

SHEET 1 OF 4

REV. AB

TITLE: B/M DR-129S BULK SEMI ARRAY, 128K x 43

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	49	18101	DIODE SILICON HIGH CONDUCTANCE	CRØ-48
2	1	10122	RESISTOR CC 1/4W 10K OHMS 5%	R156
3	1	10601	RESISTOR CC 1/4W 5.1K OHMS 5%	R161
4	4	10118	RESISTOR CC 1/4W 2.2K OHMS 5%	R155,157,164,1
5	1	10175	RESISTOR CC 1/4W 15 OHMS 5%	R162
6	84	10151	RESISTOR CC 1/4W 33 OHMS 5%	R4-8,14-20,22,23,28-32,
				38-44,46,47,52-56,62-68,
				70,71,76-80,86-92,94,95,
				100-104,110-116,118,119,
				124-128,134-140,142,143
7	24	10151	RESISTOR CC 1/4W 33 OHMS 5%	R10,11,26,27,34,35,50,51,
				58,59,74,75,82,83,98,99,
				106,107,122,123,130,131,
				146,147
8	12	10615	RESISTOR CC 1/4W 24 OHMS 5%	R12,25,36,49,60,73,84,97,
				108,121,132,145
9	12	10151	RESISTOR CC 1/4W 33 OHMS 5%	R13,24,37,48,61,72,85,96,
				109,120,133,144
10	1	10106	RESISTOR CC 1/4W 150 OHMS 5%	R163
11	1	10130	RESISTOR CC 1/4W 33K OHMS 5%	R159
12	7	10113	RESISTOR CC 1/4W 1K OHMS 5%	R2,3,148,149,150,151,152
13	1	10240	RESISTOR FILM 1/4W 909 OHMS 1%	R160
14	1	10204	RESISTOR FILM 1/10W 100 OHMS 1%	R158
15				
16	1	12313	CAPACITOR CER 2700pF ±10%	C23
17	1	12315	CAPACITOR CER .01μF ±20%	C24

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DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 62902
SHEET 2 OF 4

REV AB

TITLE: B/M DR-129S BULK SEMI ARRAY, 128K x 43

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
18	210	12316	CAPACITOR CER .1µF 20%	C1,3,5,7,10,12,14,16,17,
				20,22,27,30,31,36,40,44,
				48,52,56,60,62 (Mem Array)
19	10	12102	CAPACITOR TANT 15µF 20V	C19,21,25,63,65,67,69,71,
				73,76
20	23	12105	CAPACITOR TANT 4.7µF 10V	C2,4,6,8,9,11,13,15,18,
				26,28,29,32,33,41,49,57,
				64,66,68,70,72,74
21	155	12316	CAPACITOR CER .1µF ±20%	Mem. Array
22	1	20303	VOLTAGE REG -5V FIXED	VR2
23	12	12105	CAPACITOR TANT 4.7µF 10V	C76-79,81-84,86-88,422
24	1	16356	IC TIMER 555	Z43
25	1	16511	IC DUAL I/P NOR GATE 74S260	Z42
26	1	16505	IC QUAD EX OR GATE 74S86	Z41
27	12	16514	IC QUAD 2I/P NAND GATE 74S38	Z1,3,4,6,7,9,10,12,13,15,
				17,38
28	1	16531	IC OCTAL BUFFER/LINE DRIVER/LINE Rx 74S240	Z44
29	26	16234	IC OCTAL BUFFER/LINE DRIVER/LINE Rx 74LS240	Z2,5,8,11,14,16,18,19-37
30	344	16731	IC DYNAMIC RAM 16K x 1	Bits o-42A,B,C,D,E,F,G,H
31	1	42649	STIFFENER CIRCUIT CARD	
32	1	40821	PC BOARD DR-129/229S BSA	
33	1	42648	STIFFENER BAR LONG	
34	1	42647	STIFFENER BAR SHORT	
35	1	42944	GUIDE BLOCK	
36	2	26321	SCR PNH PHL STL 4-40 x 3/16	
37	3	26206	WASHER INT TOOTH STL #4	

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TITLE: B/M DR-129S BULK SEMI ARRAY, 128K x 43

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
38	2	26204	WASHER FLAT STL #4	
39	11	27212	SPACER RND THD NYL WHT 2-56 x 7/32 LG	
40	11	26305	SCR PNH PHL STL 2-56 x 1/2 LG	
41	11	26203	WASHER FLAT STL #2	
42	11	26205	WASHER INT TOOTH STL #2	
43	1	18403	DIODE LED RED W/INTL RES	LED1
44	5	27002	SCR PNH NYL WHT 2-56 x 1/4	
45	3	27316	TRANSISTOR PAD TO-18	
46	1	27305	TRANSISTOR PAD TO-5	
47	3	22214	BEAD PIN	
48	2	27334	CARD EJECTOR	
49				
50	2	16507	IC QUAD 2I/P NOR GATE 74S02	Z45,46
51			NOT USED	
52	A/R	24301	WIRE TINNED OPPER BUS 22 AWG	
53	REF	03333	SCHEMATIC DR-129/229S BSA	
54			NOT USED	
55	1	20304	VOLTAGE REG LM317	VR1
56	3	20104	TRANSISTOR NPN SWITCHING 2N2369A	Q1,2,3
57	A/R	30602	INK MARKING BLK	
58	1	26322	SCR PNH PHL STL 4-40 x 1/4	
59	1	26102	NUT HEX STL #4-40	

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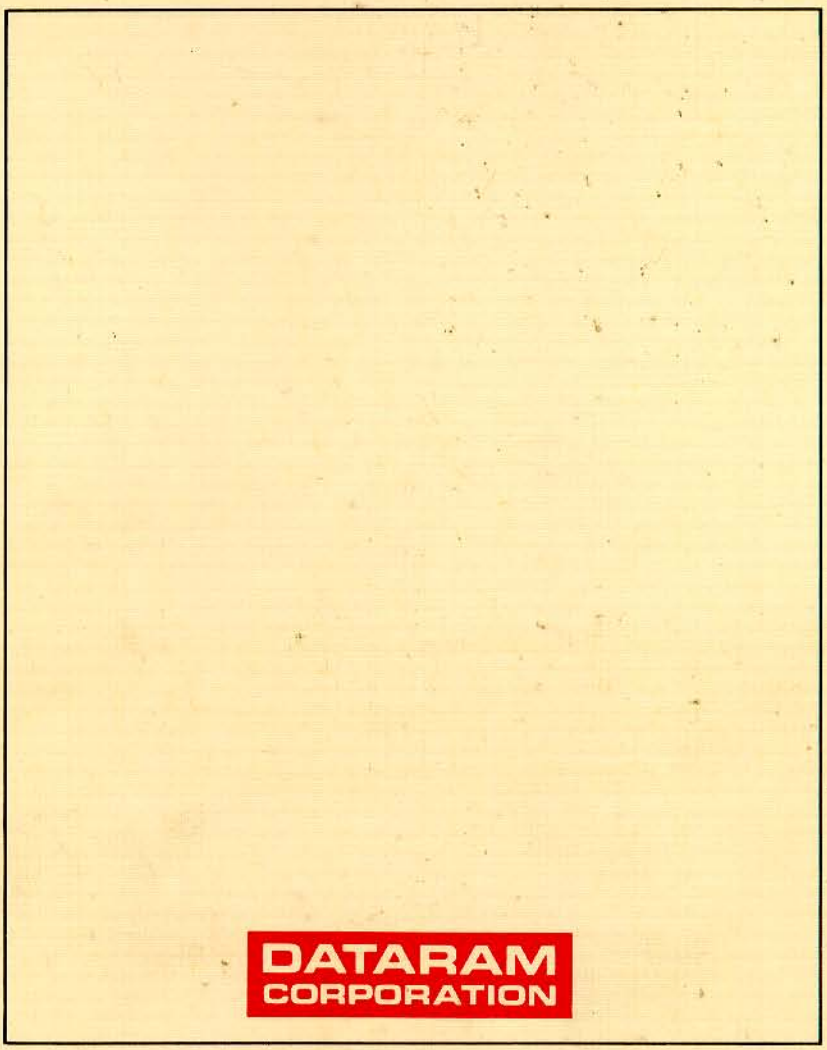
DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 62902
SHEET 4 OF 4

REV AB



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