

DR-129S



**DATARAM**  
**CORPORATION**

DR-129S

06067

| REV.                             | REVISIONS |       |                        |            |           |
|----------------------------------|-----------|-------|------------------------|------------|-----------|
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| 0<br>02126<br>1 OF 22<br>SHEET 1 | X1        |       | Preliminary Release 1  | <i>BAH</i> | 2/24/79   |
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|                                  | C         |       | ECN 1975               | <i>BAH</i> | 6-23-80   |

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|-----------------------|-------------------|--|---|----------|-------|------|----|
| DRAWN<br>MAS          | DATE<br>2-5-79    | TITLE<br><br>PRODUCT SPECIFICATION<br><br>DR-129S BULK SEMICONDUCTOR MEMORY SYSTEM |  <b>DATARAM CORPORATION</b><br>CRANBURY NEW JERSEY | DWG. NO. | 02126 | REV. | C  |
| CHECKED<br><i>BAH</i> | DATE<br>1-16-80   |  |   | DWG. NO. | 02126 | REV. | C  |
| ENGR.<br><i>BAH</i>   | DATE<br>2/20/79   |  |   | SHEET    | 1     | OF   | 22 |
| APPROVED<br><i>RK</i> | DATE<br>16 JAN 80 |  |   | SHEET    | 1     | OF   | 22 |

## 1.0 INTRODUCTION

This specification defines the functional, electrical and mechanical characteristics of the model DR-129S BULK SEMI memory system produced by Dataram Corporation.

## 2.0 GENERAL

The DR-129S consists of a Bulk Semiconductor Control (BSC) board and from 1 to 16 Bulk Semiconductor Array (BSA) boards. Each Bulk Semiconductor Array (BSA) board contains 512K bytes of storage using 16K NMOS semiconductor memory chips. The maximum system capacity is 8 megabytes (16 BSA boards).

Each DR-129S BSA board contains error correcting code (ECC) storage and the BSC board contains ECC circuitry to correct all single bit errors and detect all double bit errors which may occur during operation of the system. In addition, error logging circuitry to record up to 64 memory error locations is contained on the BSC board. The error log may be directly examined from the memory bus and when used in conjunction with a Dataram BULK SEMI chassis provides information for an error log display.

The DR-129S may be configured as either an 18 bit word or 36 bit word memory system by installation of wirewrap jumpers on the BSC board.

The DR-129S memory system is electrically compatible to the Dataram BULK CORE (DR-128) memory system and will work with all Dataram BULK CORE Interface (BI) modules. The DR-129S interface is via a handshake asynchronous bus through an exchange of request and status signals. This allows convenient access to the memory for a variety of users, both fast and slow.

### 2.1 Bulk Semiconductor Control (BSC) Board

The BSC contains all necessary logic to drive up to 16 BSA boards. This logic consists of the following circuitry:

1. Timing and Control
2. Data Registers
3. Address Registers
4. ECC Generating & Checking Logic
5. Error Logging Storage & Display Control Logic
6. Refresh Circuits

The data input/output circuitry can be configured to provide either an 18 or 36 bit interface.



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## 2.2 Bulk Semiconductor Array (BSA) Board

The BSA board is configured as a 128K x 43 bit memory array. The 43 bit word length consists of 36 bits of data and 7 bits of ECC storage. The BSA consists of 344 16K NMOS semiconductor memory chips, row/column address drivers and data buffers. Also included is inverter circuitry to generate -5 volts for the 16K semiconductor chips.

## 3.0 ELECTRICAL SPECIFICATIONS

### 3.1 System Characteristics

#### 3.1.1 Size

512K bytes expandable to 8 megabytes in 512K byte increments. A 512K byte system may be configured as 128K x 36 or 256K x 18 bits. The expanded capacity is either 2048K x 36 or 4096K x 18.

#### 3.1.2 Modes and Cycle Time

Cycle time differs for various modes of operation.

##### 3.1.2.1 18 Bit Configuration

| Mode                                 | Minimum<br>Cycle Time<br>(nsec) |
|--------------------------------------|---------------------------------|
| Read Word                            | 550                             |
| Read Even Number of Sequential Words | 400 (avg)                       |
| Write Word                           | 700                             |
| Write Either Byte                    | 700                             |
| Read Word/Modify/Write Word          | 900*                            |
| Read Word/Modify/Write Either Byte   | 900*                            |

##### 3.1.2.2 36 Bit (Double Word) Configuration

| Mode  | Minimum<br>Cycle Time<br>(nsec) |
|---|---------------------------------|
| Read Double Word                                | 550                             |
| Write Double Word                               | 550                             |
| Write Any Byte or Bytes                         | 700                             |
| Read Double Word/Modify/Write Double Word       | 900*                            |
| Read Double Word/Modify/Write Any Byte or Bytes | 900*                            |

\*Includes 75 nanoseconds Read-Modify time



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### 3.1.2.3 Refresh

An additional mode, Refresh, is necessary to prevent loss of data stored in the NMOS storage chips. NMOS Random Access Memory (RAM) devices store data on the gate capacitance of a field-effect transistor. A "1" is stored as the presence of a charge and a "0" is stored as the absence of a charge. The stored charge tends to deteriorate and must be renewed at least every two milliseconds. Therefore, one 128th of the memory (1/128th of each memory chip) is recharged (refreshed) every 14 microseconds.

Refresh cycle time is 700ns. When ADRAVN is sent to the memory during a Refresh cycle, the memory cycle and access time may be extended by up to 700ns.

### 3.1.3 Access Time

Even number of sequential words (18 Bit) 260 nanoseconds average. All other modes, 400 nanoseconds maximum.

### 3.1.4 Voltage and Current Requirements

Both the BSC and BSA boards use +5 volts and +15 volts. Separate inputs for battery backup to support memory refresh at reduced current during primary power failure are provided.

| Voltage $\pm 5\%$ | Current Max. Amps |         |
|-------------------|-------------------|---------|
|                   | Operating         | Standby |
| BSC +5V TOTAL     | 10.1              | 9.8     |
| BSC +5V BBU       | .95               | .9      |
| BSC +15V          | .1                | .1      |
| BSC +15V BBU      | .1                | .1      |
| BSA +5V TOTAL     | 1.2               | .86     |
| BSA +5V BBU       | .55               | .41     |
| BSA +15V          | .95               | .45     |
| BSA +15V BBU      | .95               | .45     |



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### 3.2 Input/Output (Refer to Figures 1-5 for Input/Output Timing)

#### 3.2.1 Logic Levels and Characteristics

Refer to MIL-STD-806B for definition of symbols.

|         |         | <u>Standard<br/>(TTL)</u> | <u>Low Power<br/>Schottky<br/>(LS)</u> | <u>Schottky<br/>(S)</u> |
|---------|---------|---------------------------|--|-------------------------|
| Logic 0 | 0.45V @ | -1.6mA                    | -.40mA                                 | -2mA                    |
| Logic 1 | 2.45V @ | 40 $\mu$ A                | 20 $\mu$ A                             | 50 $\mu$ A              |

All input commands shall have rise time ( $t_r$ ) and fall time ( $t_f$ ) of less than 50 nanoseconds. The overshoot of the leading and trailing edges shall be less than 1.0 volt. All input and output circuits are compatible with standard 830 DTL integrated circuit logic and 7400 TTL logic. If the last letter of a signal mnemonic is the letter "N", this signal is low true asserting.



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### 3.2.2 Input/Output Signal Lines

| MNEMONIC        | DESCRIPTION                            | NO. OF LINES | INPUT/OUTPUT | LOAD/DRIVE   |
|-----------------|--|--------------|--------------|--------------|
| ADRAVN          | Address Available                      | 1            | IN           | 1 S          |
| ADRACN          | Address Accepted                       | 1            | OUT          | 74S38        |
| ADROON-ADR24N   | Memory Address                         | 25           | IN           | 1 LS         |
| RADVLDN         | Response Address Valid<br>(Data Clock) | 1            | IN           | 1 S          |
| DTA00N-DTA35N   | Memory Data (Bidirectional)            | 36           | IN/OUT       | 1 LS/1 74S38 |
| ODAVN           | Output Data Available                  | 1            | OUT          | 74S38        |
| IDACN           | Input Data Accepted                    | 1            | OUT          | 74S38        |
| MRDRN           | Memory Read                            | 1            | IN           | 1 LS         |
| MWRLBN          | Memory Write Lower Byte,<br>Lower Word | 1            | IN           | 1 LS         |
| MWRUBN          | Memory Write Upper Byte,<br>Lower Word | 1            | IN           | 1 LS         |
| MWRLBAN         | Memory Write Lower Byte,<br>Upper Word | 1            | IN           | 1 LS         |
| MWRUBAN         | Memory Write Upper Byte,<br>Upper Word | 1            | IN           | 1 LS         |
| MEMSIZ0-MEMSIZ6 | Memory Size                            | 7            | OUT          | 74S38        |
| PWRINTN         | Power Interrupt                        | 1            | IN           | 1 S          |
| NORMN           | Normalize                              | 1            | IN           | 1 TTL        |
| CRERN           | Correctable Error                      | 1            | OUT          | 74S38        |
| UCERN           | Uncorrectable Error                    | 1            | OUT          | 74S38        |
| STATN           | Status                                 | 1            | IN           | 1 S          |
| STAVN           | Status Available                       | 1            | OUT          | 74S38        |
| MBN             | Memory Busy                            | 1            | OUT          | 74S38        |
| CLRBYN          | Clear Busy                             | 1            | OUT          | 74S38        |
| LGFUL           | Logful                                 | 1            | OUT          | 74S74        |
| ERR             | Error                                  | 1            | IN           | 74121        |
| BGN             | Begin Log                              | 1            | IN           | 1 S          |
| CLRN            | Clear Log                              | 1            | IN           | 1 TTL        |
| EXAMN           | Examine Log                            | 1            | IN           | 1 S          |



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### 3.2.3 Interface Signal Description

#### 3.2.3.1 Address Available (ADRAVN)

ADRAVN initiates the start of a Read, Write or Read/Modify/Write cycle. The command must be a low and remain low until the assertion of ADRAVN.

#### 3.2.3.2 Address Accepted (ADRACN)

ADRACN is asserted to indicate that the addressed memory modules have accepted the Address Available address and cycle control information which is validated by ADRAVN. This information may go invalid when ADRACN goes true. If there is no Refresh contention, ADRACN will go true within 80 nanoseconds of receipt of ADRAVN. If Refresh wins the contention, ADRACN will go true within 780 nanoseconds of receipt of ADRAVN. The ADRACN output is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

#### 3.2.3.3 Address

Addresses ADROON-ADR16N are required to select one BSA board with the system operating in a 36 bit mode. Addresses ADROON-ADR17N are required to select one BSA board with the system operating in an 18 bit mode. Addresses ADR17N-ADR20N or ADR18N-ADR21N are used to select up to 16 BSA boards in the 18 bit or 36 bit configuration. Addresses ADR22N-ADR24N are used when expansion beyond one 8 megabyte system is required. All addresses must be stable 50 nanoseconds prior to Address Available (ADRAVN) and remain stable until ADRAVN goes false.

#### 3.2.3.4 Reponse Address Valid (RADVLDN)

RADVLDN acts as Data Clock for both Read and Write transfers to and from the memory. For Read transfers, assertion of RADVLDN will enable ODAVN and DTA bus drivers. RADVLDN going false acts as "Output Data Accepted". ODAVN will go false in response to RADVLDN going false. For Write transfers, assertion of RADVLDN assumes the role of "Input Data Available". The data bus shall be valid a minimum of 20 nanoseconds before assertion of RADVLDN.

RADVLDN also assumes the role of "Start Write Half Cycle" for Write full cycle and the Write portion of Read/Modify/Write half cycle operations.

RADVLDN must be asserted and go false during or after a Read full cycle or Read half cycle prior to any further full cycle or half cycle operations. In the case of Read/Modify/Write operations, two assertions of RADVLDN are required.



### 3.2.3.5 Memory Data (DTA00N-DTA35N)

Memory Data consists of up to 36 single rail bidirectional bits. For a Read operation, DTA00N-DTA35N will be valid when ODAVN goes true and become invalid when ODAVN goes false. For a Write operation, DTA00N-DTA35N shall be valid 20 nanoseconds prior to assertion of RADVLDN and remain valid until IDACN goes true.

The data bus consists of four bytes defined as follows:

Lower Word Lower Byte - DTA08N-DTA16N  
Lower Word Upper Byte - DTA00N-DTA07N, DTA17

Upper Word Lower Byte - DTA26-DTA34  
Upper Word Upper Byte - DTA18-DTA25, DTA35

Data bus is non-inverting (a low written into memory results in a low read from memory) and is low-true. Data outputs are derived from 74S38 open collector gates and shall be pulled-up at the receiving end.

For an 18 bit configuration, upper word data bits are internally wired in parallel with the lower data bits. Address ADROON is then used to control selection of upper or lower words.

Data bits DTA00N-DTA15N are also used to provide error log information when enabled by the signal STATN or EXAMN. The memory chip in error is defined as follows:

|                     |               |
|---------------------|---------------|
| BSA Board Number    | DTA03N-DTA06N |
| Chip Row Number     | DTA00N-DTA02N |
| Exact Bit in Error  | DTA07N-DTA12N |
| Uncorrectable Error | DTA13N        |
| Log Location Empty  | DTA14N        |
| Correctable Error   | DTA15N        |

### 3.2.3.6 Output Data Available (ODAVN)

Assertion of ODAVN indicates that output data is valid and will remain valid until RADVLDN goes false. During a Read operation when RADVLDN is true, ODAVN will go true no later than 400 nanoseconds from ADRAVN and will go false after RADVLDN goes false. (See Figures 1, 2 and 5) ODAVN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.



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### 3.2.3.7 Input Data Accepted (IDACN)

Assertion of IDACN by the memory module indicates that input data validated by RADVLDN has been accepted. IDACN will go true after RADVLDN goes true and will go false after RADVLDN goes false. (See Figures 3, 4, and 5)

IDACN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

### 3.2.3.8 Cycle Control Lines (MRDRN, MWRLBN, MWRUBN, MWRLBAN, MWRUBAN)

The cycle control lines, Memory Read (MRDRN), Memory Write Lower Byte (MWRLBN), Memory Write Upper Byte (MWRUBN), Memory Write Lower Byte Upper Word (MWRLBAN) and Memory Write Upper Byte Upper Word (MWRUBAN) are used to control the various Read/Write modes of operation. MRDRN, MWRLBN and MWRUBN shall be valid 50 nanoseconds prior to ADRAVN and remain valid until ADRAVN goes false. Tables I and II define the various modes of operation for all combinations of MRDRN, MWRLBN, MWRUBN, MWRLBAN and MWRUBAN.

### 3.2.3.9 Memory Size (MEMSIZ0-MEMSIZ6)

The MEMSIZ0-MEMSIZ6 outputs are sent to the processor to indicate total memory capacity of expanded systems. The use of MEMSIZ0-MEMSIZ6 will prevent addressing of non-present memory modules to avoid hang-up conditions from failure to receive ADRAVN from non-present memory modules. The MEMSIZ0-MEMSIZ6 signals are derived from 74S38 open collector gates and shall be pulled-up at the receiving end.



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### 3.2.3.10 Power Interrupt (PWRINTN)

The power system shall drive PWRINTN when loss of logic or storage power is detected. PWRINTN shall be asserted as early as possible after power failure is detected, but in no case so late as to allow malfunction of a busy memory board. The busy memory will complete the cycle requested and will inhibit any further cycles from being initiated. A not busy memory will not initiate any cycles when PWRINTN is asserted.

### 3.2.3.11 Normalize (NORMN)

The NORMN signal acts as a general reset. The NORMN will clear all internal memory control registers, cause all memory modules to go "unbusy" and abort any outstanding data transfers. This may cause a Write cycle to store erroneous data. No further cycles may be initiated until NORMN goes false. NORMN must be asserted for at least 150 nanoseconds.

### 3.2.3.12 Correctable Error (CRERN)

The correctable error signal is asserted during valid data time in a Read cycle when a correctable error has occurred in the memory. If a correctable error has occurred, CRERN shall be true when ODAVN goes true and shall remain true until ODAVN goes false. CRERN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

### 3.2.3.13 Uncorrectable Error (UCERN)

The uncorrectable error signal is asserted during valid data time in a Read cycle when an uncorrectable error has occurred in the memory. If an uncorrectable error has occurred, UCERN shall be true when ODAVN goes true and shall remain true until ODAVN goes false. UCERN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

### 3.2.3.14 Status (STATN)

Status is asserted when the error log is to be examined from the memory bus. Assertion of STATN disables memory data and steers error log information to Data Bits DTA00N-DTA15N on the memory data bus. The command must be a low and remain low until the assertion of STAVN. When STATN is asserted in direct response to receipt of an error signal, the log will present that error information. Repetitive assertions of status will sequentially examine the 64 log locations.



### 3.2.3.15 Status Available (STAVN)

Status Available is asserted by the memory to indicate that the error log information is available. Status Available will go low 450 nanoseconds after receipt of status and remain low until status goes false. STAVN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end.

### 3.2.3.16 Memory Busy (MBN)

Memory Busy is asserted when ADRAVN is accepted by the memory and shall remain asserted until the memory has completed its cycle. MBN is also asserted upon power up while the memory is performing an internal clear. MBN is derived from a 74S38 open collector gate and shall be pulled-up at the receiving end. MBN is not asserted during a Refresh cycle.

### 3.2.3.17 Clear Busy (CLRBYN)

Clear Busy is asserted by the memory upon power up to indicate that the memory is performing an internal clear operation. An internal memory clear is necessary to establish proper parity in the ECC circuitry and to clear the error log. CLRBYN will go low at power up and remain low for 4 seconds. CLRBYN will not be asserted and the memory will not be internally cleared if BBU is utilized and main power fails. CLRBYN is derived from a 74S38 open collector gate and shall be pulled up at the receiving end.

### 3.2.3.18 Logfull (LGFUL)

Logfull is high true asserted by the memory when the maximum address of the 64 word error log has been reached. LGFUL is driven by a 74S74 and is used in conjunction with a BULK SEMI chassis to drive Logfull indicator light circuitry. After the LGFUL signal is asserted, the log will wrap around and continue to log errors beginning again at the lowest log address.

### 3.2.3.19 Error (ERR)

Error is a high true signal of approximately one second duration asserted by the memory each time a correctable or uncorrectable error has occurred. ERR is driven by 74121 and is used in conjunction with a BULK SEMI chassis to drive error indicator light circuitry.



3.2.3.20 Begin Log (BGN)

Begin Log is low true asserted when the error log is to be returned to the lowest log address. BGN must be low for a minimum of 150 nanoseconds and is normally used in conjunction with a BULK SEMI chassis.

3.2.3.21 Clear Log (CLRN)

Clear Log is asserted when all 64 locations of the error log are to be cleared. CLRN must be low for a minimum of 150 nanoseconds. A log clear operation takes 72 microseconds. Completion of a log clear results in assertion of Logfull from the memory. CLRN is normally used in conjunction with a BULK SEMI chassis.

3.2.3.22 Examine Log (EXAMN)

Examine Log is used in conjunction with a BULK SEMI chassis. Assertion of EXAMN performs the same operation as STATN. In the BULK SEMI chassis, error information will be displayed as long as EXAMN is asserted.



#### 4.0 MECHANICAL SPECIFICATIONS

The BSA and BSC cards measure 13.64" x 16.4" and are designed to fit on a minimum of 0.75 inch centers. (See Figure 6.) The cards contain two 120-pin .100 center card edge connector interfaces designated P9 and P10. Stiffeners are utilized to add additional strength to the cards.

#### 5.0 ENVIRONMENTAL SPECIFICATIONS

##### 5.1 Cooling

BSC                      50 cfm  
BSA (each)              15 cfm

##### 5.2 Storage Temperature

-40<sup>0</sup> to +80<sup>0</sup>C

##### 5.3 Operating Temperature

0<sup>0</sup> to +55<sup>0</sup>C

##### 5.4 Relative Humidity

Up to 95% without condensation

##### 5.5 Vibration

Will withstand normal stresses encountered in transport

##### 5.6 Weight

2.25 pounds (1.02 kg) per BSC  
2.75 pounds (1.25 kg) per BSA

#### 6.0 ORDERING INFORMATION

The following part numbers have been assigned to the DR-129S:

|                            |           |       |
|----------------------------|-----------|-------|
| BULK SEMI Controller (BSC) | 128K x 36 | 62904 |
| BULK SEMI Controller (BSC) | 256K x 18 | 62901 |
| BULK SEMI Array (BSA)      | 128K x 43 | 62902 |
| BULK SEMI Array (BSA)      | 64K x 43  | 62903 |



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36 BIT CONFIGURATION

| MRDRN | Lower Word |        | Upper Word |         | Cycle   |
|-------|------------|--------|------------|---------|---|
|       | MWRLBN     | MWRUBN | MWRLBAN    | MWRUBAN |   |
| LOW   | HIGH       | HIGH   | HIGH       | HIGH    | READ DBL WORD                                     |
| HIGH  | LOW        | HIGH   | HIGH       | HIGH    | WRITE LOWER BYTE LOWER WORD                       |
| HIGH  | HIGH       | LOW    | HIGH       | HIGH    | WRITE UPPER BYTE LOWER WORD                       |
| HIGH  | HIGH       | HIGH   | LOW        | HIGH    | WRITE LOWER BYTE UPPER WORD                       |
| HIGH  | HIGH       | HIGH   | LOW        | LOW     | WRITE UPPER BYTE UPPER WORD                       |
| HIGH  | LOW        | LOW    | HIGH       | HIGH    | WRITE LOWER WORD                                  |
| HIGH  | HIGH       | HIGH   | LOW        | LOW     | WRITE UPPER WORD                                  |
| HIGH  | LOW        | LOW    | LOW        | LOW     | WRITE DBL WORD                                    |
| LOW   | LOW        | LOW    | LOW        | LOW     | *READ DBL WORD MODIFY WRITE DBL WORD              |
| LOW   | LOW        | HIGH   | HIGH       | HIGH    | *READ DBL WORD MODIFY WRITE LOWER BYTE LOWER WORD |
| LOW   | HIGH       | LOW    | HIGH       | HIGH    | *READ DBL WORD MODIFY WRITE UPPER BYTE LOWER WORD |
| LOW   | HIGH       | HIGH   | LOW        | HIGH    | *READ DBL WORD MODIFY WRITE LOWER BYTE UPPER WORD |
| LOW   | HIGH       | HIGH   | HIGH       | LOW     | *READ DBL WORD MODIFY WRITE UPPER BYTE UPPER WORD |
| LOW   | LOW        | LOW    | HIGH       | HIGH    | *READ DBL WORD MODIFY WRITE LOWER WORD            |
| LOW   | HIGH       | HIGH   | LOW        | LOW     | *READ DBL WORD MODIFY WRITE UPPER WORD            |

\*The processor must accept read data from memory prior to transmitting the write data.

TABLE I



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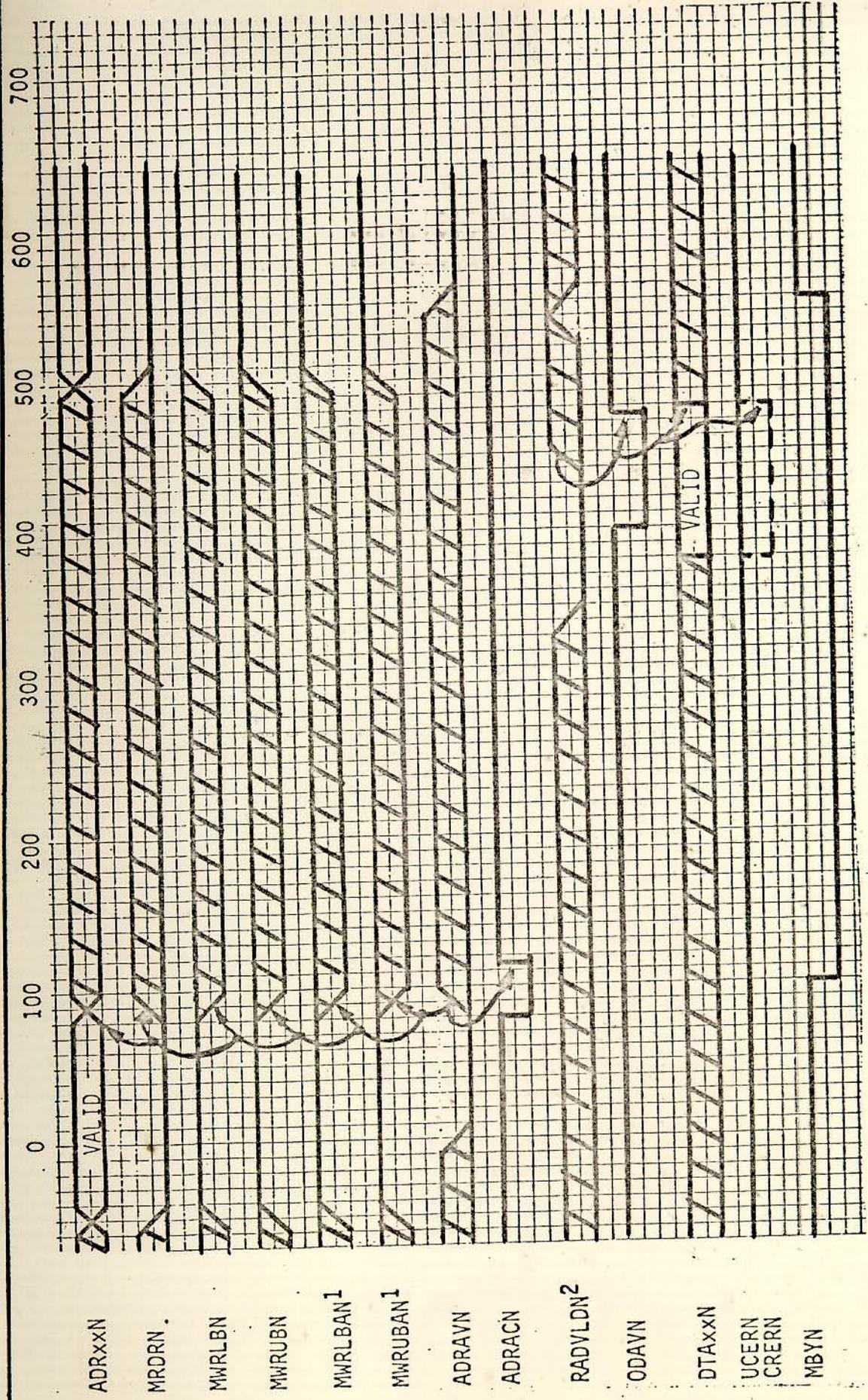
18 BIT CONFIGURATION

| MRDRN | MWRLBN | MWRUBN | Cycle                              |
|-------|--------|--------|------------------------------------|
| LOW   | HIGH   | HIGH   | READ WORD                          |
| HIGH  | LOW    | HIGH   | WRITE LOWER BYTE                   |
| HIGH  | HIGH   | LOW    | WRITE UPPER BYTE                   |
| HIGH  | LOW    | LOW    | WRITE WORD                         |
| LOW   | LOW    | HIGH   | *READ WORD MODIFY WRITE LOWER BYTE |
| LOW   | HIGH   | LOW    | *READ WORD MODIFY WRITE UPPER BYTE |
| LOW   | LOW    | LOW    | *READ WORD MODIFY WRITE WORD       |

\*The processor must accept read data from memory prior to transmitting the write data.

TABLE II





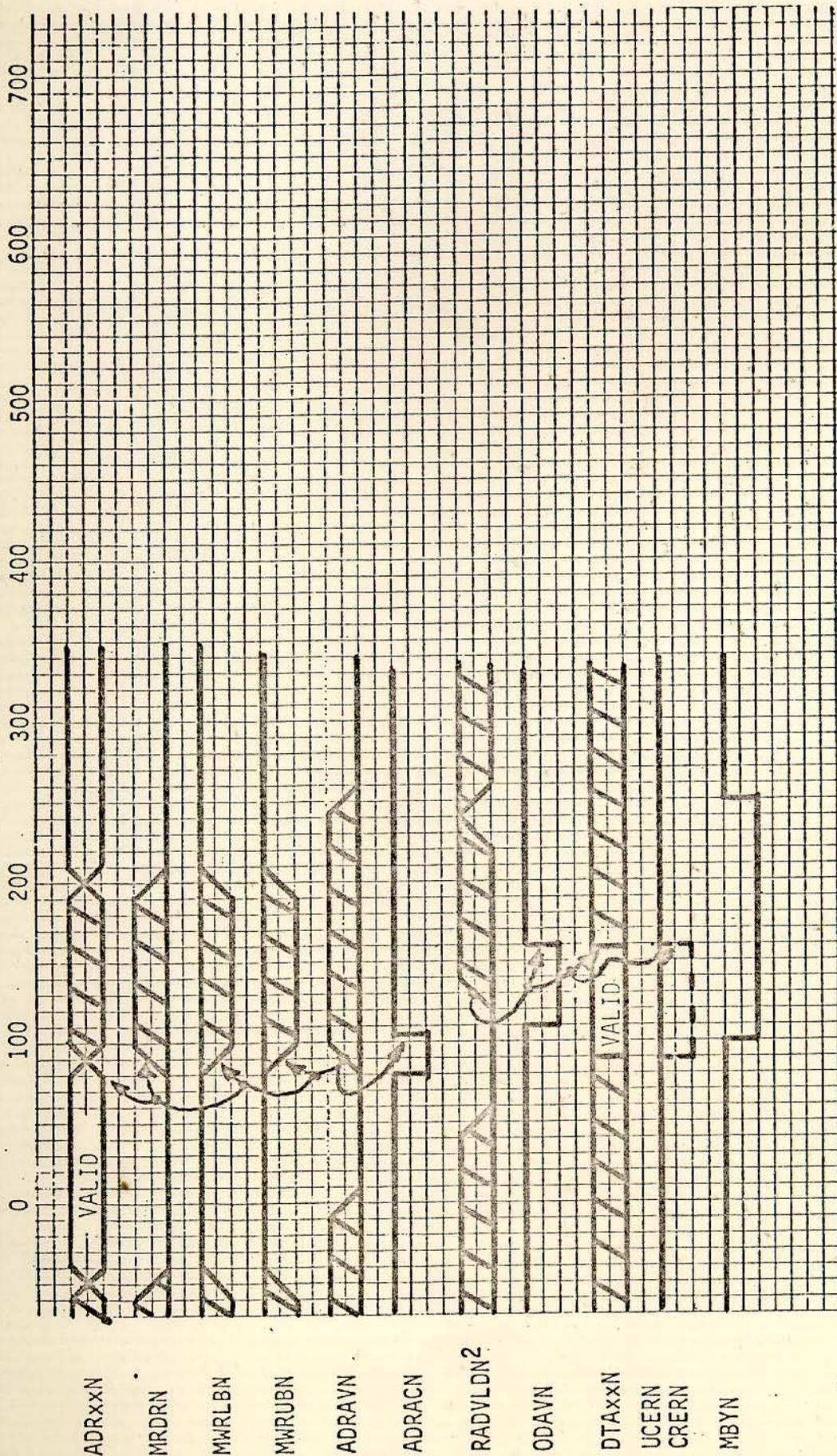
- 1 - Double Word Read Only
- 2 - During a Read Word or Double Word RADVLDN may occur at anytime, however, if it occurs later than 340 nanoseconds after ADRAVN, ODAVN and DTAXxN will be delayed by an equal amount. If RADVLDN is not set to an untrue state (high) at 460 nanoseconds or less after ADRAVN, MBYN will be extended an equal amount; thus increasing the cycle time of 550 nanoseconds.

READ WORD or DOUBLE WORD  
Figure 1



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1 - For 18 Bit BSC Only

2 - During a Match Read Word RADVLDN may occur at anytime, however, if it occurs later than 50 nanoseconds after ADRAVN, ODAVN and DTAXxN will be delayed by an equal amount. If RADVLDN is not set to an untrue state (High) at 130 nanoseconds or less, MBYN will be extended an equal amount; thus increasing the cycle time of 250 nanoseconds.

MATCH READ WORD

Figure 2



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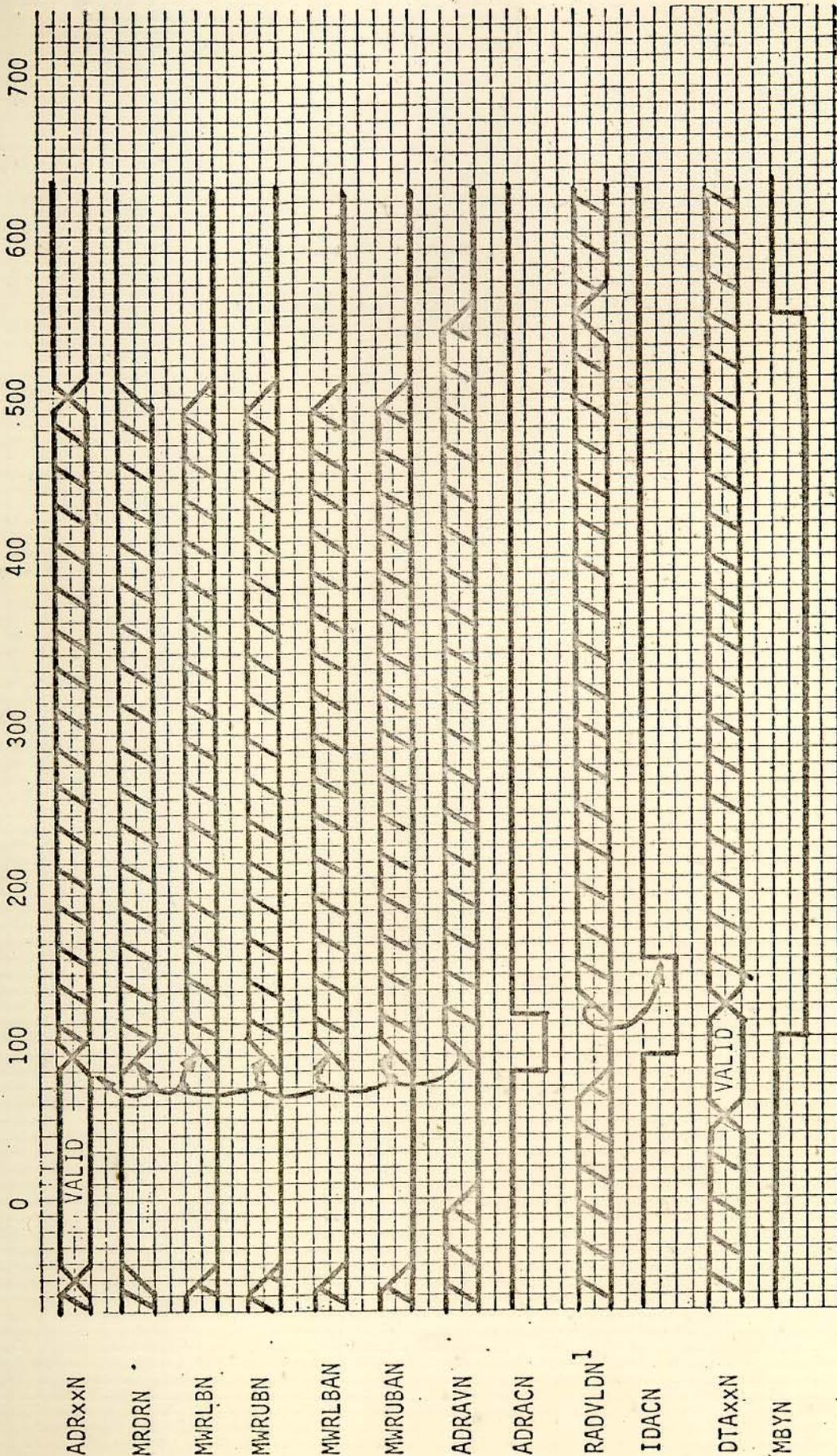
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REV.

C



1 - During a Write Double Word, RADVLDN may occur at anytime, however, if it occurs later than 65 nanoseconds after ADRAVN, IDACN will be delayed by an equal amount. If RADVLDN occurs later than 195 nanoseconds after ADRAVN, MBYN will be extended an equal amount; thus increasing the cycle time of 550 nanoseconds.

WRITE DOUBLE WORD

Figure 3



**DATARAM CORPORATION**  
CRANBURY NEW JERSEY

DWG. NO.

02126

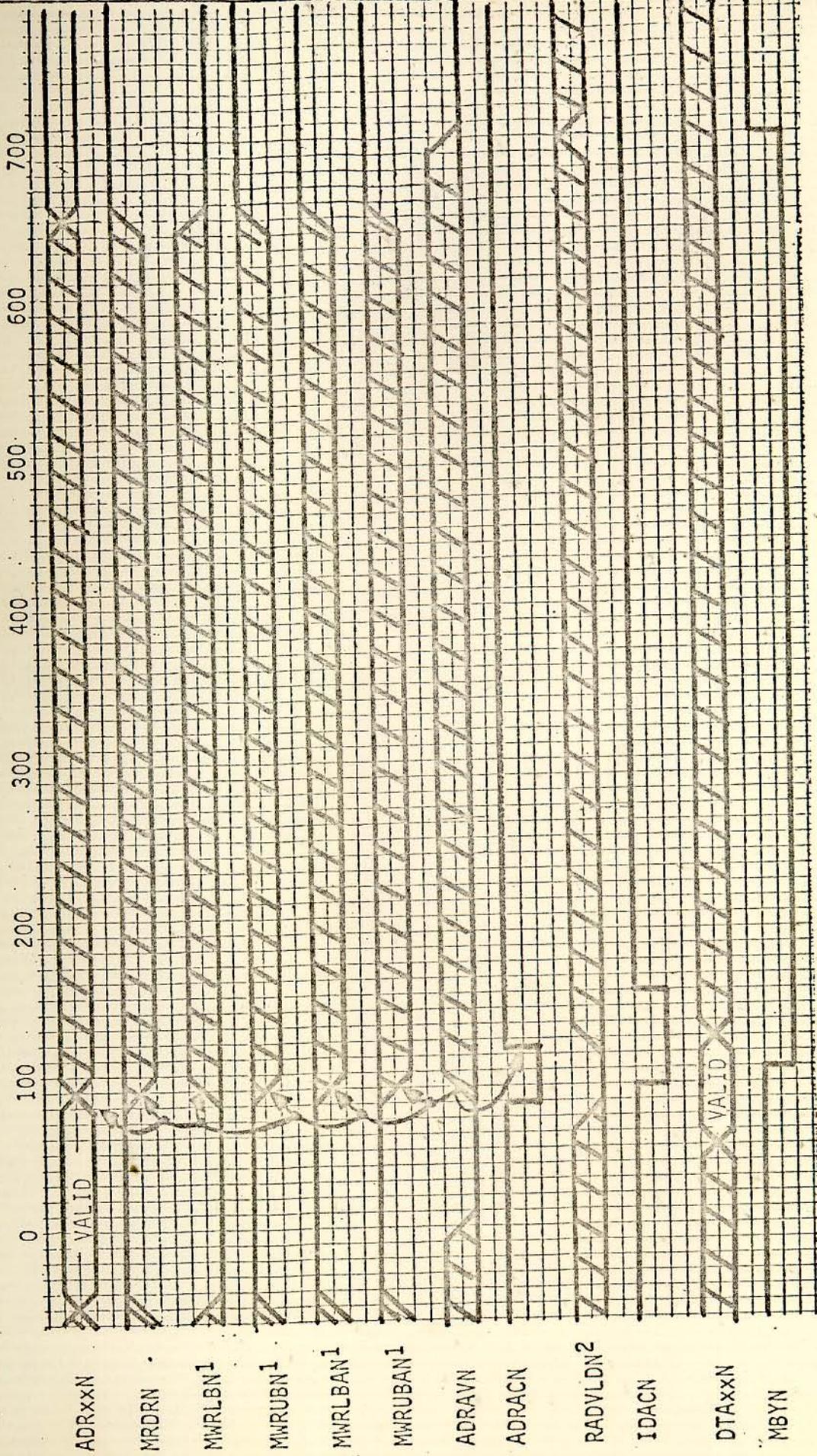
SHEET

18

OF

22

REV.



1 - Timing shown for a Write Lower Byte only. See operating mode table.

2 - During a Write/Byte, RADVLDN may occur at anytime, however, if it occurs later than 65 nanoseconds after ADRAVN, IDACN will be delayed by an equal amount. If RADVLDN occurs later than 420 nanoseconds after ADRAVN, MBYN will be extended an equal amount; thus increasing the cycle time of 700 nanoseconds.

WRITE/BYTE or WRITE/WORD

Figure 4

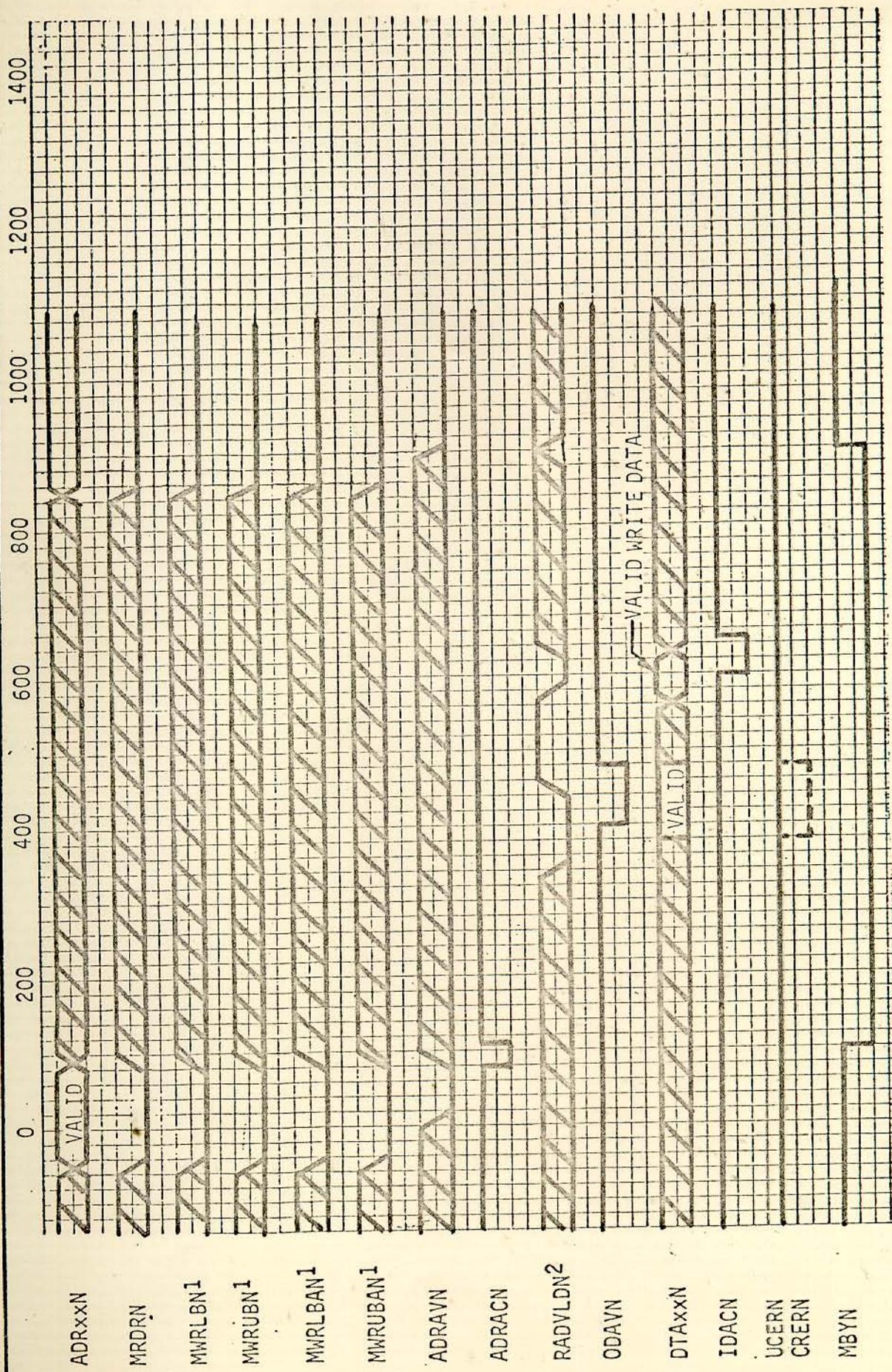


**DATARAM CORPORATION**  
CRANBURY NEW JERSEY

|          |          |
|----------|----------|
| DWG. NO. | 02126    |
| SHEET    | 19 OF 22 |

REV.

C



- 1 - Timing for R/M/Write-Byte or Word is the same as shown except as detailed in operating mode tables.
- 2 - During a R/M/W RADVLDN must occur twice. If RADVLDN occurs later than 340 nanoseconds after ADRAVN during the Read portion of the R/M/W cycle, ODAVN and DTAXxN will be delayed an equal amount. If RADVLDN is not set to an untrue state at 460 nanoseconds or less during the Read portion of the R/M/W cycle, MBYN will be extended an equal amount; thus increasing the cycle time of 900 nanoseconds.

READ/MODIFY/WRITE DOUBLE WORD

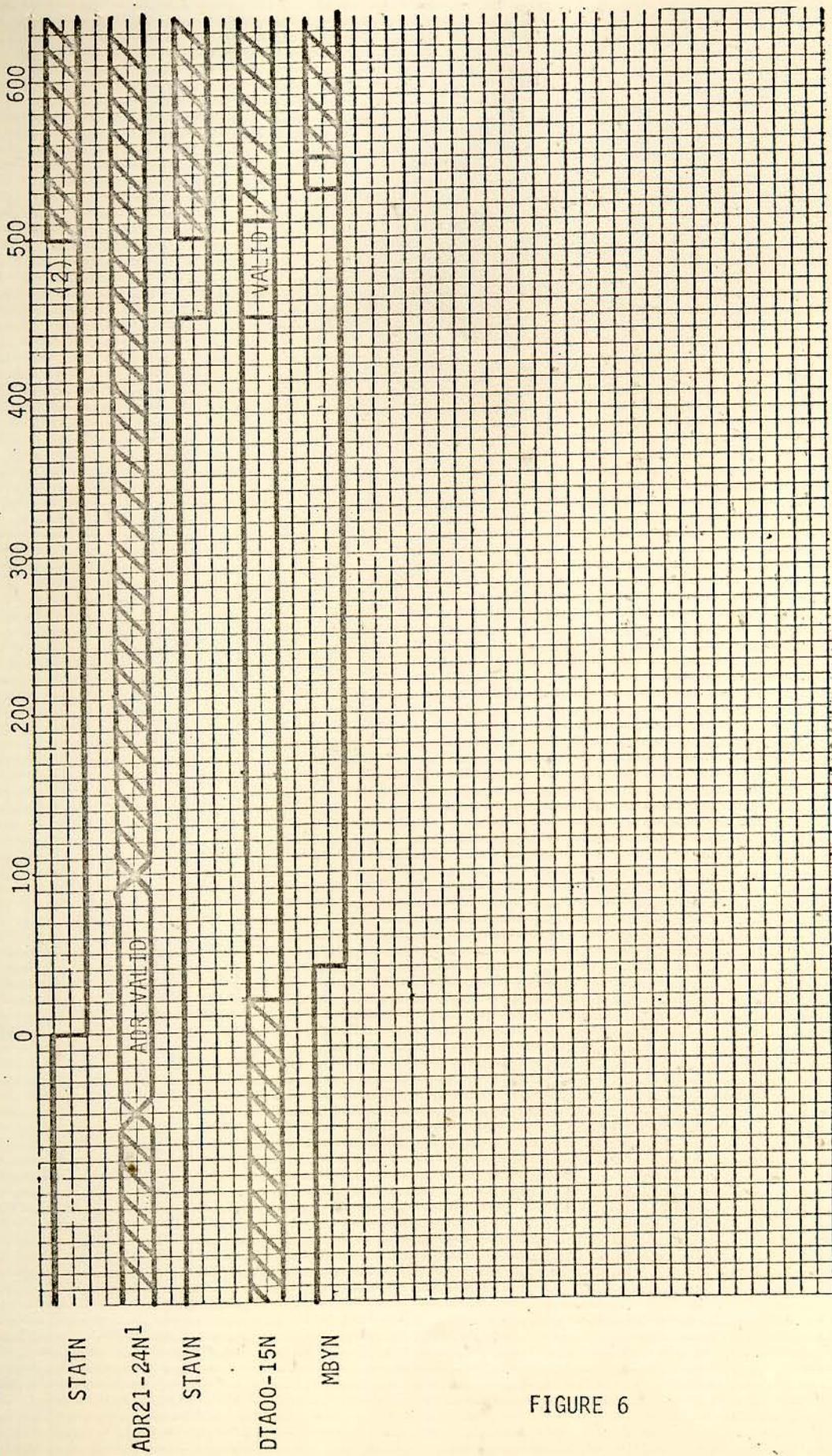
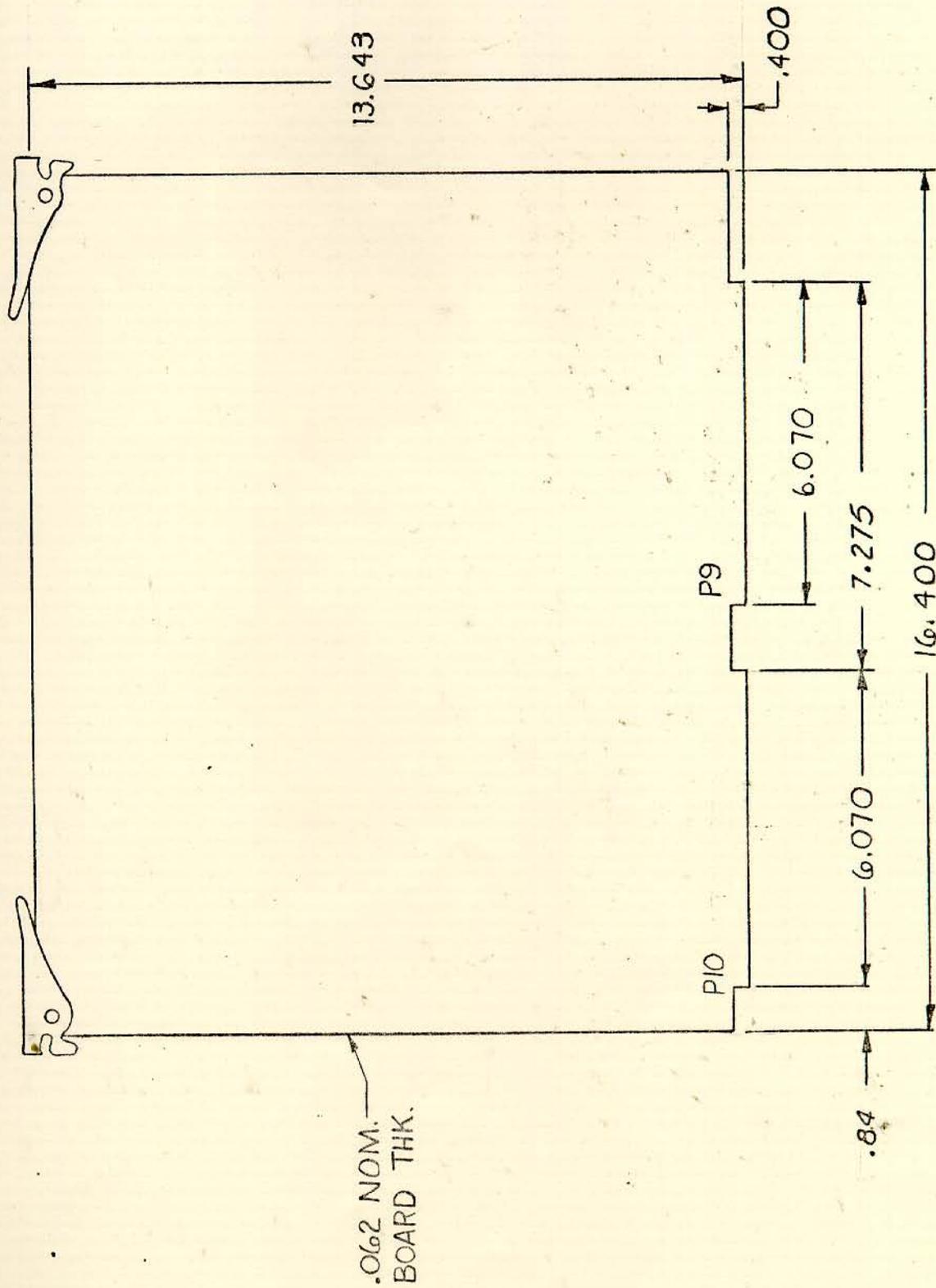


FIGURE 6

- 1 - During an Examine cycle ADR21-24N are not used.
- 2 - If STATN does not go untrue at 500 nanoseconds STAVN, DTAXXN and MBYN will be extended an equal amount.

LOG STATUS (EXAMINE) READ CYCLE



MECHANICAL OUTLINE  
BULK SEMICONDUCTOR MODULE

FIGURE 7

DOCUMENTATION

Schematic Diagram

Document No. 03191, BSC  
03183, BSA

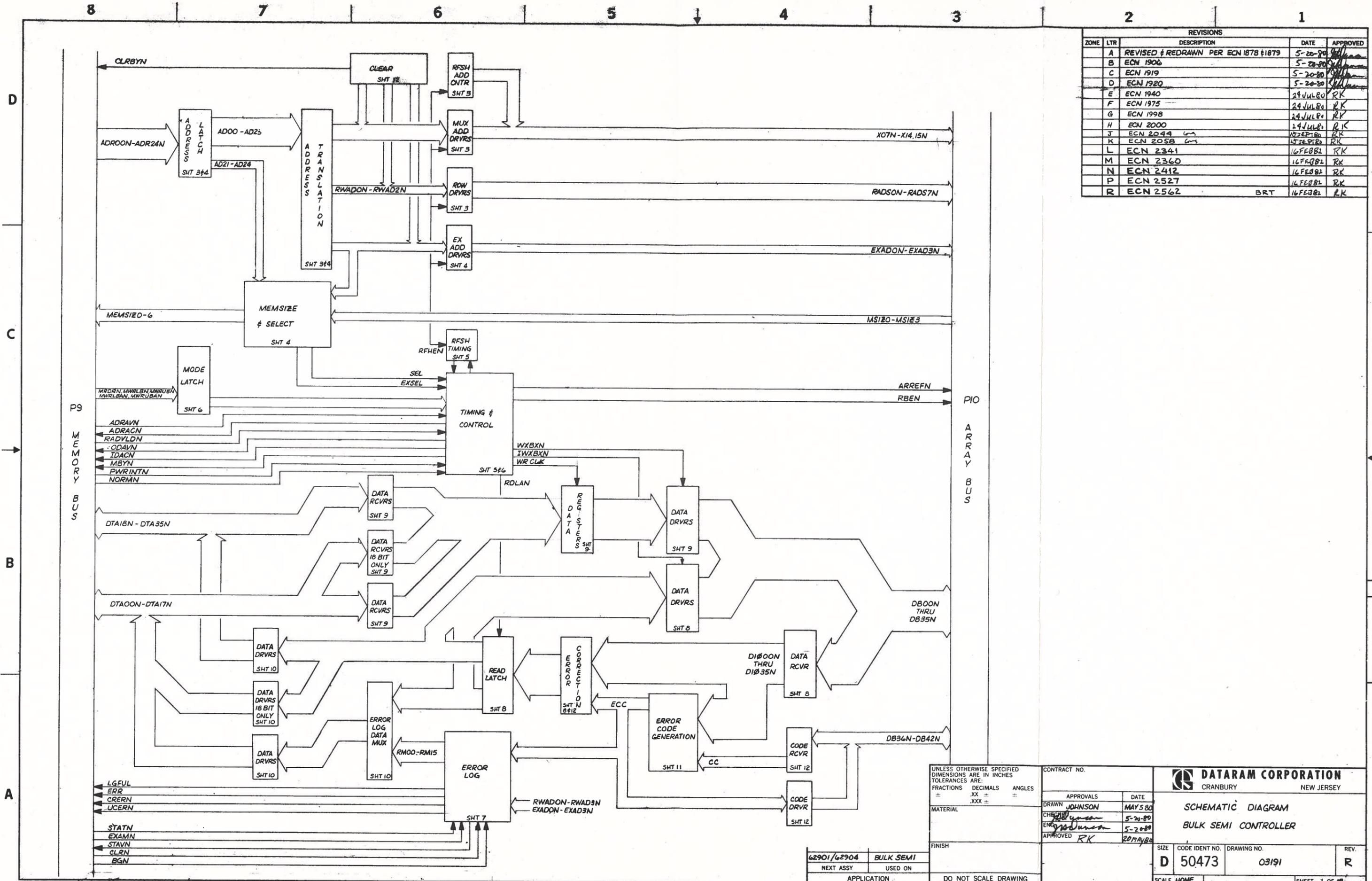
System Assembly Drawing

Document No. 62901, BSC  
62902, BSA

System Bill of Materials

Document No. 62901, BSC  
62902, BSA

| REVISIONS |     |                                       |               |          |
|-----------|-----|---------------------------------------|---------------|----------|
| ZONE      | LTR | DESCRIPTION                           | DATE          | APPROVED |
| A         |     | REVISED & REDRAWN PER ECN 1878 & 1879 | 5-20-80       |          |
| B         |     | ECN 1906                              | 5-20-80       |          |
| C         |     | ECN 1919                              | 5-20-80       |          |
| D         |     | ECN 1920                              | 5-20-80       |          |
| E         |     | ECN 1940                              | 24 JUL 80     | RK       |
| F         |     | ECN 1975                              | 24 JUL 80     | RK       |
| G         |     | ECN 1998                              | 24 JUL 80     | RK       |
| H         |     | ECN 2000                              | 24 JUL 80     | RK       |
| J         |     | ECN 2044                              | 17 SEP 80     | RK       |
| K         |     | ECN 2058                              | 15 SEP 80     | RK       |
| L         |     | ECN 2341                              | 16 FEB 82     | RK       |
| M         |     | ECN 2360                              | 16 FEB 82     | RK       |
| N         |     | ECN 2412                              | 16 FEB 82     | RK       |
| P         |     | ECN 2527                              | 16 FEB 82     | RK       |
| R         |     | ECN 2562                              | BRT 16 FEB 82 | LK       |



|  |  |              |  |   |  |
|--|--|--------------|--|---|--|
| UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:<br>FRACTIONS DECIMALS ANGLES<br>± .XX ± .XXX ± |  | CONTRACT NO. |  |   |  |
| APPROVALS  |  | DATE         |  | <b>SCHEMATIC DIAGRAM</b><br><b>BULK SEMI CONTROLLER</b> |  |
| DRAWN JOHNSON  |  | MAY 5 80     |  | SIZE CODE IDENT NO. DRAWING NO. REV.                    |  |
| CHECKED  |  | 5-20-80      |  | D 50473 03191 R   |  |
| ENGR JOHNSON   |  | 5-20-80      |  | SCALE NONE SHEET 1 OF 12                                |  |
| APPROVED RK  |  | 20 MAY 80    |  |   |  |
| FINISH   |  |              |  | APPLICATION USED ON DO NOT SCALE DRAWING                |  |
| 62901/02904 BULK SEMI  |  |              |  |   |  |
| NEXT ASSY  |  |              |  |   |  |

| REVISIONS |     |             |      |          |
|-----------|-----|-------------|------|----------|
| ZONE      | LTR | DESCRIPTION | DATE | APPROVED |
|           |     |             |      |          |

| P9  |         |         |
|-----|---------|---------|
| 2   | GND     | GND     |
| 4   | +5V     | +5V     |
| 6   | DTA06N  | DTA15N  |
| 8   | ADRO7N  | ADRO5N  |
| 10  |         | DAT07N  |
| 12  |         | ADR17N  |
| 14  | DTA32N  | DTA14N  |
| 16  | DTA24N  | ADRO6N  |
| 18  | DTA34N  | DTA16N  |
| 20  | DTA25N  | ADR13N  |
| 22  | DTA23N  | DTA05N  |
| 24  | DTA33N  | ADRO3N  |
| 26  | DTA35N  | DTA17N  |
| 28  | ADR24N  | ADR15N  |
| 30  | DTA31N  | DTA13N  |
| 32  | STATN   | ADR16N  |
| 34  | DTA22N  | DTA04N  |
| 36  | STAVN   | ADR10N  |
| 38  | UCERN   | IDACN   |
| 40  | CRERN   | ADRO0N  |
| 42  | CLRBYN  | QDAVN   |
| 44  | MEMSIZ3 | ADRO4N  |
| 46  | MEMSIZ4 | ADRACN  |
| 48  | MEMSIZ5 | ADR12N  |
| 50  | MEMSIZ6 | ADRO8N  |
| 52  |         | ADRO1N  |
| 54  | ADRZON  | ADRO9N  |
| 56  | ADR21N  | ADRO2N  |
| 58  | ADR22N  | ADR11N  |
| 60  | GND     | GND     |
| 62  | ADR23N  | ADR13N  |
| 64  | GND     | GND     |
| 66  | MWRUBAN | MWRUBN  |
| 68  |         | PWINTN  |
| 70  |         | MRDRN   |
| 72  |         | NORMN   |
| 74  | MWRUBAN | MWRUBN  |
| 76  |         | RADVLDN |
| 78  | GND     | GND     |
| 80  |         | ADR17N  |
| 82  |         | ADR18N  |
| 84  |         | ADR19N  |
| 86  |         |         |
| 88  |         |         |
| 90  |         |         |
| 92  | DTA26N  | DTA08N  |
| 94  | DTA21N  | DTA03N  |
| 96  | DTA30N  | DTA12N  |
| 98  | DTA18N  | DTA00N  |
| 100 | DTA29N  | DTA11N  |
| 102 |         | MEMSIZ2 |
| 104 | DTA27N  | DTA09N  |
| 106 |         | MEMSIZ1 |
| 108 | DTA20N  | DTA02N  |
| 110 | DTA28N  | DTA10N  |
| 112 | DTA19N  | DTA01N  |
| 114 | MBYN    | MEMSIZ0 |
| 116 | +5V     | +5V     |
| 118 | GND     | GND     |
| 120 | GND     | GND     |

| P10 |        |        |
|-----|--------|--------|
| 2   | +15V   | +15V   |
| 4   | +15V   | +15V   |
| 6   | GND    | GND    |
| 8   | GND    | GND    |
| 10  | +5V    | +5V    |
| 12  | EXAD3N | EXAD0N |
| 14  | EXAD2N | EXAD1N |
| 16  | ARREFN | RBEN   |
| 18  | MSIZ3  | MSIZ1  |
| 20  |        |        |
| 22  |        |        |
| 24  | MSIZ2  | MSIZ0  |
| 26  |        |        |
| 28  | RADS1  | RADS3  |
| 30  | RADS5  | RADS7  |
| 32  | RADS0  | RADS2  |
| 34  | RADS4  | RADS6  |
| 36  | +5B    | +5B    |
| 38  | +5B    | +5B    |
| 40  | X1415N | X411N  |
| 42  | X07N   | X310N  |
| 44  | X512N  | X18N   |
| 46  | X613N  | X29N   |
| 48  | CASN   | WRN    |
| 50  | DB42N  | GND    |
| 52  | DB41N  | GND    |
| 54  | DB40N  | GND    |
| 56  | GND    | GND    |
| 58  | DB14N  | DB00N  |
| 60  | DB12N  | DB03N  |
| 62  | DB15N  | DB02N  |
| 64  | DB13N  | DB05N  |
| 66  | GND    | GND    |
| 68  | GND    | GND    |
| 70  | DB19N  | DB01N  |
| 72  | DB16N  | DB06N  |
| 74  | DB17N  | DB04N  |
| 76  | DB23N  | DB07N  |
| 78  | +5V    | +5V    |
| 80  | +5V    | +5V    |
| 82  | DB20N  | DB08N  |
| 84  | DB22N  | DB10N  |
| 86  | DB18N  | DB11N  |
| 88  | DB21N  | DB09N  |
| 90  | DB37N  | GND    |
| 92  | DB39N  | GND    |
| 94  | DB36N  | GND    |
| 96  | DB38N  | GND    |
| 98  | DB34N  | GND    |
| 100 | DB33N  | GND    |
| 102 | DB35N  | GND    |
| 104 | DB32N  | GND    |
| 106 | DB28N  | GND    |
| 108 | DB27N  | GND    |
| 110 | DB29N  | EXAMN  |
| 112 | DB31N  | LG-FL  |
| 114 | DB30N  | ERR    |
| 116 | DB24N  | CLR    |
| 118 | DB26N  | BGN    |
| 120 | DB25N  | GND    |

| "E" POINT | LOCATION | "E" POINT | LOCATION |
|-----------|----------|-----------|----------|
| 1         | 12C3     | 61        | 7C4      |
| 2         | 12C3     | 62        | 7C4      |
| 3         | 4B1      | 63        | 7C4      |
| 4         | 4B1      | 64        | 7C4      |
| 5         | 9D3      | 65        | 7C4      |
| 6         | 9D3      | 66        | 7C4      |
| 7         | 3A6      | 67        | 5C4      |
| 8         | 3A6      | 68        | 5C4      |
| 9         | 12B7     | 69        | 12A3     |
| 10        | 12B7     | 70        | 12A3     |
| 11        | 4A6      | 71        | 12A3     |
| 12        | 4A6      | 72        | 7C4      |
| 13        | 4D2      | 73        | 10B3     |
| 14        | 4D2      | 74        | 10B3     |
| 15        | 4D2      | 75        | 12A6     |
| 16        | 4D2      | 76        | 12A6     |
| 17        | 4D2      | 77        | 12C3     |
| 18        | 4D2      | 78        | 12C3     |
| 19        | 4D2      | 79        | 7C8      |
| 20        | 4D2      | 80        | 7C8      |
| 21        | 4D2      | 81        | 7C8      |
| 22        | 4D2      | 82        | NOT USED |
| 23        | 4D2      | 83        | NOT USED |
| 24        | 4D3      | 84        | 5D8      |
| 25        | 4D3      | 85        | 5D8      |
| 26        | 4B1      | 86        | 5B7      |
| 27        | 4B1      | 87        | 5B7      |
| 28        | 4B1      |           |          |
| 29        | 4A1      |           |          |
| 30        | 4A1      |           |          |
| 31        | 4A1      |           |          |
| 32        | 4A1      |           |          |
| 33        | 4A1      |           |          |
| 34        | 4A1      |           |          |
| 35        | 4A1      |           |          |
| 36        | 4B1      |           |          |
| 37        | 4A1      |           |          |
| 38        | 4A1      |           |          |
| 39        | 4A1      |           |          |
| 40        | 4A1      |           |          |
| 41        | 4A1      |           |          |
| 42        | 4A1      |           |          |
| 43        | 4D3      |           |          |
| 44        | 4D4      |           |          |
| 45        | 4A2      |           |          |
| 46        | 4A2      |           |          |
| 47        | 6D7      |           |          |
| 48        | 6C7      |           |          |
| 49        | 6C7      |           |          |
| 50        | 6C7      |           |          |
| 51        | 4B2      |           |          |
| 52        | 4B2      |           |          |
| 53        | 6C7      |           |          |
| 54        | 6C7      |           |          |
| 55        | 6C5      |           |          |
| 56        | 6C5      |           |          |
| 57        | 4A2      |           |          |
| 58        | 4A2      |           |          |
| 59        | 63B      |           |          |
| 60        | 63B      |           |          |

| LAST DESIGNATION USED |      |
|-----------------------|------|
| INTEGRATED CIRCUIT    | Z218 |
| JUMPER                | E87  |
| RESISTOR              | R116 |
| CAPACITOR             | C99  |
| RESISTOR MODULE       | RM22 |
| TRANSISTOR            | QG   |
| DIODE                 | CR6  |
| INDUCTOR              | L4   |

| REFERENCE DESIGNATION | GATES USED PER TOTAL | PART NUMBER |
|-----------------------|----------------------|-------------|
| Z11                   | 1/4                  | 74S132      |
| Z15                   | 2/3                  | 74S10       |
| Z26                   | 3/4                  | 74LS08      |
| Z36                   | 3/4                  | 74S08       |
| Z38                   | 5/6                  | 74S04       |
| Z40                   | 2/3                  | 74S10       |
| Z25                   | 3/4                  | 74LS32      |
| Z45                   | 1/2                  | 26502       |
| Z59                   | 3/4                  | 74S132      |
| Z60                   | 1/3                  | 74S10       |
| Z64                   | 1/2                  | 26502       |
| Z70                   | 1/2                  | 74LS74      |
| Z80                   | 5/6                  | 74LS04      |
| Z81                   | 3/4                  | 74132       |
| Z89                   | 2/4                  | 74S06       |
| Z103                  | 1/8                  | 74S240      |
| Z107                  | 2/8                  | 74S240      |
| Z110                  | 2/4                  | 74S38       |
| Z121                  | 1/8                  | 74S374      |
| Z122                  | 2/8                  | 74S240      |
| Z123                  | 1/8                  | 74S373      |
| Z154                  | 5/6                  | 74S04       |
| Z162                  | 2/8                  | 74S240      |
| Z163                  | 2/8                  | 74S240      |
| Z164                  | 2/8                  | 74S240      |
| Z165                  | 1/8                  | 74S241      |
| Z173                  | 1/4                  | 74S257      |
| Z181                  | 3/4                  | 74LS32      |
| Z183                  | 1/2                  | 74S53       |
| Z185                  | 1/8                  | 74S240      |
| Z186                  | 1/8                  | 74S241      |
| Z197                  | 3/4                  | 74S08       |
| Z199                  | 3/4                  | 74S257      |
| Z201                  | 5/8                  | 74S373      |
| Z202                  | 1/6                  | 74LS241     |
| Z211                  | 1/3                  | 74S11       |
| Z212                  | 1/2                  | 74S20       |
| Z213                  |                      | SPARE       |
| Z214                  |                      | SPARE       |
| Z215                  | 1/4                  | 74S32       |
| Z217                  | 3/4                  | 74S38       |
| Z218                  | 2/4                  | 74S38       |

| OPTIONS    |                                |
|------------|--------------------------------|
| JUMPER     | FUNCTION                       |
| E1 TO E2   | ODD/EVEN PARITY                |
| E73 TO E74 | JUMPER TO DISABLE PARITY ERROR |

| JUMPER     | FUNCTION                        |
|------------|---------------------------------|
| E43 TO E44 | JUMPER FOR 16K CHIPS - ADDR MUX |
| E51 TO E52 | JUMPER TO DISABLE MEMSIZ        |
| E49 TO E71 | CUT FOR 64K CHIPS - CLRBY       |
| E69 TO E70 | JUMPER FOR 64K CHIPS - CLRBY    |
| E79 TO E80 | JUMPER FOR NORMAL LOG OPERATION |

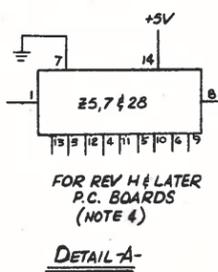
| JUMPER FOR 36 BIT OPERATION |               |
|-----------------------------|---------------|
| JUMPER                      | FUNCTION      |
| E5 TO E6                    | WORD DISABLE  |
| E7 TO E8                    | ADDR MUX      |
| E11 TO E12                  | DISABLE MATCH |
| E24 TO E25                  | ADDR MUX      |
| E49 TO E53                  | MODE CONTR    |
| E50 TO E54                  | MODE CONTR    |
| E59 TO E60                  | WORD DISABLE  |

| TEST PURPOSES ONLY |  |
|--------------------|--|
| JUMPER             | FUNCTION                                 |
| E9 TO E10          | REMOVE JUMPER TO DISABLE ECC INTO PTRREE |
| E67 TO E68         | JUMPER TO DISABLE REFRESH                |
| E75 TO E76         | JUMPER TO DISABLE ECC CORRECTION         |
| E77 TO E78         | JUMPER TO DISABLE CLEAR                  |
| E80 TO E81         | JUMPER TO SET UP LOG TIMING              |
| E84 TO E85         | OPEN FOR TEST (MBN BYPASS)               |
| E86 TO E87         | OPEN FOR TIMEOUT CHECK                   |
|                    | JUMPER FOR NORMAL OPERATION              |

| JUMPER FOR 18 BIT OPERATION |               |
|-----------------------------|---------------|
| JUMPER                      | FUNCTION      |
| E47 TO E53                  | MODE CONTR    |
| E48 TO E54                  | MODE CONTR    |
| E55 TO E56                  | WRALB DISABLE |

| MEMSIE CONFIGURATION WIRING              |  |                             |   |
|--|--|-----------------------------|---|
| CONFIGURATION                            | JUMPERS  | CONFIGURATION               | JUMPERS   |
| 18 BIT BSC<br>16K RAM CHIPS              | E3-E33, E4-E36, E29-E37,<br>E30-E38, E31-E39, E32-E40,<br>E41-E57, E42-E58                     | 36 BIT BSC<br>16K RAM CHIPS | E29-E36, E30-E37, E31-E38,<br>E32-E39, E4-E40,<br>E41-E57, E42-E58                  |
| CHASSIS 1                                | E26-E45, E27-E46   | CHASSIS 1                   | E26-E3, E27-E45, E28-E46  |
| CHASSIS 2                                | E34-E45, E27-E46   | CHASSIS 2                   | E33-E3, E27-E45, E28-E46  |
| CHASSIS 3                                | E26-E45, E35-E46   | CHASSIS 3                   | E26-E3, E34-E45, E28-E46  |
| CHASSIS 4                                | E34-E45, E35-E46   | CHASSIS 4                   | E33-E3, E34-E45, E28-E46  |
| 18 BIT BSC<br>64K RAM CHIPS<br>CHASSIS 1 | E4-E36, E57-E37, E58-E38,<br>E29-E39, E30-E40, E31-E41,<br>E32-E42, E3-33, E45-E34,<br>E46-E35 | CHASSIS 5                   | E26-E3, E27-E45, E35-E46  |
|  |  | CHASSIS 6                   | E33-E3, E27-E45, E35-E46  |
|  |  | CHASSIS 7                   | E26-E3, E34-E45, E35-E46  |
|  |  | CHASSIS 8                   | E33-E3, E34-E45, E35-E46  |
|  |  | BIT BSC<br>64K RAM CHIPS    | E4-E36, E57-E37, E29-E38,<br>E30-E39, E31-E40, E32-E41,<br>E58-E42, E3-E33, E45-E34 |
|  |  | CHASSIS 1                   | E46-E26   |
|  |  | CHASSIS 2                   | E46-E35   |

| EXTERNAL SELECT STRAPPING                    |                           |  |                           |
|--|---------------------------|--|---------------------------|
| CHASSIS                                      | JUMPERS                   | CHASSIS                                      | JUMPERS                   |
| CHASSIS 1                                    | E14-E21, E16-E22, E18-E23 | CHASSIS 1                                    | E16-E21, E18-E22, E20-E23 |
| CHASSIS 2                                    | E13-E21, E16-E22, E18-E23 | CHASSIS 2                                    | E15-E21, E18-E22, E20-E23 |
| CHASSIS 3                                    | E14-E21, E15-E22, E18-E23 | CHASSIS 3                                    | E16-E21, E17-E22, E20-E23 |
| CHASSIS 4                                    | E13-E21, E15-E22, E18-E23 | CHASSIS 4                                    | E15-E21, E17-E22, E20-E23 |
| CHASSIS 5                                    | E14-E21, E16-E22, E17-E23 | CHASSIS 5                                    | E16-E21, E18-E22, E19-E23 |
| CHASSIS 6                                    | E13-E21, E16-E22, E17-E23 | CHASSIS 6                                    | E15-E21, E18-E22, E19-E23 |
| CHASSIS 7                                    | E14-E21, E15-E22, E17-E23 | CHASSIS 7                                    | E16-E21, E17-E22, E19-E23 |
| CHASSIS 8                                    | E13-E21, E15-E22, E17-E23 | CHASSIS 8                                    | E15-E21, E17-E22, E19-E23 |
| 32MBYTES PER CHASSIS<br>36 BIT BSC 64K CHIPS |                           | 32MBYTES PER CHASSIS<br>18 BIT BSC 64K CHIPS |                           |
| CHASSIS 1                                    | E18-E22, E20-E23          | CHASSIS 1                                    | E20-E23                   |
| CHASSIS 2                                    | E17-E22, E20-E23          | CHASSIS 2                                    | E19-E23                   |
| CHASSIS 3                                    | E18-E22, E19-E23          |  |                           |
| CHASSIS 4                                    | E17-E22, E19-E23          |  |                           |



5. COMPONENTS USING +5B ARE BE INDICATED BY AN ASTERISK, \*.

4. THE PINOUTS SHOWN IN DETAIL-A- SHALL APPLY TO REV H AND LATER P.C. BOARDS USING 150ns DIGITAL DELAY LINE DATARAM P/N 14108.

3. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W

2. CAPACITANCE VALUES ARE IN MICROFARADS

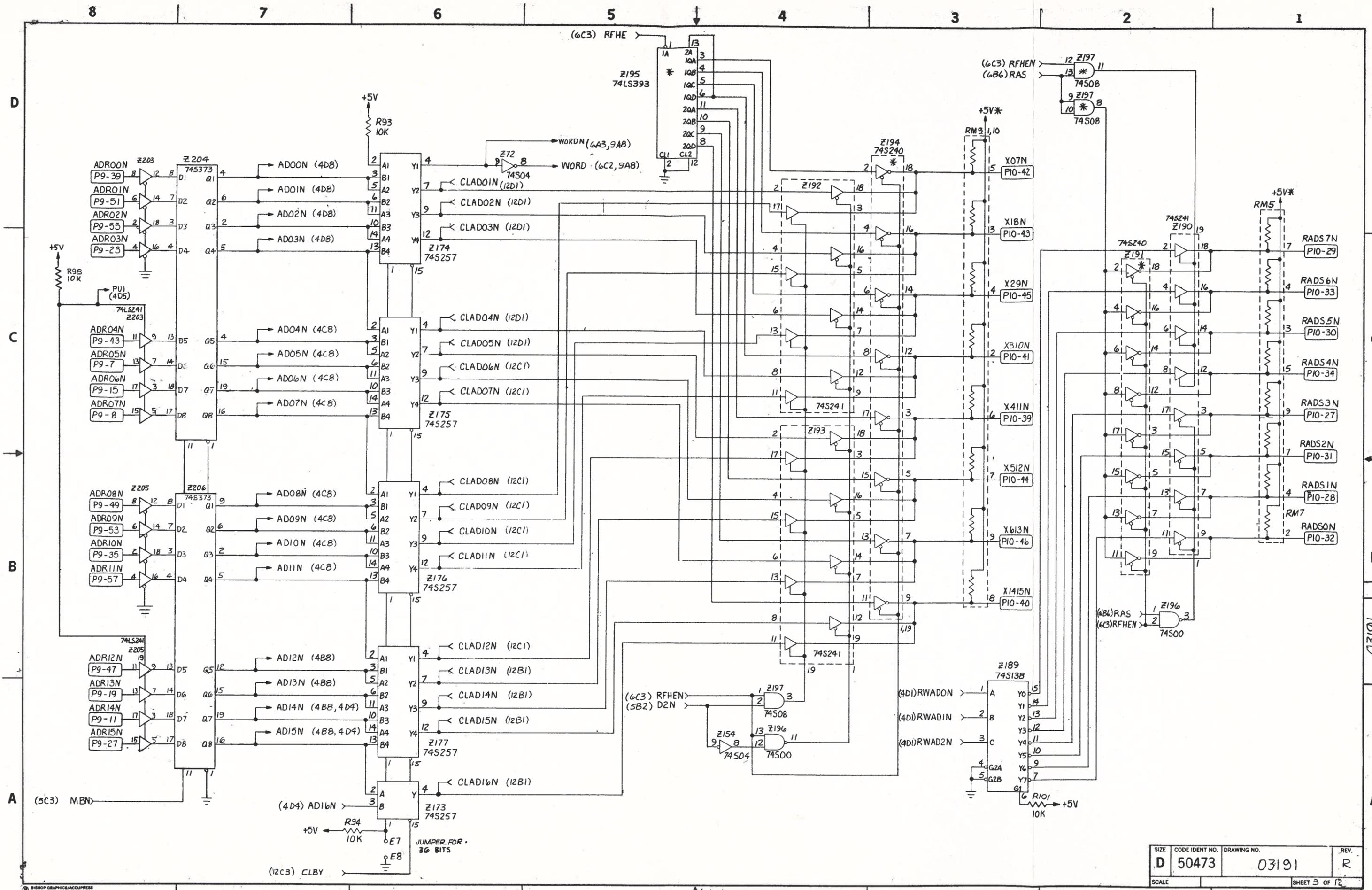
1. CAPACITANCE TOLERANCES AND VOLTAGES ARE AS FOLLOWS;  
PICOFARADS - ±5%, 100V; 4.7 MICROFARADS - ±20%, 10V;  
15 MICROFARADS - ±20% 20V

NOTES: UNLESS OTHERWISE SPECIFIED.

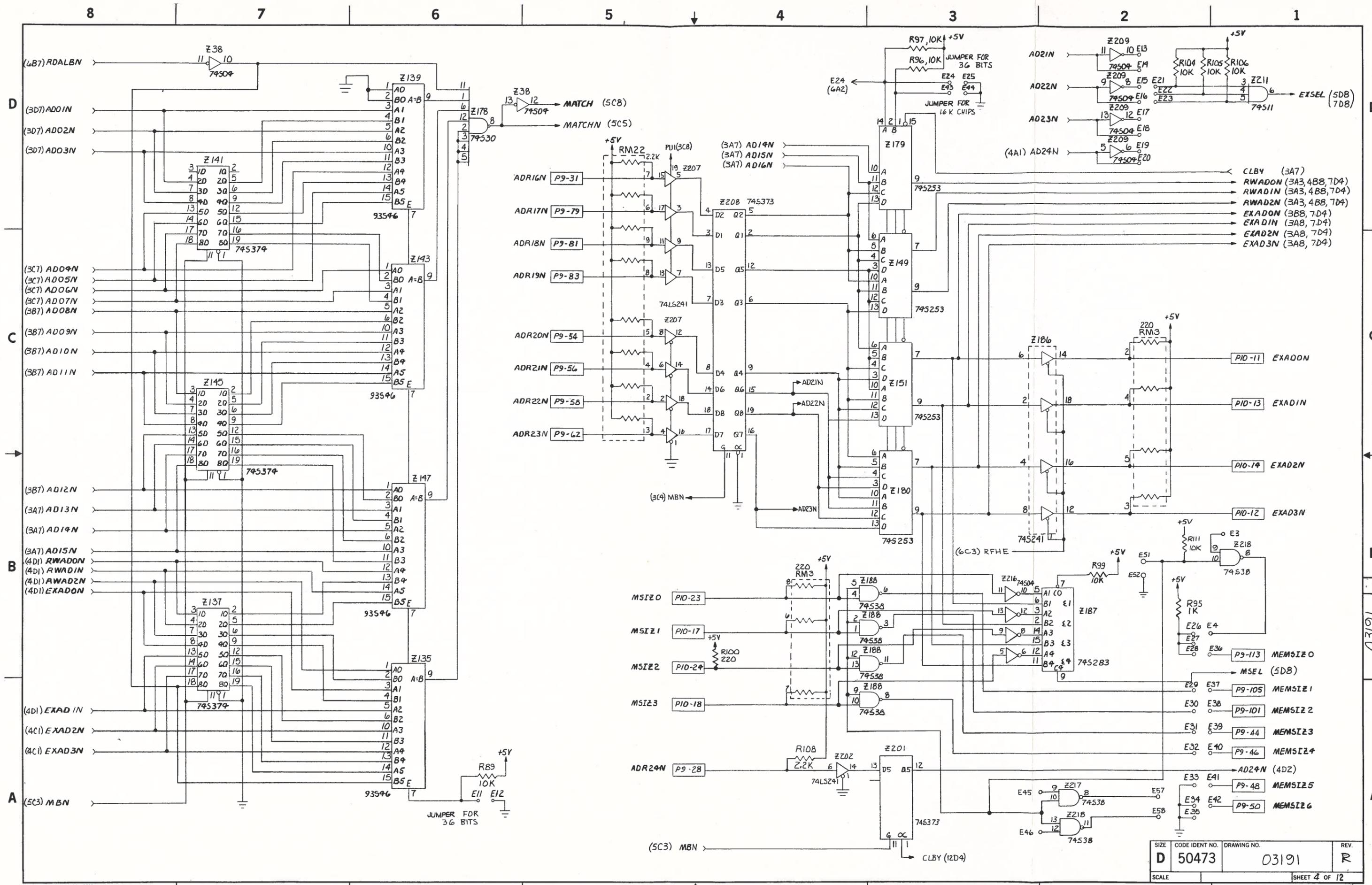
|  |                |              |         |
|--|----------------|--------------|---------|
| UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:<br>FRACTIONS DECIMALS ANGLES<br>± .010 ± .005 ± .005 ± |                | CONTRACT NO. |         |
| MATERIAL   |                | APPROVALS    | DATE    |
| FINISH   |                | DRAWN        | 8-21-79 |
| NEXT ASSY USED ON  |                | CHECKED      | 5-20-80 |
| APPLICATION  |                | ENG.         | 5-20-80 |
| BO NOT SCALE DRAWING   |                | APPROVED     |         |
| SIZE   | CODE IDENT NO. | DRAWING NO.  | REV.    |
| D  | 50473          | 03191        | R       |
| SCALE  | SHEET 2 OF 12  |              |         |

**DATARAM CORPORATION**  
CRANBURY NEW JERSEY

SCHMATIC DIAGRAM,  
BULK SEMI CONTROLLER

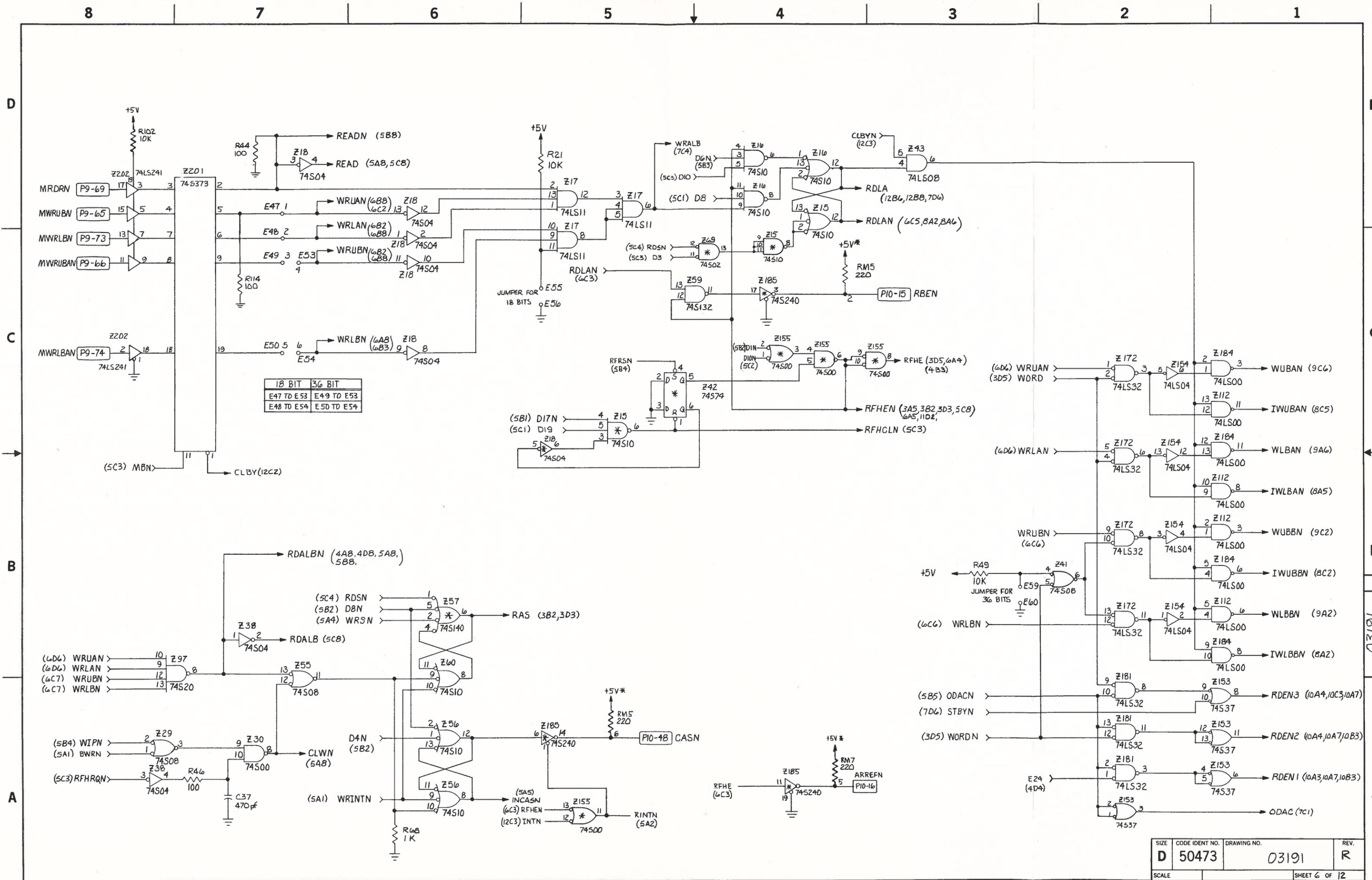


|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 3 OF 12  |             |      |



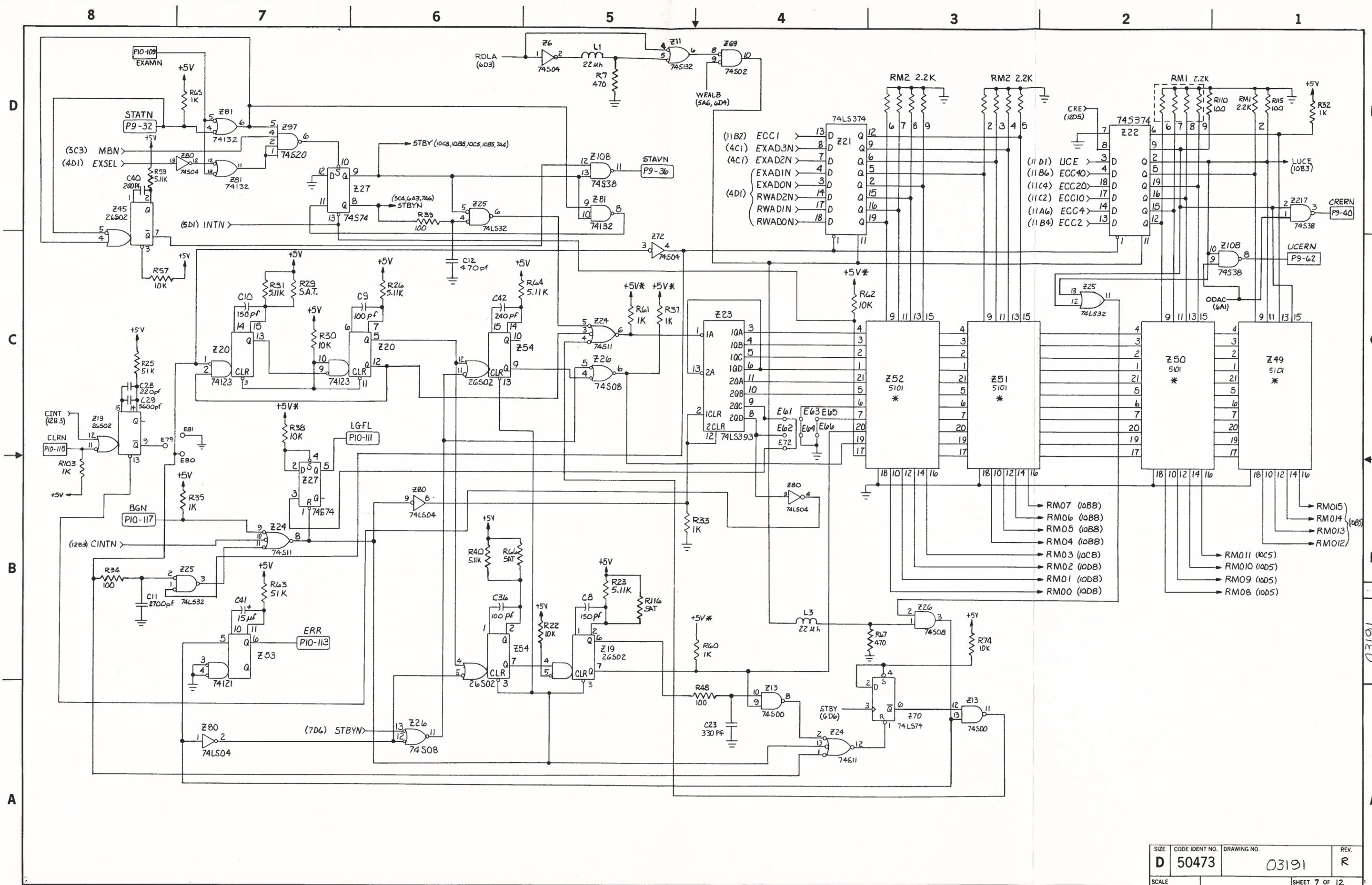
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|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 4 OF 12  |             |      |



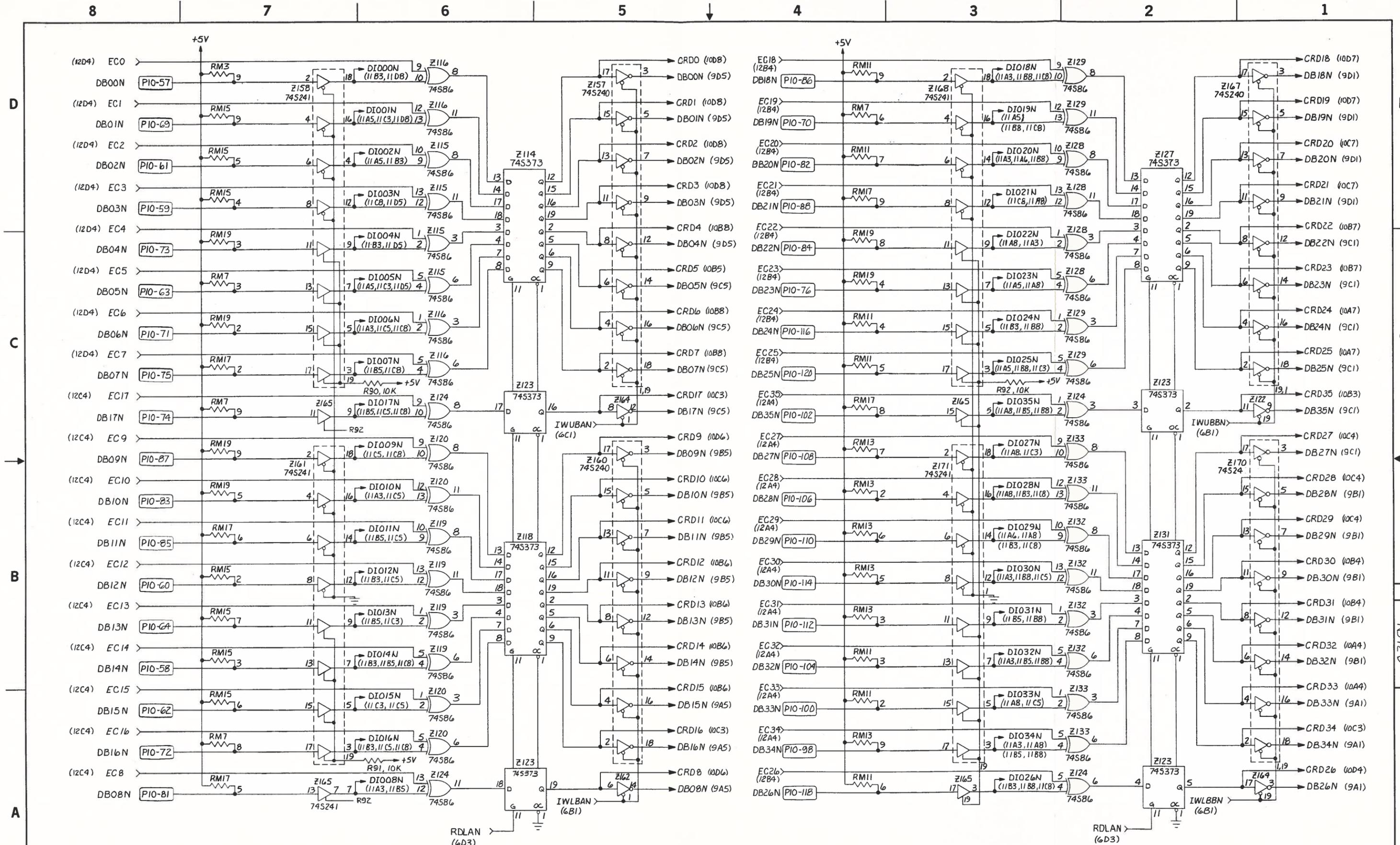


|            |            |
|------------|------------|
| 18 BIT     | 36 BIT     |
| E47 TO E53 | E49 TO E53 |
| E48 TO E54 | E50 TO E54 |

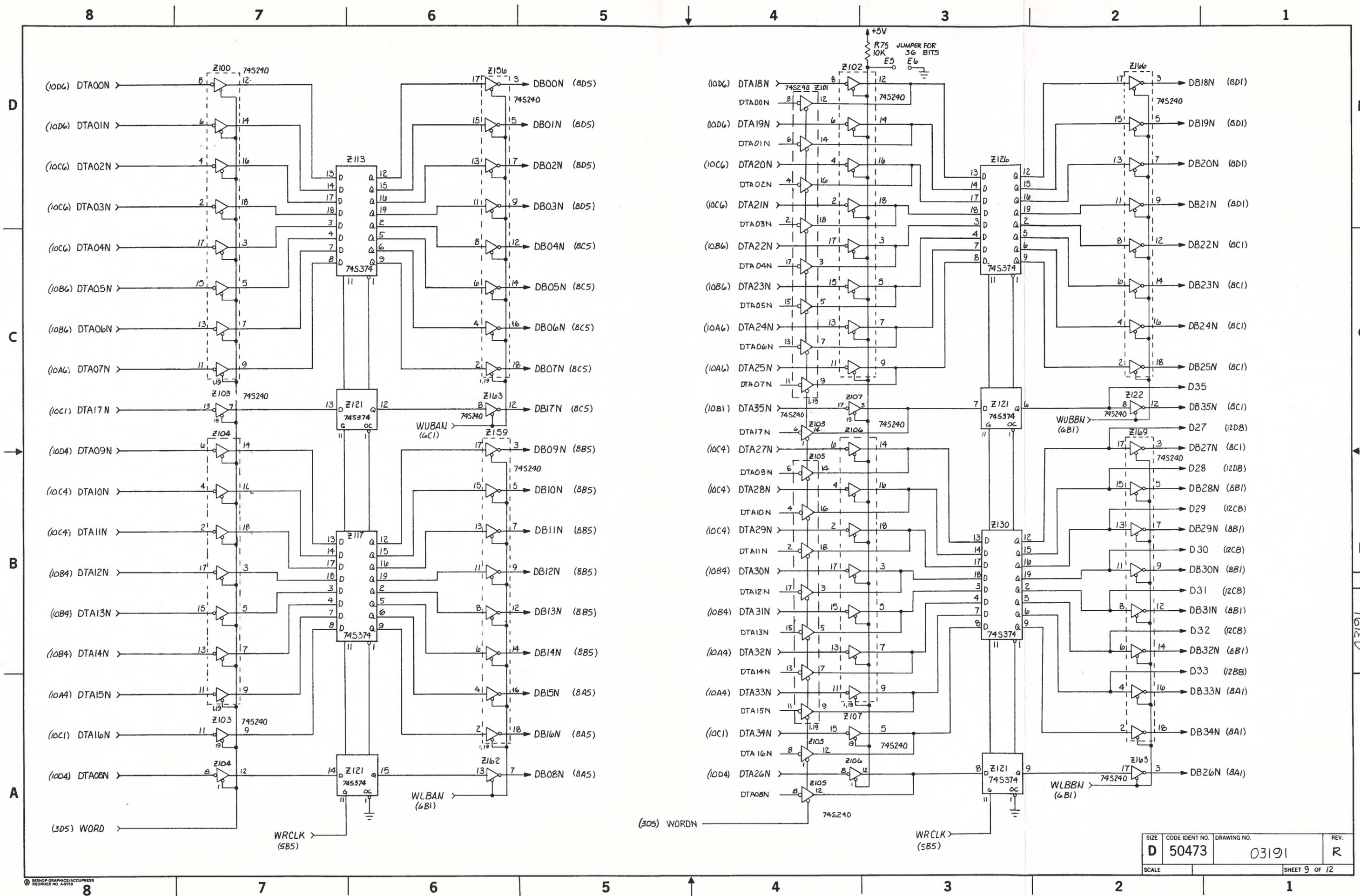
|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 6 OF 12  |             |      |



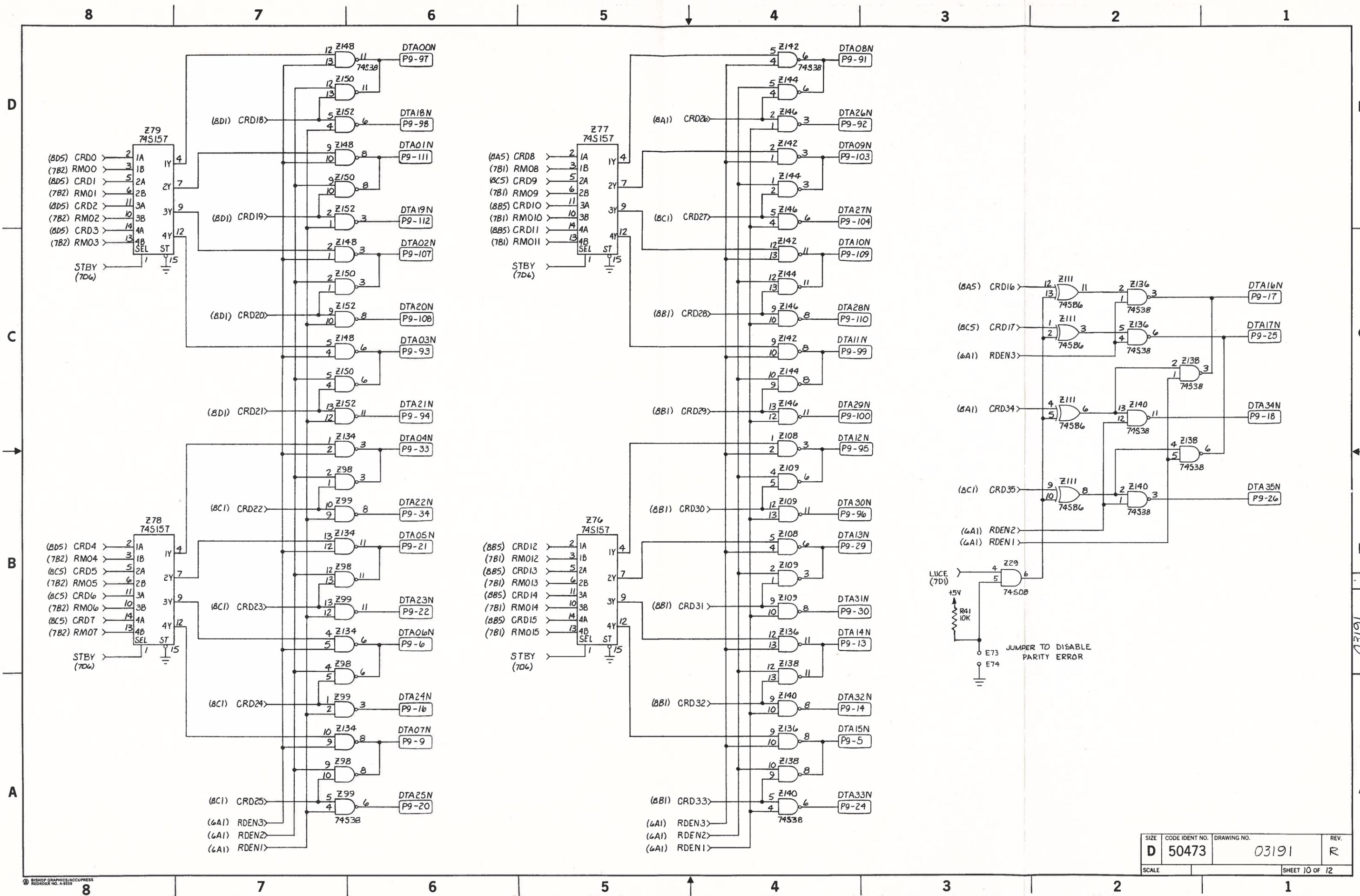
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|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 7 OF 12  |             |      |



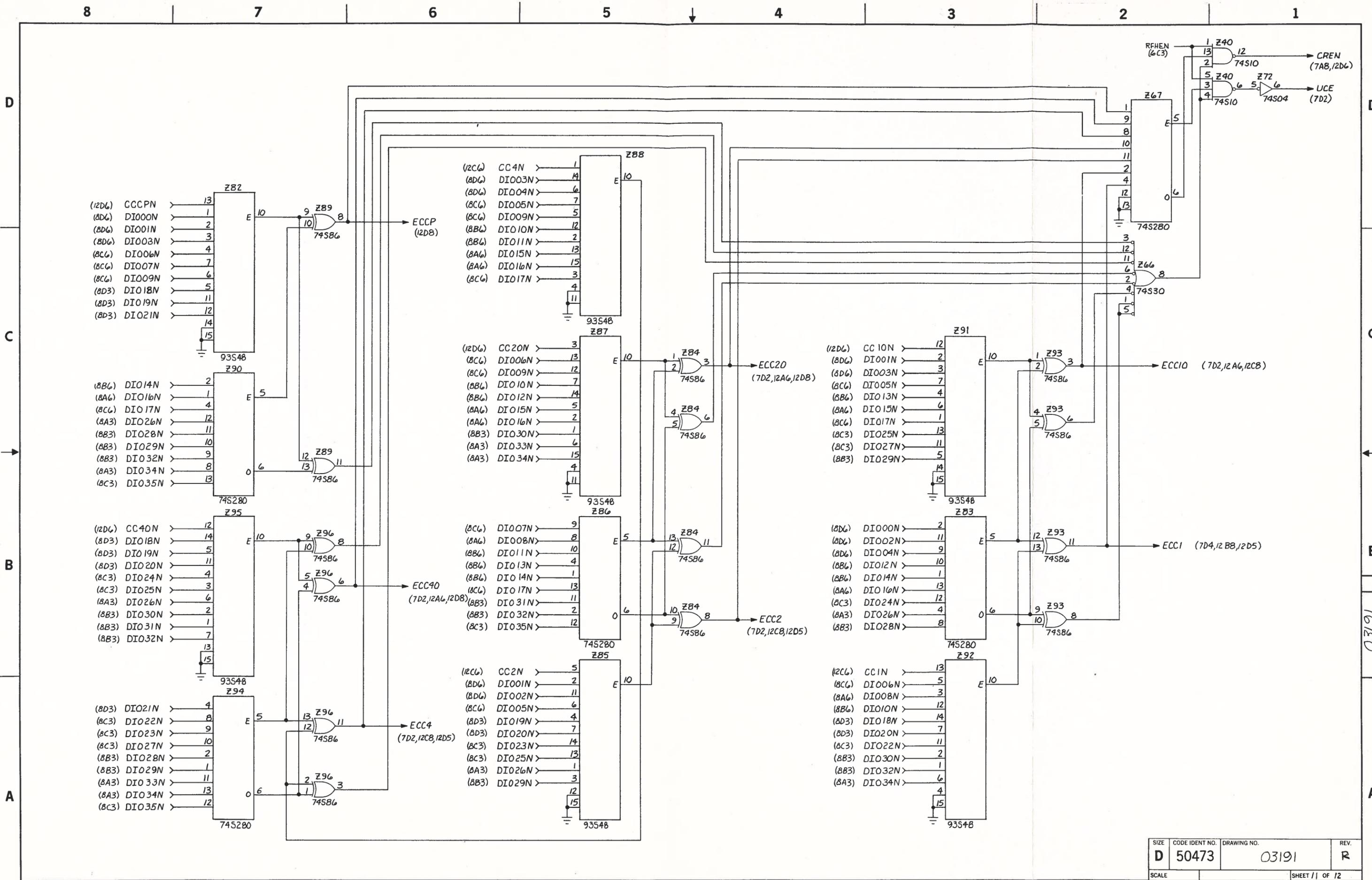
|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 8 OF 12  |             |      |



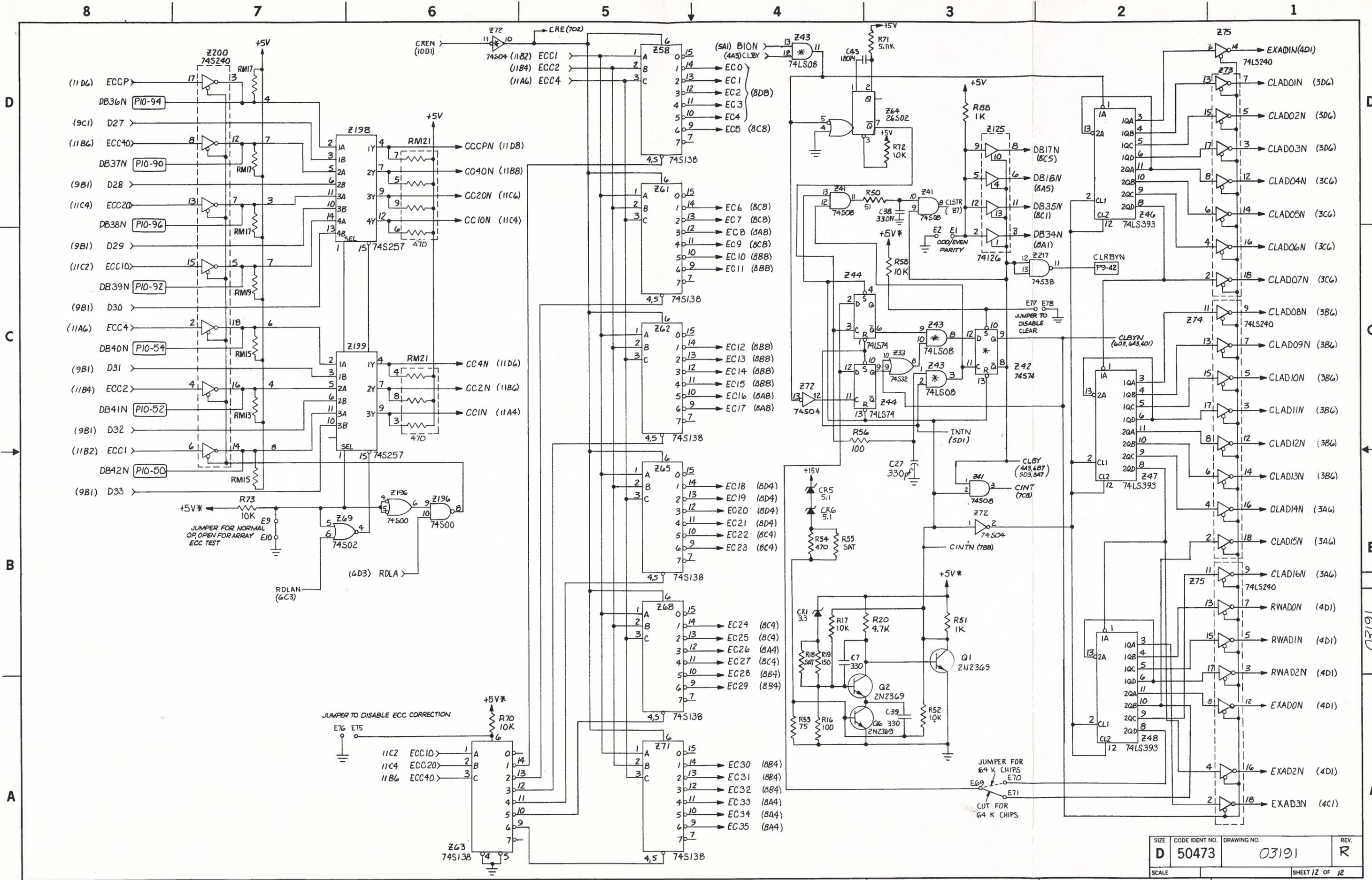
|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 9 OF 12  |             |      |



|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 10 OF 12 |             |      |

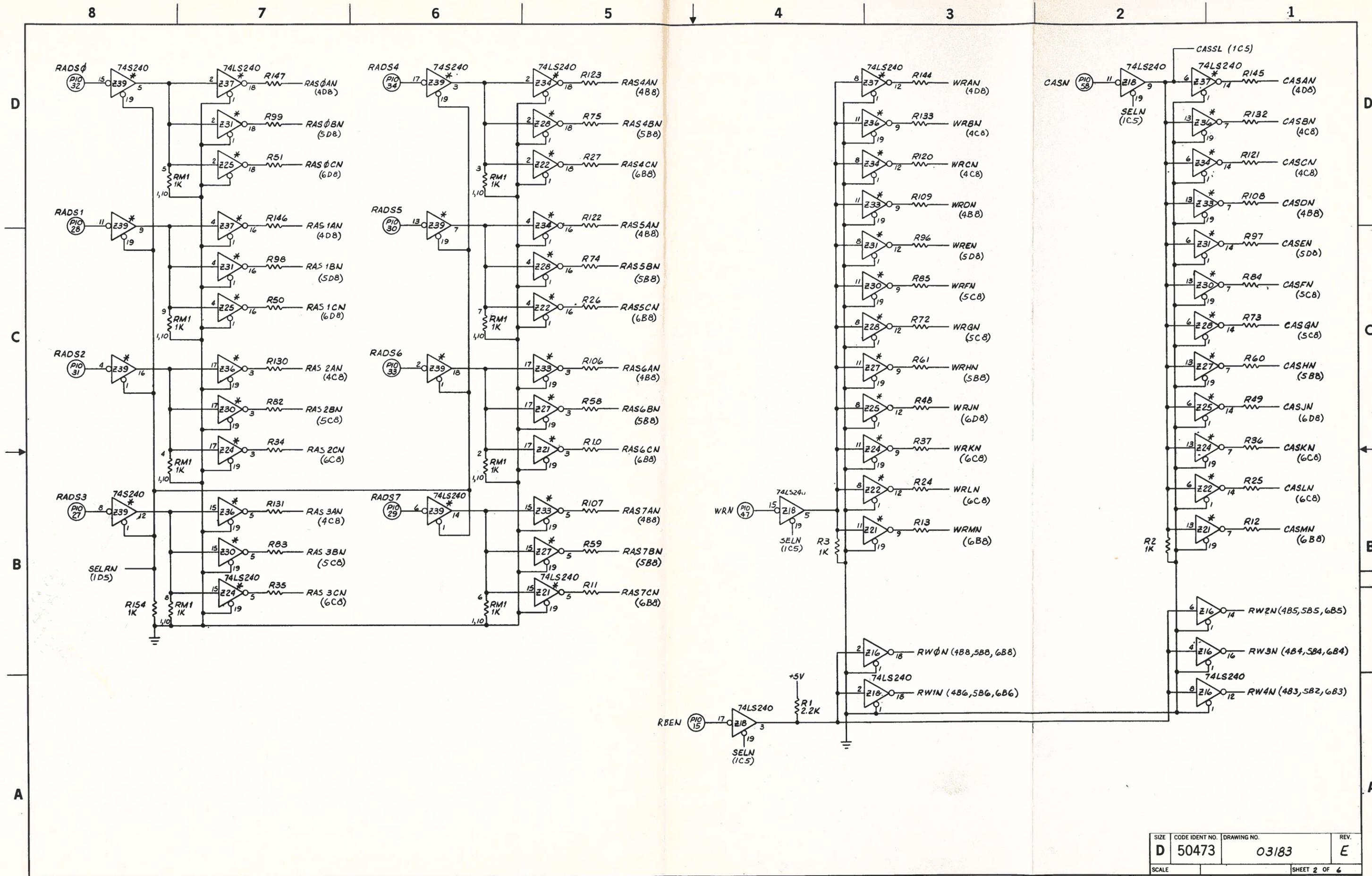


|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 11 OF 12 |             |      |

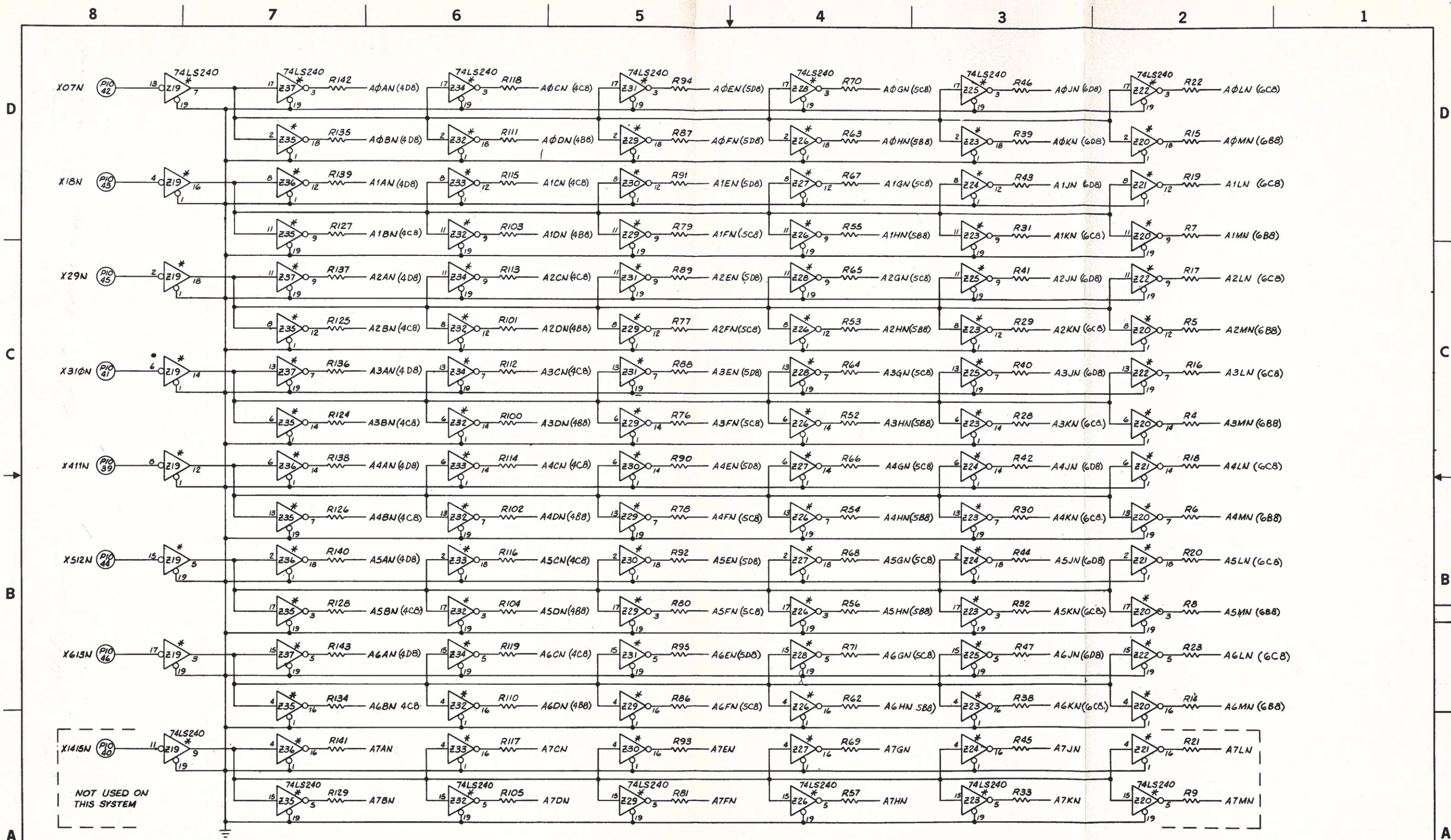


|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03191       | R    |
| SCALE | SHEET 12 OF 12 |             |      |

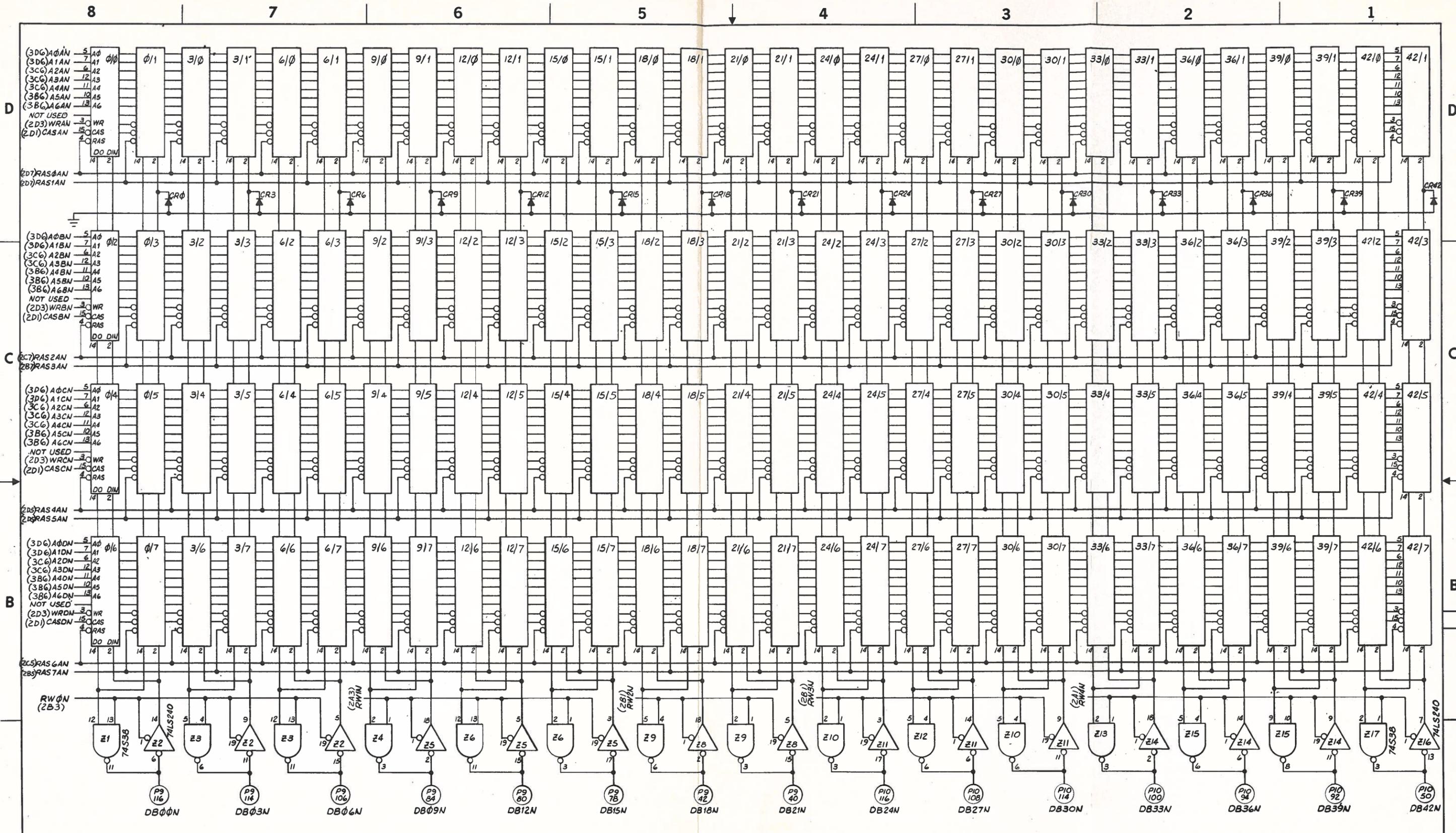




|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03/83       | E    |
| SCALE | SHEET 2 OF 6   |             |      |

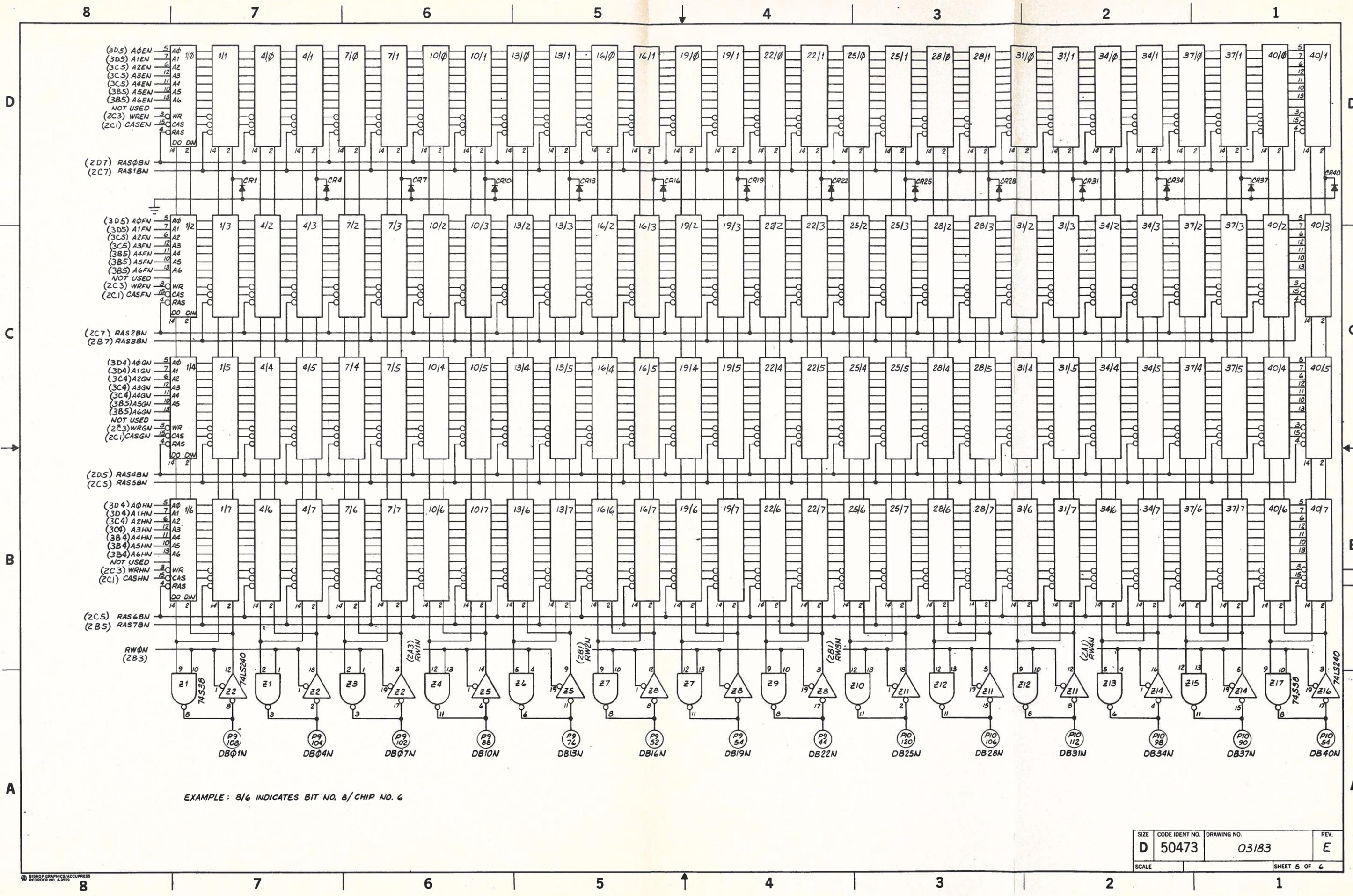


|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03183       | E    |
| SCALE | SHEET 3 OF 6   |             |      |



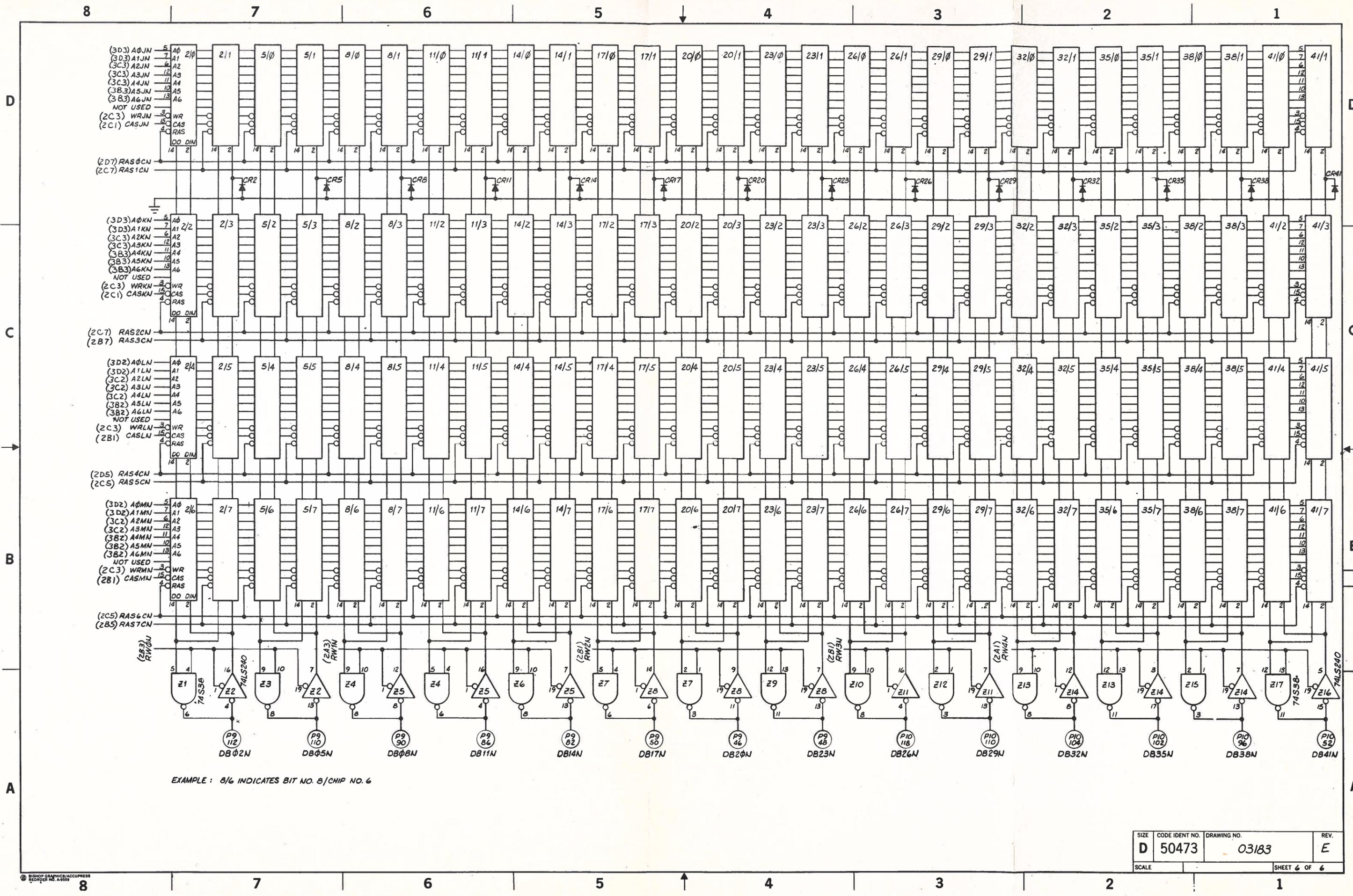
EXAMPLE: 8/6 INDICATES BIT NO. 8 / CHIP NO. 6

|       |                |              |      |
|-------|----------------|--------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO.  | REV. |
| D     | 50473          | 03183        | E    |
| SCALE |                | SHEET 4 OF 6 |      |



EXAMPLE: 8/6 INDICATES BIT NO. 8/CHIP NO. 6

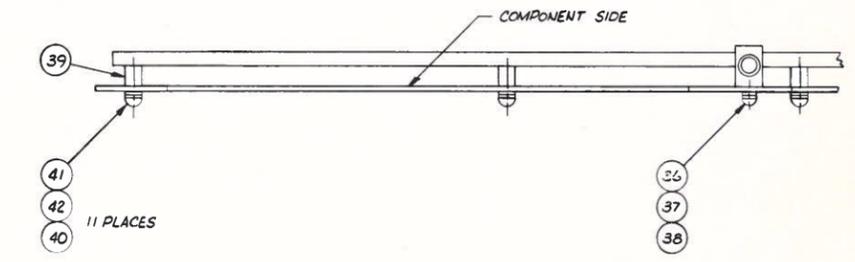
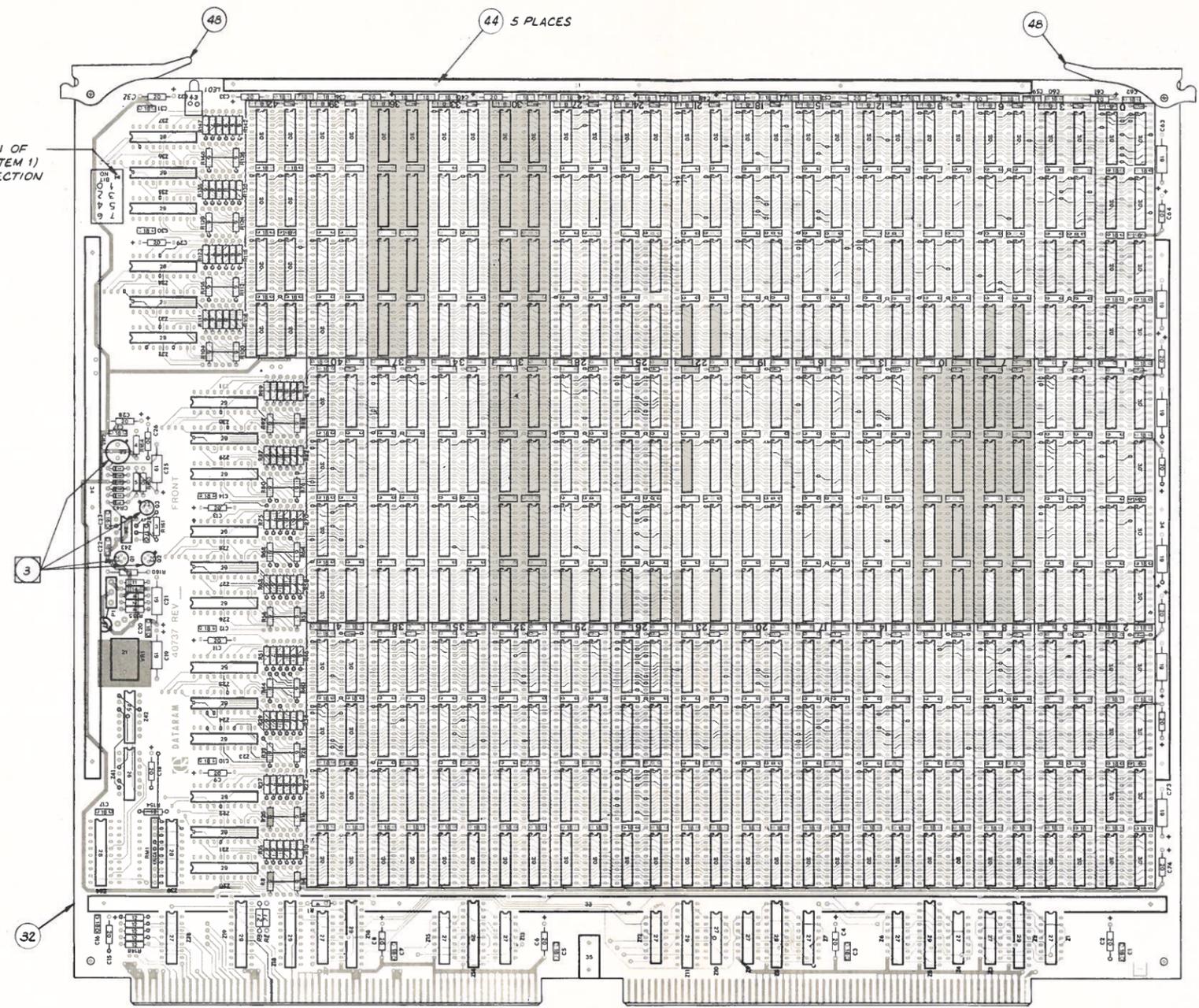
|       |                |              |      |
|-------|----------------|--------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO.  | REV. |
| D     | 50473          | 03183        | E    |
| SCALE |                | SHEET 5 OF 6 |      |



|       |                |             |      |
|-------|----------------|-------------|------|
| SIZE  | CODE IDENT NO. | DRAWING NO. | REV. |
| D     | 50473          | 03183       | E    |
| SCALE | SHEET 6 OF 6   |             |      |

| REVISIONS |     |                                |           |          |
|-----------|-----|--------------------------------|-----------|----------|
| ZONE      | LTR | DESCRIPTION                    | DATE      | APPROVED |
| X1        |     | ECN 1678                       | 18 Jun 79 | RK       |
| X2        |     | ECN 1679                       | 18 Jun 79 | RK       |
| A         |     | ECN 1680 RELEASE TO PRODUCTION | 18 Jun 79 | RK       |
| B         |     | ECN 1740                       | 16 Oct 79 | RK       |
| C         |     | ECN 1741                       | 16 Oct 79 | RK       |
| D         |     | ECN 1755                       | 6 Nov 79  | RK       |
| E         |     | ECN 1820                       | 10-9-80   | RK       |
| F         |     | ECN 1951A                      | 10-9-80   | RK       |

TYP. DIRECTION OF ALL DIODES (ITEM 1) IN MEMORY SECTION



- NOTES:
1. MAXIMUM COMPONENT HEIGHT IS .400 EXCLUDING GUIDE BLOCK (ITEM 35).
  2. MAXIMUM LEAD LENGTH IS .050.
  3. PRIOR TO INSERTION IN P.C. BOARD, INSTALL ITEM 46 ON ITEM 22 & ITEM 45 ON ITEM 23.

|           |             |   |              |   |         |
|-----------|-------------|---|--------------|---|---------|
|           |             | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS DECIMALS ANGLES ± .xx ± .xxx ± ± |              | <b>DATARAM CORPORATION</b><br>CRANBURY NEW JERSEY                     |         |
|           |             | MATERIAL:   |              | <b>ASSEMBLY</b><br><b>DR-129S</b><br><b>BULK SEMI ARRAY 128K x 43</b> |         |
| DRWN      | J. L. WEITZ | DATE  | 5-22-79      | SIZE  | D 50473 |
| CHECKED   |             | ENGR  | RK 18 Jun 79 | CODE IDENT. NO.   | 62902   |
| APPROVED  | [Signature] | DATE  | 7/8/79       | DRAWING NO.   | 62902   |
| NEXT ASSY | USED ON     | APPLICATION   |              | REV.  | F       |
|           |             |   |              | SCALE   | FULL    |
|           |             |   |              | SHEET 1 OF 1  |         |

| REVISIONS |     |                        |            |          |
|-----------|-----|------------------------|------------|----------|
| ZONE      | LTR | DESCRIPTION            | DATE       | APPROVED |
|           | A   | RELEASED TO PRODUCTION | 3-17-80    | J DUNGAN |
|           | B   | ECN 1878               |            |          |
|           | C   | ECN 1879               | 21 May 80  | RK       |
|           | D   | ECN 1884               |            |          |
|           | E   | ECN 1906               |            |          |
|           | F   | ECN 1919               |            |          |
|           | G   | ECN 1920               |            |          |
|           | H   | ECN 1922               |            |          |
|           | J   | ECN 1940               |            |          |
|           | K   | ECN 1951A              |            |          |
|           | L   | ECN 1970               |            |          |
|           | M   | ECN 1975               |            |          |
|           | N   | ECN 1998               |            |          |
|           | P   | ECN 2000               | 29 July 80 | RK       |
|           | R   | ECN 2044               | 15 Sept 80 | RK       |

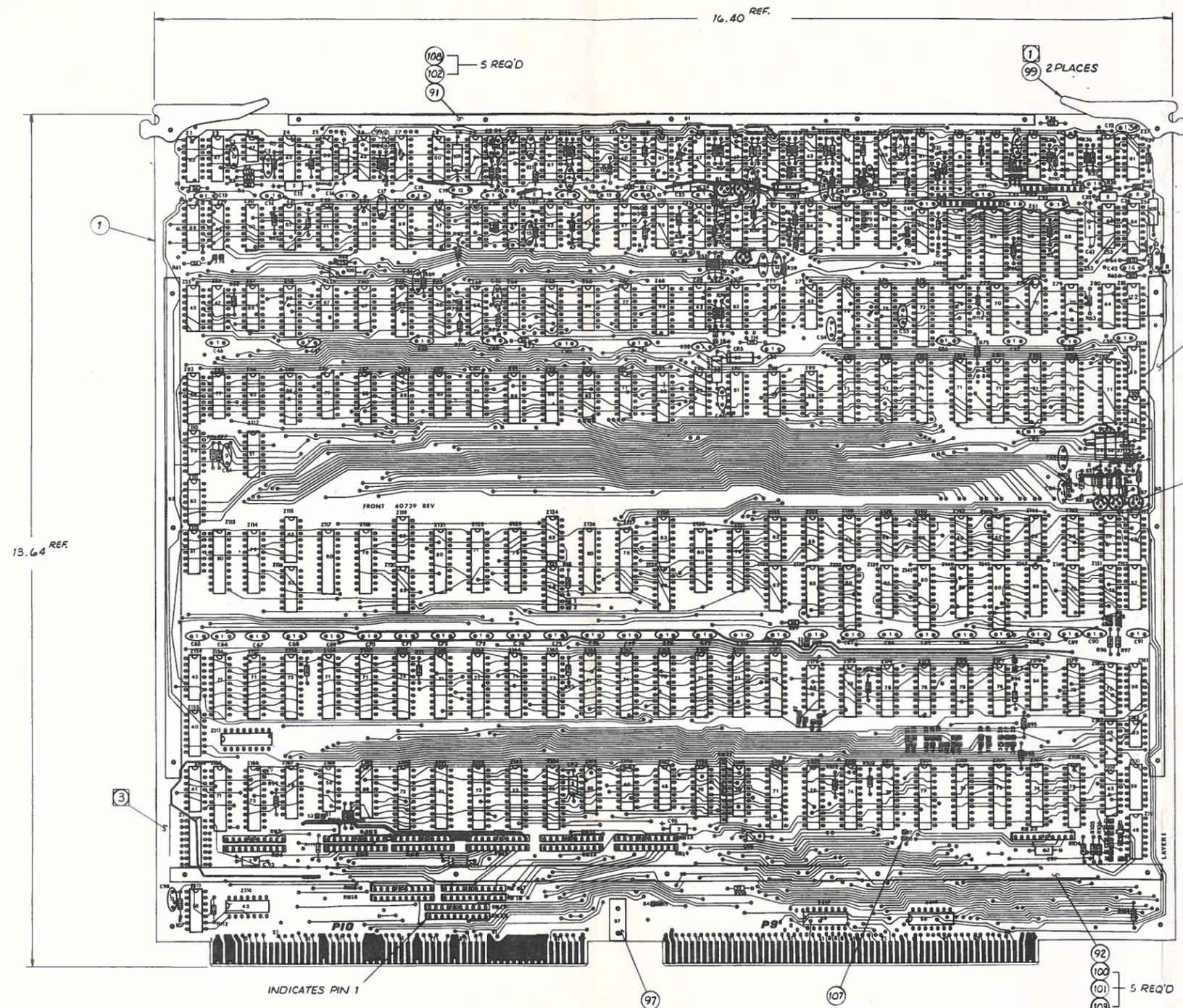


TABLE I

| 62901<br>18 BIT, 16K RAM |     | 62904<br>18 BIT, 16K RAM |     |
|--------------------------|-----|--------------------------|-----|
| FROM                     | TO  | FROM                     | TO  |
| E9                       | E10 | E5                       | E6  |
| E43                      | E44 | E7                       | E8  |
| E47                      | E53 | E9                       | E10 |
| E48                      | E54 | E11                      | E12 |
| E55                      | E56 | E24                      | E25 |
|                          |     | E43                      | E44 |
|                          |     | E49                      | E53 |
|                          |     | E50                      | E54 |
|                          |     | E59                      | E60 |

93  
100  
101  
103  
3 REQ'D 2 PLACES

2 6 PLACES

92  
100  
101  
103  
5 REQ'D

97  
98  
104  
105  
2 REQ'D

107  
85 PLACES

- NOTES: UNLESS OTHERWISE SPECIFIED
- INSTALL AFTER FLOW SOLDER.
  - INSTALL TRANSISTOR PADS ITEM 96 TO TRANSISTORS ITEM 39 6 PLACES PRIOR TO P.C. BOARD MOUNTING.
  - MARK PART NO., LATEST REV., SERIAL NO. & DATE CODE APPROX. WHERE SHOWN.
  - FOR SCHEMATIC DIAGRAM SEE DWG NO. 03191.
  - ADD JUMPER WIRES FOR 62901 OR 62904 PER TABLE I. SEE SCHEMATIC 03191 FOR OPTIONAL JUMPING INFORMATION.

.07 MAX. SOLDER BUILD-UP

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ±

|               |            |   |                      |
|---------------|------------|---|----------------------|
| CONTRACT NO.  |            | <b>DATARAM CORPORATION</b><br>CRANBURY NEW JERSEY |                      |
| APPROVALS     | DATE       | ASSEMBLY DR-129S BSC<br>18 BIT / 36 BIT           |                      |
| DRAWN JOHNSON | 5-23-80    | SIZE D  | CODE IDENT NO. 50473 |
| CHECKED       |            | DRAWING NO.                                       | 62901/62904          |
| ENGR.         |            | REV   | R                    |
| APPROVED RK   | 25 July 80 | SCALE FULL  | SHEET 1 OF 1         |
| NEXT ASSY     | USED ON    | APPLICATION                                       | DO NOT SCALE DRAWING |

| REV.                              | REVISIONS |       |                        |         |            |
|-----------------------------------|-----------|-------|------------------------|---------|------------|
|                                   | SYM.      | SHEET | DESCRIPTION            | APPROV. | DATE       |
| 62901<br>62904<br>OF 7<br>SHEET 1 | A         |       | Released to Production | JAS     | 3-17-80    |
|                                   | B         |       | ECN 1878 JAY           | RK      | 24 JUL 80  |
|                                   | C         |       | ECN 1879 JAY           |         |            |
|                                   | D         |       | ECN 1884 JAY           |         |            |
|                                   | E         |       | ECN 1906 JAY           |         |            |
|                                   | F         |       | ECN 1919 JAY           |         |            |
|                                   | G         |       | ECN 1920 JAY           |         |            |
|                                   | H         |       | ECN 1922 JAY           |         |            |
|                                   | J         |       | ECN 1940 JAY           |         |            |
|                                   | K         |       | ECN 1951A JAY          |         |            |
|                                   | L         |       | ECN 1970 JAY           |         |            |
|                                   | M         |       | ECN 1975 JAY           |         |            |
|                                   | N         |       | ECN 1998 JAY           |         |            |
|                                   | P         |       | ECN 2000 JAY           | RK      | 24 JUL 80  |
|                                   | R         |       | ECN 2044 cons          | RK      | 15 SEPT 80 |

|                |                   |   |   |                            |           |
|----------------|-------------------|---|---|----------------------------|-----------|
| DRAWN<br>MAS   | DATE<br>1-24-80   | TITLE<br><br>BILL OF MATERIALS<br>ASSY DR-129S BSC 18 BIT, 36 BIT |  <b>DATARAM CORPORATION</b><br>CRANBURY NEW JERSEY | DWG. NO.<br>62901<br>62904 | REV.<br>R |
| CHECKED<br>RK  | DATE<br>17 MAR 80 |   |   | SHEET 1                    | OF 7      |
| ENGR<br>JAS    | DATE<br>3-17-80   |   |   |                            |           |
| APPROVED<br>RK | DATE<br>17 MAR 80 |   |   |                            |           |

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

| ITEM NO | QTY | PART NUMBER | DESCRIPTION            | REFERENCE NOTES                                   |
|---------|-----|-------------|------------------------|---|
| 1       | 56  | 12316       | CAP CER .1uf 20%       | C13,14,16,18,20,22,24,26,<br>30-34,46-60,62,65-91 |
| 2       | 10  | 12105       | CAP TANT 4.7uf 10V     | C15,21,25,35,92-97                                |
| 3       | 1   | 12102       | CAP TANT 15uf 20V      | C41   |
| 4       | 1   | 12315       | CAP CER .01uf 20%      | C2  |
| 5       | 1   | 12608       | CAP SIL MICA 180pf 5%  | C45   |
| 6       | 1   | 12513       | CAP SIL MICA 100pf 5%  | C36   |
| 7       | 1   | 12516       | CAP SIL MICA 47pf 5%   | C5  |
| 8       | 2   | 12509       | CAP SIL MICA 150pf 5%  | C8,10   |
| 9       | 2   | 12519       | CAP SIL MICA 68pf 5%   | C6,61   |
| 10      | 1   | 12513       | CAP SIL MICA 100pf 5%  | C9  |
| 11      | 1   | 12504       | CAP SIL MICA 200pf 5%  | C40   |
| 12      | 8   | 12505       | CAP SIL MICA 330pf 5%  | C7, 19,23,27,38-39<br>63,64                       |
| 13      | 3   | 12506       | CAP SIL MICA 470pf 5%  | C1,C37,C12  |
| 14      | 1   | 12609       | CAP SIL MICA 240pf 5%  | C42   |
| 15      | 1   | 12311       | CAP CER 1500 pf 20%    | C3  |
| 16      | 1   | 12311       | CAP CER 1500 pf 20%    | C4  |
| 17      | 1   | 12306       | CAP CER 220pf 20%      | C28   |
| 18      | 1   | 12319       | CAP CER 5600pf 20%     | C29   |
| 19      | 2   | 10103       | RES CC 1/4W 51 OHMS 5% | R50,112   |
| 20      | 9   | 11907       | RES MDL 220 OHMS 5%    | RM3,5,7,9,11,13,15,17,19,<br>21                   |
| 22      | 1   | 11903       | RES MDL 470 OHMS       | RM21  |
| 23      | 3   | 11904       | RES MDL 2.2K OHMS 5%   | RM1,2,22  |

\*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.



**DATARAM CORPORATION**  
CRANBURY  
NEW JERSEY

DWG. NO. 62901  
B/M 62904  
SHEET 2 OF 7

REV R

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

| ITEM NO | QTY | PART NUMBER | DESCRIPTION              | REFERENCE NOTES   |
|---------|-----|-------------|--------------------------|---|
| 24      | 1   | 10159       | RES CC 1/4W 75 OHMS 5%   | R53   |
| 25      | 13  | 10105       | RES CC 1/4W 100 OHMS 5%  | R16,18,34,39,44,46,48,56,84,86,110,114,115  |
| 26      | 3   | 10602       | RES CC 1/4W 120 OHMS 5%  | R5,6,8  |
| 27      | 1   | 10108       | RES CC 1/4W 220 OHMS 5%  | R100  |
| 28      | 2   | 10111       | RES CC 1/4W 470 OHMS 5%  | R54,83  |
| 29      | 5   | 10111       | RES CC 1/4W 470 OHMS 5%  | R7,45,47,67,69  |
| 30      | 15  | 10113       | RES CC 1/4W 1K OHMS 5%   | R4,32,33,35,37, 51,60, 61,65,68,87,88,95,103, 109   |
| 31      | 2   | 10118       | RES CC 1/4W 2.2K OHMS 5% | R76,108   |
| 32      | 2   | 10121       | RES CC 1/4W 4.7K OHMS 5% | R20,85  |
| 33      | 2   | 10601       | RES CC 1/4W 5.1K OHMS 5% | R11,12  |
| 34      | 43  | 10122       | RES CC 1/4W 10K OHMS 5%  | R1,9,13-15,17,21,22, 30,38,41,42,43,49,52, 57,58,62,70,72-75,77,80, 81,89-94,96-99,101,102, 105,106,111,113,104 |
| 35      | 1   | 10145       | RES CC 1/4W 22K OHMS     | R3  |
| 36      | 3   | 10181       | RES CC 1/4W 51K OHMS 5%  | R10,25,63   |
| 37      | 2   | 18202       | DIODE ZENER 3.3V 1N746   | CR1,4   |
| 38      | 4   | 18205       | DIODE ZENER 5.1V 1N751A  | CR2,3,5,6   |
| 39      | 6   | 20104       | XSTR NPN SWG 2N2369A     | Q1-6  |
| 40      | 4   | 16513       | IC QUAD 2I/P NAND 74S00  | Z13,30, 155,196   |
| 41      | 3   | 16205       | IC QUAD 2I/P NAND 74LS00 | Z112,184,32   |
| 42      | 1   | 16507       | IC QUAD 2I/P NOR 74S02   | Z69   |
| 43      | 8   | 16501       | IC HEX INV 74S04         | Z4,6,18,38,72,154,209,216   |

\*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.



**DATARAM CORPORATION**  
NEW JERSEY  
CRANBURY

DWG. NO. 62901  
B/M 62904  
SHEET 3 OF 7  
REV R

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

| ITEM NO | QTY | PART NUMBER | DESCRIPTION                  | REFERENCE NOTES  |
|---------|-----|-------------|------------------------------|--|
| 44      | 1   | 16210       | IC HEX INV 74LS04            | Z80  |
| 45      | 6   | 16525       | IC QUAD 2I/P AND 74S08       | Z29,36,41,55,197,26  |
| 46      | 1   | 16206       | IC QUAD 2I/P AND 74LS08      | Z43  |
| 47      | 7   | 16515       | IC TPL 3I/P NAND 74S10       | Z2,15,16,35,40,56,60   |
| 48      |     |             |                              |  |
| 49      | 5   | 16503       | IC TPL 3I/P AND 74S11        | Z12,24,37,182,211  |
| 50      | 1   | 16212       | IC TPL 3I/P AND 74LS11       | Z17  |
| 51      | 2   | 16516       | IC DUAL 4I/P NAND 74S20      | Z97,212  |
| 53      | 1   | 16541       | IC DUAL 4I/P NAND 74S22      | Z39  |
| 54      | 2   | 16542       | IC 8I/P NAND 74S30           | Z66,178  |
| 55      | 2   | 16521       | IC QUAD 2I/P POS OR 74S32    | Z33,215  |
| 56      | 3   | 16220       | IC QUAD 2I/P POS OR 74LS32   | Z25,172,181  |
| 57      | 1   | 16518       | IC QUAD 2I/P NAND 74S37      | Z153   |
| 58      | 1   | 16309       | IC QUAD 2I/P NAND 7438       | Z188   |
| 59      | 18  | 16514       | IC QUAD 2I/P NAND 74S38      | Z98,99,108-110,134,136,138,<br>140,142,144,146,148,150,<br>152,210,217,218 |
| 60      | 1   | 16209       | IC DUAL AND/OR/INV 74LS51    | Z8   |
| 61      | 4   | 16522       | IC DUAL D BINARY 74S74       | Z9,14,27,42  |
| 62      | 4   | 16202       | IC DUAL D BINARY 74LS74      | Z44,70,1,31  |
| 63      | 14  | 16505       | IC QUAD EXCL OR 74S86        | Z84,89,93,96,111,115,116,<br>119,120,124,128,129,132,<br>133               |
| 64      | 1   | 16316       | IC MONSTABLE MV 74121        | Z53  |
| 65      | 2   | 16326       | IC DUAL MONOSTABLE MV 74123  | Z10,20   |
| 66      | 1   | 16317       | IC TRI-STATE AND BUFFER 8094 | Z125   |

\*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.



**DATARAM CORPORATION**  
CRANBURY  
NEW JERSEY

DWG. NO. 62901  
B/M 62904  
SHEET 4 OF 7  
REV. R

TITLE: B/M ASSY DR-129 BSC 18 BIT, 36 BIT

| ITEM NO | QTY | PART NUMBER | DESCRIPTION                     | REFERENCE NOTES  |
|---------|-----|-------------|---------------------------------|--|
| 67      | 2   | 16529       | IC QUAD 2I/P NAND ST 74S132     | Z11,59   |
| 68      | 8   | 16520       | IC 3 TO 8 DCDR/MUX 74S138       | Z58,61-63,65,68,71,189   |
| 69      | 2   | 16543       | IC 4I/P NAND 50 OHM DRVR 74S140 | Z34,57   |
| 70      | 4   | 16506       | IC QUAD 2 TO 1 MUX 74S157       | Z76-79   |
| 71      | 24  | 16531       | IC BUS DRVR/BFR 74S240          | Z100-107,122,156,157,159,<br>160,162-164,166,167,169,<br>170,185,191,194,200 |
| 72      | 3   | 16234       | IC 3STAT BFR/DRVR/RCVR 74LS240  | Z73-75   |
| 73      | 9   | 16528       | IC BUS DRVR/BFR/INV 74S241      | Z158,161,165,168,171,186,<br>190,192,193                                     |
| 74      | 4   | 16254       | IC 3STAT BFR/DRVR/RCVR 74LS241  | Z202,203,205,207   |
| 75      | 4   | 16538       | IC DUAL 4 TO 1 MUX 74S253       | Z149,151,179,180   |
| 76      | 7   | 16539       | IC QUAD 2 TO 1 MUX 74S257       | Z173-177,198,199   |
| 77      | 5   | 16544       | IC 9B PARITY GEN/CHKR 74S280    | Z67,83,86,90,94  |
| 78      | 1   | 16535       | IC 4B BINARY FULL ADDER 74S283  | Z187   |
| 79      | 9   | 16536       | IC OCTAL D LATCH 74S373         | Z114,118,123,127,131,201,<br>204,206,208                                     |
| 80      | 8   | 16551       | IC OCTAL D FLIP FLOP 74S374     | Z113,117,121,126,130,137,<br>141,145   |
| 81      | 2   | 16551       | IC OCTAL D FLIP FLOP 74S374     | Z21,22   |
| 82      | 5   | 16236       | IC DUAL 4B BIN CNTR 74LS393     | Z23,46,47,48,195   |
| 83      | 1   | 16607       | IC PRPHL POS-OR DRIVER 75453    | Z183   |
| 84      | 4   | 16532       | IC RESET MONOSTABLE MV 26S02    | Z45,54,64,19   |
| 85      | 4   | 16555       | IC 6B IDENT COMPTR 93S46        | Z135,139,143,147   |
| 86      | 7   | 16556       | IC 12B PARITY GEN/CHKR 93S48    | Z82,85,87,88,91,92,95  |
| 87      | 1   | 16356       | IC TIMER 555                    | Z3   |

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**DATARAM CORPORATION**  
CRANBURY  
NEW JERSEY

DWG. NO. 62901  
B/M 5 62904  
SHEET 5 OF 7

REV. R

TITLE: B/M ASSY DR-129S BSC 18 BIT, 36 BIT

| ITEM NO | QTY | PART NUMBER | DESCRIPTION                          | REFERENCE NOTES       |
|---------|-----|-------------|--------------------------------------|-----------------------|
| 88      | 4   | 16746       | IC STATIC RAM 256 x 4                | Z49,50,51,52          |
| 89      | 3   | 14108       | DELAY LINE, DIGITAL ISOs             | Z5,7,28               |
| 90      | 7   | 10216       | RES FLM 1/10W 5.11K OHMS 1%          | R23,26,31,40,59,64,71 |
| 91      | 1   | 42649       | STIFFENER CIRCUIT CARD               |                       |
| 92      | 1   | 42648       | STIFFENER LONG                       |                       |
| 93      | 2   | 42647       | STIFFENER SHORT                      |                       |
| 94      | 1   | 40739       | PC BOARD DR-129S CONTROLLER          |                       |
| 95      | --- | 03191       | SCHEMATIC BS CONTROLLER              |                       |
| 96      | 6   | 27316       | PAD, TRANSISTOR TO-18                |                       |
| 97      | 1   | 42944       | GUIDE BLOCK                          |                       |
| 98      | 2   | 26321       | SCR PNH PHL STL 4-40 x 3/16          |                       |
| 99      | 2   | 27334       | CARD EJECTOR (WITH PIN)              |                       |
| 100     | 11  | 27204       | SPACER RND THD NYL WHT 2-56 x .10 LG |                       |
| 101     | 11  | 26304       | SCR PNH PHL STL 2-56 x 3/8           |                       |
| 102     | 5   | 27002       | SCR PNH NYL 2-56 x 1/4               |                       |
| 103     | 11  | 26210       | WASHER FLAT NYL WHT #2               |                       |
| 104     | 2   | 26206       | WASHER INT TOOTH STL #4              |                       |
| 105     | 2   | 26204       | WASHER FLAT STL #4                   |                       |
| 106     | 4   | 14502       | INDUCTOR 22mH                        | L1-4                  |
| 107     | 85  | 22601       | CONTACT MALE                         |                       |
| 108     | A/R | 30401       | TAPE POLYEST 1/4W                    |                       |
| 109     | 1   | 12506       | CAP SIL MICA 470 pf 5%               | C98                   |
| 110     | 1   | -           | RES CC 1/4W S.A.T.                   | R107                  |
| 111     | 1   | 12313       | CAP CER 2700 pf 10%                  | C11                   |
| 112     | 1   | -           | RES CC 1/4W S.A.T.                   | R29                   |
| 113     | 1   | -           | RES CC 1/4W S.A.T.                   | R66                   |

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**DATARAM CORPORATION**  
CRANBURY  
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DWG. NO. 62901  
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REV. R



| REV. | REVISIONS |       |                                |               |           |
|------|-----------|-------|--------------------------------|---------------|-----------|
|      | SYM.      | SHEET | DESCRIPTION                    | APPROV.       | DATE      |
| F    | X1        |       | ECN 1678                       | RK            | 18 JUL 79 |
|      | X2        |       | ECN 1679                       | RK            | 18 JUL 79 |
|      | A         |       | ECN 1680 Release to Production | RK            | 18 JUL 79 |
|      | B         |       | ECN 1740                       | RK            | 16 OCT 79 |
|      | C         |       | ECN 1741                       | RK            | 16 OCT 79 |
|      | D         |       | ECN 1755                       | RK            | 6 NOV 79  |
|      | E         |       | ECN 1820                       | <del>RK</del> | 10-9-80   |
|      | F         |       | ECN 1951A                      | <del>RK</del> | 10-9-80   |

DWG. NO. 62902  
 SHEET 1 OF 4

|                                |                   |   |                                    |           |
|--------------------------------|-------------------|---|------------------------------------|-----------|
| DRAWN<br>MAS                   | DATE<br>5-1-79    | TITLE<br><br>BILL OF MATERIAL<br><br>DR-129S BULK SEMI ARRAY, 128K x 43 | DWG. NO. 62902<br><br>SHEET 1 OF 4 | REV.<br>F |
| CHECKED<br><i>[Signature]</i>  | DATE<br>5/7/79    |   |                                    |           |
| ENGR.<br>RK                    | DATE<br>18 JUL 79 |   |                                    |           |
| APPROVED<br><i>[Signature]</i> | DATE<br>7/18/79   |   |                                    |           |



**DATARAM CORPORATION**  
 CRANBURY NEW JERSEY

TITLE: B/M DR-129S BULK SEMI ARRAY, 128K x 43

| ITEM NO | QTY | PART NUMBER | DESCRIPTION                             | REFERENCE NOTES   |
|---------|-----|-------------|---|---|
| 1       | 49  | 18101       | DIODE, SILICON, HIGH CONDUCTANCE        | CRØ-48  |
| 2       | 1   | 10122       | RESISTOR, CC, 1/4 WATT, 10K OHMS, 5%    | R156  |
| 3       | 1   | 10601       | RESISTOR, CC, 1/4 WATT, 5.1K OHMS, 5%   | R161  |
| 4       | 4   | 10118       | RESISTOR, CC, 1/4 WATT, 2.2K OHMS, 5%   | R155, 157, 164, 1   |
| 5       | 1   | 10175       | RESISTOR, CC, 1/4 WATT, 15 OHMS, 5%     | R162  |
| 6       | 84  | 10151       | RESISTOR, CC, 1/4 WATT, 33 OHMS, 5%     | R4-8, 14-20, 22, 23, 28-32, 38-44, 46, 47, 52-56, 62-68, 70, 71, 76-80, 86-92, 94, 95, 100-104, 110-116, 118, 119, 124-128, 134-140, 142, 143 |
| 7       | 24  | 10151       | RESISTOR, CC, 1/4 WATT, 33 OHMS, 5%     | R10, 11, 26, 27, 34, 35, 50, 51, 58, 59, 74, 75, 82, 83, 98, 99, 106, 107, 122, 123, 130, 131, 146, 147                                       |
| 8       | 12  | 10615       | RESISTOR, CC, 1/4 WATT, 24 OHMS, 5%     | R12, 25, 36, 49, 60, 73, 84, 97, 108, 121, 132, 145   |
| 9       | 12  | 10151       | RESISTOR, CC, 1/4 WATT, 33 OHMS, 5%     | R13, 24, 37, 48, 61, 72, 96, 109, 120, 133, 144   |
| 10      | 1   | 10106       | RESISTOR, CC, 1/4 WATT, 150 OHMS, 5%    | R163  |
| 11      | 1   | 10130       | RESISTOR, CC, 1/4 WATT, 33K OHMS, 5%    | R159  |
| 12      | 8   | 10113       | RESISTOR, CC, 1/4 WATT, 1K OHMS, 5%     | R2, 3, 148, 149, 150, 151, 152, 154   |
| 13      | 1   | 10240       | RESISTOR, FILM, 1/4 WATT, 909 OHMS, 1%  | R160  |
| 14      | 1   | 10204       | RESISTOR, FILM, 1/10 WATT, 100 OHMS, 1% | R158  |
| 15      | 1   | 11910       | RESISTOR MODULE, 1K OHMS, 5%            | RM1   |
| 16      | 1   | 12313       | CAPACITOR, CERAMIC, 2700pf, ±10%        | C23   |

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**DATARAM CORPORATION**  
CRANBURY

DWG. NO. 62902  
B/M  
SHEET 2 OF 4

REV **F**

TITLE: B/M DR-129S BULK SEMI ARRAY, 128K x 43

| ITEM NO | QTY | PART NUMBER | DESCRIPTION                                   | REFERENCE NOTES   |
|---------|-----|-------------|---|---|
| 17      | 1   | 12315       | CAPACITOR, CERAMIC, .01 $\mu$ f $\pm$ 20%     | C24   |
| 18      | 393 | 12316       | CAPACITOR, CERAMIC, .1 $\mu$ f $\pm$ 20%      | C1,3,5,7,10,12,14,16,17,<br>20,22,27,30,31,34-36,38-40<br>42-44,46-48,50-52,54-56,<br>58-60,62,75-431 |
| 19      | 9   | 12102       | CAPACITOR, TANTALUM, 15 $\mu$ f, 20 VOLTS     | C19,21,25,63,65,67,69,71,<br>73   |
| 20      | 27  | 12105       | CAPACITOR, TANTALUM, 4.7 $\mu$ f, 10 VOLTS    | C2,4,6,8,9,11,13,15,18,26,<br>28,29,32,33,37,41,45,49,<br>53,57,61,64,66,68,70,72,74                  |
| 21      | 1   | 20304       | VOLTAGE REGULATOR LM317                       | VR1   |
| 22      | 1   | 20303       | VOLTAGE REGULATOR 79M05CLA                    | VR2   |
| 23      | 3   | 20104       | TRANSISTOR, NPN, SWITCHING, 2N2369A           | Q1,2,3  |
| 24      | 1   | 16356       | I.C. TIMER 555                                | Z43   |
| 25      | 1   | 16511       | I.C. DUAL I/P NOR GATE 74S260                 | Z42   |
| 26      | 1   | 16505       | I.C. QUAD EX OR GATE 74S86                    | Z41   |
| 27      | 12  | 16514       | I.C. QUAD 2 I/P NAND GATE 74S38               | Z1,3,4,6,7,9,10,12,13,15,<br>17,38  |
| 28      | 2   | 16531       | I.C. OCTAL BUFFER/LINE DRIVER/LINE RX 74S240  | Z39,44  |
| 29      | 26  | 16234       | I.C. OCTAL BUFFER/LINE DRIVER/LINE RX 74LS240 | Z2,5,8,11,14,16,18,19-37  |
| 30      | 344 | 16731       | I.C. DYNAMIC RAM, 16K x 1                     | Bits 0-42 A,B,C,D,E,F,G,H   |
| 31      | 1   | 42649       | STIFFENER, CIRCUIT CARD                       |   |
| 32      | 1   | 40737       | PRINTED CIRCUIT BOARD, DR-129S BSA 128K x 43  |   |
| 33      | 1   | 42648       | STIFFENER BAR <i>LONG</i>                     |   |
| 34      | 2   | 42647       | STIFFENER BAR <i>SHORT</i>                    |   |

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**DATARAM CORPORATION**  
CRANBURY  
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DWG. NO. 62902  
B/M  
SHEET 3 OF 4

REV **F**





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