REV. A	REVISIONS				
	SYM.	SHEET	DESCRIPTION	APPROV.	DATE
	A		Released to Production	RK	21Apr80

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TITLE

PRODUCT SPECIFICATION

BI-505/506 BUFFER DRIVER RECEIVER CARD

DATARAM CORPORATION

CRANBURY NEW JERSEY

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REV. A

1.0 GENERAL

The BI/505 Buffer Driver card and the BI/506 Buffer Receiver card are designed to provide a buffer stage between the DR-129S BULK SEMI memory and the input/output connectors located in the rear of the BULK SEMI chassis. The BI/506 Buffer Receiver card accepts address and control signals into a BULK SEMI chassis and passes data in both directions. The BI/505 Buffer Driver card is used when more than one BULK SEMI chassis is required and additional chassis are to be driven via the first chassis. The BI/505 transmits address and control from the first chassis to additional chassis and passes data in both directions. The BI/505 and BI/506 use the identical printed circuit board with appropriate strapping and insertion or removal of chips to determine direction of flow of address and control. The BI-505/506 will interface both the 18 bit and 36 bit BULK SEMI chassis (62909 and 62911 respectively).

2.0 MECHANICAL

The card measures 13.64" x 16.4" and is designed to fit in the BULK SEMI standard chassis. (See Figure 1) The card contains two 120-pin .100" center p.c. fingers which mate with card edge connectors designated P9 MEM and P10 I/O, respectively. The pin assignments for P9 MEM and P10 I/O are given in Tables I and II. The signals on the P9 MEM side contains all of the memory signals and the signals on the P10 I/O side contain the buffered memory signals that interface to connectors located on the BS-101 or BS-102 BULK SEMI chassis. The pin designation of the buffered memory signals for connectors A-D and L-P are given in Table III.

3.0 ELECTRICAL SPECIFICATION

3.1 Voltage and Current Requirements

Voltage: +5.0V DC ±5%

Current: 5.0 amps max.

3.2 Logic Levels and Characteristics

Refer to MIL-STD 806B for definition of symbols.

All control, address and data interface lines use standard 74S38 TTL drivers and 74S132 receivers and are terminated in a 220 ohm pull-up resistor and 330 ohm pull-down resistors on the buffer board.

Logic 0 0.45V @ -1.6μA

Logic 1 2.45V @ 40μA

All input commands shall have a rise time (t_r) and fall time (t_f) of less than 50 nanoseconds. The overshoot of the leading and trailing edges shall be less than 1.0 volt.

3.3 Input/Output Signal Lines

For a complete description of all the memory signal lines, consult the DR-129S Product Specification 02126.

BUFFER BOARD MNEMONIC	CORRESPONDING MEMORY SIGNAL MNEMONIC	DESCRIPTION	NO. OF LINES	INPUT/ OUTPUT (Defined for BI/506)
IADRAVN	ADRAVN	Address Available	1	IN
IADRACN	ADRACN	Address Accepted	1	OUT
IADROON-IADR24N	ADROON-ADR24N	Memory Address	25	IN
IRADVLDN	RADVLDN	Response Address Valid	1	IN
IDTAOON-IDTA17N IDTA18N-IDTA35N	DTAOON-DTA17N DTA18N-DTA35N	Memory Data	18	IN/OUT
ODAVNO	ODAVN	Output Data Available	1	OUT
IDACNO	IDACN	Input Data Accepted	1	OUT
IMRDRN	MRDRN	Memory Read/Restore Lower Word	1	IN
IMWRLBN	MWRLBN	Memory Write Lower Byte Lower Word	1	IN
IMWRUBN	MWRUBN	Memory Write Upper Byte Lower Word	1	IN
IMWRLBAN	MWRLBAN	Memory Write Lower Byte Upper Word	1	IN
IMWRUBAN	MWRUBAN	Memory Write Upper Byte Upper Word	1	IN
MEMSIZEOO-MEMSIZ6O	MEMSIZO-MEMSIZ6	Memory Size	7	OUT
PWR SAV	PWR INTN	Power Interrupt	1	IN
PWR INTLO	PWR INTL	Power Interlock	1	OUT
INORMN	NORMN	Normalize	1	IN
ICRERN	CRERN	Correctable Error	1	OUT
IUCERN	UCERN	Uncorrectable Error	1	OUT
ISTATN	STATN	Status	1	IN
ISTAVN	STAVN	Status Available	1	OUT
IMBYN	MBYN	Memory Busy	1	OUT

Note that mnemonics ending in an AN refer to upper word signals found only in the BS-102 BULK SEMI chassis.

The power interlock signal (PWR INTL) is an output signal from the BULK SEMI chassis internal power supply and is brought out to I/O Connector C or N, Pin 2. This signal provides a rapid low to high transition within 500 ±100ms of applied AC line voltage and a rapid high to low transition within 5 ±2ms after AC line voltage has been removed. The power interlock output logic level specification is:

Logic 0	0.25V ±0.25V @ -4.0 mA
Logic 1	2.45V @ 9.4 mA

The Power Interlock signal may be used to initiate a power down sequence at the end of which the PWR SAV input (Memory Signal - PWR INT) may be activated or PWR INTL may be directly connected to PWR INT by placing a jumper on the buffer board.

A schematic diagram showing typical buffered data, address and control lines is shown in Figure 2.

3.4 Signal Timing

The following set-up times shall be required when using the buffer card:

Address Lines (IADR00-IADR19)	The address lines must be stable 75 nanoseconds prior to Address Available (ADRAVN) and remain stable until ADRACN goes false.
Data (IDTA00N-IDTA17N) (IDTA18N-IDTA35N)	The data bus must be stable 75 nanoseconds before the assertion of Response Address Valid (RADVLDN). IDTA18N-IDTA35N are only used for BS-102 36 bit chassis.
Cycle Control Lines (IMRDRN, IMWRLBN, IMWRUBN, IMRDRAN, IMWRLBAN, IMWRUBAN)	The cycle control lines must be stable for 75 nanoseconds prior to assertion of Address Available (ADRAVN) and remain stable until ADRACN goes false.

For a detailed description of signal timing, see the DR-129S Product Specification 02126.

3.5 Environmental

3.5.1 Storage Temperature

$-40^{o}C$ to $+80^{o}C$

3.5.2 Operating Temperature

$0^{o}C$ to $+55^{o}C$

3.5.3 Relative Humidity

Up to 95% without condensation

3.5.4 Vibration

Will withstand stresses encountered in transportation

3.5.5 Weight

1.7 pounds (.77 kg)

TABLE I

BI-505/506 BUFFER DRIVER/RECEIVER

P9 MEM TERMINAL SIDE

Odd Pins - Component Side		Even Pins - Solder (Wirewrap) Side	
Pin	Signal	Pin	Signal
1	GND	2	GND
3	+5V	4	+5V
5	DTA15N	6	DTA06N
7	ADR05N	8	ADR07N
9	DTA07N	10	
11	ADR14N	12	PWR INTL
13	DTA14N	14	DTA32N
15	ADR06N	16	DTA24N
17	DTA16N	18	DTA34N
19	ADR13N	20	DTA25N
21	DTA05N	22	DTA23N
23	ADR03N	24	DTA33N
25	DTA17N	26	DTA35N
27	ADR15N	28	ADR24N
29	DTA13N	30	DTA31N
31	ADR16N	32	STATN
33	DTA04N	34	DTA22N
35	ADR10N	36	STAVN
37	IDACN	38	UCERN
39	ADR00N	40	CRERN
41	ODAVN	42	CLRBYN
43	ADR04N	44	MEMSIZ3
45	ADRACN	46	MEMSIZ4
47	ADR12N	48	MEMSIZ5
49	ADR08N	50	MEMSIZ6
51	ADR01N	52	
53	ADR09N	54	ADR20N
55	ADR02N	56	ADR21N
57	ADR11N	58	ADR22N
59	GND	60	GND
61	ADRAVN	62	ADR23N
63	GND	64	GND
65	MWRUBN (Upper Byte Lower Word)	66	MWRUBAN (Upper Byte Upper Word)
67	PWRINTN	68	
69	MRDRN (Lower Word)	70	
71	NORMN	72	
73	MWRLBN (Lower Byte Lower Word)	74	MWRLBAN (Lower Byte Upper Word)
75	RADVLDN	76	
77	GND	78	GND
79	ADR17N	80	
81	ADR18N	82	
83	ADR19N	84	
85		86	
87		88	
89		90	

Pin	Signal	Pin	Signal
91	DTA08N	92	DTA26N
93	DTA03N	94	DTA21N
95	DTA12N	96	DTA30N
97	DTA00N	98	DTA18N
99	DTA11N	100	DTA29N
101	MEMSIZ2	102	
103	DTA09N	104	DTA27N
105	MEMSIZ1	106	
107	DTA02N	108	DTA20N
109	DTA10N	110	DTA28N
111	DTA01N	112	DTA19N
113	MEMSIZ0	114	MBYN
115	+5V	116	+5V
117	GND	118	GND
119		120	

Data Bits 0-7, 17	Upper Byte, Lower Word
Data Bits 8-16	Lower Byte, Lower Word
Data Bits 18-25, 35	Upper Byte, Upper Word
Data Bits 26-34	Lower Byte, Upper Word

TABLE II

BI-505/506 BUFFER DRIVER/RECEIVER
P10 I/O TERMINAL SIDE

Odd Pins - Component Side		Even Pins - Solder (Wirewrap) Side	
Pin	Signal	Pin	Signal
1	GND	2	GND
3	+5 VOLTS	4	+5 VOLTS
5	SIG RTN	6	SIG RTN
7	SIG RTN	8	SIG RTN
9	ICRERN	10	IDTA18N
11	ICLRBYN	12	IDTA19N
13	IDTA00N	14	IDTA20N
15	IDTA01N	16	IDTA21N
17	IDTA02N	18	IDTA22N
19	IDTA03N	20	IDTA23N
21	IDTA04N	22	IDTA24N
23	IDTA05N	24	IDTA25N
25	IDTA06N	26	IDTA26N
27	IDTA07N	28	IDTA27N
29	IDTA08N	30	IDTA28N
31	IDTA09N	32	IDTA29N
33	IDTA10N	34	IDTA30N
35	IDTA11N	36	IDTA31N
37	IDTA12N	38	IDTA32N
39	IDTA13N	40	IDTA33N
41	IDTA14N	42	IDTA34N
43	IDTA15N	44	IDTA35N
45	IDTA16N	46	--
47	IDTA17N	48	--
49	SIG RTN	50	SIG RTN
51	SIG RTN	52	SIG RTN
53	SIG RTN	54	SIG RTN
55	SIG RTN	56	SIG RTN
57	SIG RTN	58	SIG RTN
59	SIG RTN	60	SIG RTN
61	IMBYN	62	IADR00N
63	IMEMSIZ6	64	IADR01N
65	IMEMSIZ5	66	IADR02N
67	IMEMSIZ4	68	IADR03N
69	IMEMSIZ3	70	IADR04N
71	IADRAVN	72	IADR05N
73	IADRACN	74	IADR06N
75	ISTATN	76	IADR07N
77	ISTAVN	78	IADR08N
79	IUCERN	80	IADR09N
81	IRADVLDN	82	IADR10N
83	IMRDRN	84	IADR11N
85	IMWRLBN	86	IADR12N
87	IMWRUBN	88	IADR13N
89		90	IADR14N

Pin	Signal	Pin	Signal
91	IMWRLBAN	92	IADR15N
93	IMWRUBAN	94	IADR16N
95	IODAVN	96	IADR17N
97	IIDACN	98	IADR18N
99	IMEMSIZ0	100	IADR19N
101	IMEMSIZ1	102	IADR20N
103	IMEMSIZ2	104	IADR21N
105	INORMN	106	IADR22N
107	PWRSAV	108	IADR23N
109	IPWRINTL	110	IADR24N
111	SIG RTN	112	SIG RTN
113	SIG RTN	114	SIG RTN
115	SIG RTN	116	SIG RTN
117	+5 VOLTS	118	+5 VOLTS
119	GND	120	GND

Odd Pins (1-39) on Input/Output Connector A-D and L-P are used for Signal Return.

TABLE III

BUFFERED MEMORY SIGNALS - I/O CONNECTORS A-D & L-P

Connector A and L

Pin	Signal
2	IDTA17N
4	IDTA16N
6	IDTA15N
8	IDTA14N
10	IDTA13N
12	IDTA12N
14	IDTA11N
16	IDTA10N
18	IDTA09N
20	IDTA08N
22	IDTA07N
24	IDTA06N
26	IDTA05N
28	IDTA04N
30	IDTA03N
32	IDTA02N
34	IDTA01N
36	IDTA00N
38	ICLRBYN
40	ICRERN

Connector B and M

Pin	Signal	
2	IDTA18N)	
4	IDTA19N)	
6	IDTA20N)	
8	IDTA21N)	
10	IDTA22N)	
12	IDTA23N)	
14	IDTA24N)	BS-102
16	IDTA25N)	ONLY
18	IDTA26N)	
20	IDTA27N)	
22	IDTA28N)	
24	IDTA29N)	
26	IDTA30N)	Not
28	IDTA31N)	Available
30	IDTA32N)	on
32	IDTA33N)	BS-101
34	IDTA34N)	
36	IDTA35N)	
38	--	
40	--	

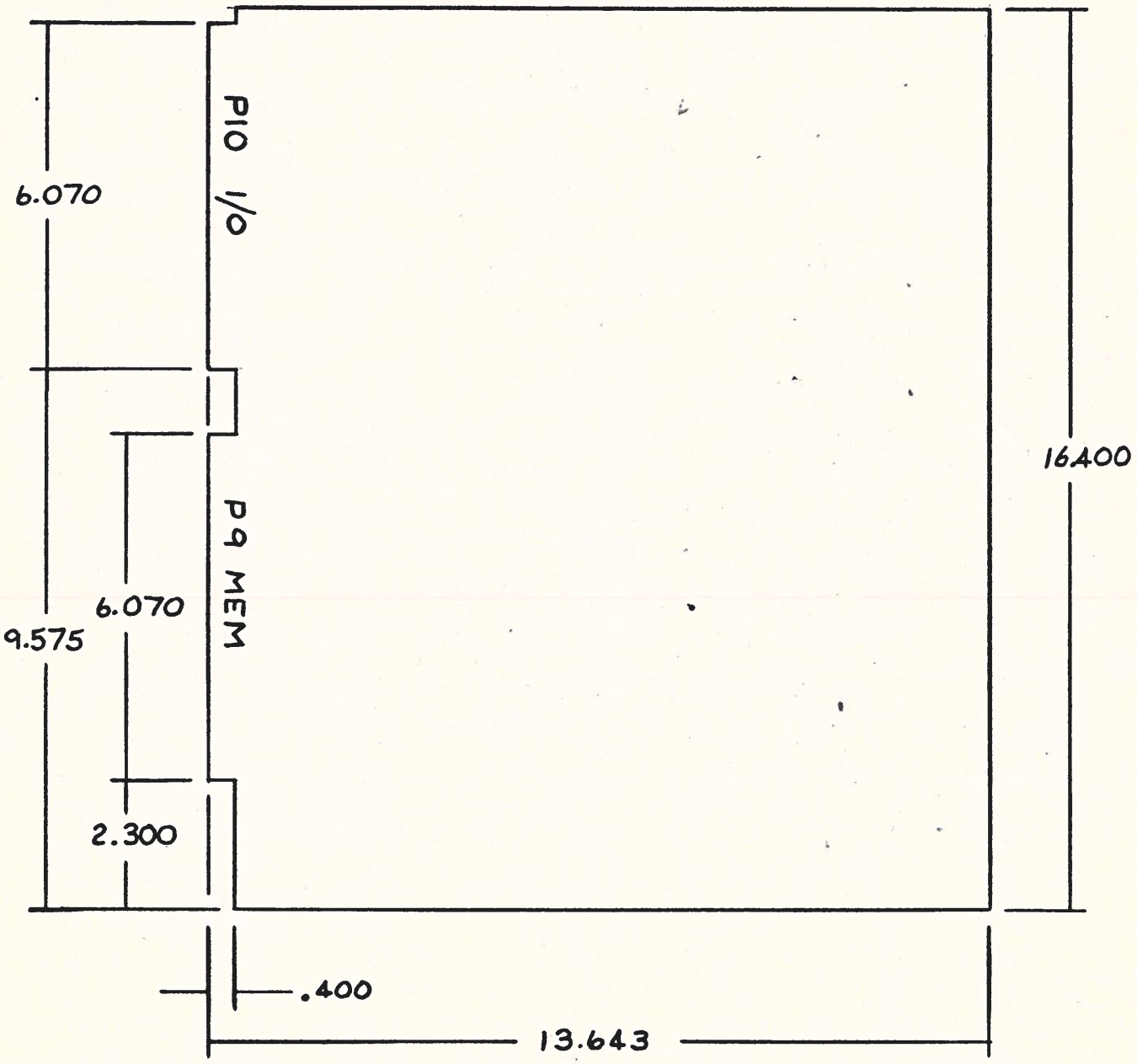
Connector C and N

Pin	Signal
2	IPWRINTL
4	PWRSAV
6	INORMN
8	IMEMSIZ2
10	IMEMSIZ1
12	IMEMSIZ0
14	IIDACN
16	IODAVN
18	IMWRUBAN (BS-102 Only)
20	IMWRLBAN (BS-102 Only)
22	
24	IMWRUBN
26	IMWRLBN
28	IMRDRN
30	IRADVLDN
32	IUCERN
34	ISTAVN
36	ISTATN
38	IADRACN
40	IADRAVN
42	IMEMSIZ3
44	IMEMSIZ4
46	IMEMSIZ5
48	IMEMSIZ6
50	IMBYN

Connector D and P

Pin	Signal
2	IADR00N
4	IADR01N
6	IADR02N
8	IADR03N
10	IADR04N
12	IADR05N
14	IADR06N
16	IADR07N
18	IADR08N
20	IADR09N
22	IADR10N
24	IADR11N
26	IADR12N
28	IADR13N
30	IADR14N
32	IADR15N
34	IADR16N
36	IADR17N
38	IADR18N
40	IADR19N
42	IADR20N
44	IADR21N
46	IADR22N
48	IADR23N
50	IADR24N

FIGURE 1



—BOARD THICKNESS IS .062 NOMINAL—

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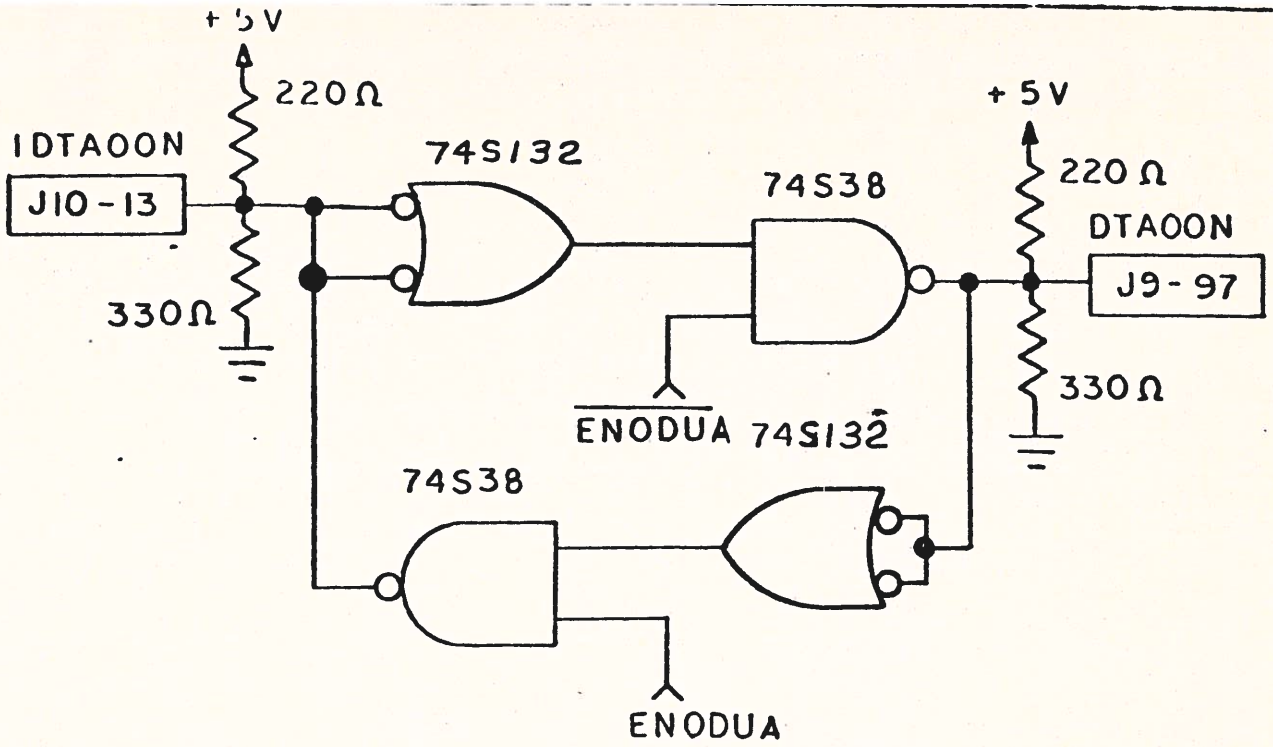
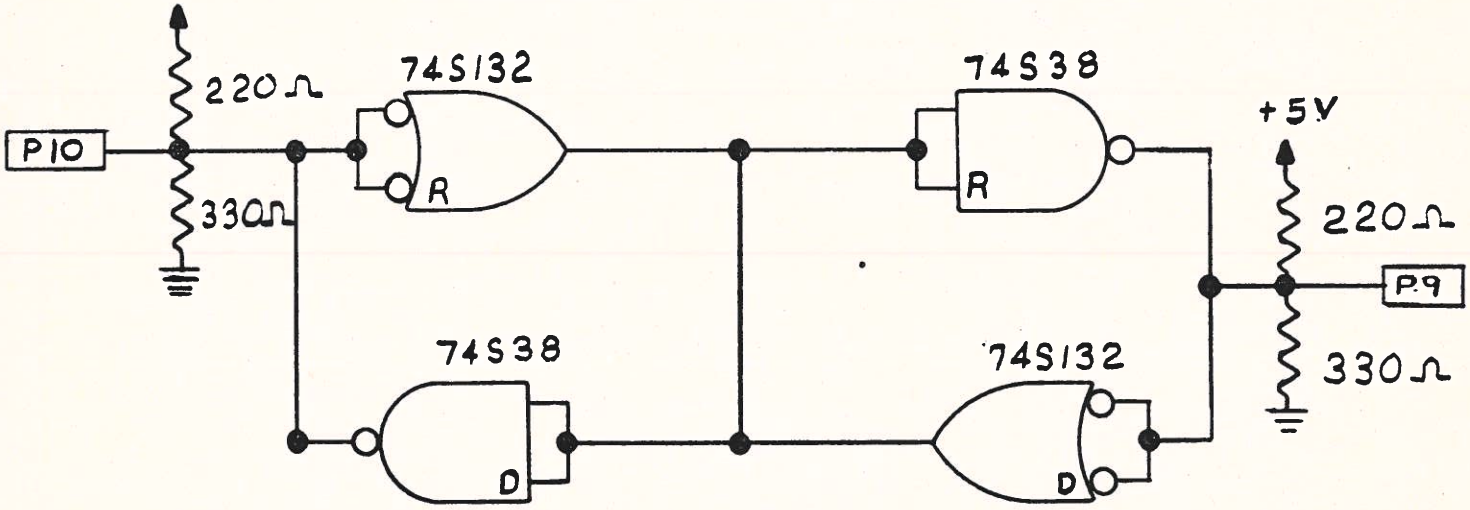


TYPICAL BUFFERED DATA SIGNAL



TYPICAL BUFFERED ADDRESS + CONTROL SIGNAL

DEVICES CONTAINING R ARE INSTALLED FOR BI 506 RECEIVER

DEVICES CONTAINING D ARE INSTALLED FOR BI 505 DRIVER

FIGURE 2