REV. C

DWG. NO. 02086 SHEET 1 OF 19

REVISIONS

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TITLE

PRODUCT SPECIFICATION

BI/501 UNIVERSAL LOGIC CARD WITHOUT TESTER &
BI/502 UNIVERSAL LOGIC CARD WITH TESTER

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 02086 SHEET 1 OF 19

REV. C

I. BI/501 UNIVERSAL LOGIC CARD WITHOUT TESTER

1.0 GENERAL

The BI/501 Universal Logic Card without tester has been designed to provide the user with ample area for any interface logic that may be required between the CPU and the memory system.

2.0 MECHANICAL

The card measures 13.64" x 16.4" and is designed to fit in the BULK CORE or BULK SEMI standard chassis. (See Figure 1) The card contains two 120-pin .100" center terminal strips designated MEM P9 and I/O P10 which mate with the CDC type connectors designated J9 and J10, respectively. The pin assignments for J9 and J10 are given in Tables I and II.

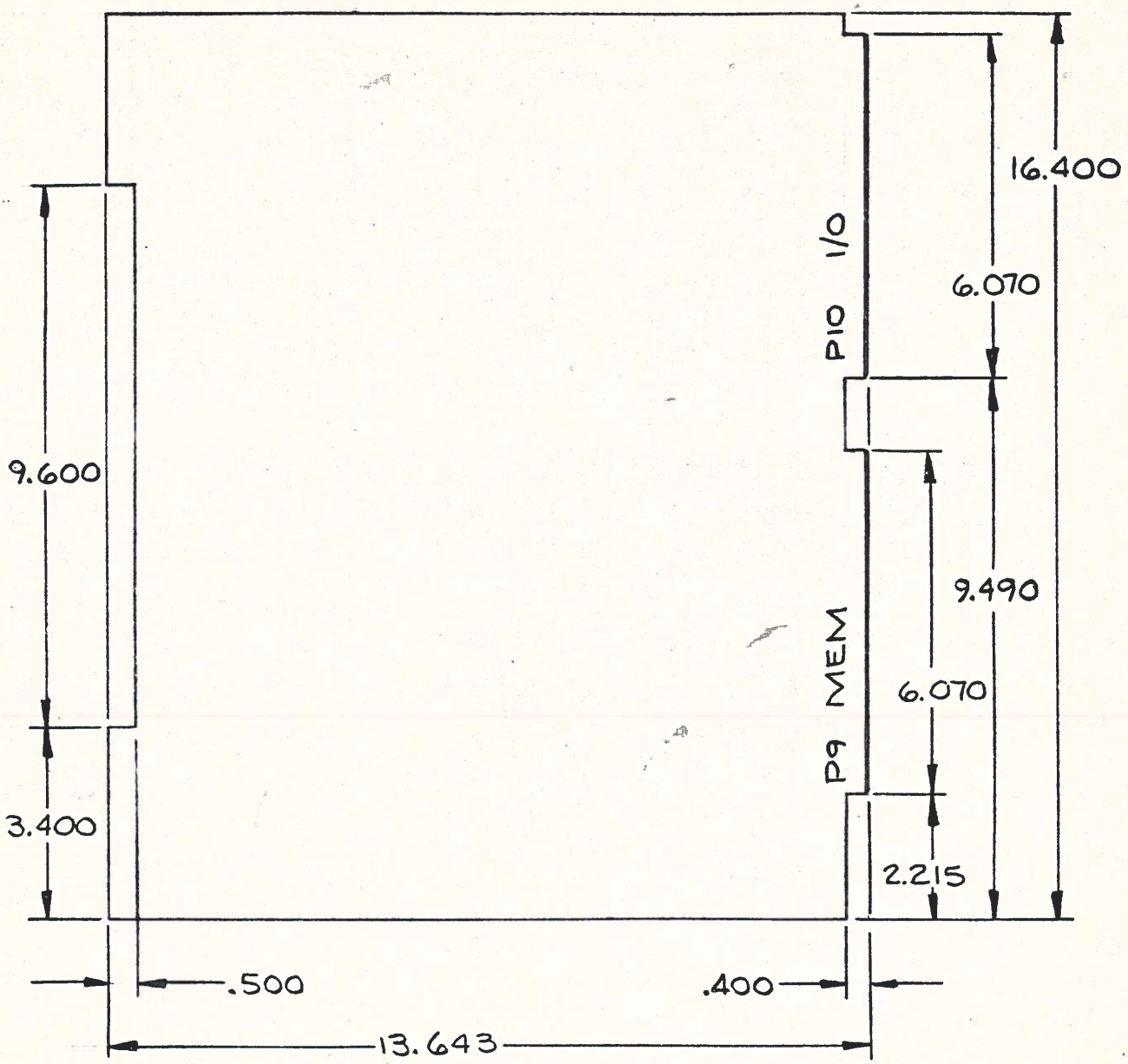
3.0 BULK CHASSIS AND UNIVERSAL LOGIC CARD

The BULK CORE and BULK SEMI chassis contain two connectors, J9 and J10, which are used for the Bulk Universal Logic Card.

Connector J9 has been dedicated to interface to the memory modules via printed circuit etch on the backplanes. Connector J10 is used to interface with the input/output connectors. The input/output connectors are four 40-pin ribbon cable connectors located at the rear of the chassis. They are designated as Connectors A, B, C, and D. The even-numbered pins on Connectors A-D may be used to carry data, address or control signals and the odd-numbered pins are dedicated to signal returns. Therefore, signals in the 40 conductor ribbon cable are arranged such that alternate conductors about an interface signal are at signal ground potential.

The BULK CORE chassis has one slot which can be used for a Universal Logic Card. The BULK SEMI chassis has three slots available that can be used for multiple Universal Logic Cards.

FIGURE 1



—BOARD THICKNESS IS .062 NOM.—

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4.0 CARD LAYOUT

I.C. socket holes are provided for and are arranged in three general areas, the I/O side corresponding to the P10 terminals, the MEM side corresponding to the P9 terminals and a central area. (See Figure 2) Each side can hold up to one hundred sixty-seven 16-pin I.C. dual-in-line sockets. The central area is provided to accommodate larger 24-40 pin dual-in-line I.C. packages.

5.0 TYPICAL INTERFACE APPLICATION

A typical interface example using the Universal Logic Card is shown in Figure 3. Address data from the CPU enters connector P10 on the I/O logic card. Bus receivers acting as buffers are wire wrapped on the card and route the data to connector P9 which provides the interface to the memory. In those instances where it is desirable to store data coming from the CPU, latches may be employed between the bus receivers and the P9 connector.

FIGURE 3

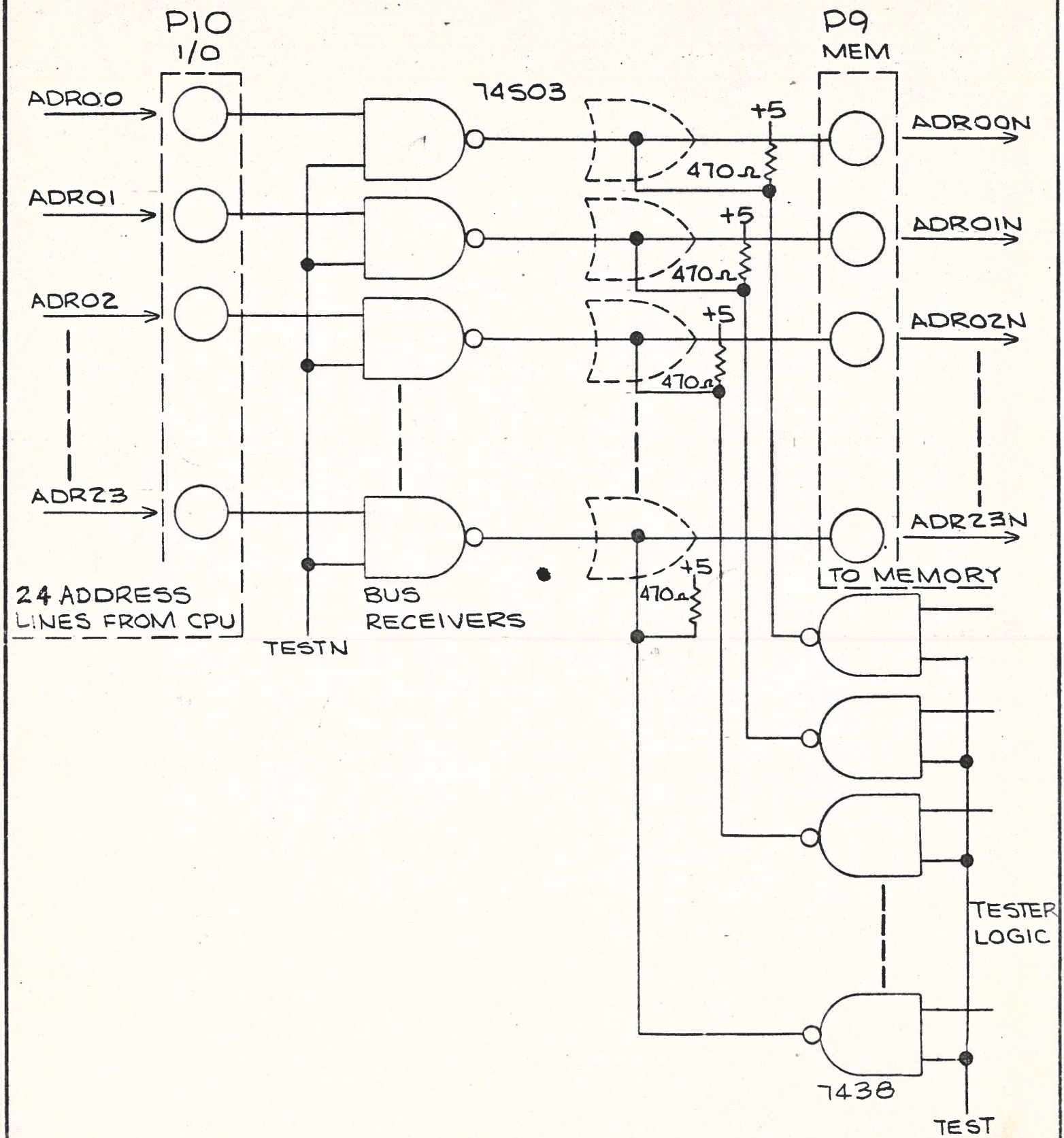

P10
I/O
P9
MEM
74S03
ADR00
ADR01
ADR02
ADR23
ADR00N
ADR01N
ADR02N
ADR23N
+5
470Ω
24 ADDRESS LINES FROM CPU
BUS RECEIVERS
TESTN
TO MEMORY
TESTER LOGIC
7438
TEST

TABLE I

UNIVERSAL LOGIC CARD
CONNECTOR J9 MEMORY INTERFACE

Odd Pins - Component Side		Even Pins - Solder (Wirewrap) Side	
Pin	Signal	Pin	Signal
1	GND	2	GND
3	+5V	4	+5V
5	DTA15N	6	DTA06N
7	ADR05N	8	ADR07N
9	DTA07N	10	
11	ADR14N	12	PWRINTL
13	DTA14N	14	DTA32N
15	ADR06N	16	DTA24N
17	DTA16N	18	DTA34N
19	ADR13N	20	DTA25N
21	DTA05N	22	DTA23N
23	ADR03N	24	DTA33N
25	DTA17N	26	DTA35N
27	ADR15N	28	
29	DTA13N	30	DTA31N
31	ADR16N	32	STATN*
33	DTA04N	34	DTA22N
35	ADR10N	36	STAVN*
37	IDACN	38	UCERN*
39	ADR00N	40	CRERN*
41	ODAVN	42	CLRBYN*
43	ADR04N	44	MEMSIZ3
45	ADRACN	46	MEMSIZ4
47	ADR12N	48	MEMSIZ5
49	ADR08N	50	MEMSIZ6
51	ADR01N	52	
53	ADR09N	54	ADR20N
55	ADR02N	56	ADR21N
57	ADR11N	58	ADR22N
59	GND	60	GND
61	ADRAVN	62	ADR23N
63	GND	64	GND
65	MWRUBN (Upper Byte Lower Word)	66	MWRUBAN (Upper Byte Upper Word)
67	PWRINTN	68	
69	MRDRN	70	
71	NORMN	72	
73	MWRLBN (Lower Byte Lower Word)	74	MWRLBAN (Lower Byte Upper Word)
75	RADVLDN	76	
77	GND	78	GND
79	ADR17N	80	
81	ADR18N	82	
83	ADR19N	84	
85	RADR1N	86	
87	RADR2N	88	
89	RADR0N	90	

* Used by BULK SEMI only

Pin	Signal	Pin	Signal
91	DTA08N	92	DTA26N
93	DTA03N	94	DTA21N
95	DTA12N	96	DTA30N
97	DTA00N	98	DTA18N
99	DTA11N	100	DTA29N
101	MEMSIZ2	102	
103	DTA09N	104	DTA27N
105	MEMSIZ1	106	
107	DTA02N	108	DTA20N
109	DTA10N	110	DTA28N
111	DTA01N	112	DTA19N
113	MEMSIZ0	114	MBYN*
115	+5V	116	+5V
117	GND	118	GND
119		120	

Data Bits 0-7, 17	Upper Byte, Lower Word
Data Bits 8-16	Lower Byte, Lower Word
Data Bits 18-25, 35	Upper Byte, Upper Word
Data Bits 26-34	Lower Byte, Upper Word

* Used by BULK SEMI only

TABLE II

UNIVERSAL LOGIC CARD
INPUT/OUTPUT CONNECTOR J10

Odd Pins - Component Side		Even Pins - Solder (Wirewrap) Side	
Pin	Signal	Pin	Signal
1	GND	2	GND
3	+5 VOLTS	4	+5 VOLTS
5	SIG RTN CONN A	6	SIG RTN CONN B
7	SIG RTN CONN A	8	SIG RTN CONN B
9	CONN A PIN 40	10	CONN B PIN 2
11	CONN A PIN 38	12	CONN B PIN 4
13	CONN A PIN 36	14	CONN B PIN 6
15	CONN A PIN 34	16	CONN B PIN 8
17	CONN A PIN 32	18	CONN B PIN 10
19	CONN A PIN 30	20	CONN B PIN 12
21	CONN A PIN 28	22	CONN B PIN 14
23	CONN A PIN 26	24	CONN B PIN 16
25	CONN A PIN 24	26	CONN B PIN 18
27	CONN A PIN 22	28	CONN B PIN 20
29	CONN A PIN 20	30	CONN B PIN 22
31	CONN A PIN 18	32	CONN B PIN 24
33	CONN A PIN 16	34	CONN B PIN 26
35	CONN A PIN 14	36	CONN B PIN 28
37	CONN A PIN 12	38	CONN B PIN 30
39	CONN A PIN 10	40	CONN B PIN 32
41	CONN A PIN 8	42	CONN B PIN 34
43	CONN A PIN 6	44	CONN B PIN 36
45	CONN A PIN 4	46	CONN B PIN 38
47	CONN A PIN 2	48	CONN B PIN 40
49	SIG RTN CONN A	50	SIG RTN CONN B
51	SIG RTN CONN A	52	SIG RTN CONN B
53	SIG RTN CONN A	54	SIG RTN CONN B
55	SIG RTN CONN C	56	SIG RTN CONN D
57	SIG RTN CONN C	58	SIG RTN CONN D
59	SIG RTN CONN C	60	SIG RTN CONN D
61	NOT USED	62	CONN D PIN 2
63	NOT USED	64	CONN D PIN 4
65	NOT USED	66	CONN D PIN 6
67	NOT USED	68	CONN D PIN 8
69	NOT USED	70	CONN D PIN 10
71	CONN C PIN 40	72	CONN D PIN 12
73	CONN C PIN 38	74	CONN D PIN 14
75	CONN C PIN 36	76	CONN D PIN 16
77	CONN C PIN 34	78	CONN D PIN 18
79	CONN C PIN 32	80	CONN D PIN 20
81	CONN C PIN 30	82	CONN D PIN 22
83	CONN C PIN 28	84	CONN D PIN 24
85	CONN C PIN 26	86	CONN D PIN 26
87	CONN C PIN 24	88	CONN D PIN 28
89	CONN C PIN 22	90	CONN D PIN 30

Pin	Signal	Pin	Signal
91	CONN C PIN 20	92	CONN D PIN 32
93	CONN C PIN 18	94	CONN D PIN 34
95	CONN C PIN 16	96	CONN D PIN 36
97	CONN C PIN 14	98	CONN D PIN 38
99	CONN C PIN 12	100	CONN D PIN 40
101	CONN C PIN 10	102	NOT USED
103	CONN C PIN 8	104	NOT USED
105	CONN C PIN 6	106	NOT USED
107	CONN C PIN 4	108	NOT USED
109	CONN C PIN 2	110	NOT USED
111	SIG RTN CONN C	112	SIG RTN CONN D
113	SIG RTN CONN C	114	SIG RTN CONN D
115	SIG RTN CONN C	116	SIG RTN CONN D
117	+5 VOLTS	118	+5 VOLTS
119	GND	120	GND

Odd Pins (1-39) on Input/Output Connector A-D are used for Signal Return.

II. BI/502 UNIVERSAL LOGIC CARD WITH TESTER

1.0 GENERAL

The BI/502 Universal Logic Card with tester provides self-test capability for the DR-128 and DR-129S and is compatible with the BULK CORE and BULK SEMI chassis. The BI/502 tester card is mechanically the same as the BI/501 Universal Logic Card. The tester hardware is located on the MEM P9 terminal side leaving the other half of the board on the I/O P10 terminal side for interface between the CPU and the memory system. See Schematic Dwg. 03102.

A control panel, which is part of the tester card, contains all of the required controls and indicators for self-test. See Figure 4. A single front panel switch is used to disconnect the memory from the internal interface for self test. A selector switch, located on the tester card, is used to expand the word length to 36 bits and 4 additional address bits. The front panel lights will display data or address during test.

2.0 TESTER CHARACTERISTICS

2.1 Address

24 bits are provided to sequentially test through 16M* locations.

2.2 Data

18 bits of data with the option of multiplexing to 36 bits by means of a selector switch located on the tester card.

2.3 Test Modes

Clear/Write

Read/Restore

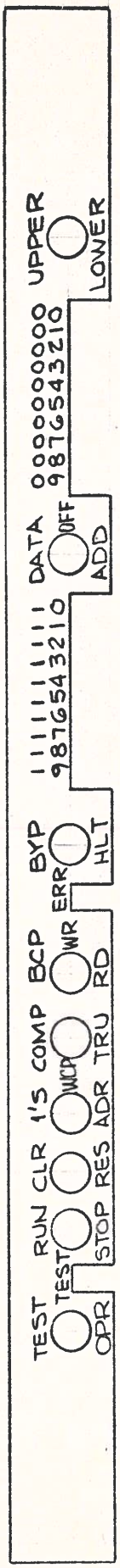
Alternate Read/Restore, Clear/Write with Bit Complemented Data Pattern

2.4 Cycle Time

The time required to do a Read/Restore or a Clear/Write cycle at each memory location is 1.6μs.

* M = 1024K

FIGURE 4



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2.5 Test Patterns

2.5.1 All "1's"

2.5.2 All "0's" (1's Complement)

2.5.3 Worst Case Pattern

2.5.4 Worst Case Pattern Complemented

2.5.5 Random Data (Address)

2.5.6 Random Data Complemented (Address Complemented)

2.5.7 Bit Complemented form of all Data Patterns above.

2.6 Error Check

2.6.1 Stop on Error (HLT)

2.6.2 Error Bypass (BYP)

2.7 Display

2.7.1 Test (1 light)

2.7.2 Error (1 light)

2.7.3 Address or Data (20 lights which may be turned off when not in use)

Light ON is "1". Light OFF is "0". Address and data lights are shared and selected by a single switch.

NOTE: Logic polarity here conforms to the DR-129S and DR-128 logic convention, i.e., "1" is negative true (0V) and "0" is +5V.

2.8 Power Requirements

Voltage +5.0 Volts DC ±5%

Current 2.2 Amps Max.

3.0 OPERATING INSTRUCTIONS

3.1 Control Switches (See Figure 4)

3.1.1 TEST/OPR

TEST - When switch is in the TEST position, the memory system is in the self-test mode.

OPR - When the switch is in the OPR position, the memory system is in the normal operational mode.

3.1.2 RUN/STOP

RUN - (Momentary Up) Resets the address counter and initiates a test cycle. The test display light will turn on indicating that the tester is scanning and testing at each memory address.

STOP - (Momentary Down) Immediately halts the test cycle at the address being accessed during this time and prevents advancement ot the next address location. The test display light will turn off indicating that the tester is in an idle condition. Initiation of the clear switch is required prior to resuming test.

3.1.3 CLR/RES

CLR - (Momentary Up) Resets all internal registers on the test module and abruptly terminates the test cycle at the address being accessed during this time. The CLR switch also activates the NORMN memory input and clears the memory control registers of all memory modules.

RES - (Momentary Down) Resumes the test cycle from the last address location to be sequenced. If the error switch is in the HLT position, the tester will resume testing until the next error is detected and stop at that location.

3.1.4 1's/WCP/ADR

1's - Sets all data bits to a "1" state at each address.

WCP - Selects the worst case data pattern. For the DR-128, worst case data pattern occurs when address bits ADROON and ADR16N are equal.

ADR - Sets all data bits at each address location to the actual address. This is defined as Random Data.

3.1.5 COMP/TRU

TRU - Selects the true data selected by the 1's/WCP/ADR switch.

COMP - Complements the data selected by the 1's/WCP/ADR switch. Data is, therefore, 0's/WCP/ADR.

3.1.6 BCP/WR/RD

BCP - The tester generates a bit complement data pattern of the data selected by the 1's/WCP/ADR switch at each address. The pattern consists of the following sequence at each address location: Read Data, Write $\overline{\text{Data}}$, Read $\overline{\text{Data}}$, Write Data.

WR - The tester performs a Clear/Write cycle at each address location.

RD - The tester performs a Read/Restore cycle at each address location.

3.1.7 BYP/HALT

BYP - The tester will continually sequence through all address locations even if an error is detected and displayed on the ERR indicator light.

HLT - The tester will stop on error prior to advancing to the next address location and terminate the test cycle. The error indicator ERR will turn on.

3.1.8 DATA/OFF/ADD

DATA - Indicator lights will display the 18 bits of test data from memory. The data is read from right to left with the LSB to the far right of the DATA/OFF/ADD switch.

OFF - All front panel indicator lights are turned off.

ADD - Indicator lights will display the test cycle address. The address is read from the 17 indicator lights from right to left with the LSB to the far right of the DATA/OFF/ADD switch. The last three display lights on the left (9, 8, 7) indicate which memory system module (one of eight maximum) is being accessed when more than one memory module is used. The tester accesses the higher order modules first and sequences in descending order (111, 110, etc.)

3.1.9 UPPER/LOWER

This switch allows the tester to be used in either the single word BULK CORE or BULK SEMI chassis (BC-101/BS-101) or the double word BULK CORE or BULK SEMI chassis (BC-102/BS-102).

UPPER - When the switch is in the UPPER position, the tester is accessing the higher order 18 bits (Upper Word) and Addresses A20-A23.

LOWER - When the switch is in the LOWER position, the tester is accessing the lower order 18 bits (Lower Word).

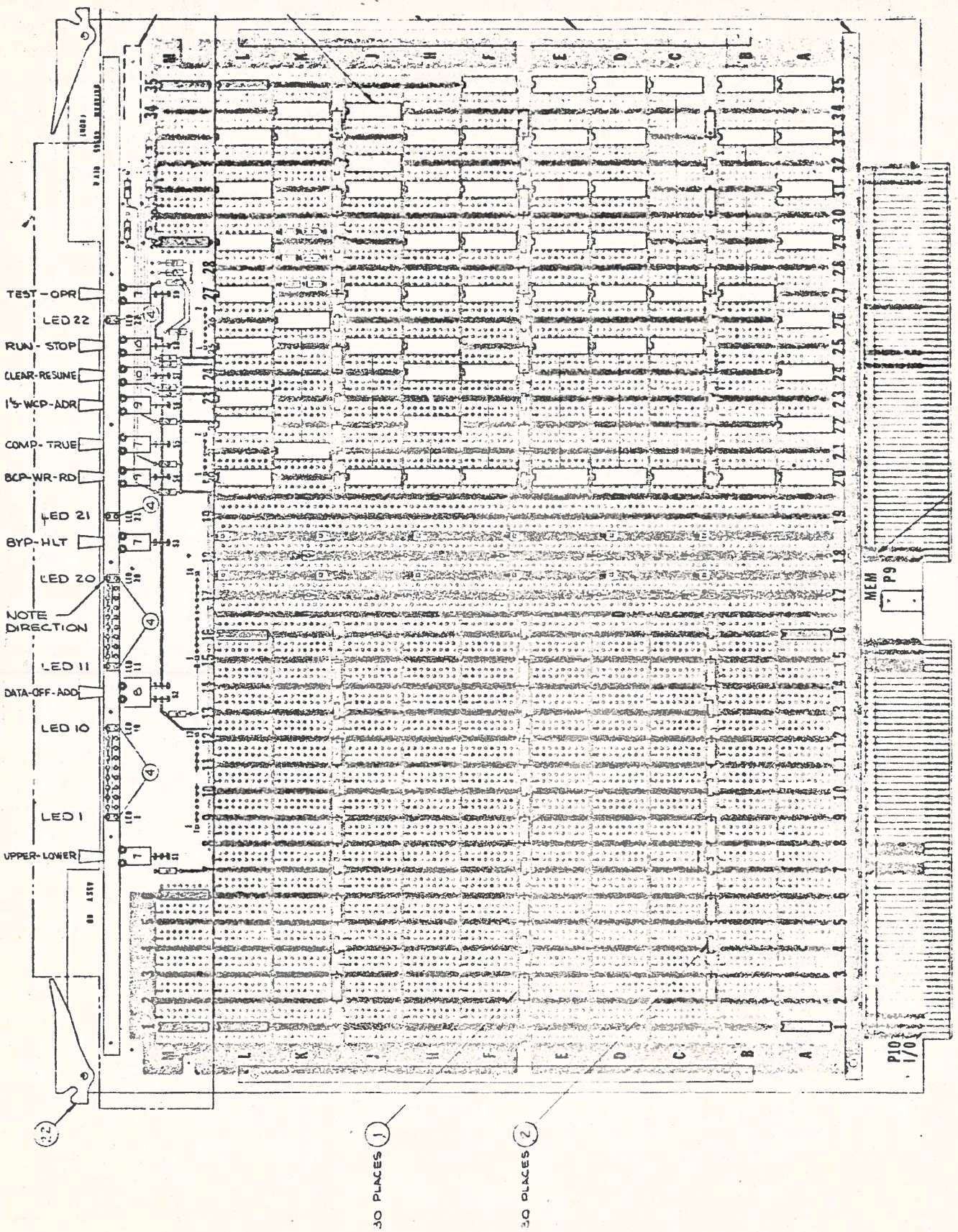
TEST-OPR
LED 22
RUN-STOP
CLEAR-RESUME
I'S-WCP-ADR
COMP-TRUE
BCP-WR-RD
LED 21
BYP-HLT
LED 20
NOTE DIRECTION
LED 11
DATA-OFF-ADD
LED 10
LED 1
UPPER-LOWER
MEM
P9
P10
I/O
COMPONENT SIDE
30 PLACES
30 PLACES

Figure 2A

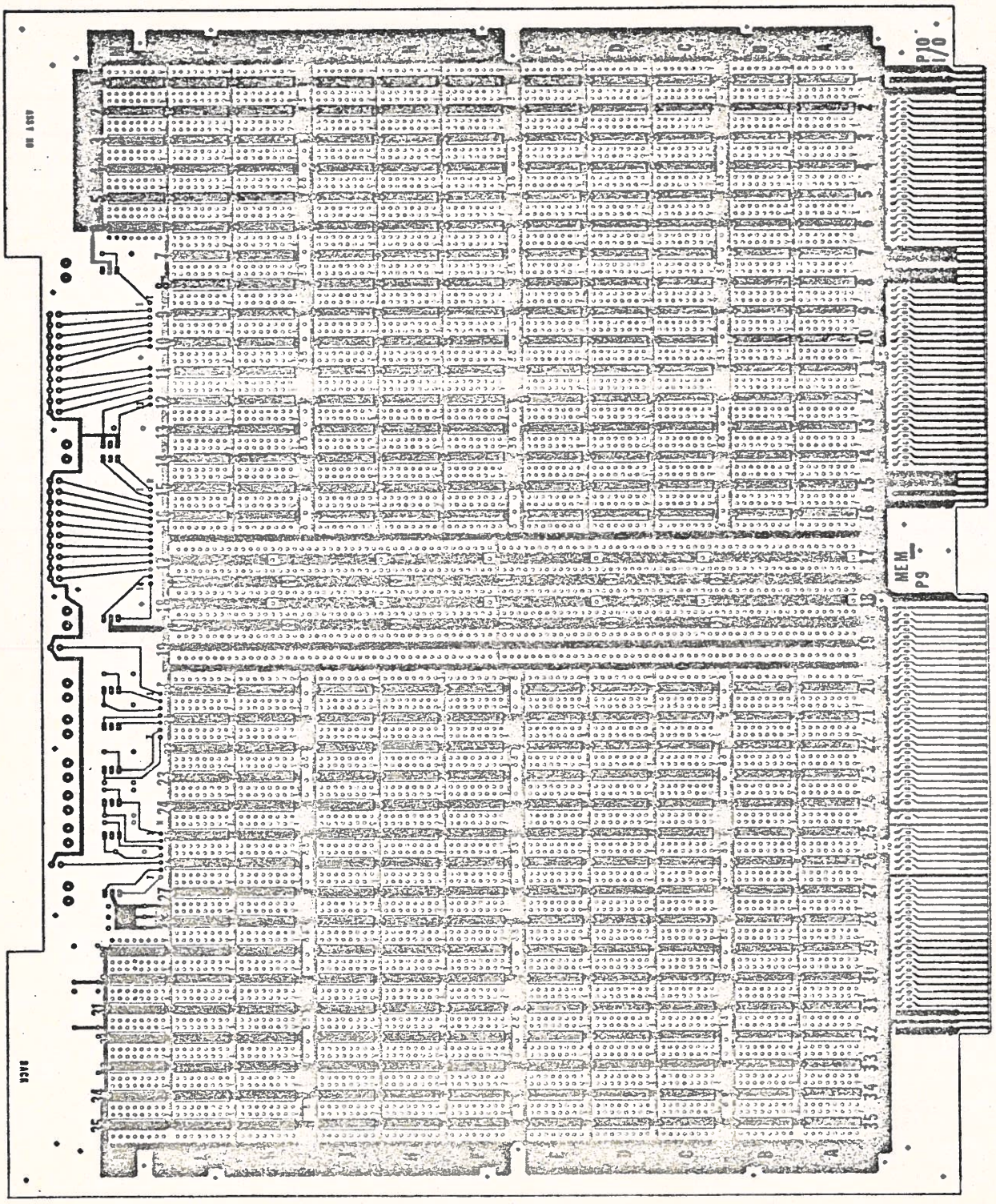

Figure 2B

3.2 Test Procedure

3.2.1 Set the front panel switches to the following postions:

TEST/OPR	TEST
1's/WCP/ADR	1's
COMP/TRU	TRU
BCP/WR/RD	WR
BYP/HLT	BYP
DATA/OFF/ADD	DATA or ADD

3.2.2 Momentarily depress the CLR switch first and then the RUN switch upward. The TEST light should turn on indicating that the tester is cycling through each address and writing in the data selected by the 1's/WCP/ADR switch. Allow the tester enough time to scan all of the addresses in each memory module. This can be noted by monitoring the address display, particularly the last three bits (9, 8, 7) which will indicate which module is being accessed.

3.2.3 Depress the STOP switch. The TEST light should turn off indicating that the test sequence has stopped. Move the BCP/WR/RD switch to the READ position. Momentarily depress the CLR switch first and then the RUN switch upward. The tester will now cycle through each address performing Read/Restore cycles.

3.2.4 To test other patterns, depress the STOP switch, move the 1's/WCP/ADR switch and the COMP/TRU switch to the desired data pattern and the BCP/WR/RD switch to WR. Momentarily depress the CLR switch first and then the RUN switch upward. Repeat 3.2.3 to read back the data that was entered.

3.2.5 To test in the bit complement pattern (BCP), momentarily depress the STOP switch and move the BCP/WR/RD switch to BCP. Move the 1's/WCP/ADR switch and the COMP/TRU switch to the desired data pattern. Momentarily depress the CLR switch first and then the RUN switch upward. The tester will now sequence through each address performing a Read Data, Write Data, Read Data, Write Data cycle at each memory location.

3.2.6 If an error is detected, the ERR light will turn on. In order to determine the location of the error, move the BYP/HLT switch to the HLT position. The tester will stop cycling when an error is detected. The Address/Data display lights will indicate the error address and the data bits at that address. By momentarily depressing the RES switch, the tester will initiate a test cycle from the last address sequenced and will advance to the next location that contains an error.

In order to fully test each module, it is necessary to test in all possible combinations. A suggested test routine would be the following:

1's-True - Write, Read
WCP-True - Write, Read
ADR-True - Write, Read
1's-Comp - Write, Read
WCP-Comp - Write, Read
ADD-Comp - Write, Read
1's-True, Comp - BCP
WCP-True, Comp - BCP
ADR-True, Comp - BCP

4.0 ORDERING INFORMATION

The following Dataram part numbers have been assigned to the Universal Logic Card:

Part Number	Configuration
62803	Universal Logic Card w/o Tester BI/501
62804	Universal Logic Card with Tester BI/502