TECHNICAL MANUAL

MODEL B03
LSI-II COMPATIBLE SYSTEM CHASSIS

DATARAM CORPORATION

TECHNICAL MANUAL

MODEL BO3
LSI-II COMPATIBLE SYSTEM CHASSIS

06140

REV. C	REVISIONS				
	SYM.	SHEET	DESCRIPTION	APPROV.	DATE
DWG. NO. 02122 SHEET 1 OF 14	A		Released to Production	BDN	2/21/79
	B		Revised to include LSI-11/23 and new wiring of slots 6 & 7	BDA	4/2/80
	C		Revised to add all Q-Bus Backplane version.	BDA	7/15/82

DRAWN MAS	DATE 1-29-79	TITLE PRODUCT SPECIFICATION B03 LSI-11 COMPATIBLE SYSTEM CHASSIS	
CHECKED DY	DATE 8/1/79		
ENGR. [illegible]	DATE 8/1/79		
APPROVED [illegible]	DATE 8/1	DATARAM CORPORATION CRANBURY NEW JERSEY	DWG. NO. 02122 SHEET 1 OF 15 REV. C

1.0 GENERAL

The Dataram Corporation Model B03 System Chassis is a 5¼ high rack mountable chassis which contains an eight slot backplane compatible to the DEC* LSI-11* microcomputer.

Power supply, cooling and operator controls are also contained in the B03 chassis.

1.1 LSI-11 Backplane and Processor (See Figure 1)

The LSI-11 backplane consists of 8 DEC standard quad slots on 0.5 inch centers. The first slot can accomodate the quad (8.5" x 10") LSI-11 processor board (KD11-F) or either of the dual (8.5" x 5") processor boards, LSI-11/2 (KD11-HA) or LSI-11/23 (KDF11-AA).

Two versions of the backplane are available:

1.1.1 Version I

Slots 1 through 5 and slot 8 are wired with the LSI-11 Bidirectional Asynchronous BUS on the A and B connectors and on the C and D connectors. These slots will accept any quad or dual width device which is compatible to the LSI-11 BUS including memory and peripheral controllers. Slots 6 and 7 are wired with the LSI-11 BUS on the A and B connectors. The C and D connectors are wired with the DEC C-D BUS. These slots are compatible to two board controllers which require board to board interwiring such as the DEC RLV11-AK Disk Controller.

1.1.2 Version II

All slots are wired with the LSI-11 BUS.

1.2 Memory Systems

A total of 28K x 16 bits words of core of MOS memory may be addressed by the LSI-11 or LSI-11/2 processor. The upper 4K of 32K words is reserved for I/O device addresses. Two Dataram DR-115 16K x 16 core memory modules or one DR-115S 32K x 16 semiconductor memory module may be plugged into the B03 backplane.

A total of 124K x 16/18** bit words of core of MOS memory may be addressed by the LSI-11/23 procewsor. The upper 4K of 128K words is reserved for I/O device addresses. One Dataram DR-113S 128K x 16/18 or four DR-115S 32K x 16/18 semiconductor memory modules may be plugged into the B03 backplane. Physical space

*Registered trademark of Digital Equipment Corporation
**A parity control module Model P03 (P/N 69936) is available from Dataram to provide parity trap logic for the LSI-11/23.

within the B03 backplane does not allow the entire 124K of address space to be configured using DR-115 16K x 16 core memory. However, combinations of various sizes of DR-115 core and DR-115S or DR-113S semiconductor memory may be installed into the B03 backplane in order to fill the address space. The DR-115 core memory utilizes LSI-11 BUS signals on the C and D connectors as well as the A and B connectors and cannot be plugged into slots 6 or 7 of the Version I backplane.

The DR-115, DR-115S and DR-113S are described in Product Specifications 02097, 02108, and 02127 respectively.

1.3 Operators Console Unit (OCU)

The OCU module, located on the lefthand side of the B03 chassis, contains all the necessary circuitry and controls for the operation of the LSI-11 microcomputer.

The power sequencing logic, line clock and operator control interface circuits are located on the OCU module. The operator control and indicator lights are installed on a panel (see Figure 1) which is mounted on the front of the OCU module.

2.0 SPECIFICATIONS

2.1 Front Panel Controls and Indicators

As shown in Figure 1, a set of control switches and indicators is located on the front of the B03. The following control switches and indicators are used for the operation of the LSI-11 computer:

Control/ Indicator	Type	Function
ENABLE/HALT	Two Postion Toggle Switch	When set to ENABLE, the B HALTL line to the processor is not asserted and the processor is in the RUN mode. When set to HALT, the B HALTL line is asserted allowing the processor to execute console ODT microcode. See Section 2.3
LTC ON/OFF	Two Position Toggle Switch	When set to ON, enables the generation of the Line Time Clock (LTC) B EVNTL signal. When set to OFF, disables the Line Time Clock.
INIT	Two Position Momentary Action Toggle Switch	When lifted up, this switch will momentarily set BDCOKH low to initialize the system.

AC ON/OFF	Two Position Switch	When set to ON, applies AC power to the BO3.
CPU RUN	LED Indicator	Illuminates when LSI-11 processor is in RUN state.
DC ON	LED Indicator	Illuminates when the DC voltages are within tolerance (+5>4.6 volts and +12>11.2 volts)

2.2 Backplane Bus Signals

2.2.1 LSI-11 BUS

Backplane pin assignments are listed and described in the following table. Only slots A and B are listed. However, for slots 1-5 and slot 8 of Version I and slots 1-8 of Version II, they are identical to slots C and D.

Bus Pin	Mnemonic	Description
AA1	BIRQ5 L	Interrupt Request Priority Level 5 (LSI-11/23)
AB1	BIRQ6 L	Interrupt Request Priority Level 6 (LSI-11/23)
AC1	BDAL16 L	Extended Address Bits (LSI-11/23)
AD1	BDAL17 L	
AE1	SSPARE1	Special Spare (not assigned, not bussed) Available for User Interconnections
AF1	SSPARE2	
AH1	SSPARE3	
AJ1	GND	Ground - System Signal Ground and DC Return
AK1	MSPAREA	Maintenance Spares - Normally connected together on the backplane at each option location (not bussed connection)
AL1	MSPAREA	
AM1	GND	Ground - System Signal Ground and DC Return
AN1	BDMRL	Direct Memory Access (DMA) Request - A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master(it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt - When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored, but memory refresh interrupts

		(enabled if W4 on M7264 and M7264-YA processor modules is removed) and DMA request/grant sequences are enabled. When in HALT state, processor executes ODT microcode and console device operation is invoked.
AR1	BREF L	Memory Refresh-Asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by a DMA device. This signal forces all dynamic MOS memory units requiring bus refresh signals to be activated for each BSYNC L/BDIN L bus transaction CAUTION The user must avoid using multiple DMA data transfers (Burst or "hog" mode) that could delay refresh operation. Complete refresh cycles must occur once every 1.6 ms, if required.
AS1	+12B	+12V Battery Power-Secondary +12V power connection Battery power can be used with certain devices.
AT1	GND	Ground-System signal ground and DC return
AU1	PSPARE1	Spare (Not assigned-Customer usage not recommended)
AV1	+5B	+5V Battery Power-Secondary +5V power connection Battery power can be used with certain devices.
BA1	BDCOK H	DC Power OK-Power supply-generated signal that is asserted when there is sufficient DC voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK-Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BC1	BDAL 18L	Extended address bits LSI-11/23 REV C or later only
BD1	BDAL 19L	Extended address bits LSI-11/23 REV C or later only
BE1	BDAL 20L	Extended address bits LSI-11/23 REV C or later only
BF1	BDAL 21L	Extended address bits LSI-11/23 REV C or later only
BH1	SSPARE8	Special spare-Bussed connection all LSI-11 Bus slots
BJ1	GND	Ground-System signal ground and DC return
BK1	MSPAREB	Maintenance Spare-Normally connected together on
BL1	MSPAREB	the backplane at each option location (not a bussed connection).
BM1	GND	Ground-System signal ground and DC return
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal indicating that the DMA device is bus master.
BP1	BIRQ7 L	Interrupt request priority level 7 (LSI-11/23)

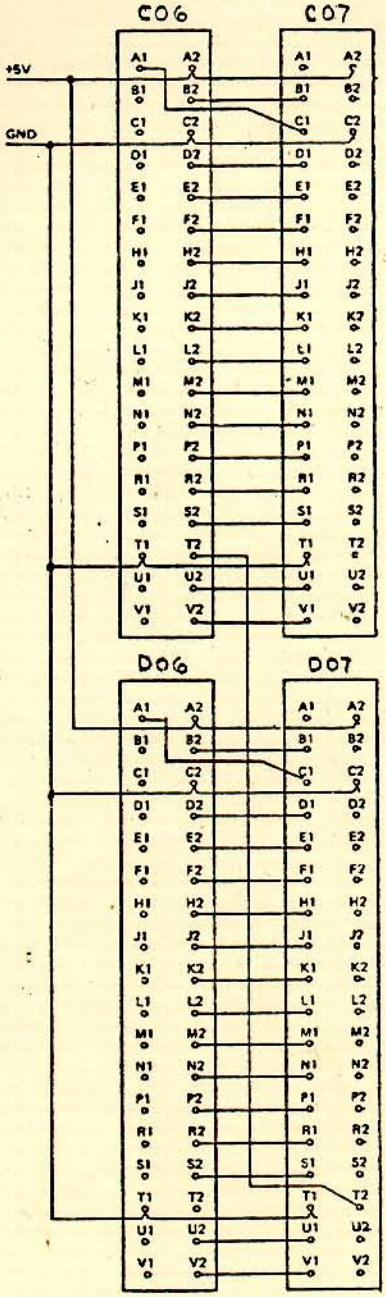
Bus Pin	Mnemonic	Description
BR1	BEVNT L	External Event Interrupt Request-When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100$_8$. A typical use of this signal is a line time clock interrupt.
BS1	PSPARE 4	Spare (Not assigned. Customer usage not recommended.)
BT1	GND	Ground-System signal ground and DC return
BU1	PSPARE2	Spare (not assigned. Customer usage not recommended.)
BV1	+5	+5V Power-Normal +5V DC system power
AA2	+5	+5V Power-Normal +5V DC system power
AB2	-12	-12V Power-Voltage (Available as an option in the BO3)
		NOTE DRC and DEC LSI-11 modules which require negative voltages contain an inverter circuit (on each module) which generates the required voltage(s), hence, -12V power is not required with Dataram or Digital-supplied options.
AC2	GND	Ground-System signal ground and DC return
AD2	+12	+12V Power-12V DC system power
AE2	BDOUT L	Data Output-BDOUT, when asserted, implies that valid data is available on BDAL<0:15>L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply-BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
AH2	BDIN L	Data Input-BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device.

Bus Pin	Mnemonic	Description
		2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize-BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL<0:17>L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte-BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L in a DATOB bus cycle for byte addressing.
AL2	BIRQ4 L	Interrupt Request-A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. If the PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output-This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device BIAKI L pin. (See Figure 2).
AP2	BBS7 L	Bank 7 Select-The bus master asserts BBS7 L when an I/O device address in the upper 4K address range is placed on the bus. BSYNC L is then asserted and BBS7 remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant-Input and DMA Grant Output-This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus.

Bus Pin	Mnemonic	Description
		If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership and executing the required bus cycle. (See Figure 2.)
		CAUTION DMA device transfers must not interfere with the memory refresh cycle.
AT2	BINIT L	Initialize-BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H) or by executing a RESET instruction.
AU2	BDAL0 L	Data/Address Lines-These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.
BA2	+5	+5V Power-Normal +5V DC system power
BB2	-12	-12V Power-Voltage is not available in BO3.
BC2	GND	Ground-System signal ground and DC return
BD2	+12	+12V Power-+12V system power
BE2	BDAL2 L	Data/Address Lines-These 14 lines are part of the 16-line data/address bus previously described.
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

2.2.2 C-D Bus

The C and D connectors of slots 6 and 7 of Version I are wired according to the diagram below.



C-D BUS

Viewed from Wiring Side

2.3 LSI-11 Microcomputer Installation

The Quad LSI-11 (KD11-F), the Dual LSI-11/2 (KD11-HA) or the LSI-11/23 (KDF11-HA) Microcomputer may be installed into the BO3 backplane.

Figures 2 and 3 show the recommended locations for installation of the LSI-11 processor and also the routing of the bus priority chain signals.

2.4 Module Installation

LSI-11 compatible memory systems and interface modules may be installed in the BO3 backplane using the following rules:

1. The first Dataram DR-115 (16K) core memory system should be installed in slot 8.

2. If a second DR-115 core memory system is required, it should be installed in slot 5 or above. Do not install in either slot 6 or slot 7.

3. Bus priority chain shall not be broken between DMA devices. Non-DMA devices (such as memory) have jumpers to continue priority chain. Dataram LSI continuity cards (P/N 69915) may also be installed in unused slots to continue chain.

2.5 Power Supply

The power supply in the standard BO3 chassis provides two DC voltages +5V and +12V. These voltages are supplied to the LSI backplane.

Another version of the BO3 has an additional voltage of -12 volts at 1 amp.

The specifications for the power supply in the standard BO3 are as follows.

2.5.1 Output Current

(a) +12 Volts : 8.0 Amps
(b) +5 Volts : 24.0 Amps

2.5.2 Regulation, DC

The maximum deviation with AC line voltage variations, load current varied from min. load to full load and AC line frequency variations of ±2Hz are as follows:

(a) +12 Volts : ±0.1% (0.5 Amp minimum load)
(b) +5 Volts : ±0.1% (1.5 Amps minimum load)

2.5.3 Ripple and Noise

The maximum ripple and noise for the output voltage under all specified AC line and load conditions is:

(a)	+12 Volts	:	24 mvpp
	+5 Volts	:	10 mvpp

2.5.4 Transient Response

Voltage variation for the +12 volt and +5 volt outputs does not exceed +2% for load current changes.

(a)	+12 Volts	:	A 4 amp/microsecond change
(b)	+5 Volts	:	A 2 amp/microsecond change

2.5.5 AC Input Requirements

Voltage

115/230 VAC, Single Phase, 47-63Hz
Voltage changeover from 115 to 220 VAC is via an internal slide switch.

Current

With a fully loaded power supply:

115V - 4 amps
230V - 2 amps

2.6 LSI-11 Processor and Software

Complete hardware and software specifications are available from the Digital Equipment Corporation publication "Microcomputer Handbook". The BO3, being LSI-11 based, will run all operating systems and programming languages available for the LSI-11 microcomputer. At present, three operating systems are available from DEC. These are RT-11, RSX-11S and RSX-11M.

2.7 Mechanical and Environmental Data

The BO3 chassis occupies 5¼" of space in a standard 19" rack. Depth clearance required is 21".

All modules are plugged horizontally into the front of the BO3 chassis. The power supply is located in the rear of the chassis. A fan assembly is located between the memory modules and the power supply for system cooling. Air flow is from right to left. The BO3 chassis is supplied with mounting rails.

2.7.1 Weight

61 pounds (27.67kg)

2.7.2 Storage Temperature

-40°C to +80°C

2.7.3 Operating Temperature

0° to +60°C

2.7.4 Relative Humidity

Up to 95% without condensation

3.0 ORDERING INFORMATION

The following part numbers have been assigned to the BO3 system chassis and accessories:

Part Number	Description
69910	BO3 System Chassis consisting of 8 slot Version I backplane, OCU, power supply and chassis slides
69916	BO3 System Chassis as above with additional -12 volt power supply
69974	BO3 System Chassis consisting of 8 slot all Q-BUS Version II backplane OCU, power supply and chassis slides
69983	BO3 System Chassis as above with additional -12 volt power supply
69939	OCU Module
65040	Chassis Slide Set
60078	Power Supply BO3 (+5, +12)
60035	BO3 Subchassis and Version I Backplane Assembly
69981	BO3 Subchassis and Version II Backplane Assembly
69915	LSI Continuity Card

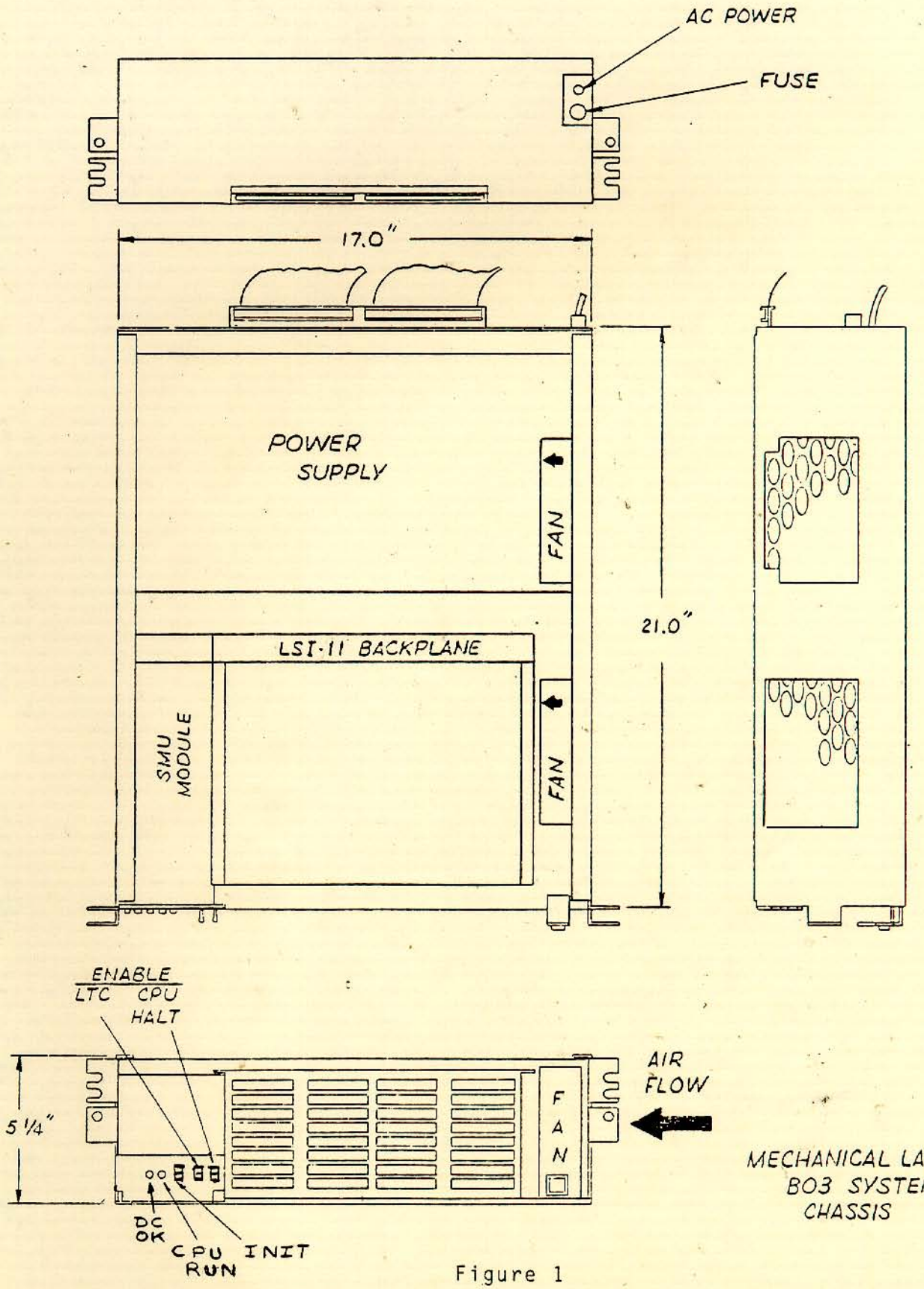
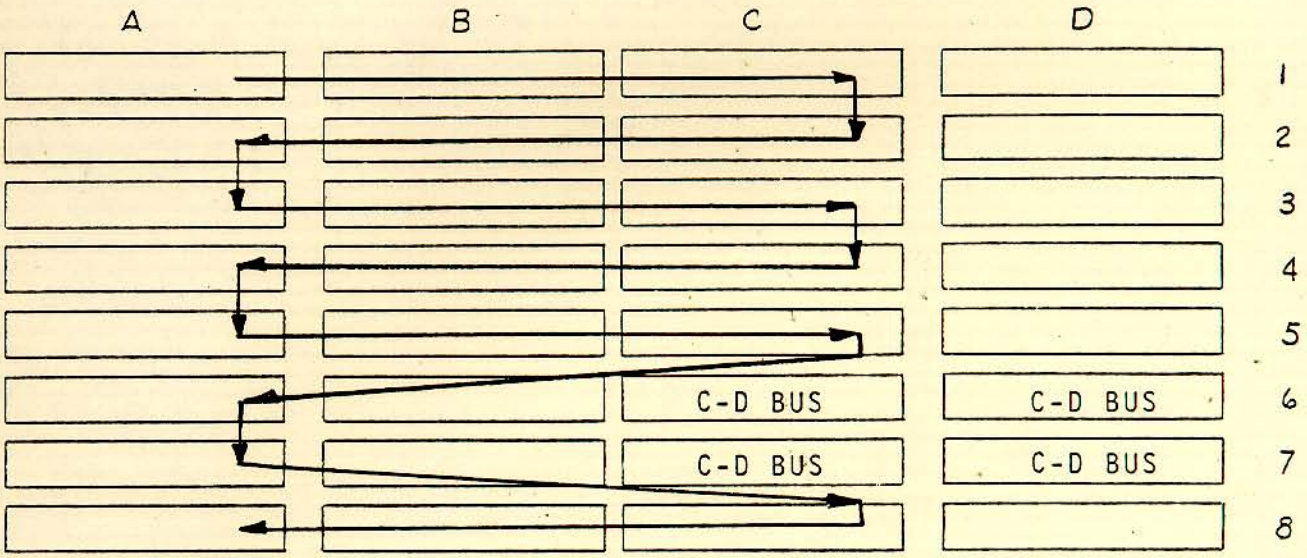

AC POWER
FUSE
17.0"
POWER SUPPLY
FAN
21.0"
LSI-11 BACKPLANE
SMU MODULE
FAN
ENABLE
LTC CPU
HALT
AIR FLOW
5 1/4"
F A N
DC OK
CPU RUN
INIT
MECHANICAL LAYOUT
BO3 SYSTEM
CHASSIS

Figure 1

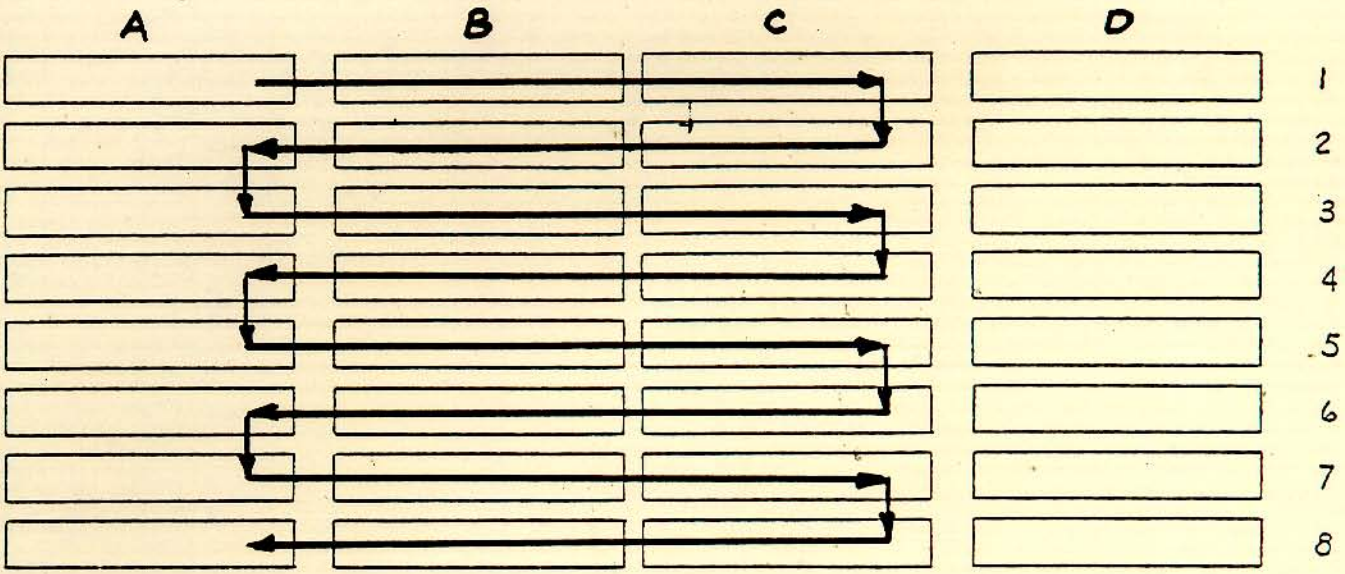


LSI-11 BACKPLANE (VERSION I)
FRONT VIEW

NOTES:

1. Quad LSI-11 (KD11-F) should be installed in slot 1.
2. Dual LSI-11 (KD11-HA) or LSI-11/23 (KDF11-AA) should be installed in connectors A and B of slot 1.
3. LSI-11 BUS is wired on A and B connectors of all slots and C and D connectors of slots 1-5 and 8. C and D connectors of slots 6 and 7 are wired with C-D Bus.
4. RLV11-AK controllers should be installed in slots 6 and 7.
5. Do not install DRC DR-115 core memory or DEC MMV11-A core memory in slots 6 or 7.

Figure 2



LSI-11 BACKPLANE (VERSION II)
FRONT VIEW

NOTES:

1. Quad LSI-11 (KD11-HF) should be installed in slot 1.
2. Dual LSI-11 (KD11-HA) should be installed in connectors A and B of slot 1.
3. LSI-11 BUS is wired on A and B connectors and C and D connectors of all slots.

Figure 3

DOCUMENTATION

The following assembly drawings, schematic diagrams, and bills of material are contained in this manual.

Document Number	Title
69910	Assembly Drawing B03
69910	Bill of Materials B03 with Version I Backplane
69916	Bill of Materials B03 with Version I Backplane and -12V
69974	Bill of Materials B03 with Version II Backplane
69983	Bill of Materials B03 with Version II Backplane and -12V
69939	Assembly - OCU
69939	Bill of Materials - OCU
03250	Schematic Diagram OCU
60078	Outline/Mounting Power Supply
03365	Schematic Diagram
03209	Schematic Diagram B03 Backplane Version I
65027	Assembly Backplane B03 Backplane Version I
65027	Bill of Materials B03 Backplane Version I
03341	Schematic Diagram B03 Backplane Version II (ALL-Q-BUS)
69984	Bill of Materials B03 Backplane Version II (ALL-Q-BUS)

REV. J

DWG. NO. 69910 SHEET 1 OF 3

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		Released to Production	FC	7-10-78
B		Drawing Number was B03201001	[illegible]	10/29/80
C		RELEASED TO DRCE	[illegible]	4/29/82
D		ECN W2861	REW	10-18-82
E		ECN W2954A	REW	10-18-82
F		ECN 3047	[illegible]	1/7/83
G		ECN 3055	[illegible]	1/7/83
H		ECN 3098 R. P.		
J		ECN 3100 R. P.		

DRAWN	DATE
MAS	10-28-80
CHECKED	DATE
[illegible]	10/29/80
ENGR.	DATE
[illegible]	[illegible]
APPROVED	DATE
[illegible]	[illegible]

TITLE

BILL OF MATERIALS

FINAL ASSEMBLY - MODEL B03 SYSTEM CHASSIS (LSI-11)

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 69910

SHEET 1 OF 3

REV. J

TITLE: B/M FINAL ASSEMBLY MODEL B03 SYSTEM CHASSIS (LSI-11)

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	1	42082	CHASSIS, EXTERNAL SUBASSEMBLY, B03	
2	1	69935	CHASSIS, INTERNAL SUBASSEMBLY	
3	1	42090	COVER, TOP, B03	
4	1	42091	PANEL, REAR, B03	
5	1	42924	PANEL, FRONT	
6	1	42950	BRACKET AC SWITCH MOUNT	
7	1	42993	BRACKET STRAIN RELIEF	
8	1	42092	COVER POWER SUPPLY	
9	1	27370	CHASSIS SLIDE SET 22"	
10	1	60078	POWER SUPPLY +5V@24A +12V@8A	
11	1	14703	FAN 5¼"	
12	1	22245	EXTERNAL POWER CORD	
13	1	22915	SWITCH ROCKER LIGHTED DPDT WHT 125V 15A	
14	1	23047	FUSE HOLDER SHOCK-SAFE	
15	1	23042	FUSE "SLO-BLO" 2.5 AMP	
16	1	22296	LINE FILTER, 6 AMP, EMI	
17	2	24134	LUG RING 18-22 AWG #6	
18	1	30606	LABEL (LOGO)	
19	1	42093	BRACKET, CABLE TROUGH	
20	1	42966	BRACKET, STRAIN RELIEF, ROUND CABLE	
21	4	22297	RECEPTACLE, FASTON, SERIES 250, INS, 22-18AWG	
22	2	22298	" " " " " 14-16 AWG	
23	2	27367	BALL STUD	
24	5	24111	SPADE LUG 16-22 AWG/#6	
25	2	24144	SPADE LUG 18-14 AWG / #6	
26	1	23041	FUSE 5 AMP, SLOW BLOW	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 69910
SHEET 2 OF 3

REV J

TITLE: B/M FINAL ASSEMBLY MODEL B03 SYSTEM CHASSIS (LSI-11)

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
27	8	26614	SPACER .171 X .125 LG	
28	11	24107	CABLE TIE NYL WHT	
29	4	26446	SCR FH PHL 100° STL 6-32 x 318	
30	A/R	30618	TAPE FOAM 1/8 THK x 1/2 W ADHESIVE BACKED	
31	A/R	24123	SHRINK TUBING 1/4" BLK	
32	A/R	24620	WIRE STRD WHT TEF 18AWG	
33	A/R	24628	WIRE STRD GRN/YEL TEF 18AWG	
34	9	26346	SCR PNH PHL STL 6-32 x 3/8	
35	A/R	24610	WIRE STRD BLK TEF 18AWG	
36	2	26331	SCREW PNH PHL STL 4-40 x 7/8	
37	8	26323	SCREW PNH PHL STL 4-40 x 3/8	
38	2	26509	SCR FH PHL 100° STL 4-40 x 1/2	
39				
40	8	26504	SCREW FH PHL 100° STL 6-32 x 1/4	
41	4	26448	SCREW FH PHL 82° STL 6-32 x 3/4	
42	6	26457	SCREW FH PHL 100° STL 8-32 x 1/2	
43	2	26102	NUT HEX STL 4-40	
44	4	26103	NUT HEX STL 6-32	
45	10	26204	WASHER FLAT STL #4	
46	10	26206	WASHER INT TOOTH STL #4	
47	14	26215	WASHER FLT STL #6	
48	15	26207	WASHER INT TOOTH STL #6	
49	1	26343	SCR PNH PHL STL 6-32 x 5/8	
50	1	69939	B03/B04 OCU MODULE	
51	2	14707	PLUG IN FAN CORD	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 69910
SHEET 3 OF 3

REV.

REV.	REVISIONS				
	SYM.	SHEET	DESCRIPTION	APPROV.	DATE
	C	-	RELEASE TO DRCE	[signature]	8/2/82
	E		ECN W2954A	REW	10/18/82
	F		ECN 3098 R.A		

DWG. NO. 69916 SHEET 1 OF 2

DRAWN P.L.	DATE 5-27-82	TITLE	BILL OF MATERIALS B03 SYSTEM CHASSIS WITH ADDITIONAL -12 VOLT
CHECKED [signature]	DATE 5/27/82		
ENGR.	DATE		
APPROVED [signature]	DATE 8/2/82	DATARAM CORPORATION CRANBURY NEW JERSEY	DWG. NO. 69916 SHEET 1 OF 2 REV. F

USE B/M & ASSEMBLY 69910
WITH THE EXCEPTIONS

ITEM NO.	QTY.	CHANGE TO	REFERENCE NOTES
10	1	60072, B03 POWER SUPPLY WITH -12 VOLT MODIFICATION	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 69916
SHEET 2 OF 2
REV. F

BRUNING 40-107 11929

MF 042

REV. F

DWG. NO. 69974 SHEET 1 OF 2

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
C	-	RELEASE TO DRCE	[signature]	8/2/82
E		ECN W2954A	REW	10/18/82
F		ECN 3098 R.P		

DRAWN	DATE
P.L.	4-13-82
CHECKED	DATE
[signature]	7.30.82
ENGR.	DATE
APPROVED	DATE
[signature]	8/2/82

TITLE

BILL OF MATERIALS

B03 SYSTEM CHASSIS WITH ALL Q-BUS BACKPLANE

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 69974

SHEET 1 OF 2

REV. F

USE B/M & ASSEMBLY 69910
WITH THE EXCEPTIONS

ITEM NO.	QTY.	CHANGE TO	REFERENCE NOTES
2	1	69981, BO3 SUBCHASSIS & BACKPLANE ALL Q-BUS	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 69974
SHEET 2 OF 2
REV. F

MF 0/2

REV. F

DWG. NO. 69983 SHEET 1 OF 2

REVISIONS				
SYM.	SHEET	DESCRIPTION	APPROV.	DATE
C	-	RELEASE TO DRCE	[illegible]	8/2/82
E		ECN W2954A	RW	10/19/82
F		ECN 3098 R.P.		

DRAWN P.L.	DATE 4-13-82	TITLE BILL OF MATERIALS B03 SYSTEM CHASSIS W/ -12V OPTION Q-BUS	
CHECKED [signature]	DATE 7.30.82		
ENGR.	DATE		
APPROVED [signature]	DATE 8/2/82	DATARAM CORPORATION CRANBURY NEW JERSEY	DWG. NO. 69983 REV. F SHEET 1 OF 2

USE B/M & ASSEMBLY 69910
WITH THE EXCEPTIONS

ITEM NO.	QTY.	CHANGE TO	REFERENCE NOTES
2	1	69981, B03 SUBCHASSIS & BACKPLANE ALL Q-BUS	
10	1	60072, B03 POWER SUPPLY WITH -12 V MODIFICATION	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 69983
SHEET 2 OF 2
REV. F

BRUNING 40-107 11829

MF 042

REV. J

DWG. NO. 69939 SHEET 1 OF 4

REVISIONS				
SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		Release to Production	[illegible]	8/1/80
B		ECN W001 & W010		
C		RELEASED TO DRCE	[illegible]	11/8/82
D		ECN W2653 BL	[illegible]	4/2/82
E		ECN W2696 BL	[illegible]	6/24/82
F		ECN W2769 BL	[illegible]	6/28/82
G		ECN W2860 JG	[illegible]	7.19.82
H		ECN 3048	[illegible]	1/7/83
J		ECN 3057	[illegible]	1/7/83

DRAWN	MAS
DATE	7-24-80
CHECKED	[illegible]
DATE	[illegible]
ENGR.	
DATE	
APPROVED	[illegible]
DATE	8/1/80

TITLE

BILL OF MATERIALS

ASSEMBLY B03/04 OCU MODULE

DATARAM CORPORATION

CRANBURY NEW JERSEY

DWG. NO. 69939

SHEET 1 OF 4

REV. J

TITLE: B/M ASSEMBLY B03/04 OCU MODULE

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	9	18101	DIODE, SILICON, HIGH CONDUCTANCE	CR3-11
2	1	40767	PCB OCU MODULE B04	
3	2	18104	DIODE 1N4001	CR1,2
4	2	18402	LED RED PANEL MT	
5	10	12315	CAP CER .01µF 20%	C3,4,5,8,10,11,14,15,19,
				20
6	6	12119	CAP TANT 1.0µF 15V	C12,13,17,18,22,23
7	5	12105	CAP TANT 4.7µF 10V	C6,7,9,16,21
8	1	12117	CAP TANT 10µF 20V	C2
9	1	12114	CAP TANT 500µF 25V	C1
10	1	10621	RES CC 1/4W 4.7 OHMS 5%	R1
11	4	10108	RES CC 1/4W 220 OHMS 5%	R52-55
12	2	10164	RES CC 1/4W 330 OHMS 5%	R38,44
13	1	10111	RES CC 1/4W 470 OHMS 5%	R3
14	2	10177	RES CC 1/4W 680 OHMS 5%	R39,45
15	8	10113	RES CC 1/4W 1K OHMS 5%	R2,13,16,29,36,43,46,48
16	2	10118	RES CC 1/4W 2.2K OHMS 5%	R23,37
17	2	10121	RES CC 1/4W 4.7K OHMS 5%	R26,28
18	8	10122	RES CC 1/4W 10K OHMS 5%	R5,7,24,25,31,32,50,51
19	1	10193	RES CC 1/4W 24K OHMS 5%	R22
20	1	10626	RES CC 1/4W 15K OHMS 5%	R40
21	2	10189	RES CC 1/4W 47K OHMS 5%	R17,18
22	3	10607	RES CC 1/4W 100K OHMS 5%	R30,47,49
23	2	10622	RES CC 1/4W 200K OHMS 5%	R27,35
24	2	10623	RES CC 1/4W 240K OHMS 5%	R41,42
25	1	10628	RES CC 1/4W 750K OHMS 5%	R15

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 69939
B/M
SHEET 2 OF 4

REV J

TITLE: B/M ASSEMBLY B03/04 OCU MODULE

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
26	2	10198	RES CC 1/4W 20K 5%	R4,6
27	1	10254	RES FLM 1/10W 2.00K OHMS 1%	R9
28	3	10255	RES FLM 1/10W 2.49K OHMS 1%	R8,19,21
29	1	10253	RES FLM 1/10W 5.62K OHMS 1%	R20
30	1	10256	RES FLM 1/10W 8.66K OHMS 1%	R10
31	1	10194	RES CC 1/4W 39K OHMS 5%	R34
32	1	10616	RES CC 1/4W 150K OHMS 5%	R33
33	2	16513	IC QUAD 2I/P NAND GATE 74S00	Z5,9
34				
35	1	16309	IC QUAD 2I/P NAND GATE 7438	Z6
36	2	16202	IC DUAL D BIN FF 74LS74	Z8,12
37	3	16214	IC DUAL MONOSTABLE MV 74LS123	Z7,11,14
38	3	16334	IC HEX UN BUS RCVR 8837/8T37	Z10,13,15
39	4	16375	IC DUAL VOLT COMPTR L17 393	Z1-4
40	1	20309	VOLT REG LM 340T-5	Q3
41	2	20504	XSTR FET J109	Q1,2
42	2	22935	SWITCH SPDT ON-NONE-ON LARGE PADDLE PC	SW1,2
43	1	22937	SWITCH SPDT MOM-NONE-MOM LARGE PADDLE PC	SW3
44	1	20317	VOLT. REG. TO-39 2.5 ±25 MV	Q4
45	1	23005	SOCKET IC 14 PIN	J1
46	5	22601	CONTACT MALE .025 SQ	E1-5
47	1	42949	BRACKET SWITCH/INDICATION OCU	
48	1	27356	PAD TRANSISTOR .082 THK TO-5	
49	2	26726	SPCR HEX THD AL 4-40 x .625 LG	
50	3	26204	WASHER FLAT STL #4	
51	2	27346	LENS-CLIP RED	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 69939
B/M
SHEET 3 OF 4

REV J

TITLE: B/M ASSEMBLY B03/04 OCU MODULE

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
52	4	26322	SCR PNH PHL STL 4-40 x 1/4	
53	4	26206	WASHER INT TOOTH STL #4	
54	1	26102	NUT HEX STL 4-40	
55	A/R			
56	REF	03250	SCHEMATIC OPERATORS CONSOLE UNIT B04	
57	3	26508	SCR FH PHL 100° 4-40 x 1/4	
58	1	26730	SPCR HEX THD AL 4-40 x 3/8 LG 1/4" HEX	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 69939
SHEET 4 OF 4

REV. J

REV. F

DWG. NO. 65027 SHEET 1 OF 2

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		RELEASED TO PRODUCTION		
B		PER ECN #W013	JMJ	11/26/80
C		PER ECN #W014	JMJ	11/26/80
D		RELEASED TO DRCE	BOH	4/29/82
E		ECN 3054	BOH	1/7/83
F		ECN 3080	BOH	3/31/83

DRAWN	DATE	TITLE
JW	11-4-80	BILL OF MATERIALS - ASSY. BACKPLANE B03 C-D BUS
CHECKED JMJ	DATE 11/26/80	
ENGR.	DATE	
APPROVED JMJ	DATE 11/26/80	

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 65027 REV. F
SHEET 1 OF 2

TITLE: BILL OF MATERIALS - ASSEMBLY B03 BACKPLANE C-D BUS

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE NOTES
1	1	40753	PCB BACKPLANE	
2	4	22276	CONNECTOR DUAL 4 ROW	
3	1	22104	CONNECTOR SINGLE 1 ROW	
4	2	22342	CONNECTOR WAFER 12 POSITION	P1, P2
5	1	22284	CONNECTOR HOUSING, 4 PIN, FEMALE	
6	2	42893	BAR CONNECTOR MTG	
7	4	22331	PIN, MALE PC MOUNT	
8	8	27372	SCREW, 8-32 X 5/8 FIL HEAD PHILLIPS	
9	REF	03209	SCHEMATIC, B03 BACKPLANE LSI-11	
10	1	22615	10 PIN HEADER	
11	16	26105	NUT HEX NYL WHT #4-40	

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. B/M 65027
SHEET 2 OF 2

REV. F

REV. A	REVISIONS				
	SYM.	SHEET	DESCRIPTION	APPROV.	DATE
DWG. NO. 69984 SHEET 1 OF 2	D		RELEASED TO PRODUCTION	BOH	6-17-82

DRAWN	DATE	TITLE
P.L.	4-14-82	BILL OF MATERIALS
CHECKED	DATE 5/25/82	ASSY BACKPLANE B03 - ALL Q-BUS
ENGR.	DATE 6/17/82	
APPROVED BOH	DATE 6-17-82	

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 69984 REV. D
SHEET 1 OF 2

USE B/M & ASSEMBLY 65027
WITH THE EXCEPTIONS

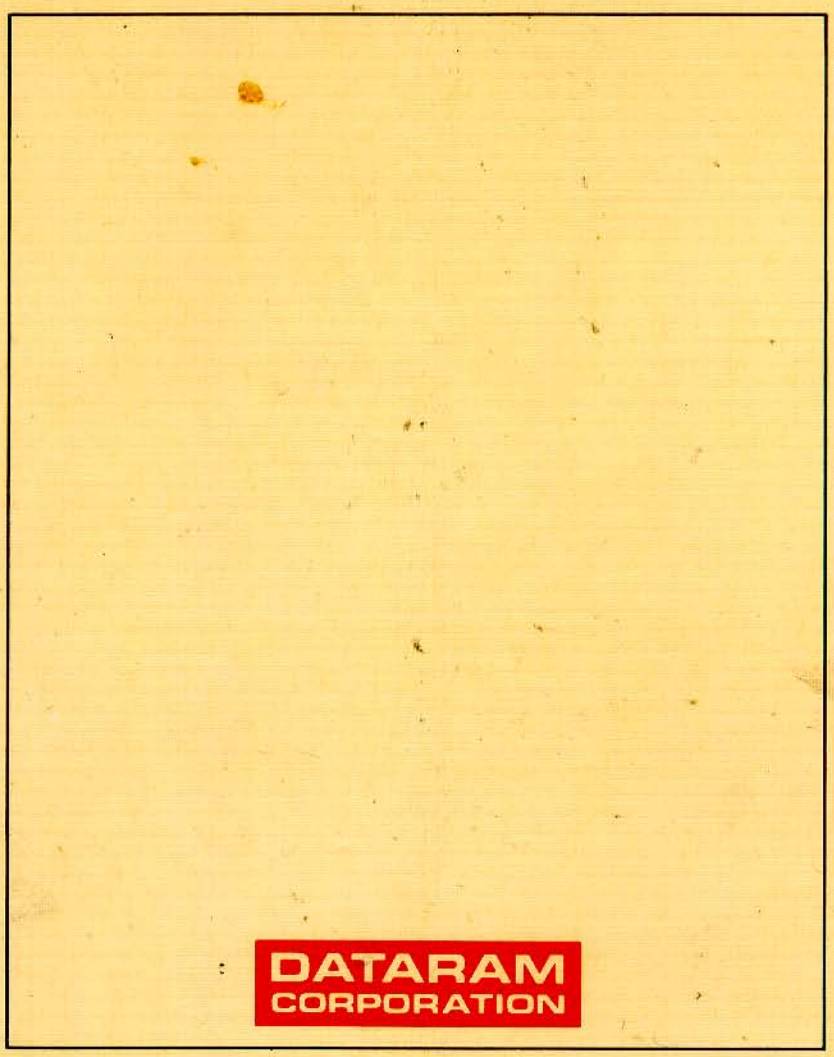
ITEM NO.	QTY.	CHANGE TO	REFERENCE NOTES
1	1	40834, PCB B03 BACKPLANE - ALL Q-BUS	
9	REF	03341, SCHEMATIC, B03/B04 BACKPLANE - ALL Q-BUS	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 69984
REV. D
SHEET 2 OF 2

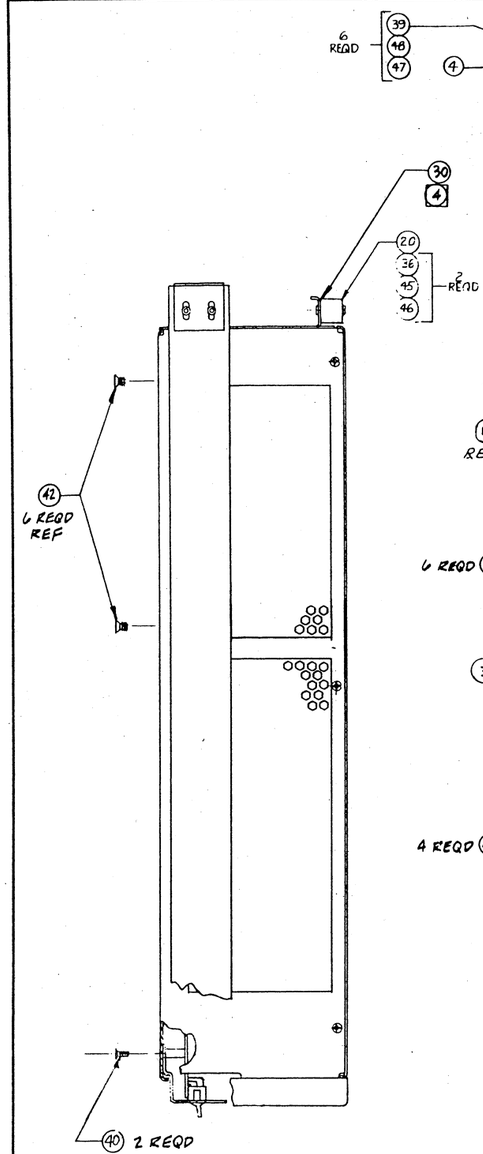
BRUNING 40-107 11829

MF 042

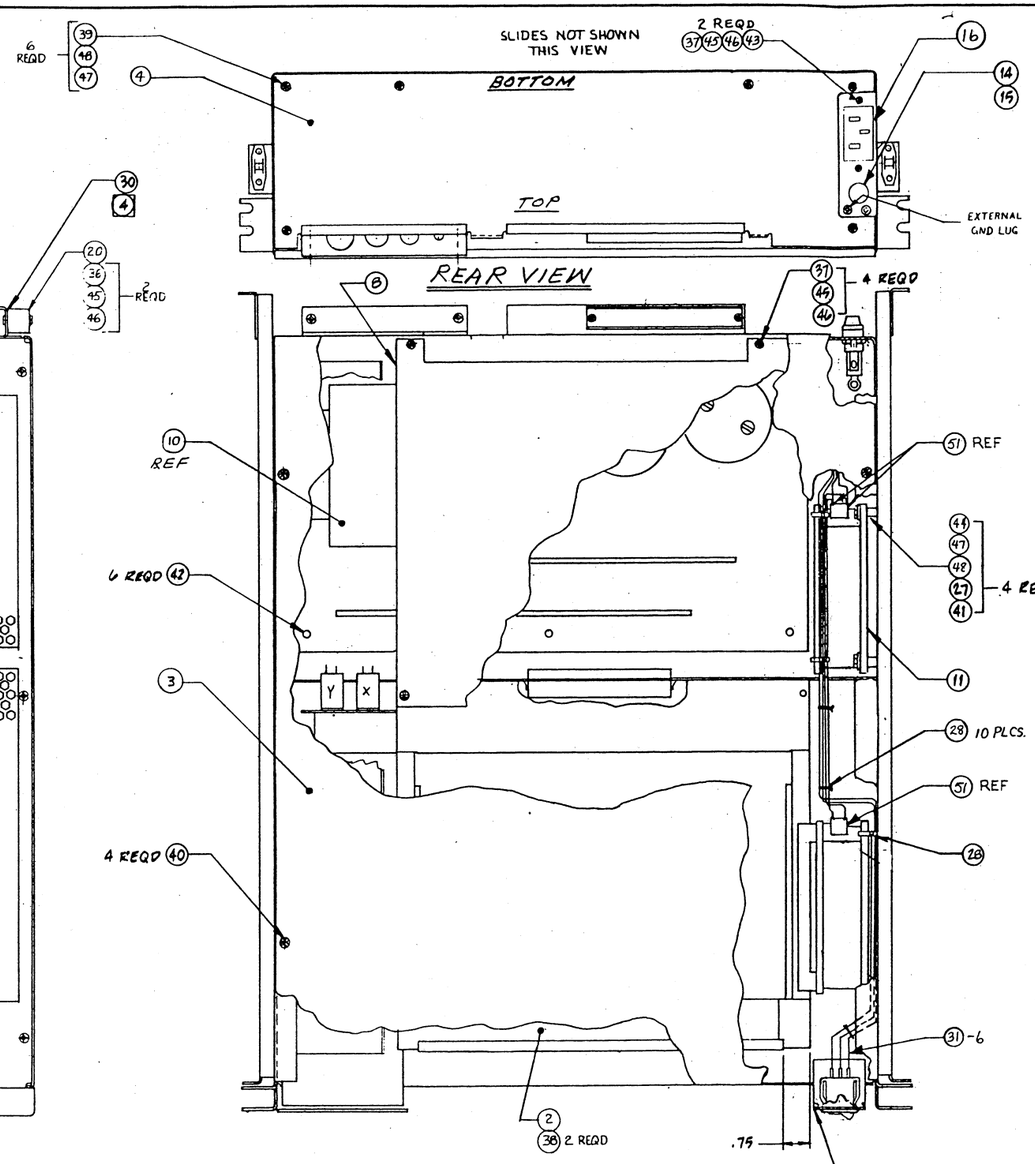


Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

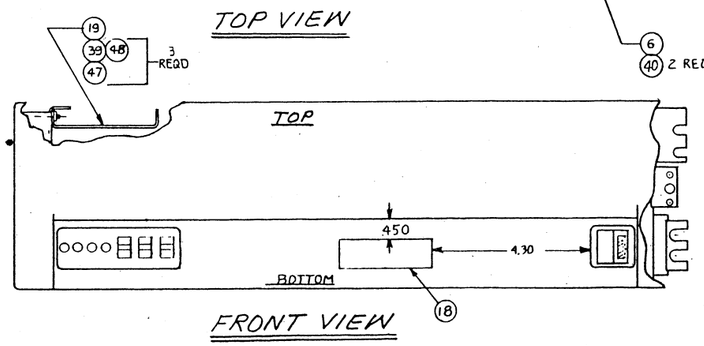
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION		
	B	WAS DWG. NO. B03201001		
	C	DRCE RELEASE	4/28/82	[illegible]



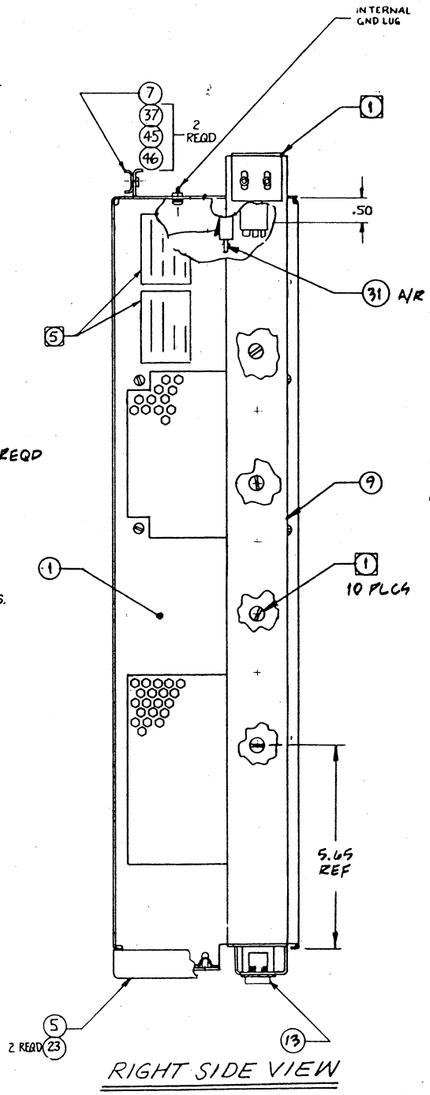
LEFT SIDE VIEW



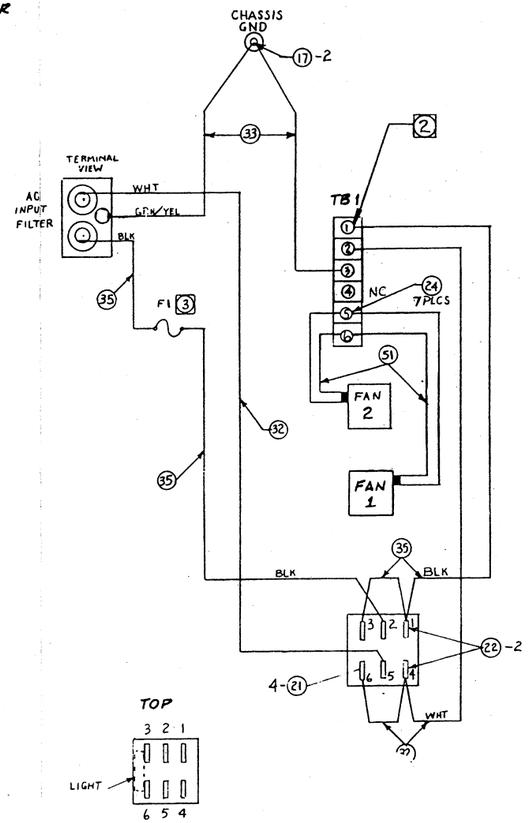
TOP VIEW



FRONT VIEW



RIGHT SIDE VIEW



AC POWER SWITCH (ITEM 13)
REAR VIEW

LABEL 1	LABEL 2
DATARAM CORPORATION	DATARAM CORPORATION
B03 CHASSIS P/N 69910 REV___ S/N_____ "DATE CODE"_____	110-120/220-240 5A/2.5A 60HZ/50HZ 500W

5

4. APPLY FOAM TAPE (ITEM 30) TO BOTH SURFACES OF CABLE RELIEF ASSEMBLY.
3. USE ITEM 26, 5A, FOR 115 V OPERATION
   USE ITEM 15, 2.5A FOR 230V OPERATION
2. TB1 MOUNTED ON REAR OF POWER SUPPLY
1. ALL MOUNTING HARDWARE SUPPLIED WITH SLIDE.

NOTES: UNLESS OTHERWISE SPECIFIED

FINAL	B03
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± ___ DECIMALS .XX ± .02 .XXX ± .010 ANGLES ± ___
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	12-13-77
CHECKED	1/5/82
ENG.	
APPROVED	4/28/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

FINAL ASSEMBLY - MODEL B03
SYSTEM CHASSIS (LSI-11)

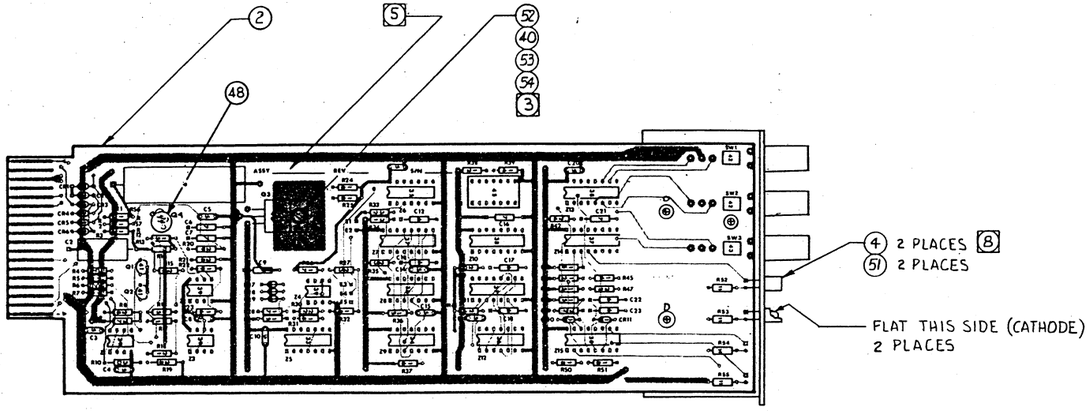
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
C	50473	69910	C

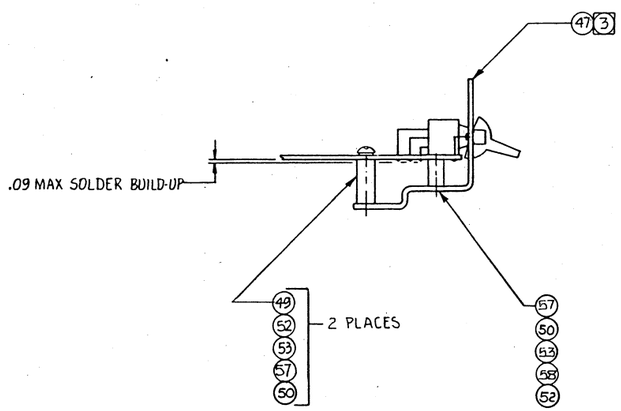
SCALE | SHEET 1 OF 1

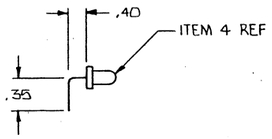
A

3 2 1

REVISIONS					
ZONE	LTR	DESCRIPTION		DATE	APPROVED
	A	RELEASED TO PRODUCTION			
	B	ECN # W001 & W010			
	C	RELEASED TO DRCE		11/8/82	
	D	ECN W2653	BL	4/12/82	
	E	ECN W2696	BL	6/14/82	
	F	ECN W2769	BL	6/29/82	
	G	ECN W2860	JG.	7.19.82	







DETAIL-A- 8
SCALE: NONE

8 SEE DETAIL -A-

6. SQUARE PADS INDICATE PIN 1 ON ALL INTEGRATED CIRCUITS, SOCKETS, POSITIVE POLARITY ON CAPACITORS, AND CATHODE ON LED'S.
5 MARK ASSEMBLY NUMBER LATEST REVISION LETTER AND SERIAL NUMBER. CHARACTERS SHALL BE .12 HIGH, PERMANENT AND LEGIBLE, COLOR BLACK.
4. COMPONENT LEAD TRIM AND SOLDER BUILD-UP AS NOTED.
3 INSTALL AFTER AFTER FLOW SOLDER.
2. COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PARTS.
1. FOR SCHEMATIC DIAGRAM SEE DRAWING NUMBER 03250.

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	USED ON
69910	
69916	
69940	
69955	

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± — DECIMALS XX ± .02 XXX ± — ANGLES ± —
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	4.25.80
CHECKED	8/Jan/81
ENG.	10-21-80
APPROVED	11/8/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY- B03/B09
OPERATORS CONSOLE
UNIT

SIZE	CODE IDENT NO.	DRAWING NO.	REV:
D	50473	69939	G

SCALE 1:1 SHEET 1 OF 1

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PROD-DATARAM PART # AT	3-3-80	
	B	PER ECN # LV 16.	10-16-80	
	C	PER ECN # W0022	2-19-81	
	D	ECN W2653 BL	4/6/82	
	E	ECN W2860 JG.	7-19-82	

ACV1 (1B6)
ACV1 ZV1
RET ZT1,ZC2
ACV2 ZV2
CR1 1N4001
CR2 1N4001
CR6 1N4607
CR5 1N4607
CR4 1N4607
CR3 1N4607
R1 4.7
R2 1K
R3 470
C1 500µf 25V
C2 10µf 25V
Q3 LM340T-5 IN OUT GND
C7 4.7µf
C6 4.7µf
C5 .01µf 25V
R21 2.49K 1%
R20 5.42K 1%
Q4 SG3503 VIN VOUT GND
VREF (1C5)(1C2) (1B6)(1B4)
R13 1K
Z2 LM393
R22 24K
+5VP
E2 E1 R34 39K R33 150K
R23 2.2K
C12 1.0µf 10V
Z7 74LS123
Z9 74S00
R37 2.2K
-17V
R25 10K
ZR1 BEVNTL
(LTC ON) (LTC OFF) SW2
Z13 8837*
Z6 7438*
R38 330
(1B4) LTC
E5 E4 E3
Z10 8837*
EVENTL ZR2
R39 680
(RUN) (HALT) SW1
R24 10K
ZP1 BHALT
+5V
R16 1K
R9 2.00K 1%
R8 2.49K 1%
R10 866K 1%
R19 2.49K 1%
R17 47K
R18 47K
(10S) VREF
+5V ZA2
C16 4.7µf 10V
.01µf 25V
+12V ZD2
Z1 LM393
R35 200K
C13 1.0µf 10V
R36 1.0K
PUR1 (1C4)
POK (1B4)
Z8 74LS574
R7 10K
R5 10K
ZB1 BPOKH
(10S) VREF
R4 20K
Q1 J109
ZA1 BDCOKH
Q2 J109
R6 20K
R40 15K
C17 1.0µf
Z11
Z12
(10Z) PUR1
R41 240K
C18 1.0µf
Z10 8837*
NC NO SW3 (INT)
7438*
R55 220
R50 10K
R48 1K
CR10 IN4607
C23 1.0µf 10V
R49 100K
J1-6
Z15 8837*
(1D5) VREF
R32 10K
R15 750K
(1D8) ACV1
R27 200K
Z4 LM393
(1D5) VREF
LTC (1C1)
R26 4.7K
POK (1D2)
Z15 (DCOK) R53 220
R29 1K
R30 100K
R28 4.7K
R31 10K
CR9 IN4607
CR8 IN4607
CR7 IN4607
R54 220
R51 10K
R46 1K
CR11 IN4607
C22 1.0µf 10V
R47 100K
J1-7
J1- 8 THRU 14
R42 240K
C21 4.7µf
R52 220
(RUN)
Z14 74LS123
R43 1K
R44 330
R45 680
SRUNL ZH1
5

5 INTEGRATED CIRCUITS MARKED WITH THIS SYMBOL, * HAVE VOLTAGE SUPPLIED BY +5V, ALL OTHERS HAVE VOLTAGE SUPPLIED BY +5VP

4 FOR 60 CYCLE OPERATION JUMPER E1 TO E2.

3. FOR ASSEMBLY DRAWING SEE DRAWING NO. B03104001.

2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.

1. CAPACITANCE VALUES ARE IN MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ± /
MATERIAL
FINISH
69939 NEXT ASSY
B03/B04 USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN H D KOGA	3-3-80
CHECKED	11-12-80
ENG.	10/16/80
APPROVED	11-26-80

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM

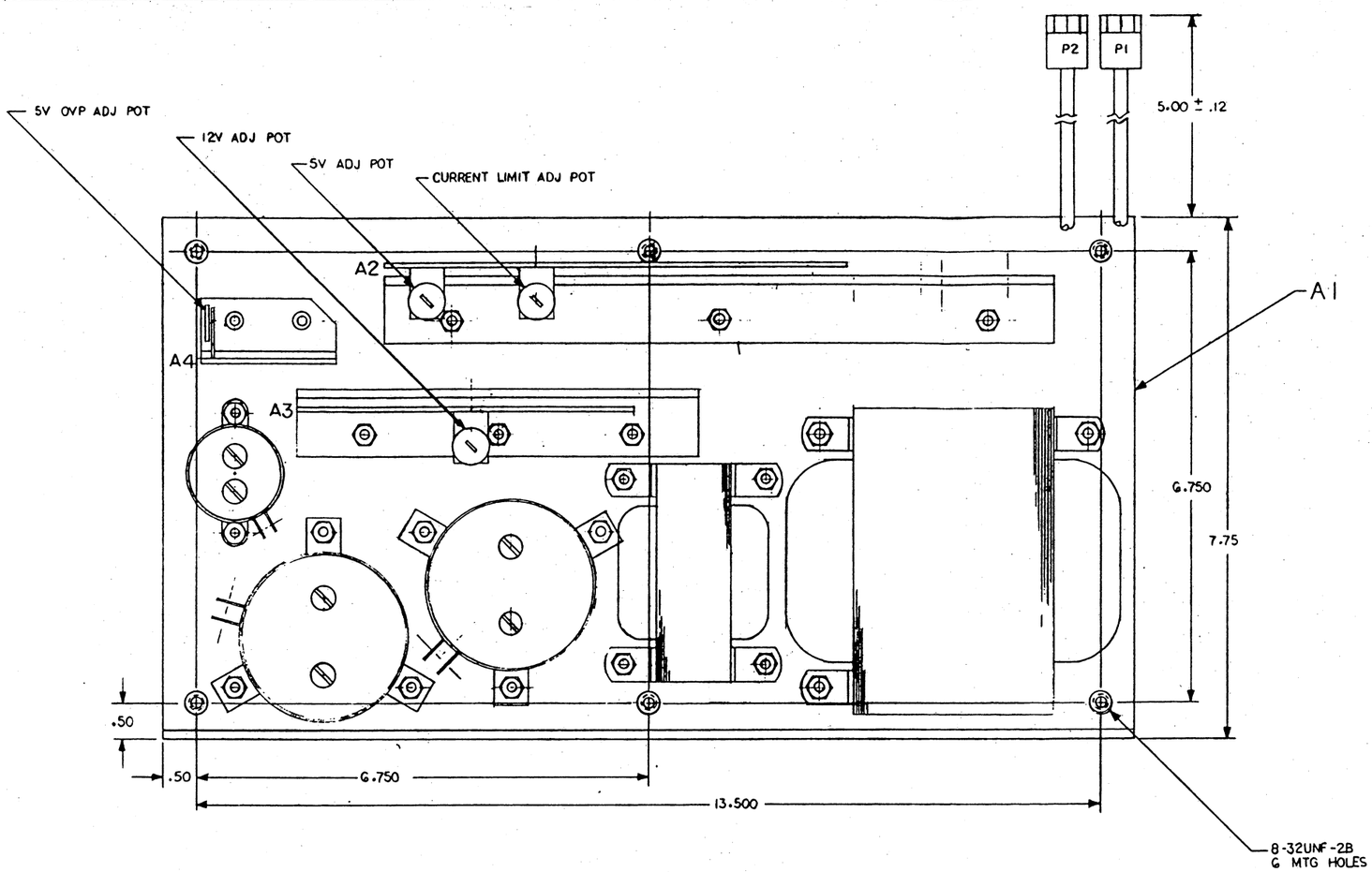
OPERATORS CONSOLE UNIT
B03/B04

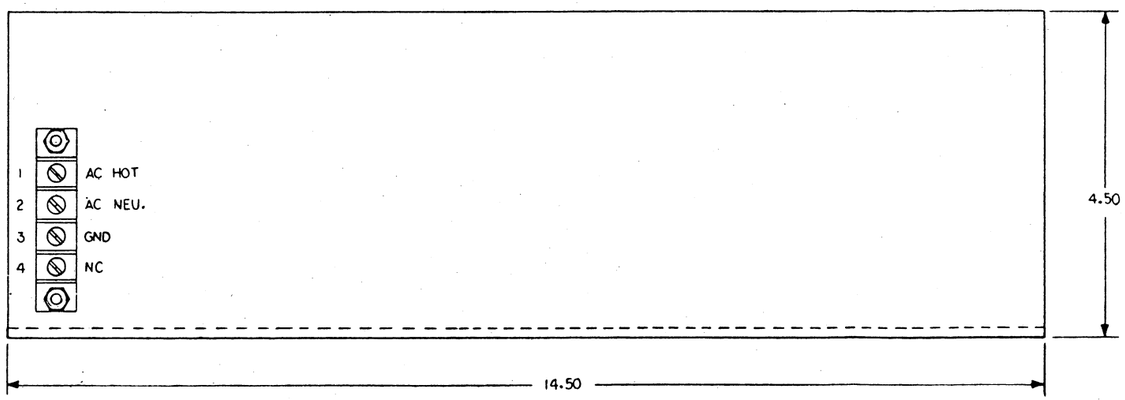
SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03250	E

SCALE NONE SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-9518

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED PER EO 2364	5-78	J.H.





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NO. REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIAL

	J. HOLLAND	12-20-77
TOLERANCES UNLESS OTHERWISE SPECIFIED	Terry Pough	12/20/77
X ± XX ± .020 XXX ± .010 ANGLES ±		

ELPAC ELEXON POWER SYSTEMS SANTA ANA, CALIF.

OUTLINE/MOUNTING

SIZE	CODE IDENT NO.	
D		60078

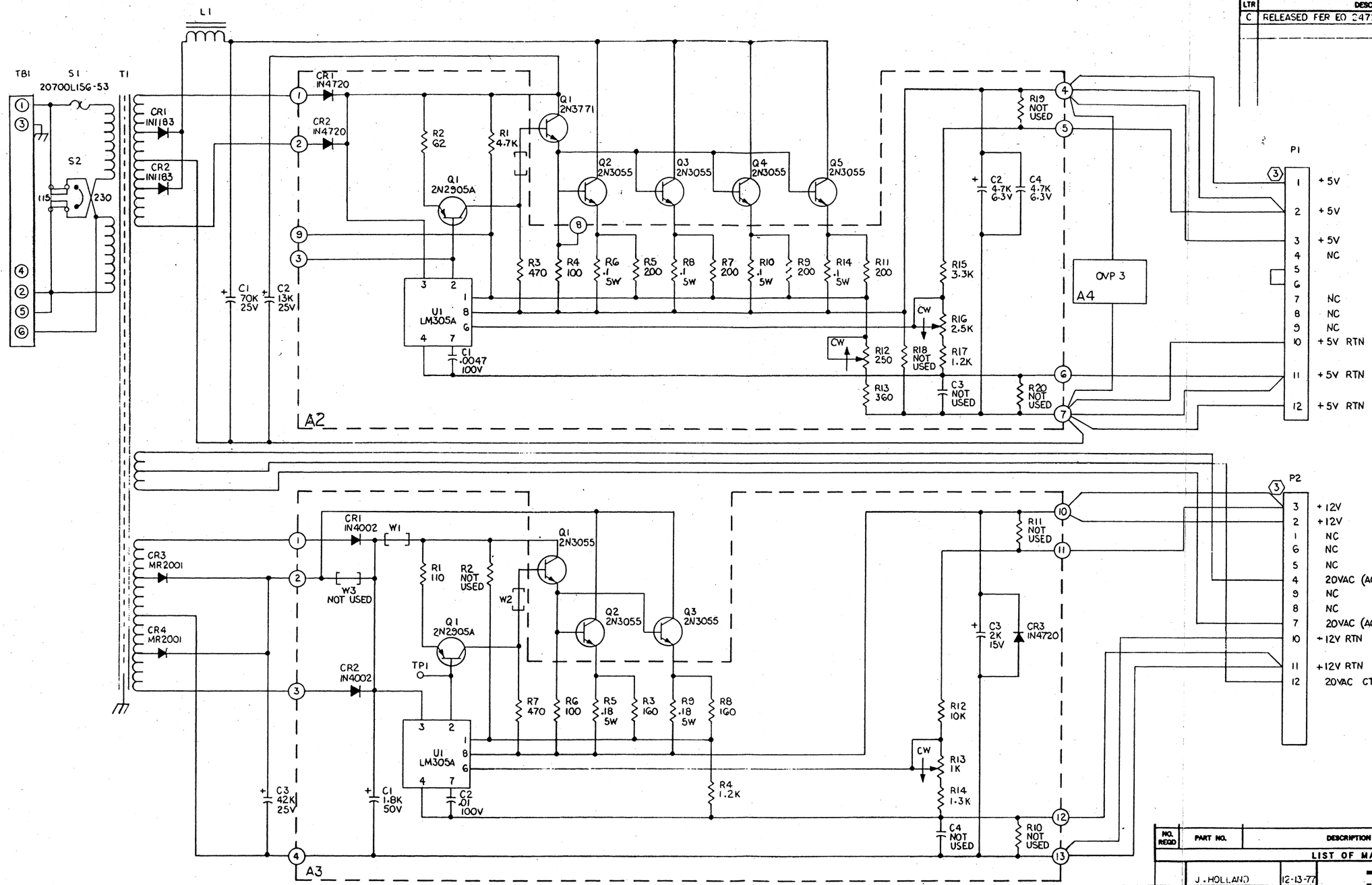
SCALE: 1/1 SHEET 1

NEXT ASSY	1GOG
APPLICATION	USED ON

REV A

6/76 COOK DRAFTING SUPPLY—ANAHEIM

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	RELEASED PER EO 2472	11-78	J.H.



(3) DENOTE MALE PIN, PINS NOT CODED ARE FEMALE
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
1. ALL RESISTOR VALUES ARE IN OHMS 1/2W, 5%
NOTES: UNLESS UNLESS OTHERWISE SPECIFIED

NO. REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIAL

J. HOLLAND	12-13-77	
Terry Gough	12/20/77	

TOLERANCES UNLESS OTHERWISE SPECIFIED
X ±
XX ±
XXX ±
ANGLES ±

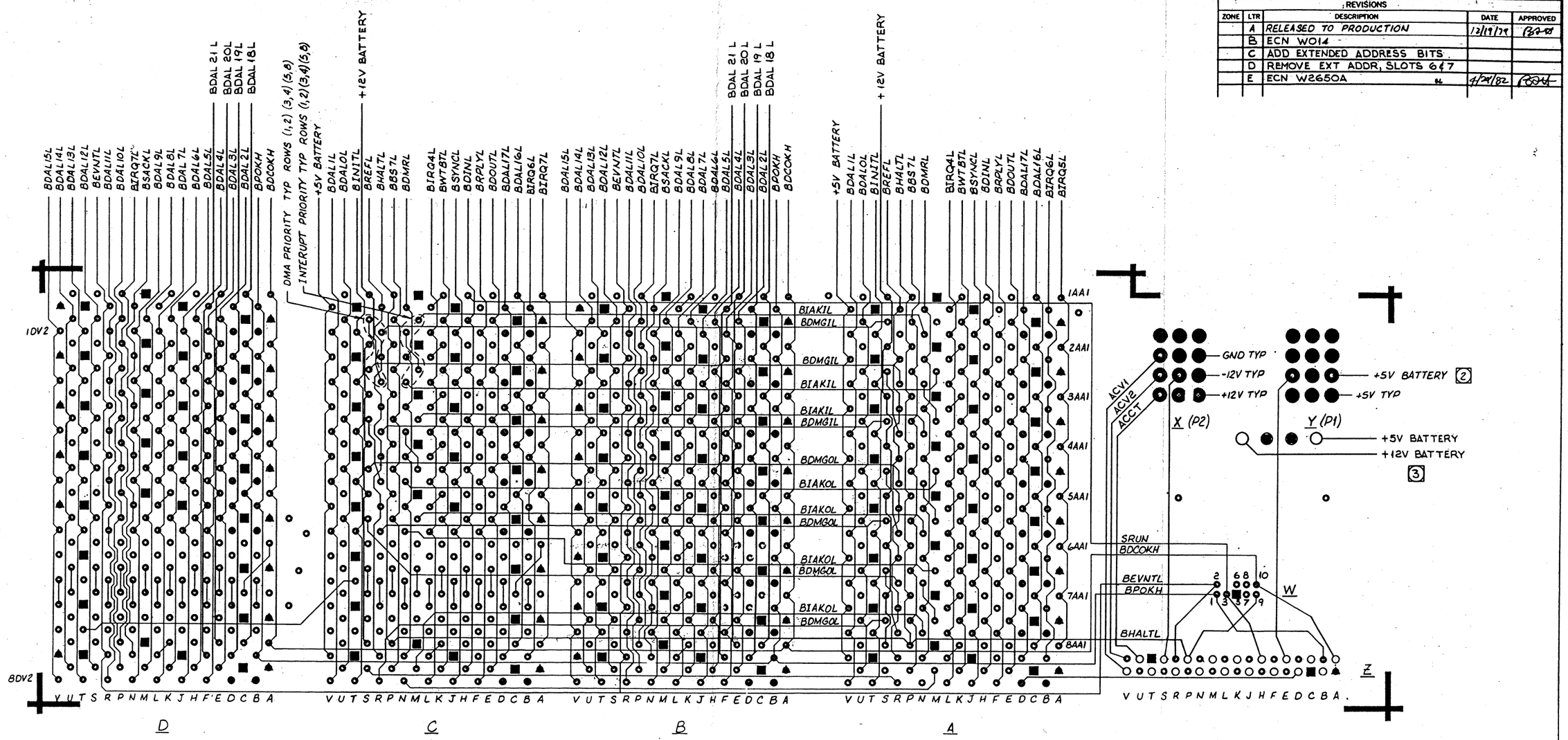
ELEXON POWER SYSTEMS
ELPAC SANTA ANA, CALIF.

SCHEMATIC DIAGRAM

NEXT ASSY	USED ON
	ICOGA
APPLICATION	

SIZE	CODE IDENT NO.	
D		03365
SCALE: NONE		SHEET 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	12/19/79	[illegible]
	B	ECN W014		
	C	ADD EXTENDED ADDRESS BITS		
	D	REMOVE EXT ADDR, SLOTS 6 & 7		
	E	ECN W2650A	4/21/82	[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. POWER AND GROUND ARE DENOTED BY THE FOLLOWING SYMBOLS:
   - ■ - DENOTES GROUND
   - ▲ - DENOTES +5V
   - ● - DENOTES -12V
   - ⊗ - DENOTES +12V
2. BATTERY CONNECTION (P1-6) NORMALLY JUMPERED TO +5V (P1-5) VIA POWER SUPPLY P1 CONNECTOR. WHEN EXTERNAL BATTERY IS USED, REMOVE POWER SUPPLY CONNECTOR JUMPER.

[3] +12V BATTERY IS NOT NORMALLY CONNECTED TO +12V.

65027	MODEL B03
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN R.J.L. WEITZ	12/13/79
CHECKED [illegible]	12/19/79
ENGR	
APPROVED [illegible]	12/19/79

DATARAM CORPORATION
CRANBURY NEW JERSEY

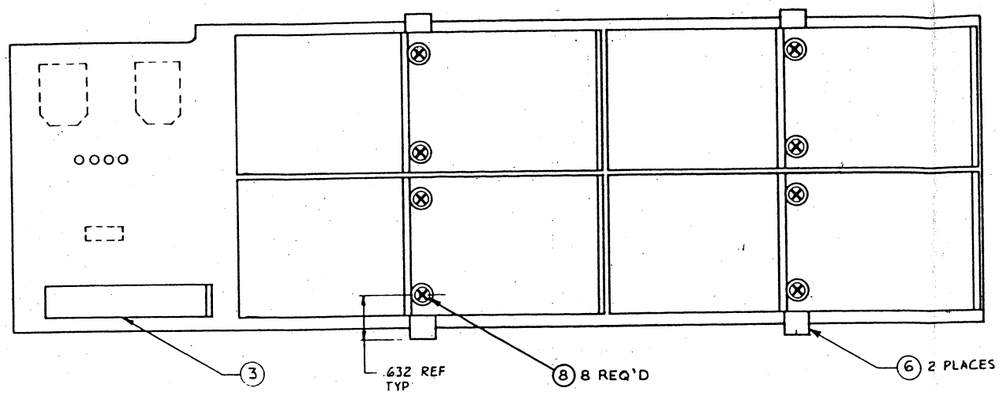
SCHEMATIC' BACKPLANE
B03 C-D BUS

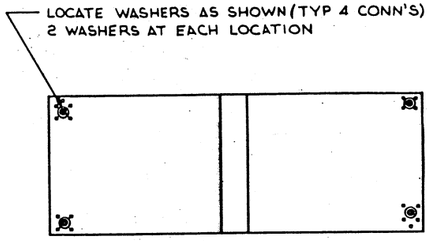
SIZE	CODE IDENT NO.	DRAWING NO.	
D	50473	03209	E

SCALE | SHEET 1 OF 1

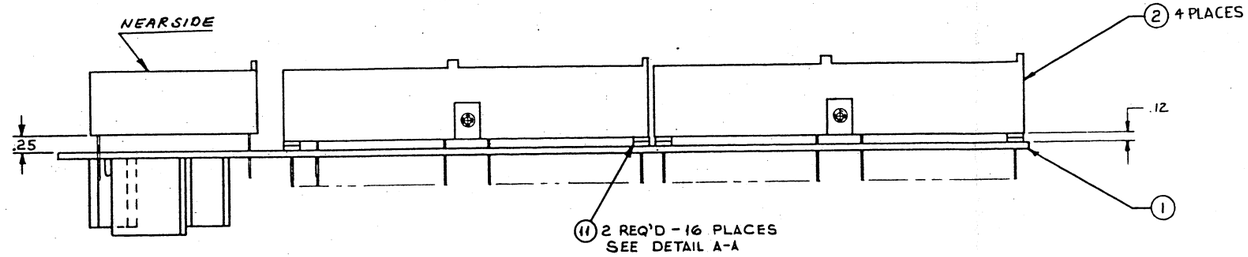
B03106002

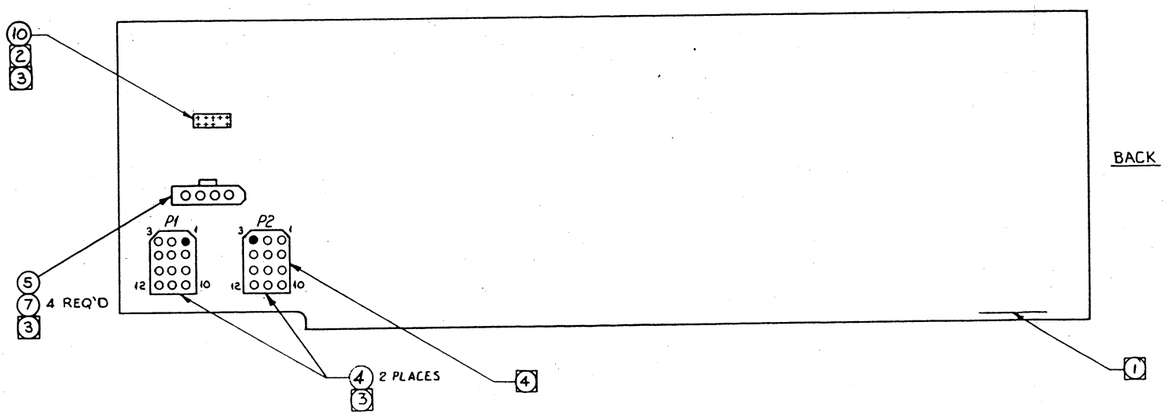
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	12/19/79	CJ-ot
	B	ECN W013		
	C	ECN W014		
	D	RELEASED TO DRCE	4/27/82	CJ-ot





DETAIL A-A
(BOTTOM VIEW ITEM 2)





4 REVERSE PINS 1 & 3 IN THIS CONNECTOR ONLY, PRIOR TO SOLDERING (● DENOTES PIN 1).

3 INSTALL AFTER FLOW-SOLDERING.

2 REMOVE PIN AS SHOWN

1 MARK WITH SER. NO. AND LATEST REV. LTR., CHARACTERS TO BE .12 HIGH PERMANENT AND LEGIBLE.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. L. WEITZ	12/13/79
CHECKED	
ENGR.	
APPROVED	4/29/82

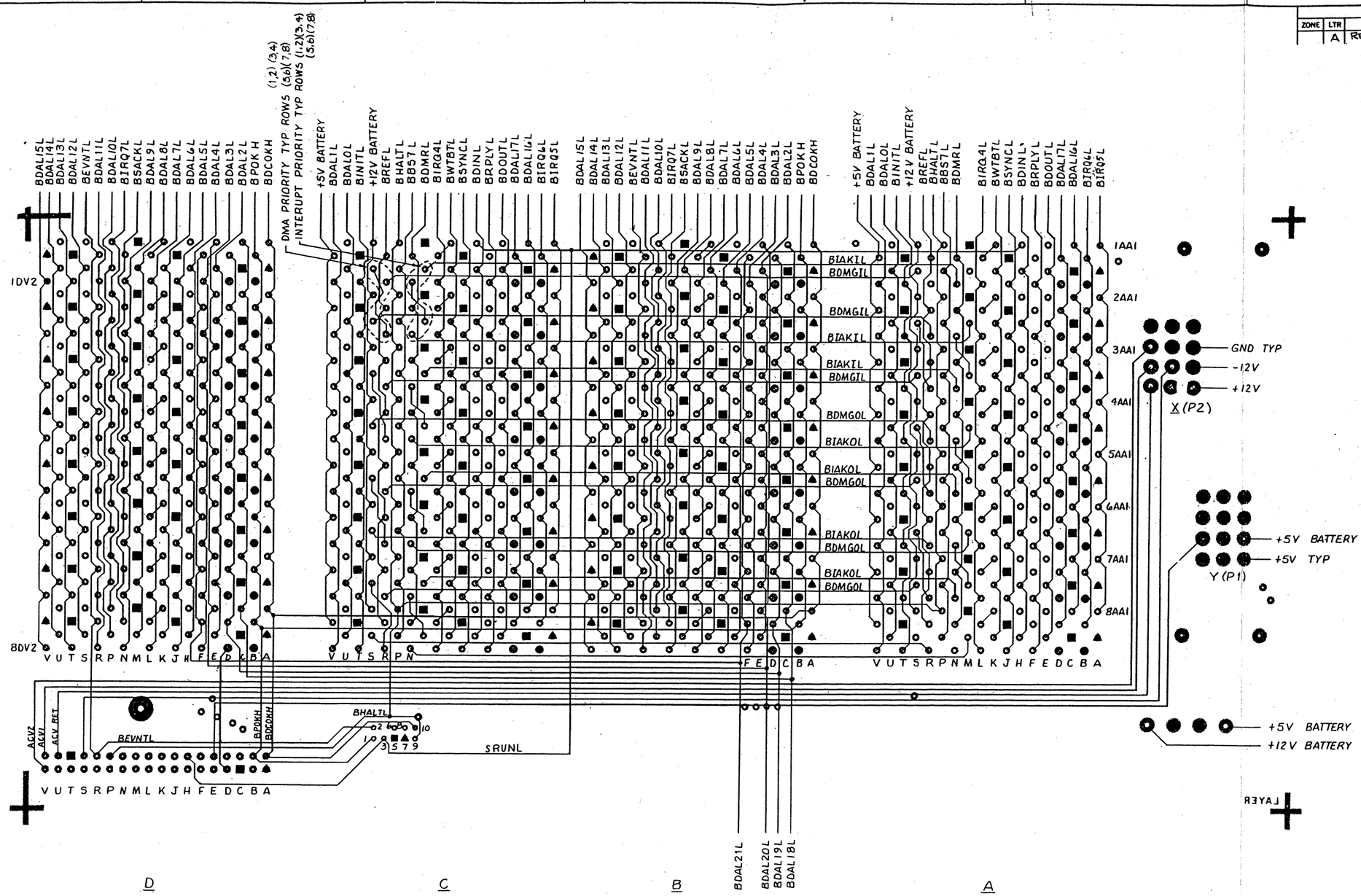
DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY BACKPLANE
B03 C-D BUS

SIZE	CODE IDENT NO.	DRAWING NO.	
D	50473	65027	D

SCALE FULL SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION DRCE	9/2/82	



NOTES: UNLESS OTHERWISE SPECIFIED

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   - ■ DENOTES GROUND
   - ▲ DENOTES +5V
   - ● DENOTES -12V
   - ⊗ DENOTES +12V
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3. +12V BATTERY IS NOT NORMALLY CONNECTED TO +12V.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .XXX ± ANGLES ± /
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN BUZZ	2-1-82
CHECKED DBP	2-27-82
ENG.	3/1/82
APPROVED	4/14/82

DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
B03/ B04 BACKPLANE ALL Q-BUS

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03341	A

SCALE | SHEET 1 OF 1