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REVISIONS DATE CHG. NO. REV	12-79	INT. RELEASE A	USED ON OPTION/MODEL		DRN. H.	DATE	TITLE: MS11-M ECC MOS MEMORY SIZE CODE NUMBER REV.									
			11/44		DARAKJIAN	31 JAN 79										
					CHK'D	DATE										
					<i>J. Manton</i>	<i>1-15-80</i>										
					PROJ. ENG.	DATE										
					J. MANTON	19 DEC 79										
					FIELD SERV.	DATE										
					<i>Steve Martel</i>	<i>JAN-9 80</i>										
			SHEET 1 OF 1													

100

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DRB 106A

[illegible]

DRB 108A

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MODIFIED HAMMING CODE MATRIX

DATA BITS

SYNDROME BITS

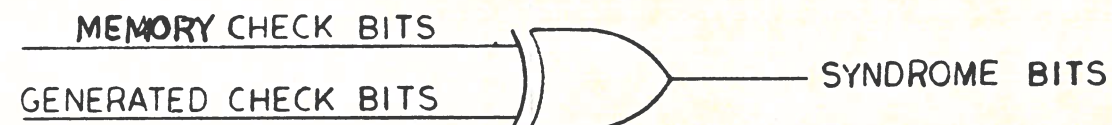
BYTE 0								BYTE 1								BYTE 2								BYTE 3								CHECK BITS									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	C ₁	C ₂	C ₄	C ₈	C ₁₆	C ₃₂	T			
	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		
		X	X			X	X			X	X			X	X			X	X			X	X			X	X			X		X		X		X		X			
				X	X	X	X					X	X	X	X				X	X	X	X					X	X	X	X				X							
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X				X						
X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X					X					
								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X						X				
X			X		X	X		X			X	X				X		X	X		X	X			X	X		X											X		

EACH CHECK BIT IS THE RESULT OF ODD PARITY GENERATED ON THE DATA BITS DESIGNATED BY X. I.E. C₁ IS $\Phi(1,3,5,7,9, \dots, 29,31)$. C₃₂ IS $\Phi(8 \text{ THRU } 31)$. THE EXCEPTION IS C_T, WHICH IS THE RESULT OF EVEN PARITY.

- SYNDROME BITS (S₁ ETC.) ARE FORMED BY A COMPARISON OF THE CHECK BITS READ FROM MEMORY AND THE NEW CHECK BITS GENERATED ON THE DATA READ FROM MEMORY.
- A SINGLE ERROR WILL CAUSE AN ODD NUMBER OF SYNDROME BITS TO GO HIGH
E.G. IF BIT 1 FAILS S₁, S₈ & S₁₆ WILL GO HIGH.
IF BIT 15 FAILS S₁, S₂, S₄, S₈ & S₃₂ WILL GO HIGH.

A DOUBLE ERROR WILL CAUSE AN EVEN NUMBER OF SYNDROME BITS TO GO HIGH.

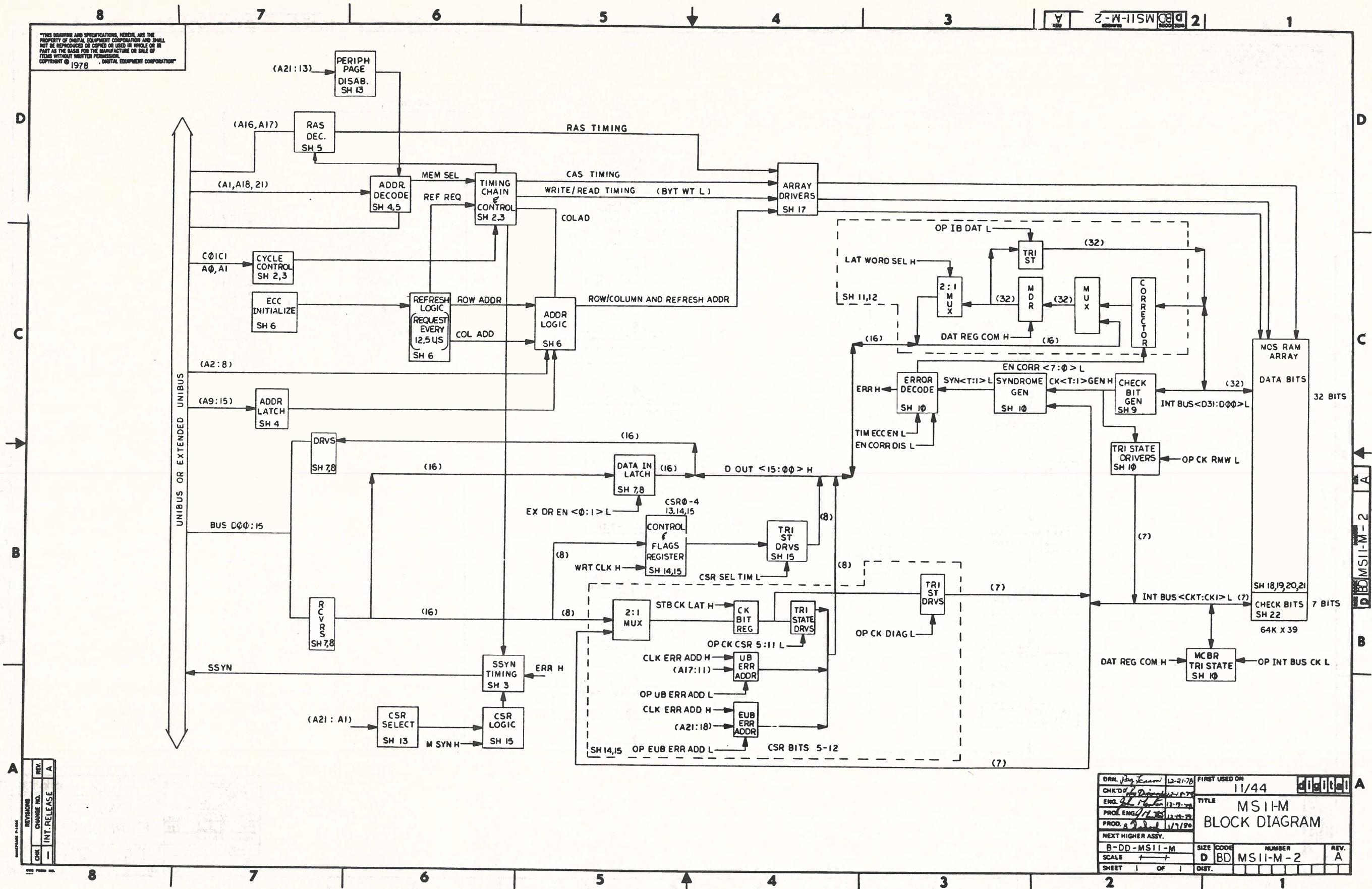
E.G. IF BITS 0 & 1 FAIL S₁ & S_T WILL GO HIGH; BUT S₈ & S₁₆ WILL NOT SINCE C₈ & C₁₆ ARE COMMON TO BITS 0 & 1 AND THE PARITY REMAINS UNCHANGED.



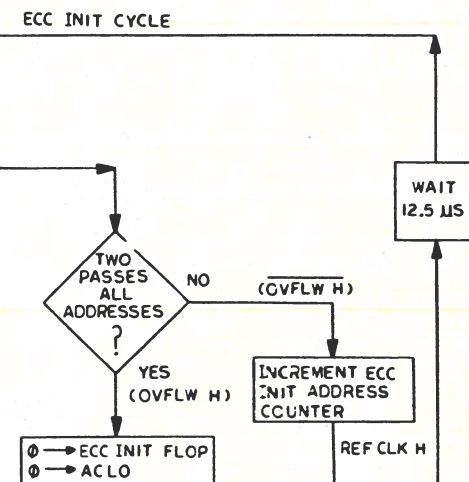
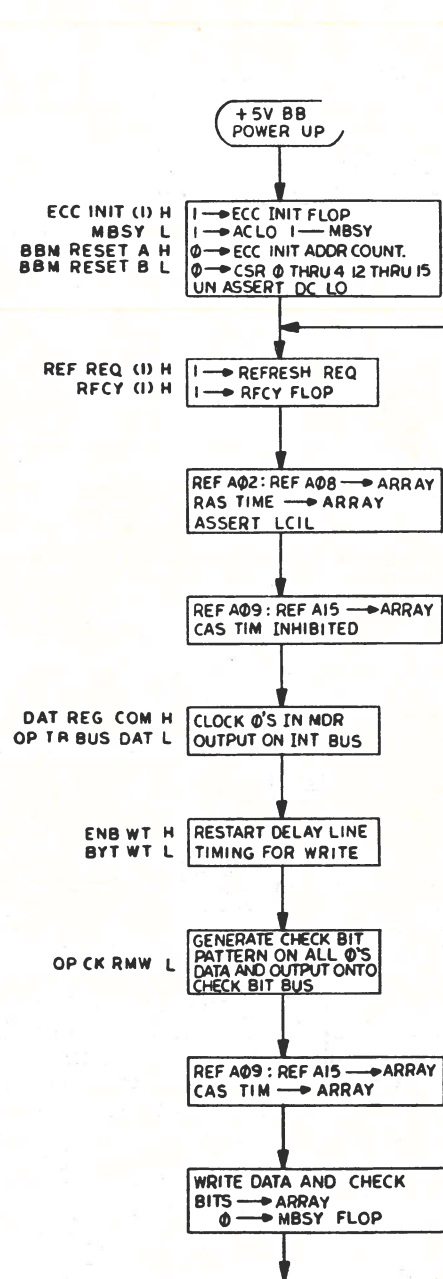
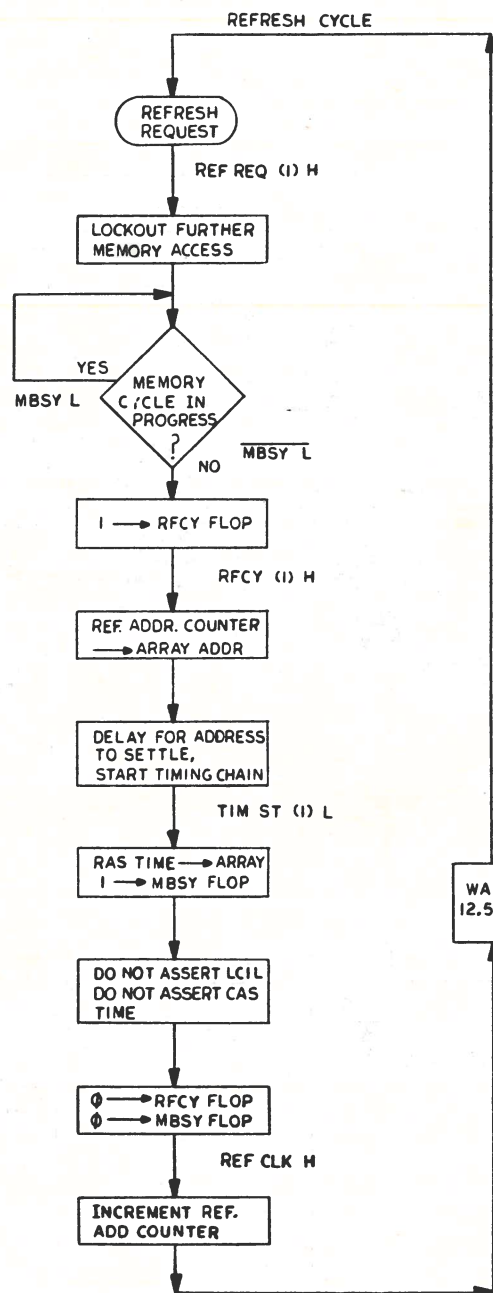
REV. NO.	INT. RELEASE
1	A

DRB 100A

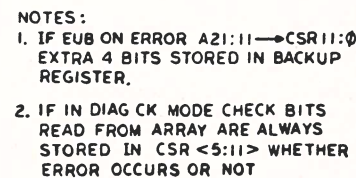
DESCRIPTION		DWG./PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			
ANGLES ± 0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES	
SURFACE QUALITY IN	MEDIUM ☐	OVER 0 TO 0.3	OVER 0.3 TO 1.3
MICROINCHES	PREFERRED ☐	OVER 1.3 TO 4.0	OVER 4.0 TO 12.0
		OVER 12.0 TO 48.0	OVER 48.0 TO 96.0
THIRD ANGLE PROJECTION	DRN. <i>Pagibanon</i> 12-22-78	FIRST USED ON	
REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D <i>By Dirigault</i> 12-20-79	11/44 digital	
DO NOT SCALE DWG	ENG. <i>J.B. Mabe</i> 12-14-79	TITLE	
MATERIAL <i>++</i>	PROD. <i>B. Schaff</i> 1/9/80	MS11-M	
FINISH <i>++</i>	NEXT HIGHER ASSY.	ERROR CHECK CODE	
	B-DD-MS11-M	SIZE	CODE
	SCALE <i>++</i>	B	BS
	SHEET <i>++</i>	NUMBER	REV.
	OF <i>++</i>	MS11-M-7	A
		DIST.	



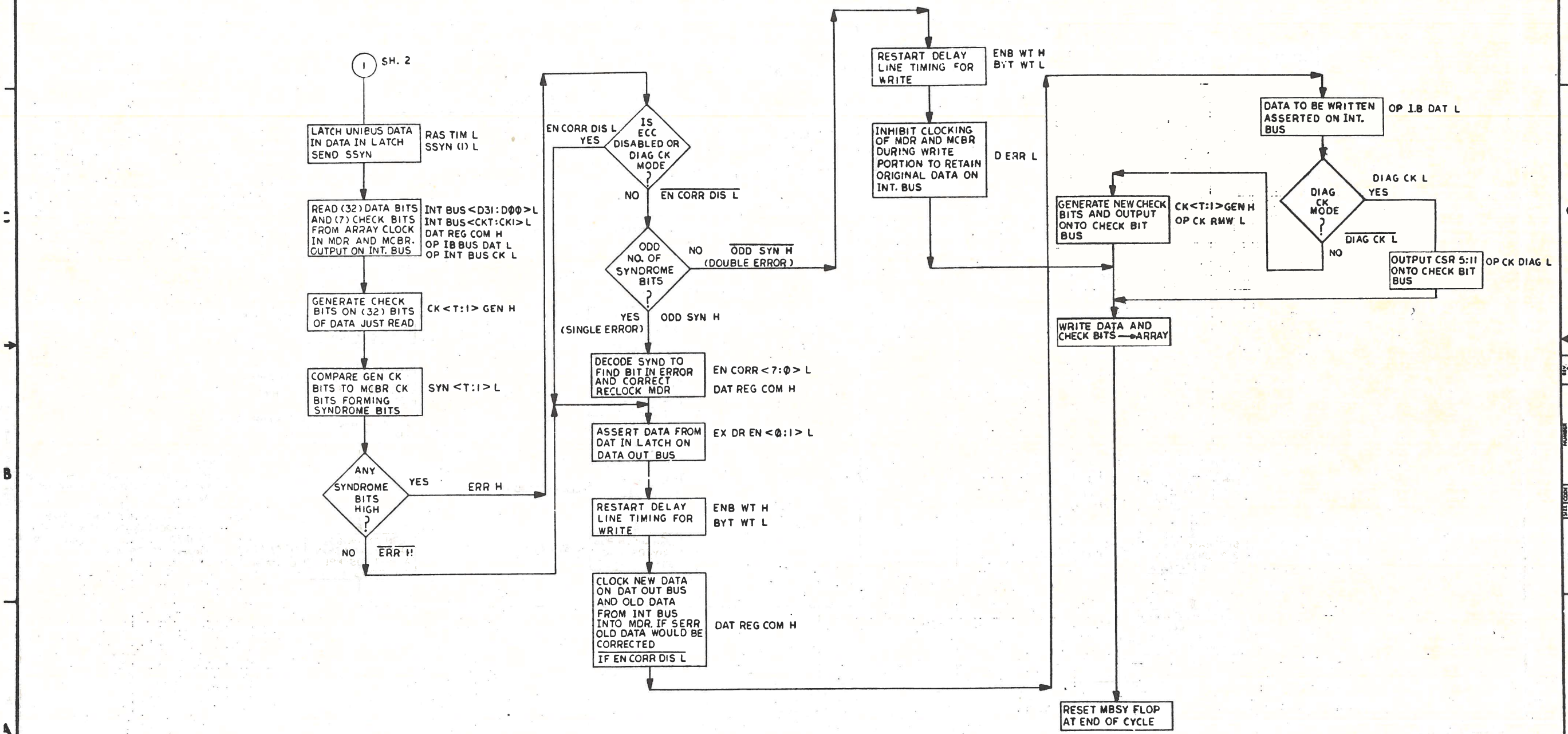
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DRN. <i>By...</i>	12-2778	FIRST USED ON	11/44
CHK'D <i>By...</i>	12-2778	TITLE	MS11-M
ENG. <i>By...</i>	12-2778	NUMBER	11/44
PROJ. ENG. <i>By...</i>	12-2778	SCALE	D
PROD. <i>By...</i>	12-2778	SHEET	1 OF 4
NEXT HIGHER ASSY.	B-DD-MS11-M	SIZE CODE	D
SCALE	1 OF 4	DIST.	
REV. A			



(DATI,DATIP CYCLE)									
TITLE MSII-M FLOW DIAGRAM				SIZE CODE D FD	NUMBER MSII-M-3			REV A	
SCALE		SHEET 2 OF 4		DIST.					



REVISIONS		
CHK	CHANGE NO.	REV.

(DATO, DATOB CYCLE)		TITLE		SIZE CODE	NUMBER		REV.
MSII-M		FLOW DIAGRAM		D/FD	MSII-M-3		A
SCALE		SHEET 3 OF 4		DIST.			

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CSR REQUEST

IS ADDRESS DECODED?

CSR ADD SEL L

CSR ADD SEL L

IS DATOUT BUS IN USE BY MEMORY CYCLE?

MEM TIM BSY L

MEM TIM BSY L

CI ASSERTED?

CIH

CIH

WRITE DATA INTO CSR

WRT CLK H
STB CK LAT H

OUTPUT FLAG AND CONTROL DATA ON DOUT BUS

CSR <04:00> H
CSR <15:13> H
CSR SEL TIM L

DIAG CK MODE?

YES
DIAG CK L

NO
DIAG CK L

SERR OR UNCORR ERR FLAG SET?

NO
CSR 15 (1) H
CSR 4 (1) H

CSR 15 (1) H + CSR 4 (1) H

ASSERT CK BIT DATA ON DOUT BUS

OP CK CSR 5-11 L

ASSERT UB ERR ADDR (A17:A11) ON DOUT BUS

OP UB ERR ADD L

ASSERT EUB ERR ADDR (A21:A18) ON DOUT BUS

OP EUB ERR ADD L

DELAY TO ALLOW DOUT BUS TO BE VALID

DEL CSR SEL TIM L

ASSERT SSYN. TURN ON UNIBUS DRIVERS IF DATI

SSYN (1) L

REVISIONS		
CHK	CHANGE NO.	REV.

(CSR READ AND WRITE)

TITLE MS11-M
FLOW DIAGRAM

SIZE CODE DFD

NUMBER MS11-M-3

REV. A

SCALE 1 OF 4

SHEET 4 OF 4

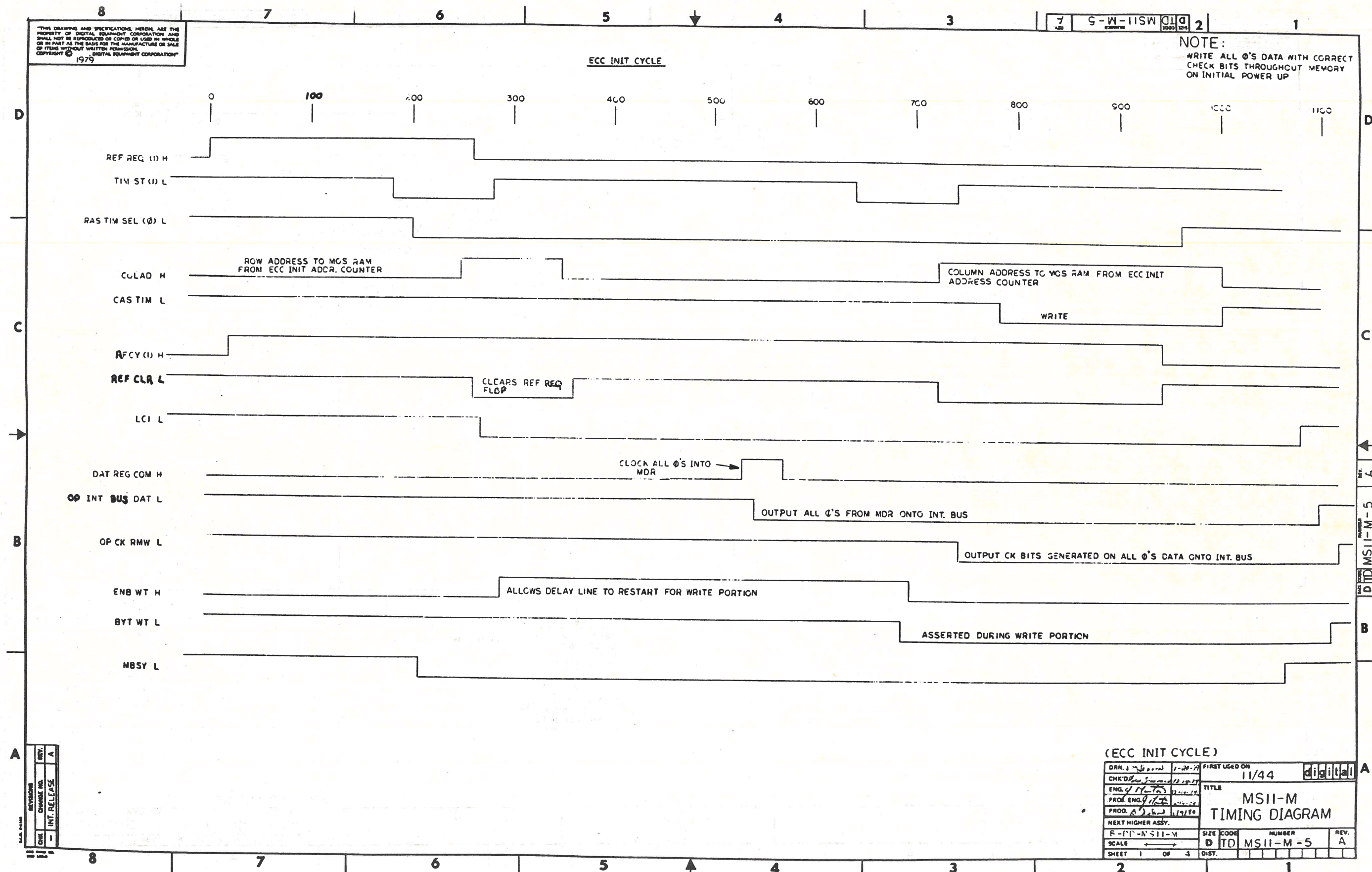
DIST.

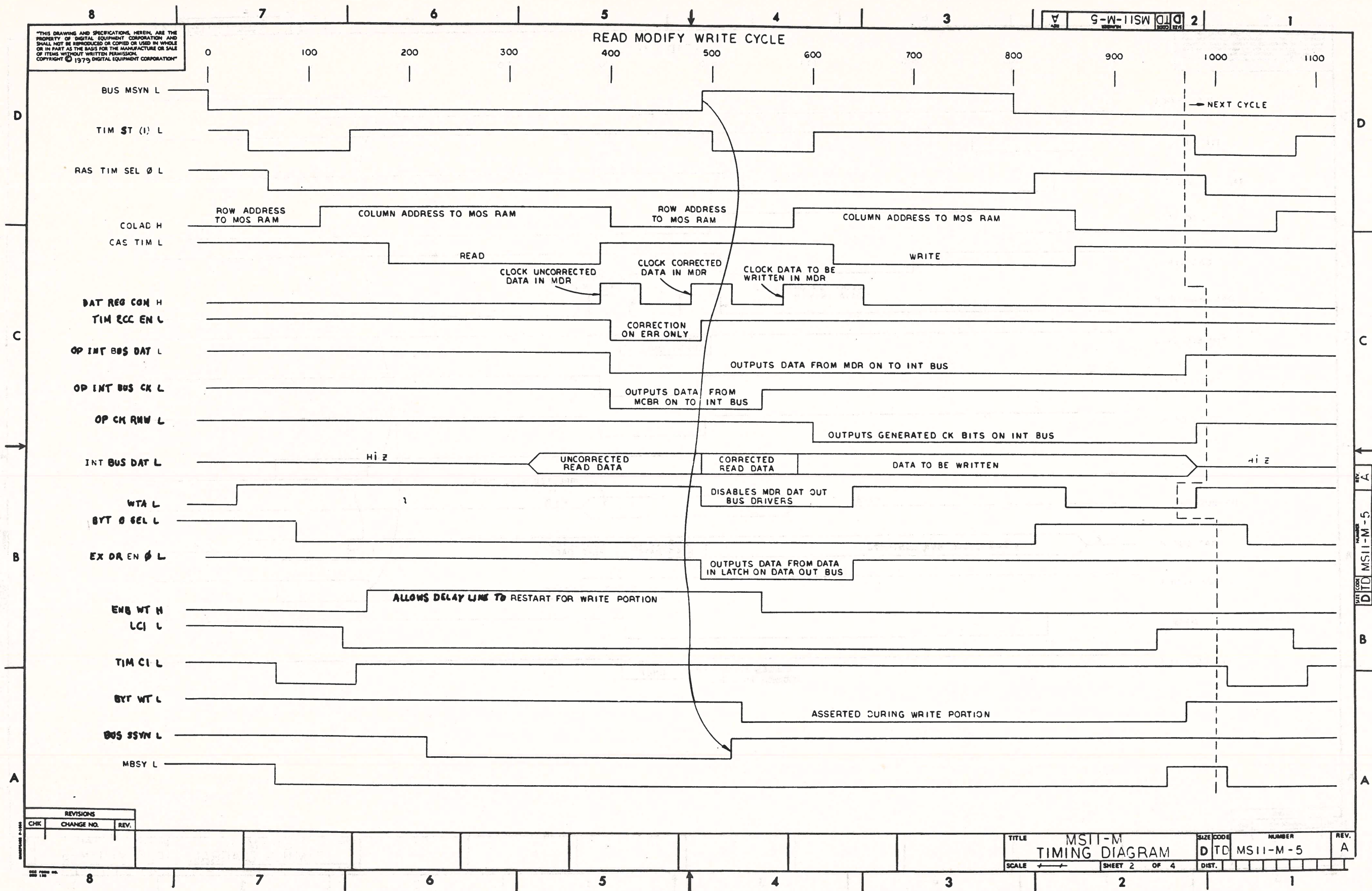
1

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NOTE:

WRITE ALL 0'S DATA WITH CORRECT
CHECK BITS THROUGHOUT MEMORY
ON INITIAL POWER UP





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9-W-11SW 2

READ CYCLE

BUS MSYN L

TIM ST (I) L

RAS TIM SEL Ø L

COLAD H

CAS TIM L

DAT REG COM H

TIM ECC EN L

OP IB DAT L

OP IB CK L

WTA L

INT BUS DAT L

DAT OUT H

BUS SSYN L

MBSY L

CLK CSR5-11 L

CLOCK UNCORRECTED
DATA IN MDR

CLOCK CORRECTED
DATA IN MDR

CORRECTION ON
ERROR ONLY

CORRECTED READ DATA

PREVIOUS CYCLE MDR CONTENTS

UNCORRECTED
READ DATA

CORRECTED
READ DATA

NO ERROR

ERROR

CLOCKS ERROR
ADDRESS IN CSR

ERROR ONLY

REVISIONS
CHK CHANGE NO. REV.

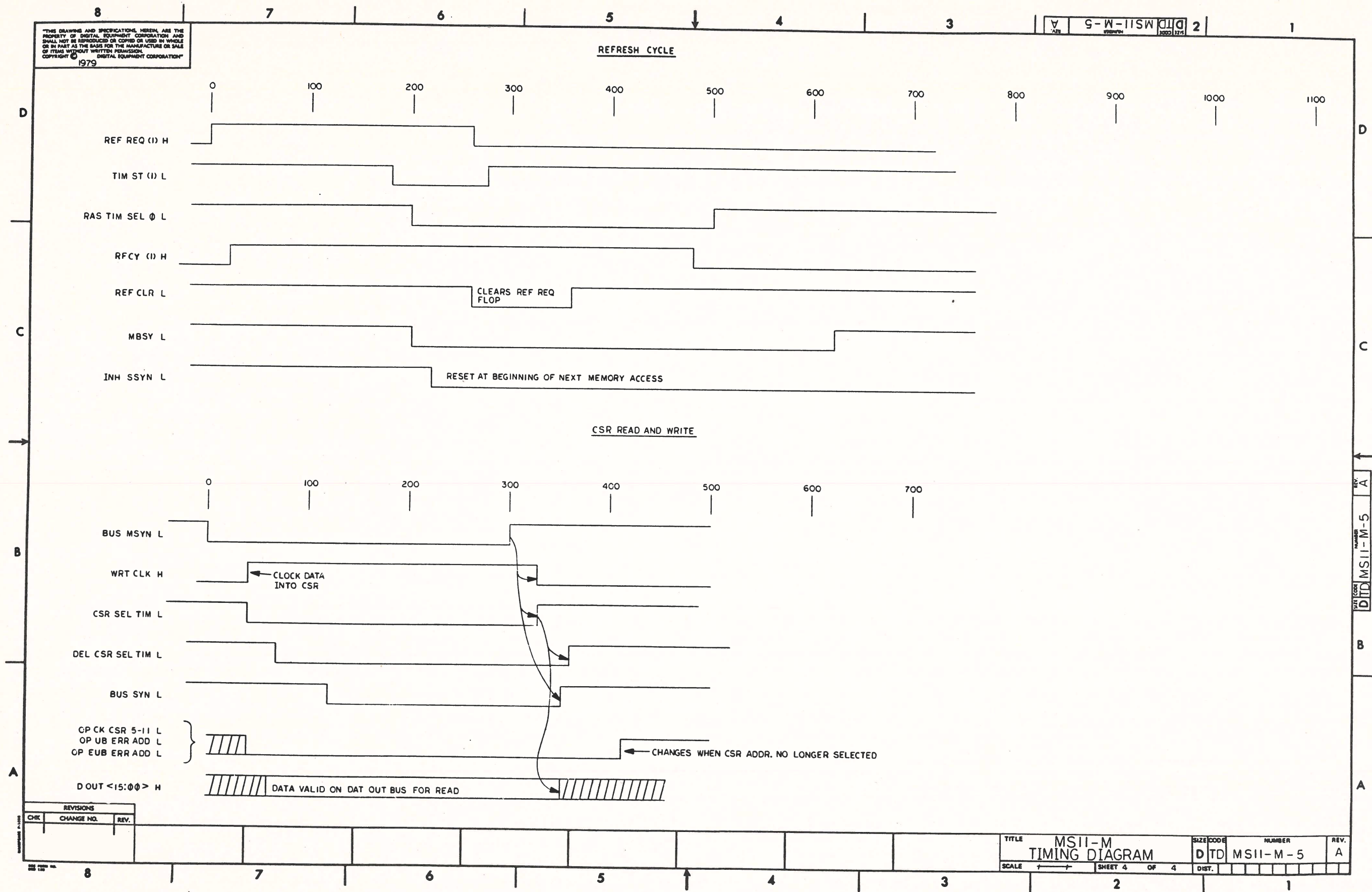
TITLE MS11-M
TIMING DIAGRAM

SIZE CODE DTD MS11-M-5

NUMBER
REV. A

SCALE SHEET 3 OF 4

DIST.



[illegible]

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION			REFERENCE DESIGNATOR
					BB	BC	BF	
1	1		5013505-00	128K ECC UNIBUS MEM ETCH CIR. BD	1	1	1	
2	2		1012219-00	47 MFD 30V +75-10% AL EL	2	2	2	C400,C401
3	3		1012121-00	220.0 MMF 100V 1%200PPM MICA	4	4	4	C1,C3,C4,C7
4	4		1001610-00	.01 MFD 50V +80-20% Z5U CER	33	33	33	C2,C111-C131,C220-C230
5	5		1012084-01	8 MFD 25V +75-10% AL EL	5	5	5	C100-C103,C200
6	6		1010279-01	.47 MFD 25V 20% CER	101	101	101	C210-C214,C310-C357,C410-C457
7	7		1110994-00	1N 751A VZ= 5.1 5% .40W	1	1	1	D5
8	8		1109991-00	1N 754A VZ= 6.8 5% .40W	1	1	1	D4
9	9		1104860-00	*** THIS ITEM IS NOT USED ***	-	-	-	
10	10		1110324-00	LED 1MCD@10MA PIV=3	1	1	1	D2
11	11		1114384-00	LED 105MW 35MA GREEN	1	1	1	D3
12	12		1210711-02	/REPLACED BY 12-16988-02	1	1	1	
13	13		1211164-04	SW,DIP 08POS/1PST 5VDC100MA F	1	1	1	E46
14	14		1211164-00	SW,DIP 4POS/1PST 5VDC100MA F	1	1	1	E61
15	15		1302124-00	18.0 .25 W 5.0 % CC	2	2	2	R7,R31
16	16		1301890-00	560.0 .25 W 5.0 % CC	1	1	1	R2
17	17		1304863-00	316.0 .25 W 1.0 % RN55D-F10	2	2	2	R11,R12
18	18		1301424-00	*** THIS ITEM IS NOT USED ***	-	-	-	
19	19		1300447-00	4.70 K .25 W 5.0 % CC	11	11	11	R10,R13,R14,R18-R20,R22-R24,R26,R30
20	20		1300316-00	470.0 .25 W 5.0 % CC	1	1	1	R21
21	21		1300365-00	1.0 K .25 W 5.0 % CC	1	1	1	R15
22	22		1300309-00	*** THIS ITEM IS NOT USED ***	-	-	-	
23	23		1300229-00	100.0 .25 W 5.0 % CC	1	1	1	R5
24	24		1301972-00	270.0 .25 W 5.0 % CC	2	2	2	R27,R28
25	25		1300202-00	47.0 .25 W 5.0 % CC	1	1	1	R29
26	26		1300444-00	3.90 K .25 W 5.0 % CC	1	1	1	R4
27	27		1311594-00	30.10 K .25 W 1.0 % RN55D-F10	1	1	1	R6
28	28		1315339-00	R NETWORK 4-5K 5.0 % 5PIN	3	3	3	R100-R102
29	29		1316187-00	R NETWORK 3-18 5.0 % 6PIN	8	8	8	R200-R207

REVISION HISTORY			BASIC PART NO: M8722			DRN: J.LIZOTTE			DATE: 14-DEC-78			D I G I T A L		
ENG	ECO NUMBER	REV	SECTION A OF A			CHK'D: D.CARUSSO			DATE: 14-DEC-78			TITLE PARTS LIST		
---	INITIAL	B	SECTION VARIATION INDEX			DES.ENG: J.MANTON			DATE: 14-DEC-78			ECC MOS MEMORY		
A.Z	M8722-ML004	D	[A] BB,BC,BF											
			[B]											
			[C]											
			[D]											
			[E]									DOCUMENT NUMBER		
			[F]			RESP.ENG.: J.MANTON			DATE: 14-DEC-78			SIZE CODE NUMBER REV		
			[H]											
			[J]											
			[K]			MFG.ENG.: R.SCHAAF			DATE: 14-DEC-78			K PL M8722-BA-DBP D		
			[L]											
			[M]			ASSEMBLY NUMBER:			TOP DOCUMENT NUMBER:			FILE NAME: EDIT #		
			[N]			D-UA-M8722-0-0			B-DD-M8722-0			Z0472D.PLS 7		
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ML2

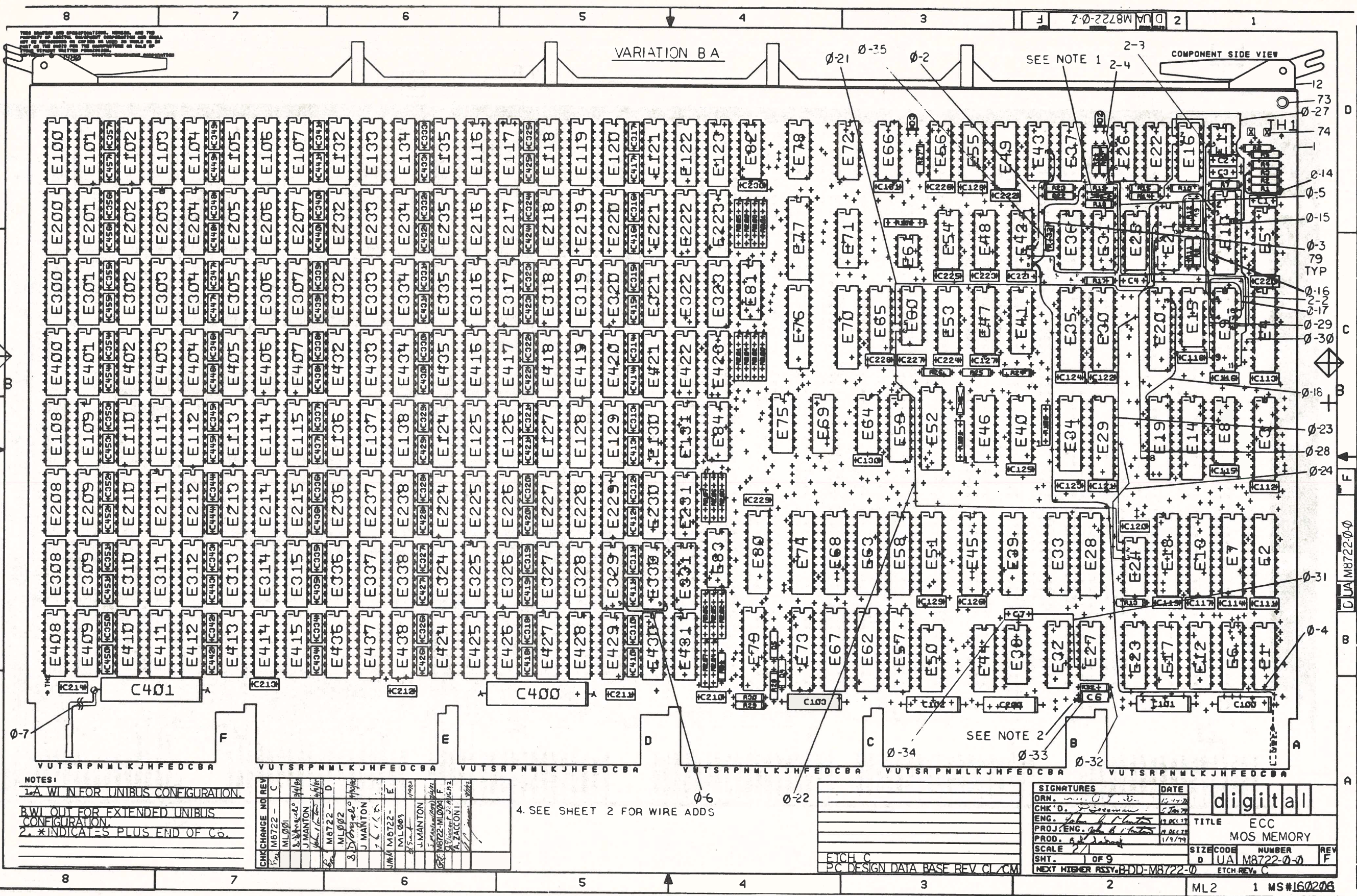
LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION			REFERENCE DESIGNATOR
					BB	BC	BF	
30	30		1316186-00	R NETWORK 1-12 2-18 6PIN	8	8	8	R300-R307
31	31		1613120-00	DELAY= 200NS,10TAPS	2	2	2	E5,E21
32	32		1910532-00	74S00 NAND GATE-QUAD 2IN	1	1	1	E31
33	33		1912799-00	LS00 NAND-GATE-QUAD 2IN,P	1	1	1	E25
34	34		1912388-00	74S02 NOR GATE-QUAD 2IN,PO	1	1	1	E42
35	35		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	1	1	1	E38
36	36		1910533-00	74S03 NAND GATE-QUAD 2IN,O	1	1	1	E22
37	37		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	1	1	1	E27
38	38		1914451-00	74LS393 COUNTER,BINARY,4BIT	2	2	2	E54,E56
39	39		1910547-00	74S153 MUX 1 OF 4 (DUAL)	5	5	5	E40,E41,E47,E49,E53
40	40		1911944-00	555CN TIMER,FUNCT.BLOCK	1	1	1	E11
41	41		1910534-00	74S04 INVERTER GATE-HEX 1I	1	1	1	E60
42	42		1910544-01	74S74-60GG-D DUAL,EDGE TRIG	1	1	1	E26
43	43		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	2	2	2	E15,E43
44	44		1911116-00	DEC 8837 RECEIVER,BUS,HEX,UN	4	4	4	E23,E32,E44,E50
45	45		1915219-00	LS373 FF-D OCTAL-TRANSPARE	3	3	3	E3,E18,E39
46	46		1914214-00	LS374 FF-D OCTAL EDGE TRIG	3	3	3	E7,E28,E68
47	47		1911579-00	8641 TRANSCEIVER,BUS,QUA	4	4	4	E1,E6,E12,E17
48	48		1910539-00	74S20 NAND GATE-DUAL 4INPU	1	1	1	E37
49	49		1912828-00	LS85 COMPARATOR,4BIT MAGN	1	1	1	E65
50	50		1912697-00	LS174 FF-D HEX W/CLEAR	1	1	1	E8
51	51		1915193-00	LS244 DRIVER,LINE,OCTAL,T	1	1	1	E14
52	52		1911573-00	74S280 PARITY GEN/CHKR,9BIT	11	11	11	E48,E66,E69,E71,E72,E75,E78, CONT E81-E84
53	53		1912096-00	DEC 74S86 XOR GATE,QUAD 2IN	2	2	2	E36,E64
54	54		1914086-00	74S30 NAND GATE-POS 8IN	1	1	1	E55
55	55		1913777-00	LS240 DRIVER,LINE,OCTAL,T	1	1	1	E9
56	56		1912389-00	74S08 AND GATE-QUAD 2IN,PO	1	1	1	E24
57	57		1912125-00	74S135 XOR/NOR GATE-QUAD 2I	1	1	1	E59
58	58		1913493-00	74S241 OCTAL BUFFER,TRI-STA	5	5	5	E70,E76,E77,E79,E80
59	59		2113825-01	16K MOS RAM 200NS 1	156	-	-	E100-E138,E200-E238,E300-E338, CONT E400-E438
60	60		23259F1-00	F1-01	1	1	1	E34
61	61		23001J5-00	J5-01,J5-02	1	1	1	E10
62	62		23002J5-00	J5-01,J5-02	1	1	1	E19
63	63		23003J5-00	J5-01,J5-02	1	1	1	E4
64	64		23011J5-00	J5-02	1	1	1	E30
65	65		23005J5-00	J5-01,J5-02	1	1	1	E35
66	66		23006J5-00	J5-01,J5-02	1	1	1	E33
67	67		23007J5-00	J5-01,J5-02	1	1	1	E20
68	68		23008J5-00	J5-01,J5-02	1	1	1	E29
69	69		23009J5-00	J5-01,J5-02	1	1	1	E52
70	70		23001K3-00	K3-01,K3-02	8	8	8	E45,E51,E57,E58,E62,E63,E67,E73
71	71		23002K3-00	K3-01,K3-02	2	2	2	E2,E13
72	72		9009185-00	*** THIS ITEM IS NOT USED ***	-	-	-	
73	73		9000024-01	EYELET,ROLLED 0.1210DX0.192	12	12	12	
74	74		9009149-00	PIN,STAKING 0.235 HX0.345LG SQUA	2	2	2	TP1,TP2
75	75		2114408-01	16K MOS RAM 200NS 1	-	156	-	E100-E138,E200-E238,E300-E338,

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							ECC MOS MEMORY				M8722-BA-DBP	D

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION			REFERENCE DESIGNATOR
					BB	BC	BF	
								CONT E400-E438
76	76		2114895-01	*** THIS ITEM IS NOT USED ***	-	-	-	
77	77		2114927-01	*** THIS ITEM IS NOT USED ***	-	-	-	
78	78		2114897-01	16K MOS RAM 200NS 1	-	-	156	E100-E138,E200-E238,E300-E338,
								CONT E400-E438
79	79		9105740-55	WIRE(WRAP) 30AWG KYNAR UL14	A/R	A/R	A/R	
80	80	B-DD-M8722-0-0		DWG DIRECTORY	REF	REF	REF	
81	81	D-UA-M8722-0-0		UNIT ASSY	REF	REF	REF	
82	82	D-MD-5013505-0-0		DRILL & ETCH DWG	REF	REF	REF	
83	83	D-CS-M8722-0-1		CIRCUIT SCHEMATIC	REF	REF	REF	
84	84		9107256-09	*** THIS ITEM IS NOT USED ***	-	-	-	
85	85		1000064-00	3.9MFD 10V 10% S.TANT	1	1	1	C6
86	86		1302956-00	196.0 .25 W 1.0 % RN55D-F10	1	1	1	R3
87	87		1302858-00	100.0 .25 W 1.0 % RN55D-F10	2	2	2	R17,R25
88	88		1313583-00	150.0 .25 W 1.0 % RN55D-F10	2	2	2	R1,R33
89	89		1303047-00	464.0 .25 W 1.0 % RN55D-F10	2	2	2	R8,R9
90	90		1913462-00	74S240 OCTAL BUFFER,INVERTI	1	1	1	E74
91	91		1309418-00	24.30 K .25 W 1.0 % RN55D-F10	1	1	1	R32
92	92		1912746-00	DEC 74S37 NAND GATE-QUAD 2IN	1	1	1	E16
93	93		1215006-04	*** THIS ITEM IS NOT USED ***	-	-	-	

- 94 NOTE: 0 M8722-BA IS THE PRIMARY VARIATION OF THE 128K X 16 BITS SYSTEM (NOT A MODULE TYPE).
95 NOTE: 1 M8722-BB IS A MODULE TYPE USING MOSTEK 16K MOS DEVICES.
96 NOTE: 2 M8722-BC IS A MODULE TYPE USING FUJITSU 16K MOS DEVICES.
97 NOTE: 3 M8722-BF IS A MODULE TYPE USING HITACHI MOS DEVICES.

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							ECC MOS MEMORY		K	PL	M8722-BA-DBP	D



NOTES:
 1. A WIN FOR UNIBUS CONFIGURATION.
 B.WI OUT FOR EXTENDED UNIBUS CONFIGURATION.
 2. *INDICATES PLUS END OF C₀.

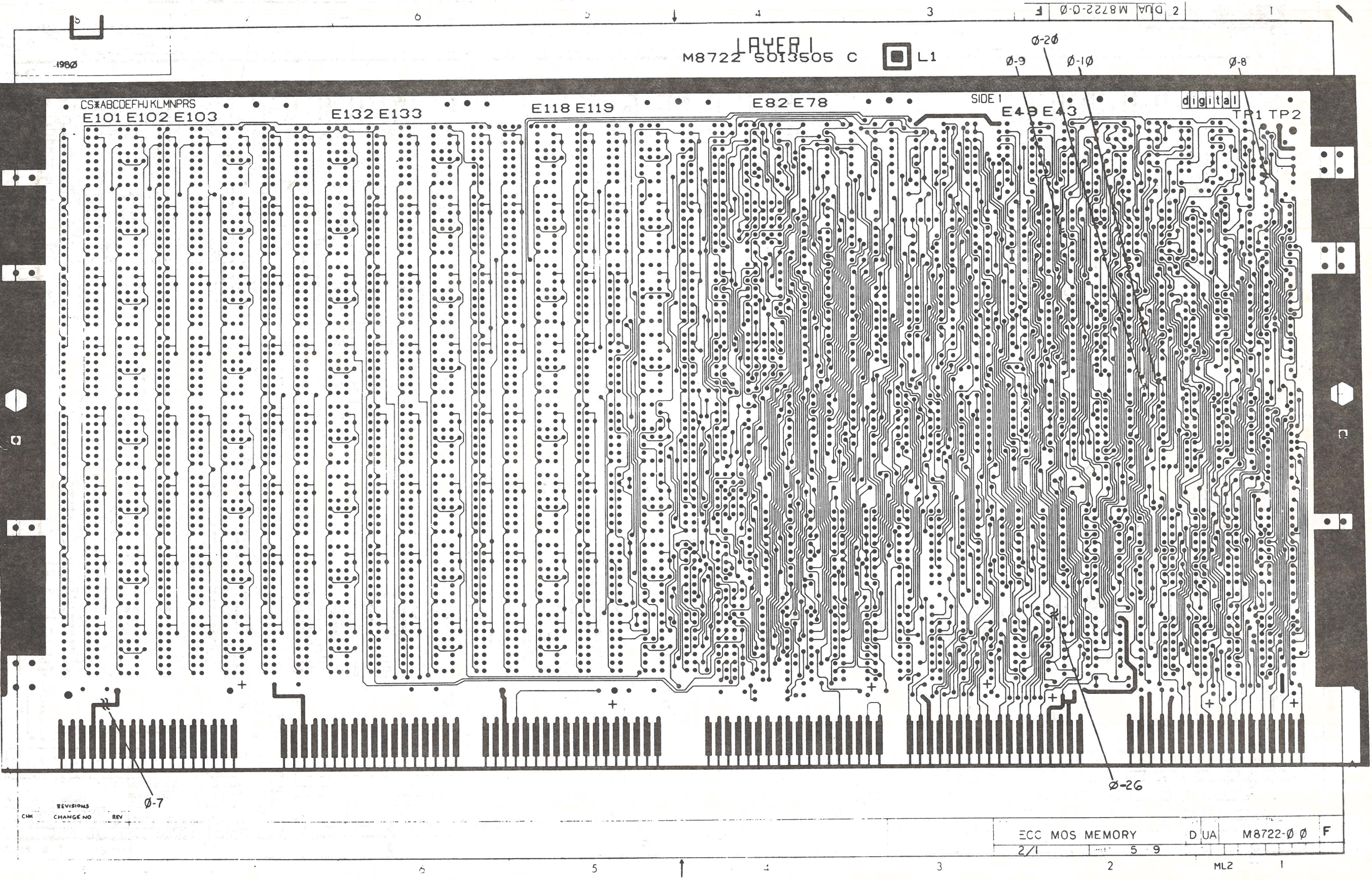
CHANGE NO	REV	DATE	BY	CHK'D	APP'D
1	ML001	1/1/79	J. MANTON		
2	ML002	1/1/79	J. MANTON		
3	ML003	1/1/79	J. MANTON		
4	ML004	1/1/79	J. MANTON		
5	ML005	1/1/79	J. MANTON		
6	ML006	1/1/79	J. MANTON		
7	ML007	1/1/79	J. MANTON		
8	ML008	1/1/79	J. MANTON		
9	ML009	1/1/79	J. MANTON		
10	ML010	1/1/79	J. MANTON		

4. SEE SHEET 2 FOR WIRE ADDS

ETCH C
PC DESIGN DATA BASE REV. CLZCM

SIGNATURES		DATE	digital
ORN. <i>[Signature]</i>	1/1/79		
CHK'D. <i>[Signature]</i>	1/1/79		
ENG. <i>[Signature]</i>	1/1/79		
PROD. <i>[Signature]</i>	1/1/79		
SCALE 2/			
SHT. 1 OF 9			
NEXT HIGHER ASSY. BDD-M8722-0			
ETCH REV. C			

ML2 1 MS#160206



REVISIONS
CHANGE NO. REV

ECC MOS MEMORY			D UA	M8722-00	F
2/1	5	9	ML2	1	

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1 DUA M8722-0-0 2

AY34AJ

L4

Ø-13 Ø-11

Ø-1

Ø-25 2-1

Ø-12

1-1

ECC MOS MEMORY

M8722 5013505 C SIDE 2

REVISIONS		
CHK	CHANGE NO	REV

ECC MOS MEMORY

D U A

M8722-0-0

F

2/1

SHEET 8

OF 9

ML2

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REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 000 107

M8722

FIRST RELEASE

ETCH CUT - SIDE 2:

- B - 1. CUT ETCH BETWEEN E43-11 AND R19 (TO THE LEFT OF THE FEED THRU).
- B - 11. CUT ETCH BETWEEN E10-9 AND FEED THRU (RIGHT SIDE OF PIN).
- B - 12. CUT ETCH BETWEEN E10-9 AND FEED THRU (LEFT SIDE OF PIN, ISOLATING E10-9).
- B - 13. CUT ETCH BETWEEN E10-3 AND FEED THRU (RIGHT SIDE).
- B - 25. CUT ETCH BETWEEN E10-16 AND FEED THRU (RIGHT SIDE).

ETCH CUTS - SIDE 1:

- B - 7. CUT ETCH BETWEEN C401 AND FINGER FS1.
- B - 8. CUT ETCH BETWEEN R1 AND R3.
- B - 9. CUT ETCH BETWEEN THE 1ST AND 2ND FEED THRU E42-13 (RIGHT SIDE).
- B - 10. CUT ETCH BETWEEN E19-1 AND E20-3.
- B - 20. CUT ETCH BETWEEN THE FIRST AND SECOND FEED THRU OF E30-18 (RIGHT SIDE).
- B - 26. CUT ETCH NO MORE THAN 1/4" FROM C7 (220PF) (RIGHT SIDE) AS SHOWN.

WIRE ADDS:

- B - 2. ADD A WIRE FROM E42-10 TO E43-11.
- B - 3. ADD A WIRE FROM E42-8 TO R19 (LEFT SIDE).
- B - 4. ADD A WIRE FROM E42-8 THRU A FEED THRU TO FINGER AB2.
- B - 5. ADD A WIRE FROM E42-9 TO E26-6.
- B - 6. ADD A WIRE FROM E330-9 TO E329-9 FOR 'BA' VARIATIONS ONLY.
- B - 14. ADD WIRE FROM R1 TO R3 (AS SHOWN).
- B - 15. ADD WIRE FROM E10-3 TO E21-13.
- B - 16. ADD WIRE FROM E10-9 TO E21-14.
- B - 17. ADD WIRE FROM E9-17 TO E21-3.
- B - 18. ADD WIRE FROM E20-19 TO E19-1.
- B - 21. ADD WIRE FROM E60-5 TO E21-5.
- B - 22. ADD WIRE FROM E60-6 TO E24-2.
- B - 23. ADD WIRE FROM E24-1 TO FIRST FEED THRU OF E30-18 (AS SHOWN).
- B - 24. ADD WIRE FROM E24-3 TO SECOND FEED THRU OF E30-18 (AS SHOWN).
- B - 27. ADD WIRE FROM E16-1 TO E10-17.
- B - 28. ADD WIRE FROM E16-3 TO E19-8.
- B - 29. ADD WIRE FROM E16-2 TO E9-9.
- B - 30. ADD WIRE FROM E9-11 TO E10-2.
- B - 31. ADD WIRE FROM C7 (220PF) (RIGHT SIDE) TO E27-6.

REPLACEMENT COMPONENTS:

- B - 32. REPLACE D1 WITH R32, 24.3K, 1%.
- B - 33. REPLACE R16 WITH C6, 3.9uF, 10V.
- B - 34. REPLACE C5 WITH C7, 220PF, 100V.

COMPONENT ADD:

- B - 35. ADD R33, 150 $\frac{1}{4}$ W, 1% AS SHOWN.

ECO # 1

ETCH CUT - SIDE 2

- 1-1. CUT ETCH BETWEEN E10-11 AND FEEDTHRU (RIGHT SIDE).

WIRE ADDS - SIDE 1

- 1-2. ADD WIRE FROM E24-11 TO E10-11.
- 1-3. ADD WIRE FROM E24-12 TO E9-7.
- 1-4. ADD WIRE FROM E24-13 TO E29-19.

ECO NO. 2

ETCH CUT - SIDE 2:

- 2-1. CUT ETCH BETWEEN E11-3 TO E26-3.

WIRE ADDS - SIDE 1:

- 2-2. ADD WIRE FROM E9-4 TO E9-18.
- 2-3. ADD WIRE FROM E9-2 TO E11-3.
- 2-4. ADD WIRE FROM E9-16 TO E26-3.

TITLE		SIZE CODE	NUMBER		REV.
ECC MOS MEMORY		DUA	M8722-0-0		F
SCALE	2/1	SHEET	9 OF 9		DIST.

ML?

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1-0-2278W 2

NOTES:

- SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:
[X/Z] SIGNAL NAME [X/Z]
NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.
DESTINATION SHEET NUMBER.
NUMBER OF CONNECTION POINTS ON SOURCE SHEET.
SOURCE SHEET NUMBER.

2. * INDICATES BATTERY BACKED UP.

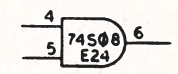
3. GND AND +5V ARE AS FOLLOWS:

	GND	+5V
14 PIN DIP	7	14
16 PIN DIP	8	16
18 PIN DIP	9	18
20 PIN DIP	10	20

EXCEPTIONS ARE

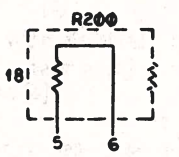
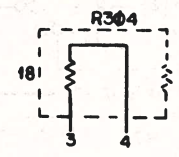
8640	1	8
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SPARES

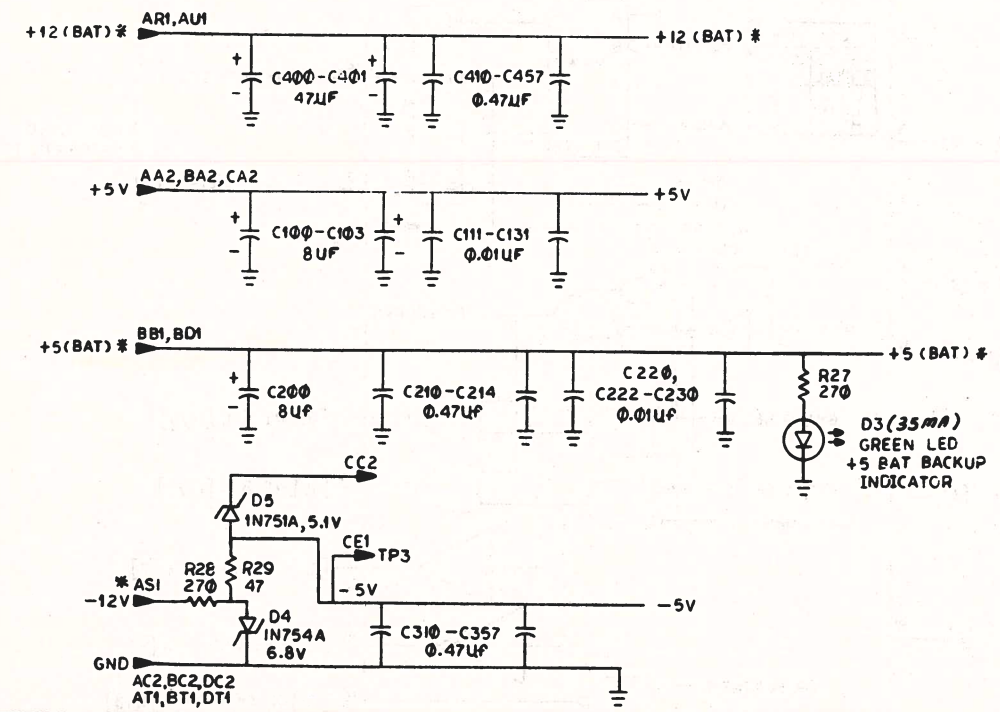
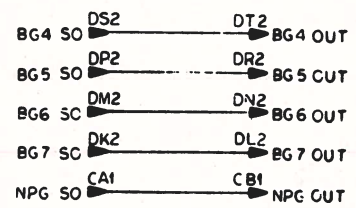


[2] OP CK RMW L [1, 10]

[9] PAR D H [1, 9/2]

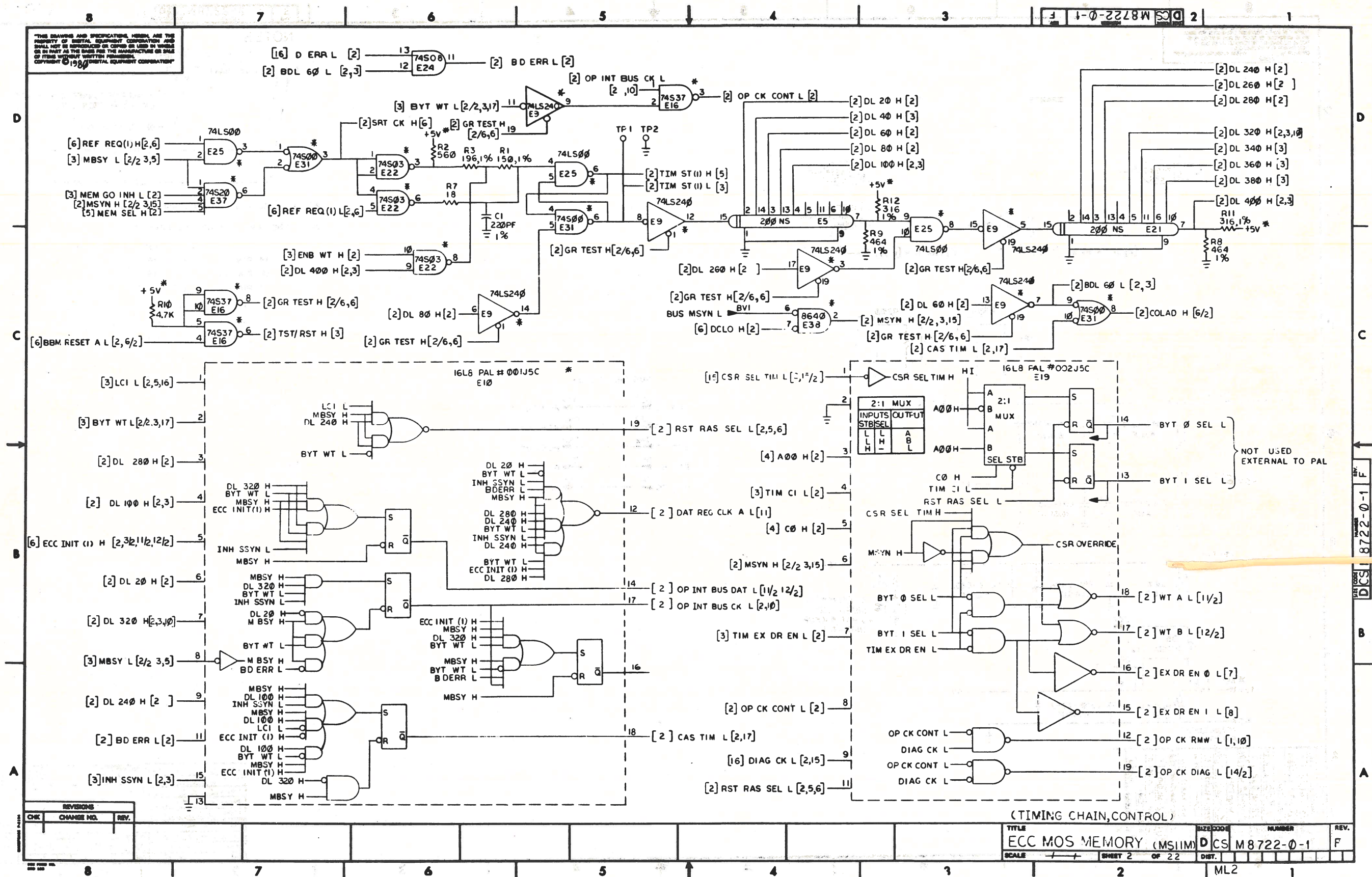


BUS GRANT LINES

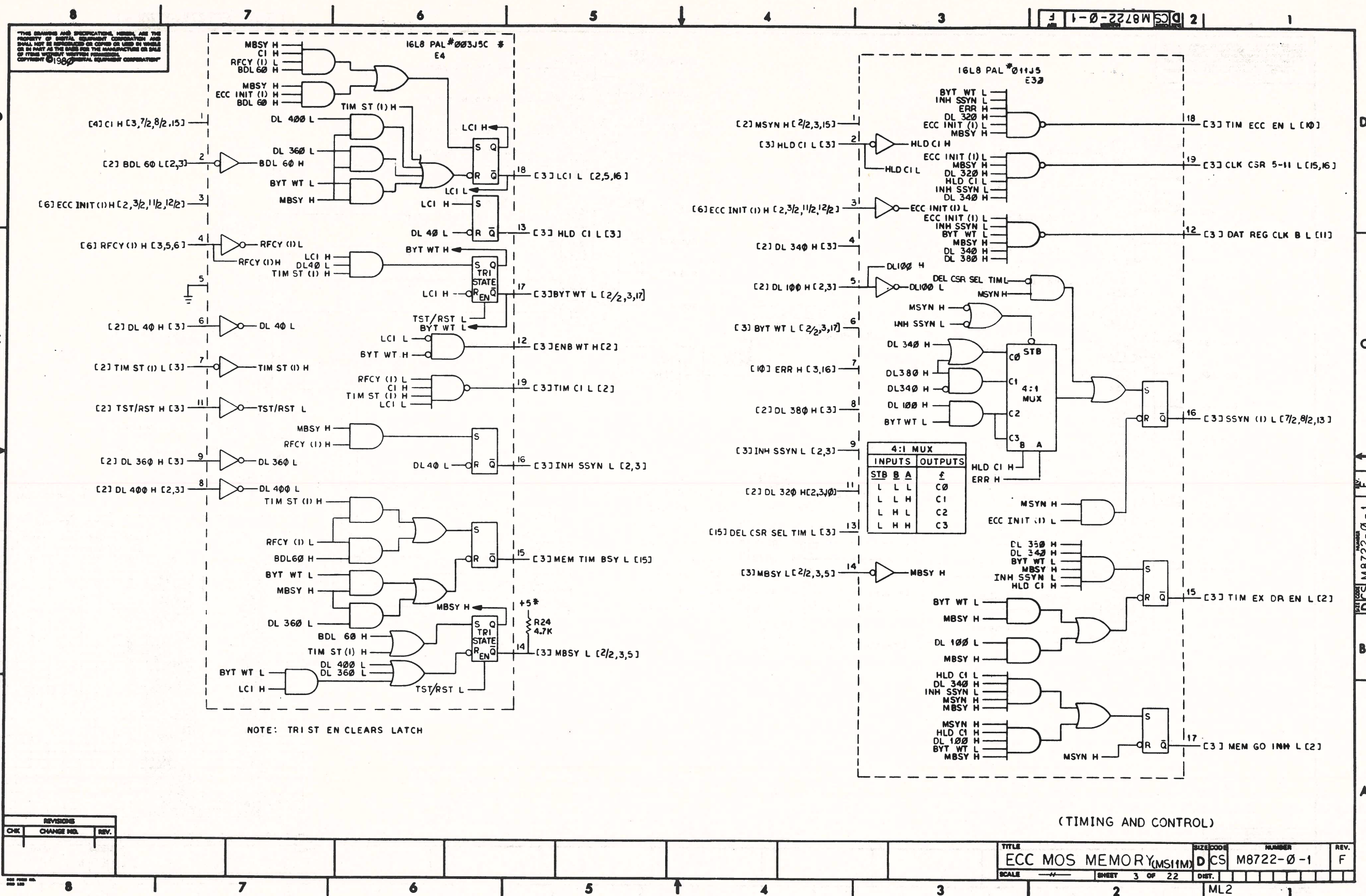


REV	DATE	BY	CHK	DESCRIPTION
1	11/44	JOHN MANTON		INITIAL DESIGN
2	11/44	JOHN MANTON		REVISION 1
3	11/44	JOHN MANTON		REVISION 2
4	11/44	JOHN MANTON		REVISION 3
5	11/44	JOHN MANTON		REVISION 4
6	11/44	JOHN MANTON		REVISION 5
7	11/44	JOHN MANTON		REVISION 6
8	11/44	JOHN MANTON		REVISION 7
9	11/44	JOHN MANTON		REVISION 8
10	11/44	JOHN MANTON		REVISION 9
11	11/44	JOHN MANTON		REVISION 10
12	11/44	JOHN MANTON		REVISION 11
13	11/44	JOHN MANTON		REVISION 12
14	11/44	JOHN MANTON		REVISION 13
15	11/44	JOHN MANTON		REVISION 14
16	11/44	JOHN MANTON		REVISION 15
17	11/44	JOHN MANTON		REVISION 16
18	11/44	JOHN MANTON		REVISION 17
19	11/44	JOHN MANTON		REVISION 18
20	11/44	JOHN MANTON		REVISION 19
21	11/44	JOHN MANTON		REVISION 20

DRN. 1-0-2278W	FIRST USED ON 11/44	20-0000
CHK'D. 11/44	TITLE	
ENG. 11/44	ECC MOS MEMORY	
PROD. ENG. 11/44	(MS11M)	
NEXT HIGHER ASSY.		
B-DD-M8722-0	SIZE CODE	NUMBER
SCALE	D	CS M8722-0-1
SHEET 1	OF 22	DIST.
ML2	1	

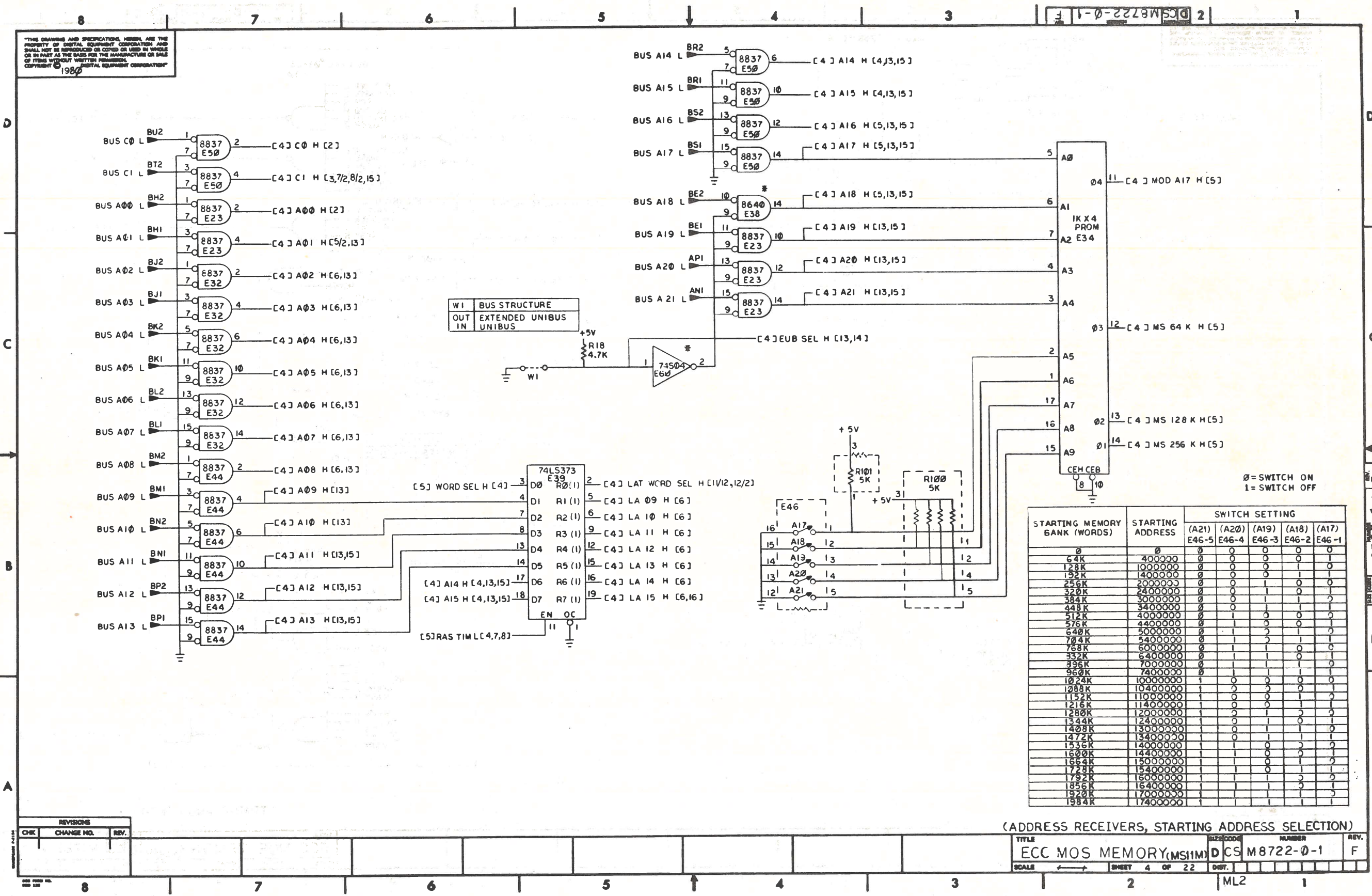


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REV. 1
M8722-0-1
DCS

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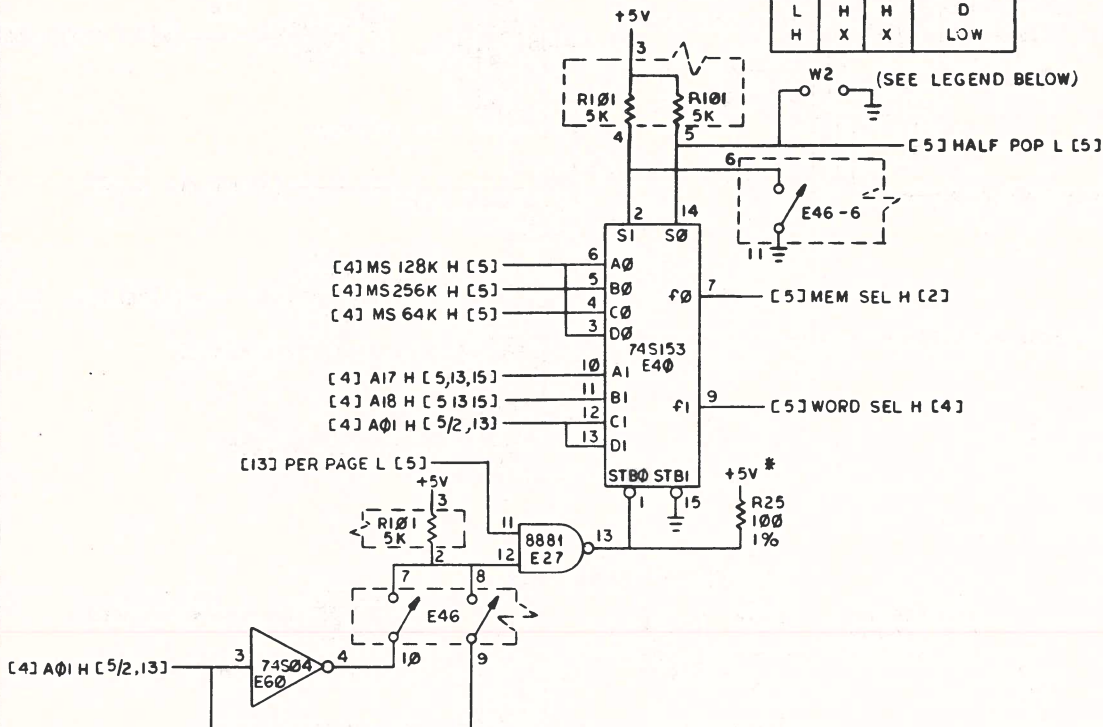


(ADDRESS RECEIVERS, STARTING ADDRESS SELECTION)

TITLE	SIZE/TYPE	NUMBER	REV.
ECC MOS MEMORY (MS11M)	DCS	M8722-0-1	F
SCALE	SHEET 4 OF 22	DIST.	

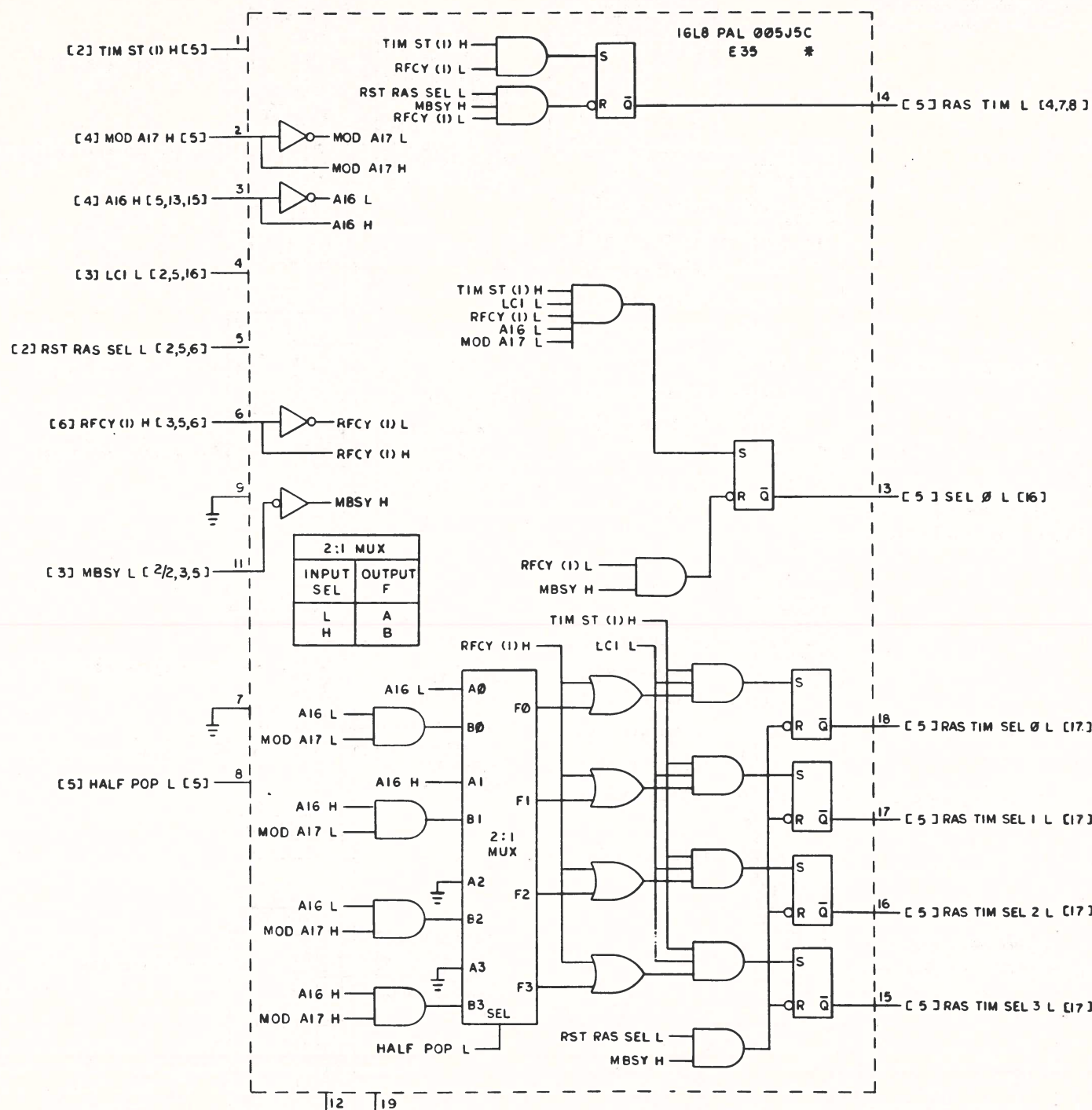
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74S153 4:1 MUX				
INPUTS			OUTPUTS	
STB	S1	S0	F	
L	L	L	A	
L	L	H	B	
L	H	L	C	
L	H	H	D	
H	X	X	LOW	



SW POSITION			USAGE	MEMORY CAPACITY AND INTERLEAVING
8	7	6		
OFF	OFF	OFF	IN	64K 1/2 POP NON INTERL.
OFF	OFF	OFF	OUT	128K FULLY POP NON INTERL.
OFF	ON	ON	IN	64K 1/2 POP INTERL RESPONDS TO A01 H NON ASSERTED
OFF	ON	ON	OUT	128K FULLY POP INTERL RESPONDS TO A01 H NON ASSERTED
ON	OFF	ON	IN	64K 1/2 POP INTERL RESPONDS TO A01 H ASSERTED
ON	OFF	ON	OUT	128K FULLY POP INTERL RESPONDS TO A01 H ASSERTED

NOTE: SW 8 & 7 MUST NOT BE ON AT THE SAME TIME



(MEMORY SELECT, INTERLEAVING
RAS TIM GENERATION)

DCS M8722-0-1

REV. F

B

A

D

C

1

1

ML2

OF 22

SHEET 5

SCALE

DIST.

NUMBER

REV.

F

M8722-0-1

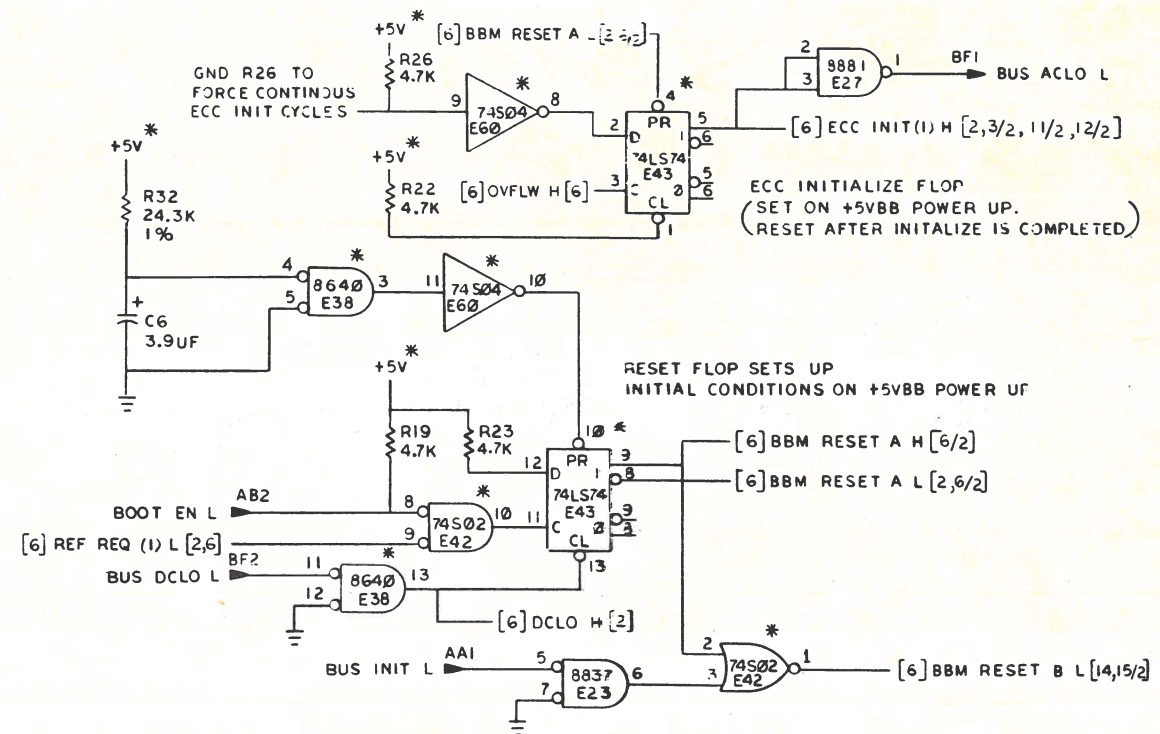
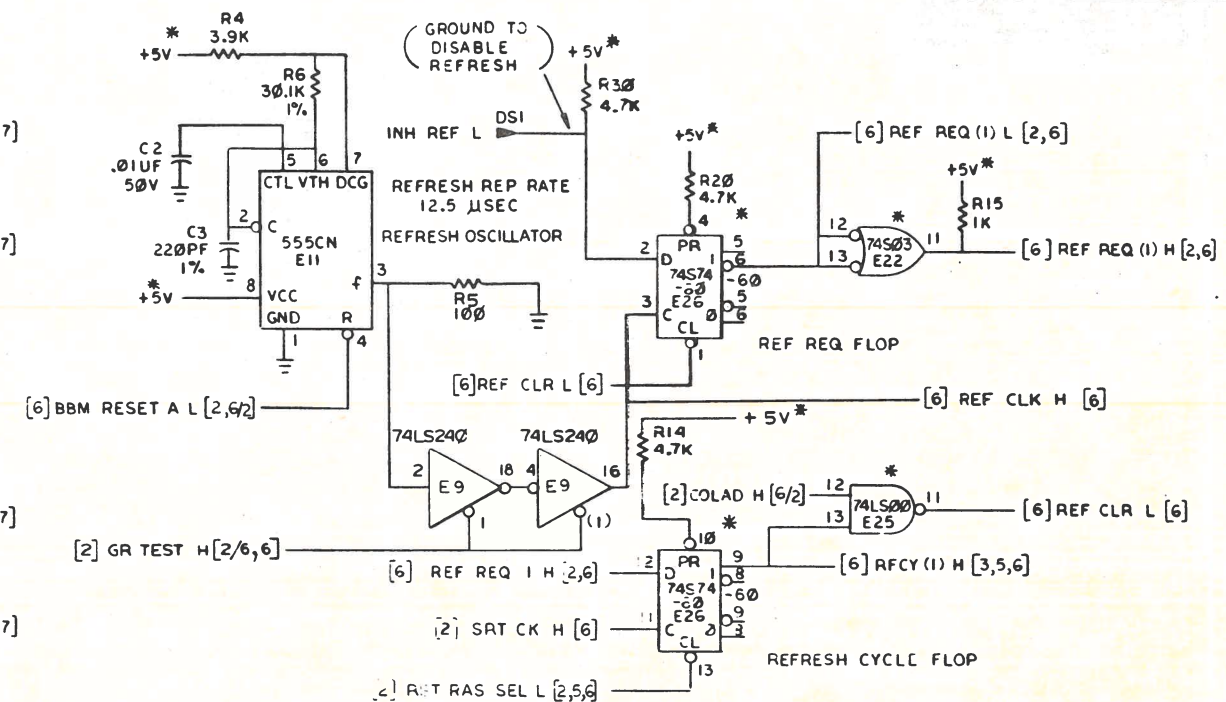
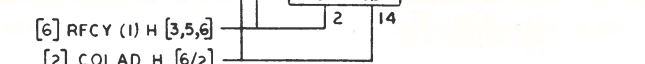
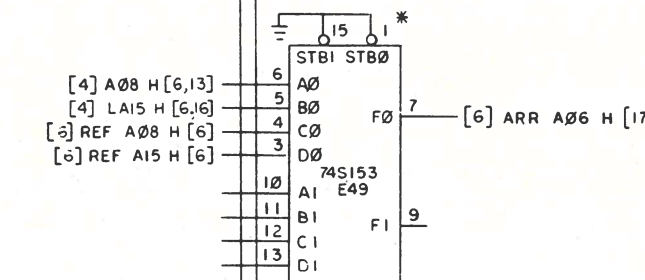
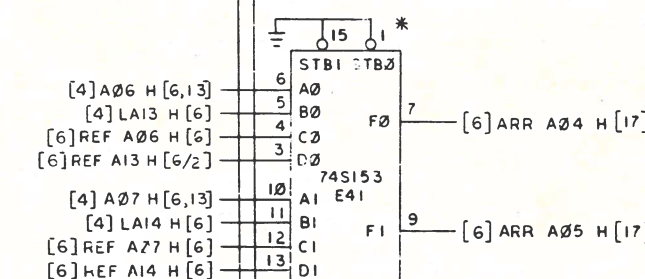
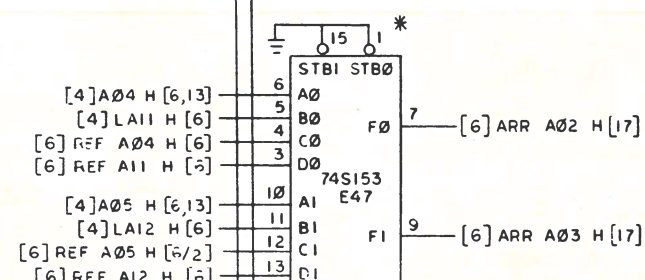
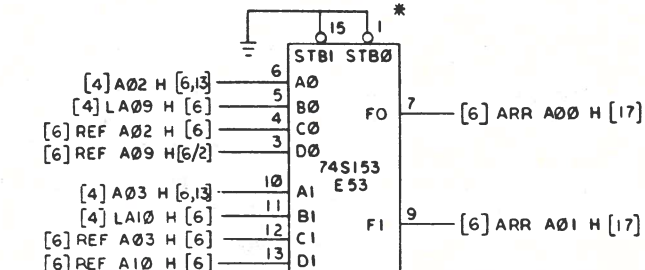
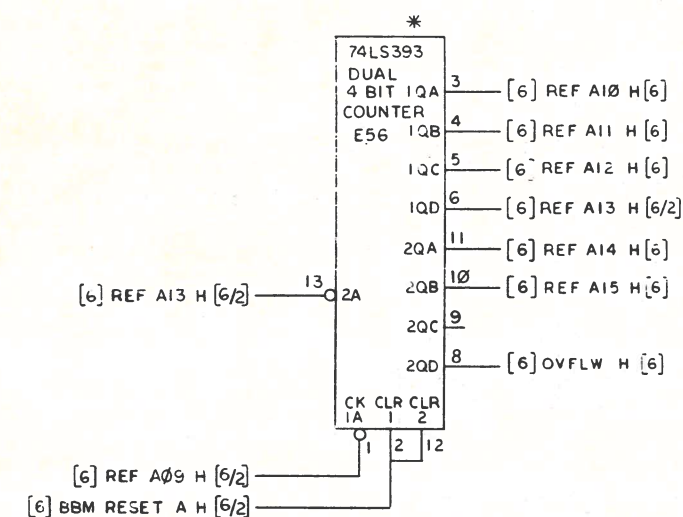
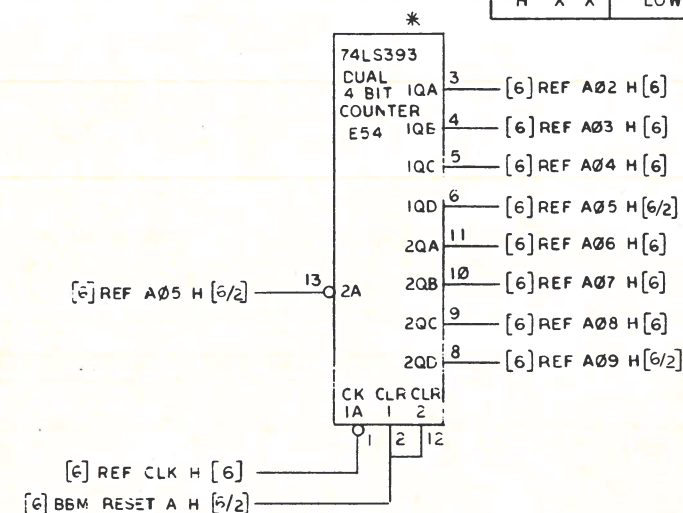
DCS

ECC MOS MEMORY(MSIIM)

TITLE

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74SI153 4:1 MUX				
INPUTS			OUTPUTS	
STB	SI	SO	f	
L	L	L	A	
L	L	H	B	
L	H	L	C	
L	H	H	D	
H	X	X	LOW	



(REFRESH, ECC INITIALIZE, ARRAY ADDRESS MUX)

DCS M8722-0-1

B

A

REV. F

ML2

1

2

3

4

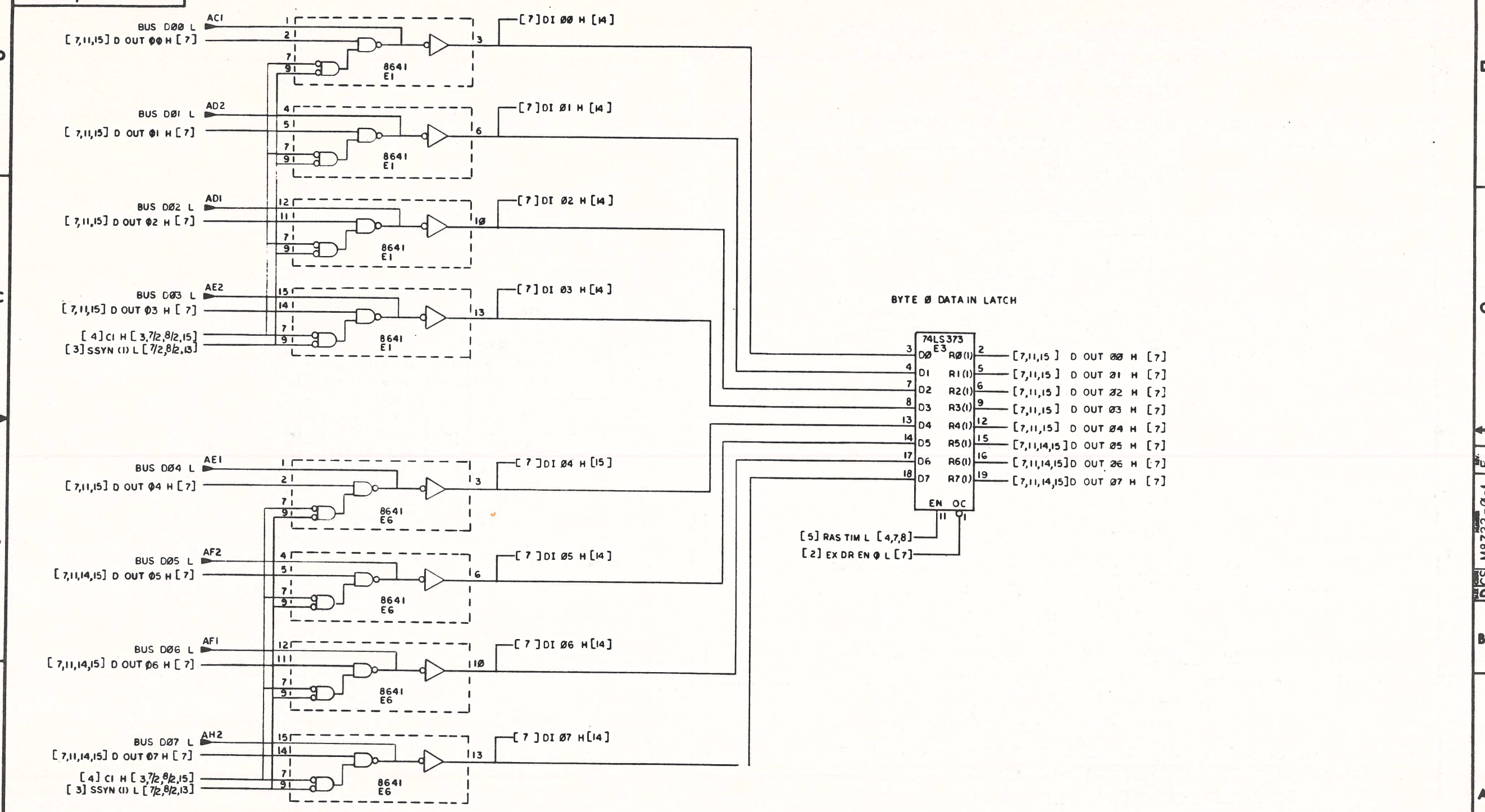
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6

7

8

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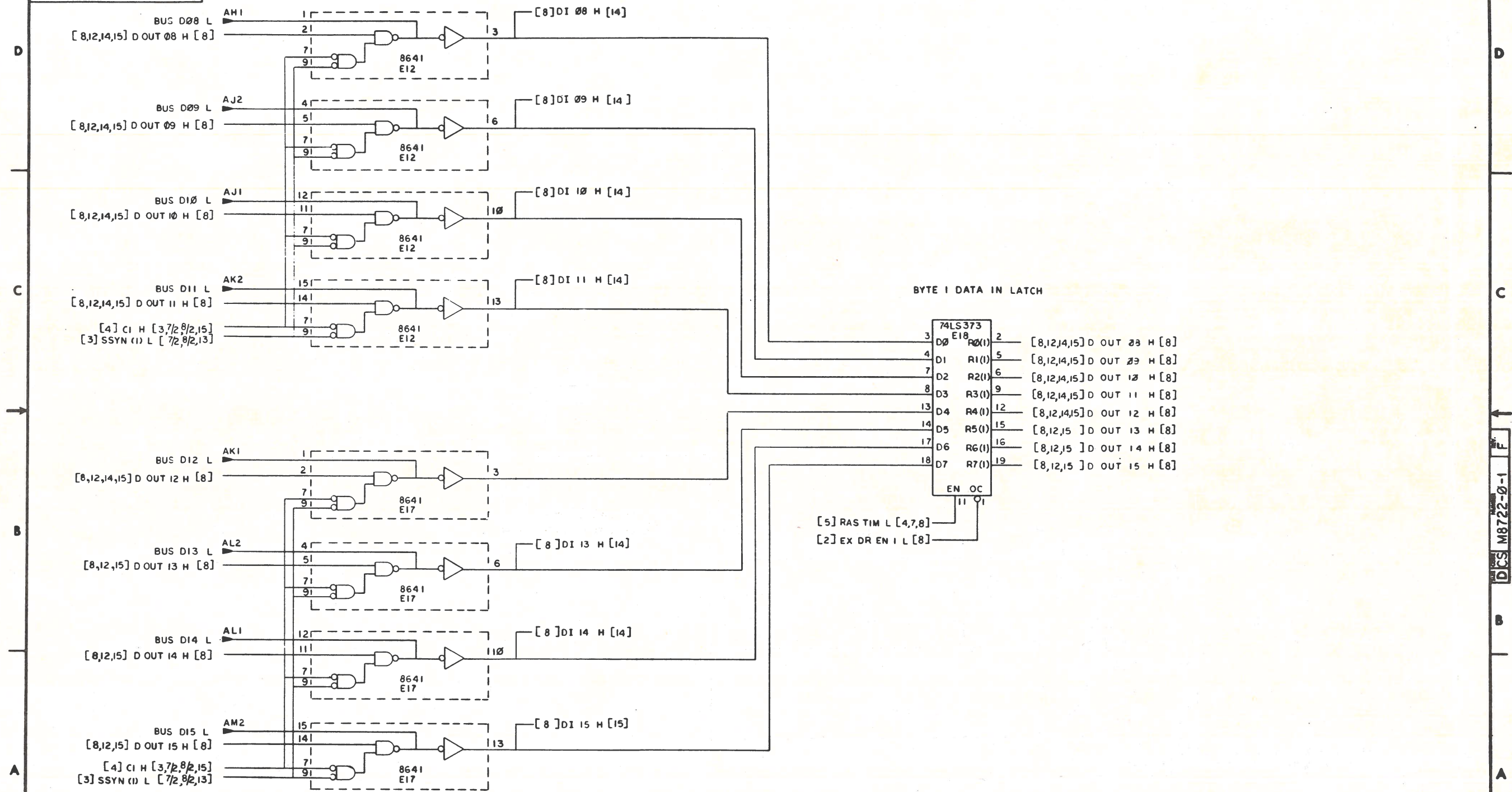


REVISIONS		
CHK	CHANGE NO.	REV.

(BYTE 0 DATA DRIVERS, RECEIVERS AND LATCH)

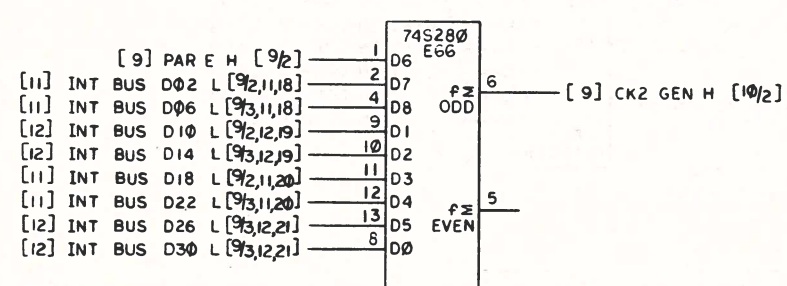
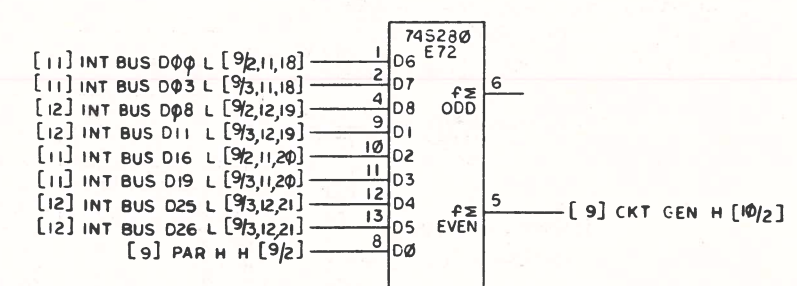
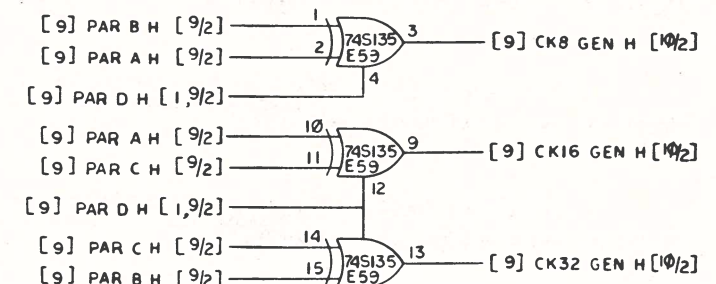
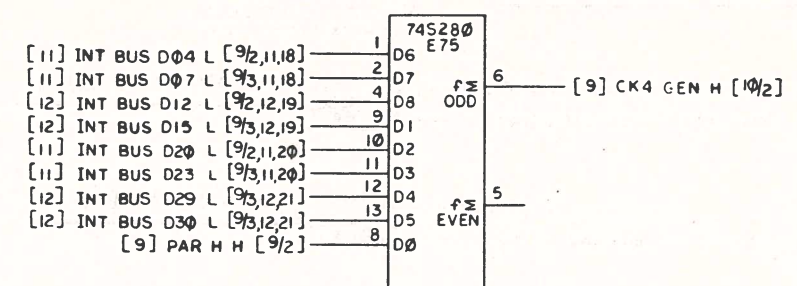
TITLE		SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MSIIM)		D CS	M8722-0-1	F
SCALE	SHEET 7 OF 22	DIST.		

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REVISIONS		
CHK	CHANGE NO.	REV.

(BYTE 1 DATA DRIVERS, RECEIVERS AND LATCH)			
TITLE	SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)	DCS	M8722-0-1	F
SCALE	SHEET 8	OF 22	DIST.
	ML2	1	



NOTE: CHECK BIT PATTERN FOR
ALL 0'S OR ALL 1'S DATA

IS:	CKT	CK32	CK16	CK8	CK4	CK2	CK1
	0						

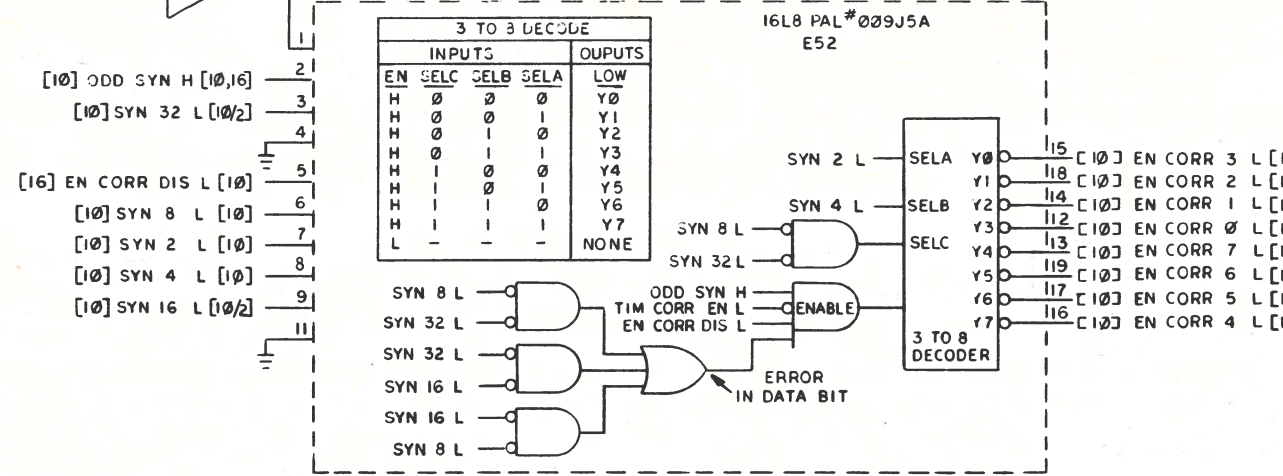
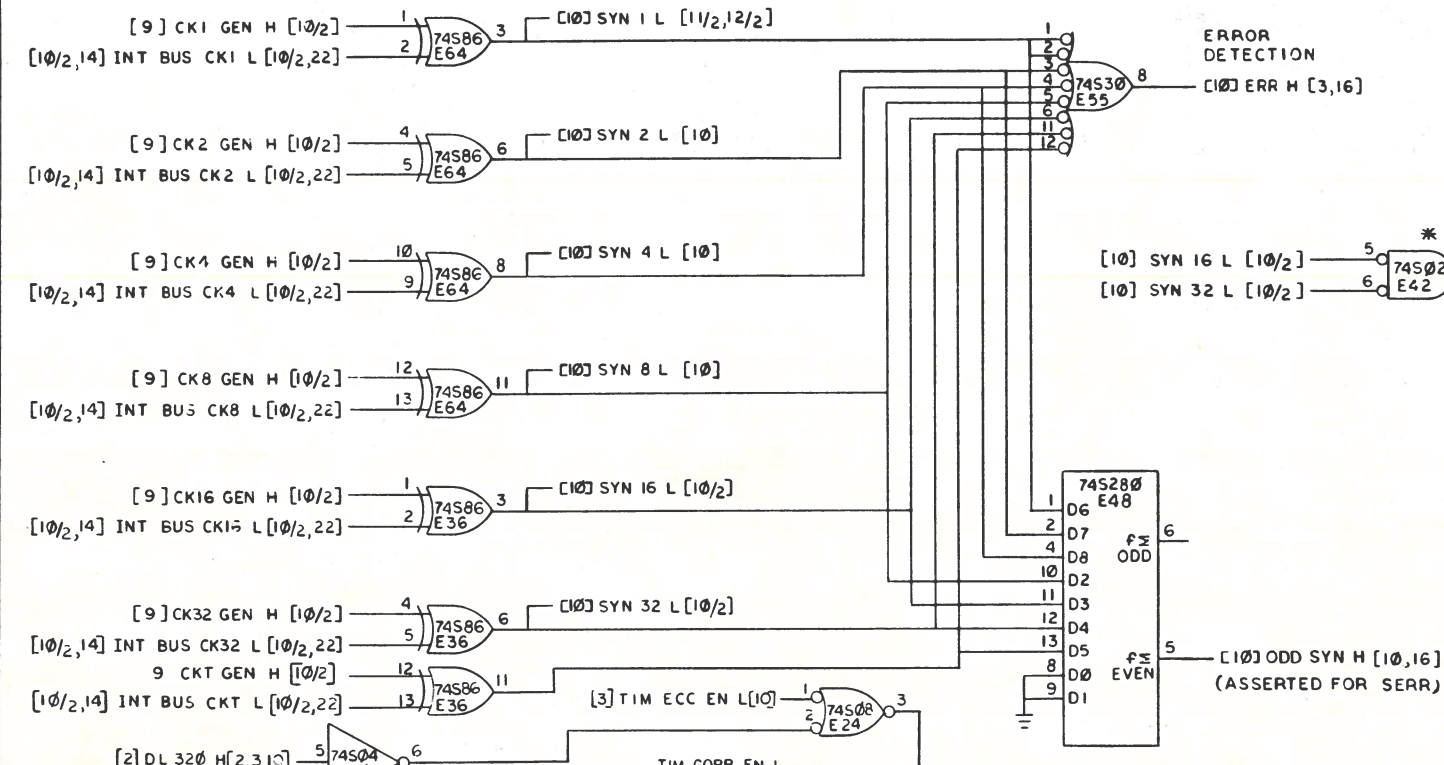
(CHECK BIT GENERATION)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE		ECC MOS MEMORY (MSIM)		SIZE CODE		NUMBER		REV.	
				D CS		M8722-0-1		F	
SCALE		SHEET		OF		DST.			
— //		9		22					
		2		ML2		1			

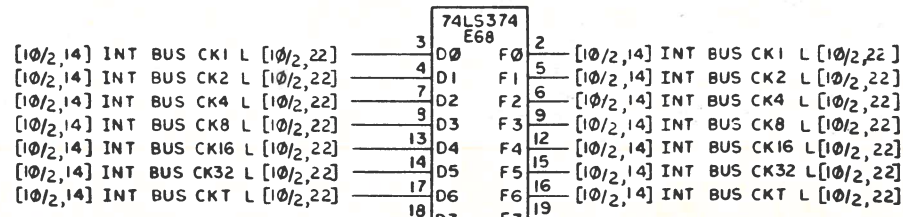
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SYNDROME GENERATION
ON CHECK BIT COMPARE



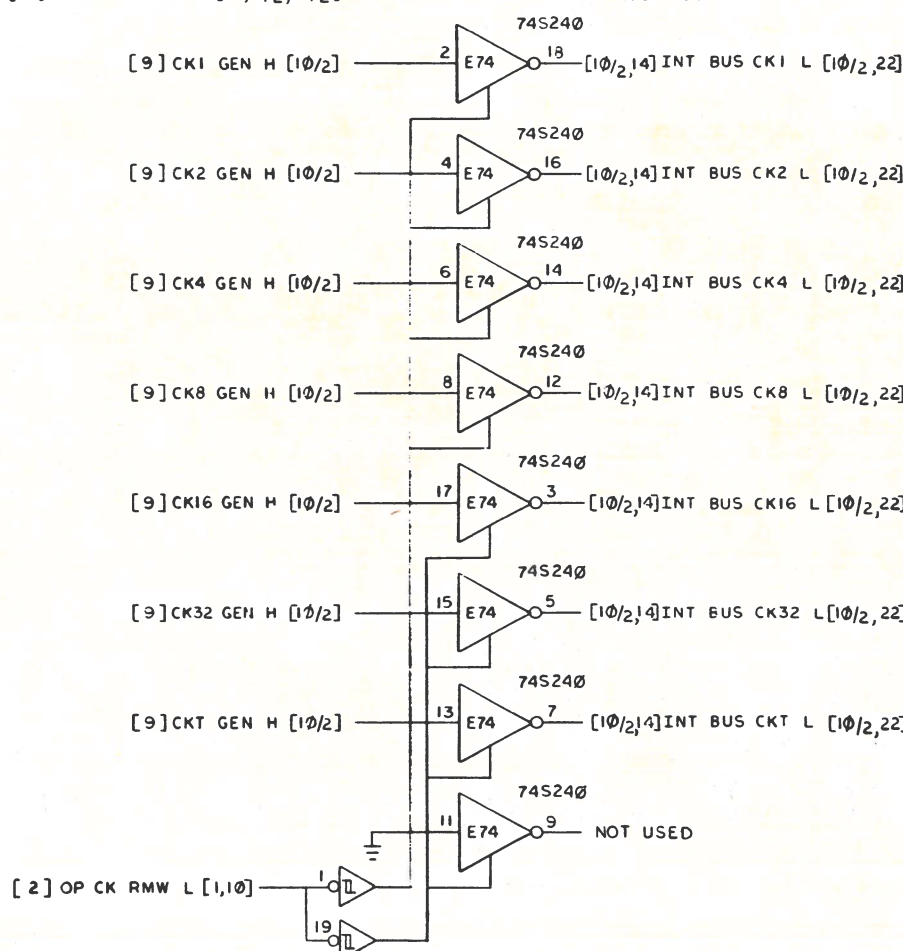
ERROR IN DATA BIT DECODE
i.e. EN CORR 0 L ASSERTED FOR ERROR IN BITS 0 OR 1
OF LOWER WORD OR UPPER WORD.
EN CORR 1 L ASSERTED FOR ERROR IN BITS 2 OR 3
OF LOWER WORD OR UPPER WORD ETC.
NO OUTPUTS ASSERTED FOR ERROR IN CHECK BIT

CHECK BIT REGISTER



[2] OP INT BUS CK L [2,10]
[11] DAT REG COM H [10,11/2,12/2]

CHECK BIT DRIVER
TO MOS ARRAY



(SYNDROME GENERATION, ERROR
DECODE, CHECK BIT REGISTER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)		DCS	M8722-0-1	F
SCALE		SHEET 10 OF 22	DIST.	

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PAL #001K3D
E73

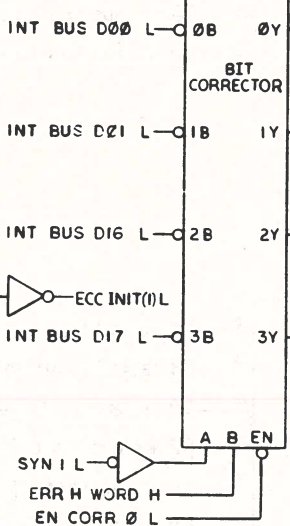
ECC INIT (1) L
WTA L

2 TO 1 MUX		DATA INPUTS		OUTPUT
SELECT INPUT	SEL	CO	CI	Y
L	L	X	X	L
L	H	X	X	H
H	X	L	L	L
H	X	H	H	H

LAT WORD SEL H

4:1 MUX		DATA INPUTS		OUTPUT
SELECT INPUT	SEL	CO	CI	Y
L	L	X	X	L
L	H	X	X	H
H	X	L	L	L
H	X	H	H	H

4 BIT REGISTER		DATA INPUTS		OUTPUT
SELECT INPUT	SEL	CO	CI	Y
L	L	X	X	L
L	H	X	X	H
H	X	L	L	L
H	X	H	H	H



BIT CORRECTOR		INPUTS		ENABLE		OUTPUTS			
SELECT	EN	B	A	EN		0Y	1Y	2Y	3Y
X	X	H	H	H		0B	1B	2B	3B
L	L	L	L	L		0B	1B	2B	3B
L	H	L	L	L		0B	1B	2B	3B
H	L	L	L	L		0B	1B	2B	3B
H	H	L	L	L		0B	1B	2B	3B

NOTE:
EN CORR 0 L AND WTA L MUST NOT
BE ASSERTED SIMULTANEOUSLY
DURING DAT REG COM H

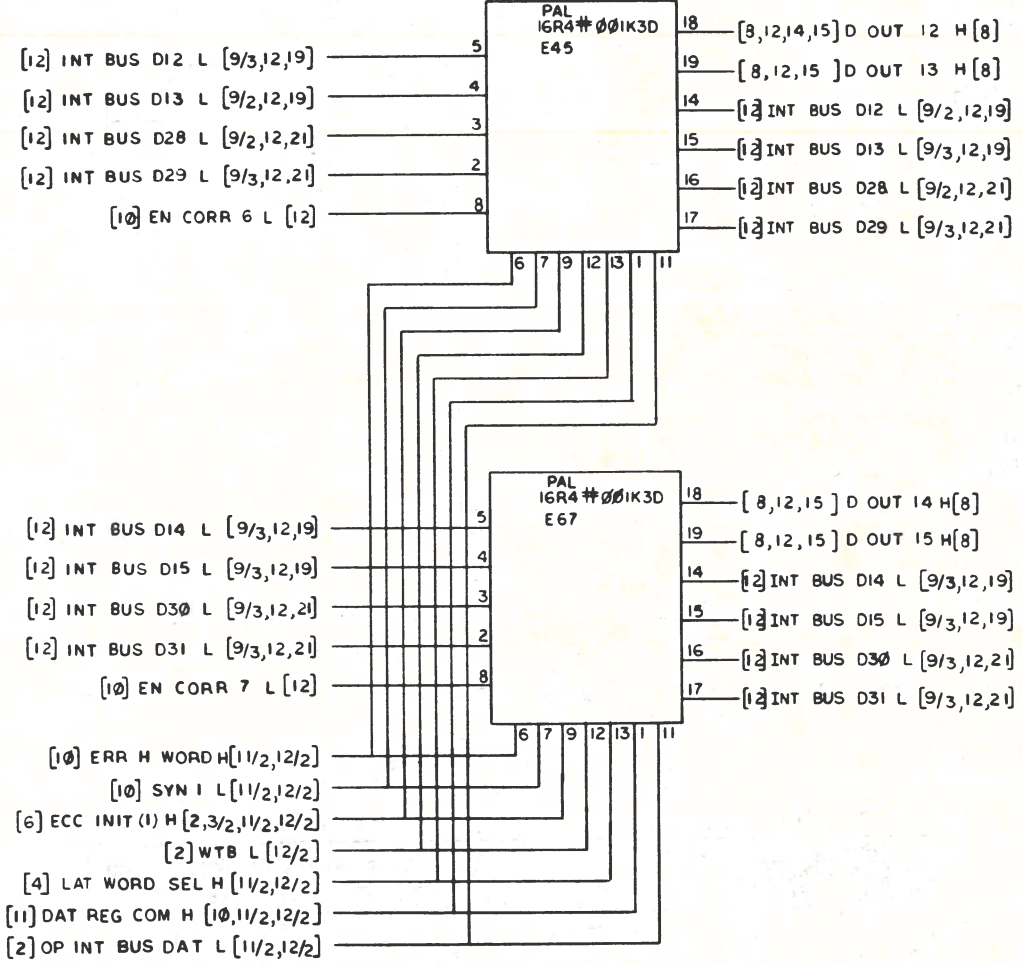
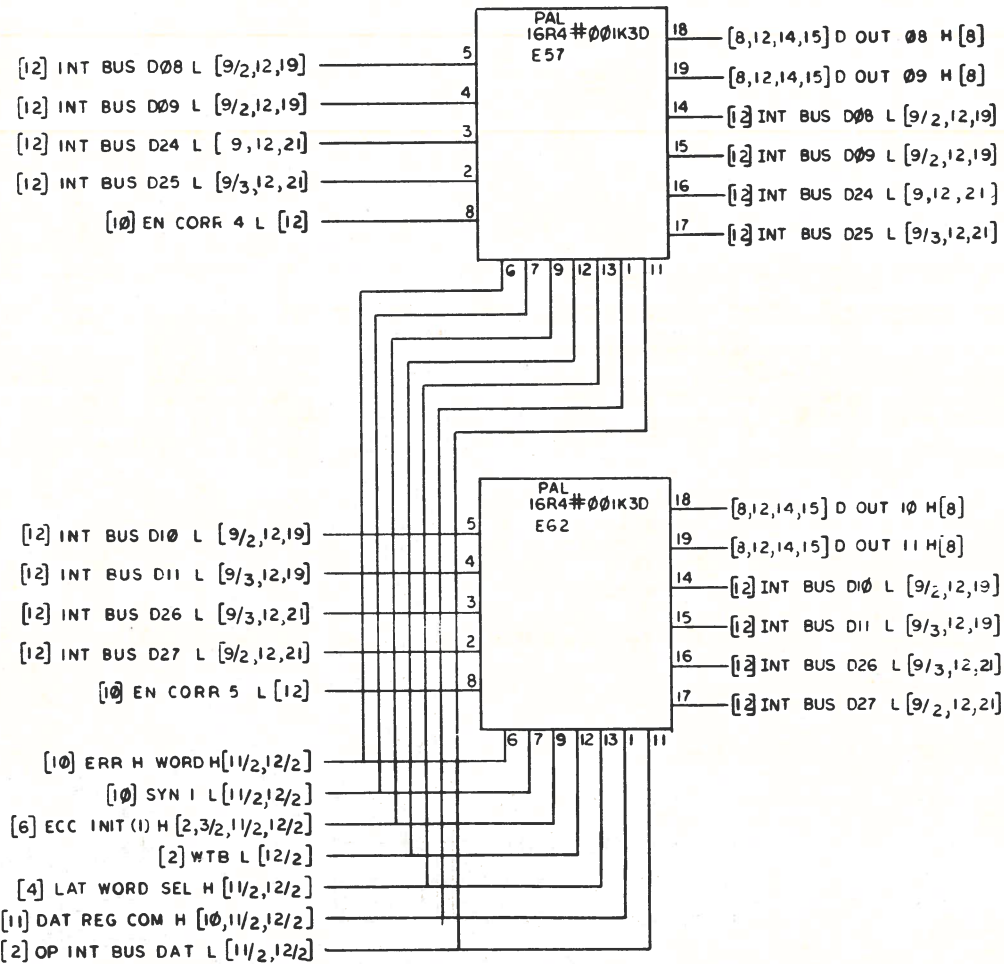
4 TO 1 MUX		SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
SELECT INPUT	SEL	B	A	CO	CI	C2	C3	STB	Y
X	X	X	X	X	X	X	X	L	L
L	L	L	L	X	X	X	X	H	L
L	L	L	L	X	X	X	X	H	H
L	H	X	L	X	X	X	X	H	L
L	H	X	L	X	X	X	X	H	H
H	L	X	X	L	X	X	X	H	L
H	L	X	X	L	X	X	X	H	H
H	H	X	X	X	L	X	X	H	L
H	H	X	X	X	L	X	X	H	H

[2] DAT REG CLK A L [11] 12
[3] DAT REG CLK B L [11] 13

(DATA CORRECTOR, MDR)

TITLE		SCALE	SHEET	OF	22	DATE	REV.
ECC MOS MEMORY (MS11M)			11	22			F
ML2							

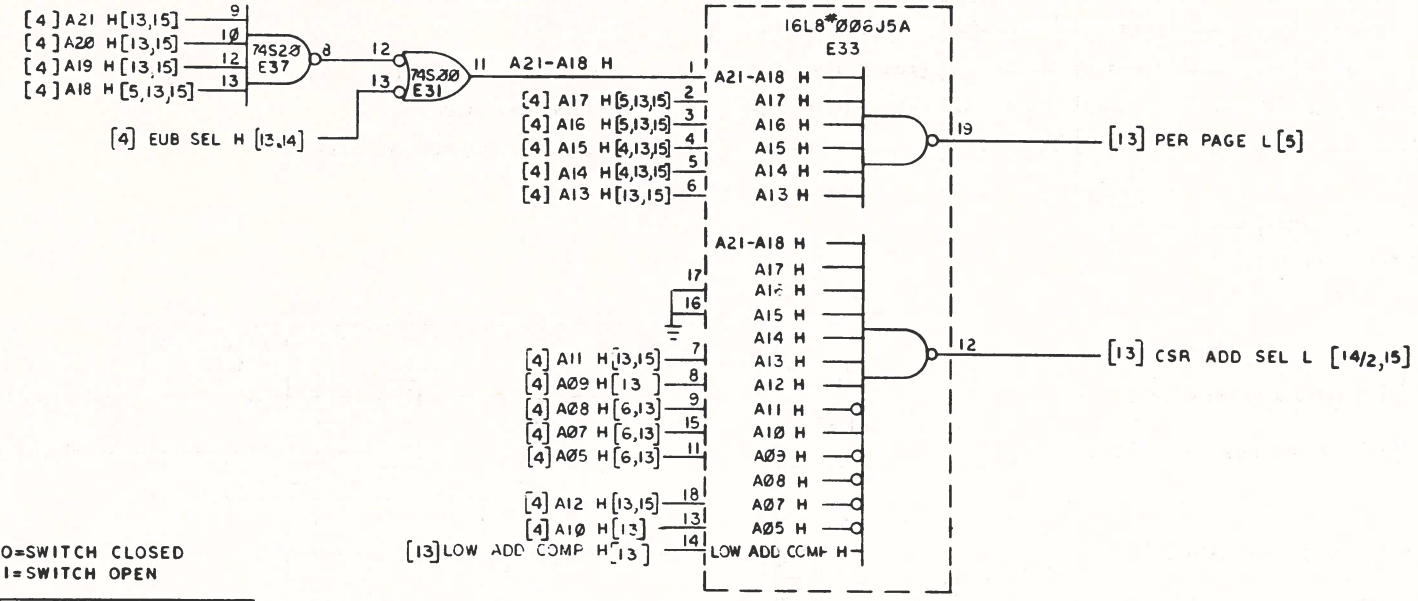
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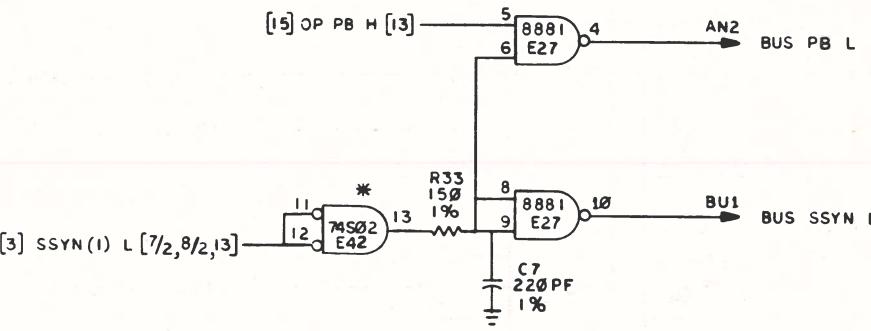
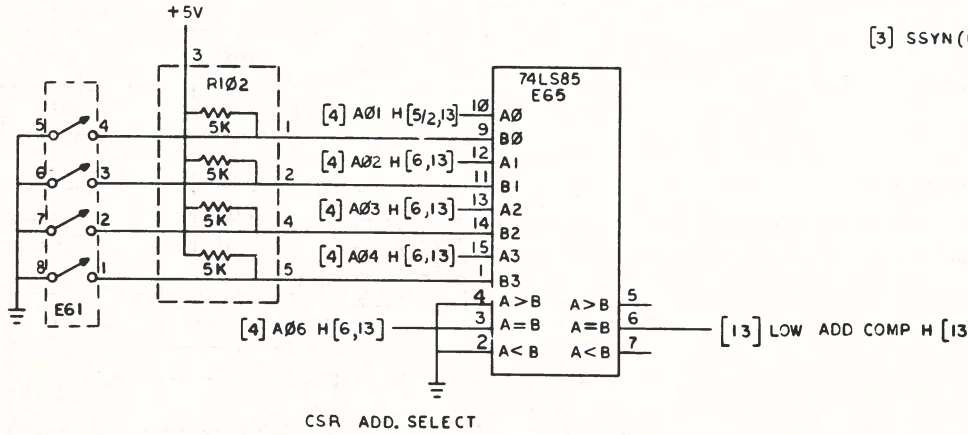
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE			SIZE CODE			NUMBER			REV.		
ECC MOS MEMORY (MS11M)			DCS			M8722-0-1			F		
SCALE 1/1			SHEET 12 OF 22			ML2					

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CSR ADDRESS	E61			
	A04 1	A03 2	A02 3	A01 4
772100	0	0	0	0
772102	0	0	0	1
772104	0	0	1	0
772106	0	0	1	1
772110	0	1	0	0
772112	0	1	0	1
772114	0	1	1	0
772116	0	1	1	1
772120	1	0	0	0
772122	1	0	0	1
772124	1	0	1	0
772126	1	0	1	1
772130	1	1	0	0
772132	1	1	0	1
772134	1	1	1	0
772136	1	1	1	1



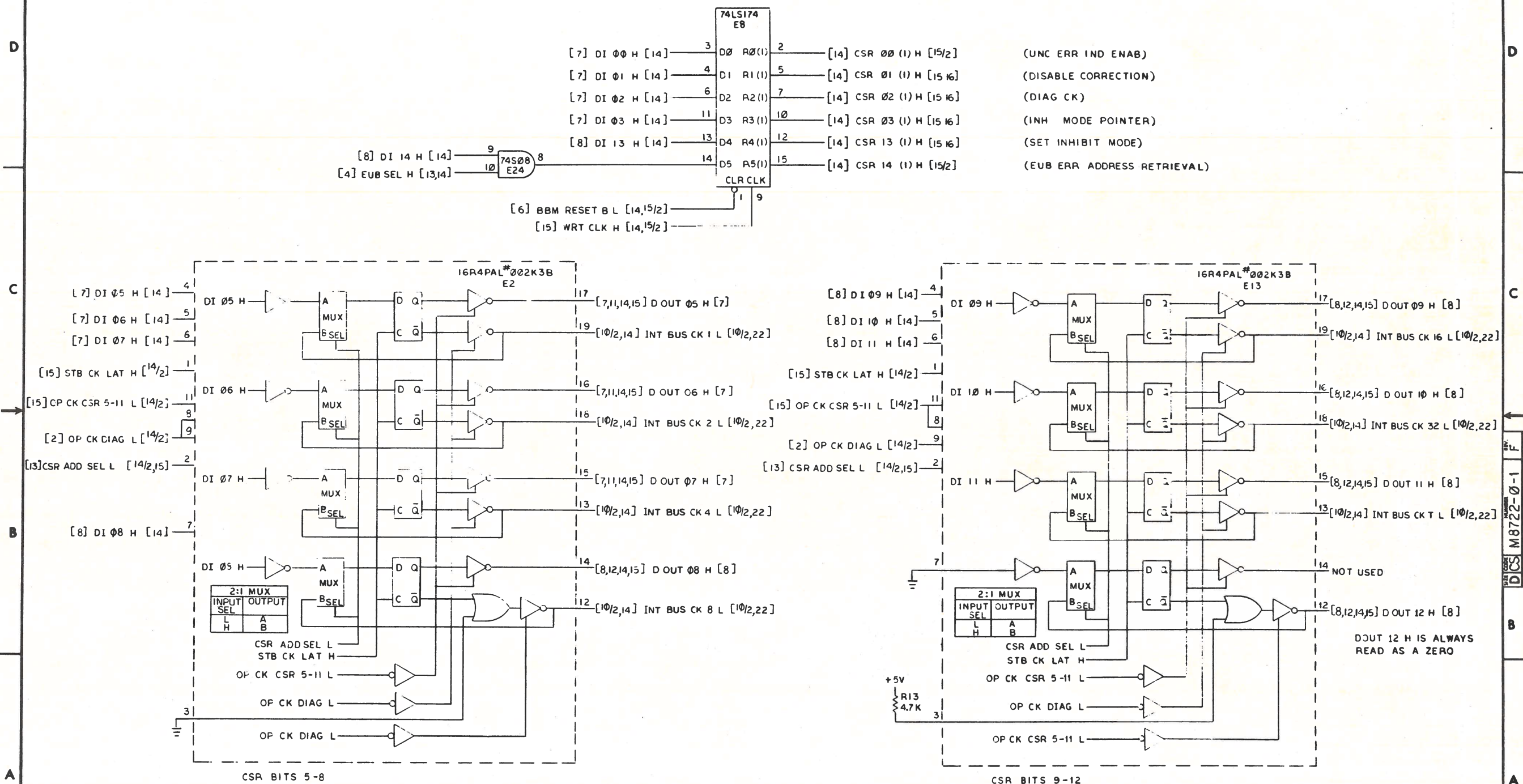
REVISIONS		
CHK	CHANGE NO.	REV.

(CSR ADDRESS SELECTION)

TITLE	SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)	D CS	M8722-0-1	F
SCALE	SHEET 13 OF 22	DIST.	

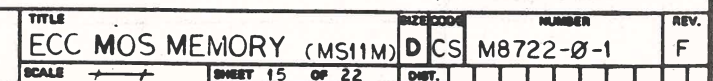
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1-0-2278W SC 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)		D CS	M 8722-0-1	F
SCALE	SHEET 14 OF 22	DIST.		



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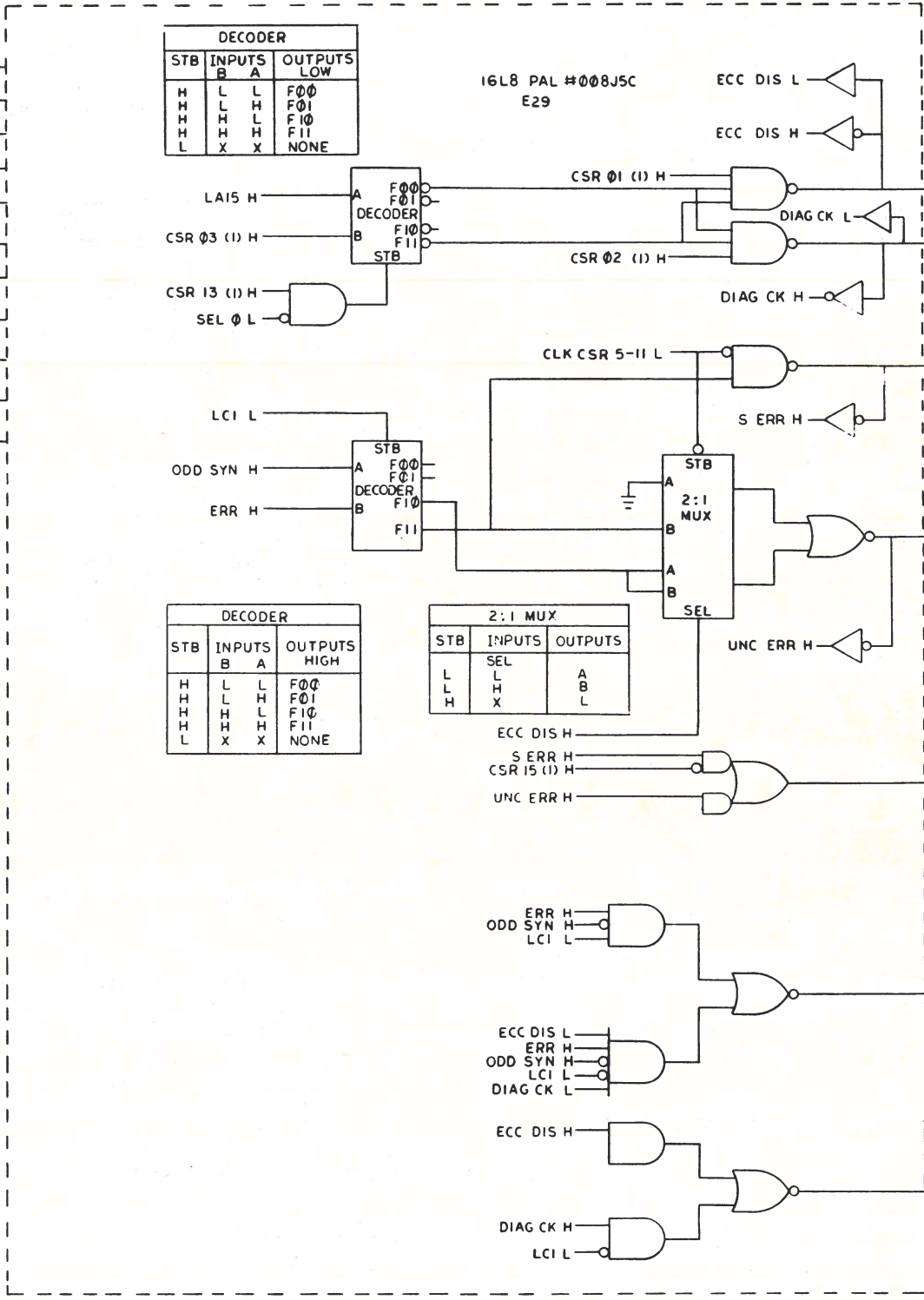
- [14] CSR 01 (1) H [15,16] 1
- [4] LA 15 H [6,16] 2
- [14] CSR 03 (1) H [15,16] 3
- [14] CSR 02 (1) H [15,16] 4
- [14] CSR 13 (1) H [15,16] 5
- [5] SEL 0 L [16] 6
- [10] ODD SYN H [10,16] 7
- [10] ERR H [3,16] 8
- [3] CLK CSR 5-11 L [15,16] 9
- [3] LCI L [2,5,16] 11
- [15] CSR 15 (1) H [15/2,16] 13

DECODER			
STB	INPUTS	A	OUTPUTS LOW
H	L	L	F00
H	L	H	F01
H	H	L	F10
H	H	H	F11
L	X	X	NONE

DECODER			
STB	INPUTS	A	OUTPUTS HIGH
H	L	L	F00
H	L	H	F01
H	H	L	F10
H	H	H	F11
L	X	X	NONE

16L8 PAL #008J5C
E29

2:1 MUX		
STB	INPUTS	OUTPUTS
L	SEL	A
L	H	B
H	X	L

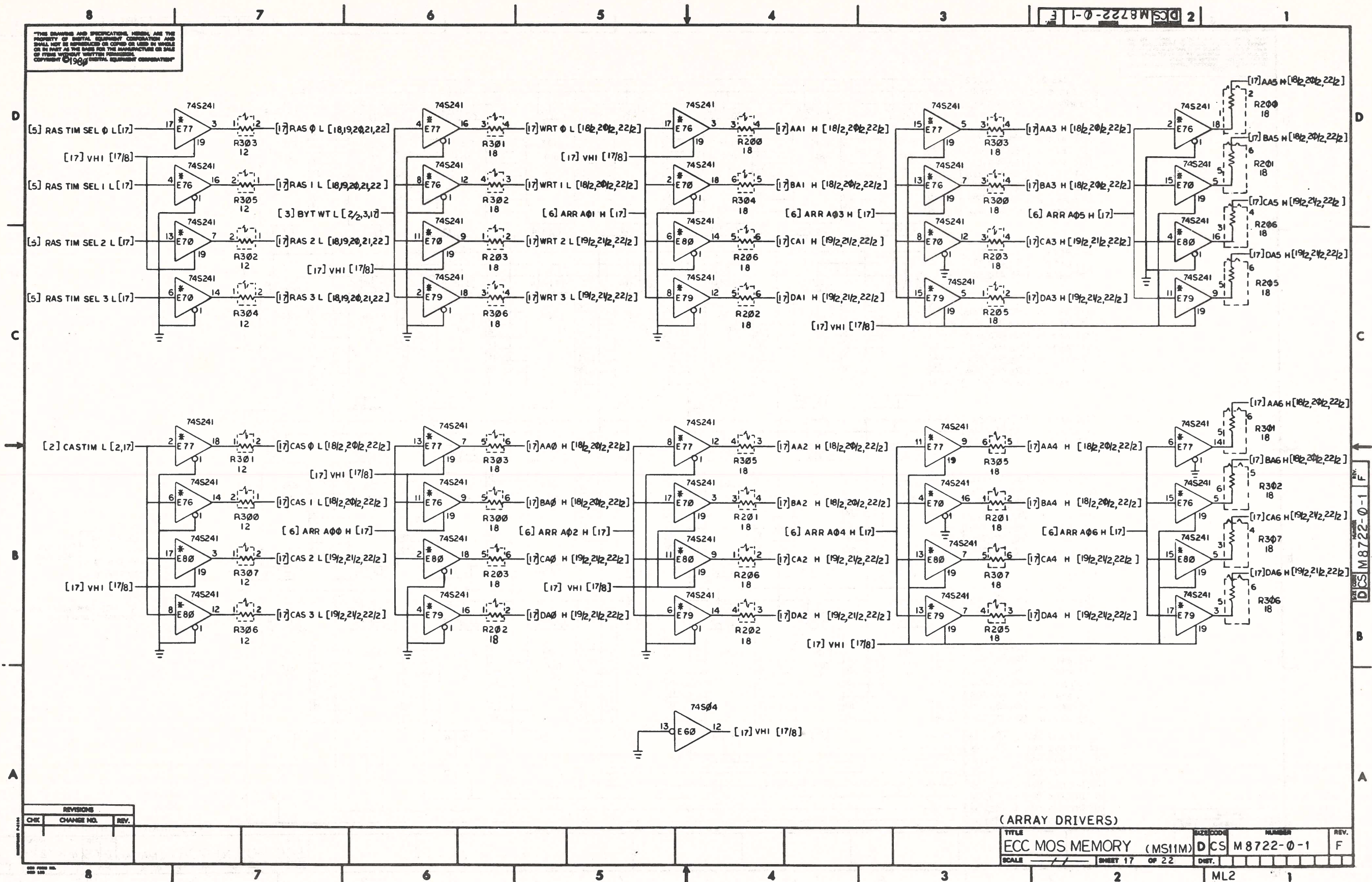


(ERROR CONTROL)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)	DCS	M 8722-0-1	F
SCALE	SHEET 16 OF 22	DIST.	

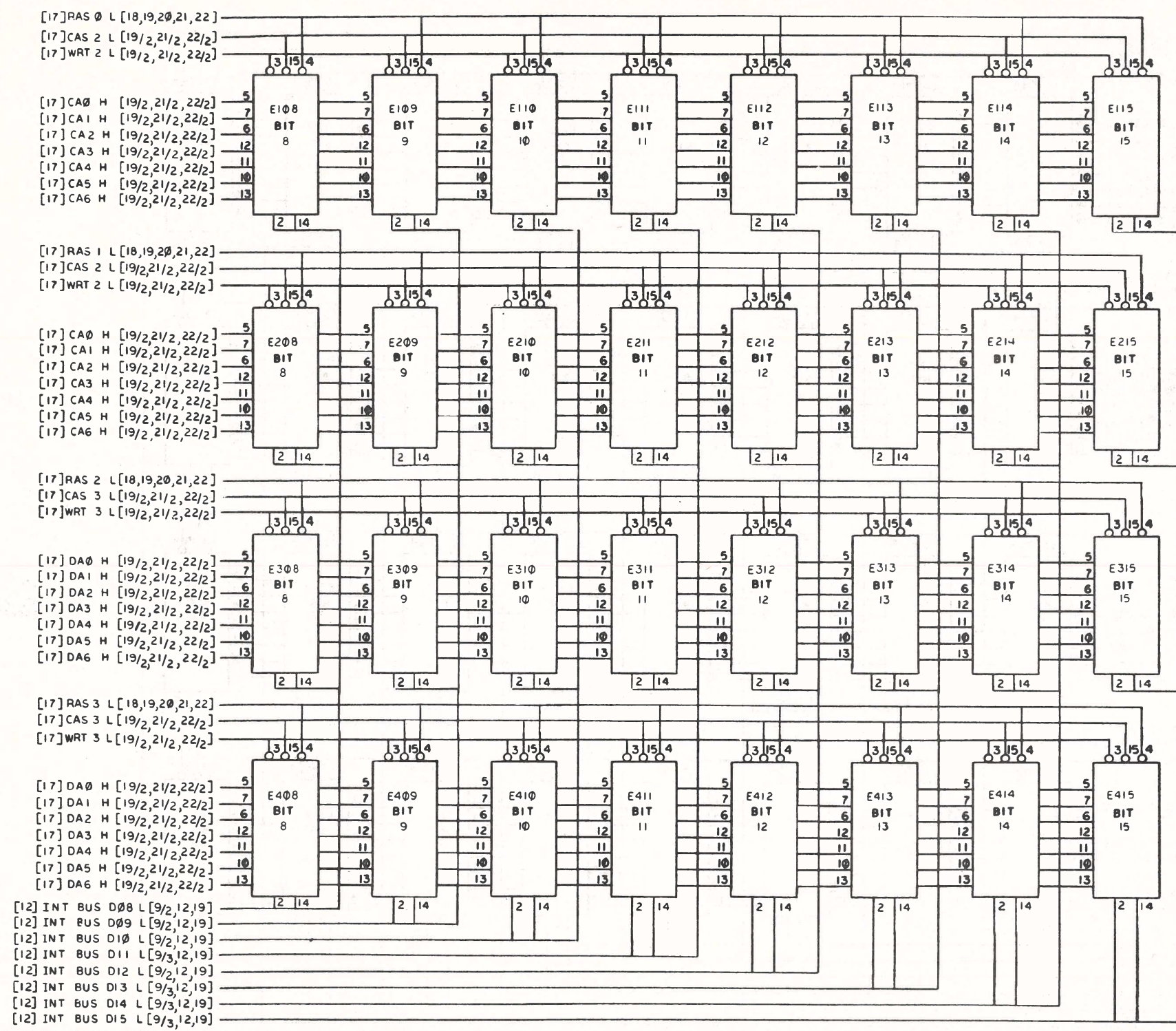
REVISIONS		
CHK	CHANGE NO.	REV.



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GND PIN 16 FOR 16K
-5V PIN 1 MOS RAM
+5V PIN 9
+12V PIN 8

NOTE: ALL MOS RAM VOLTAGES ARE BATTERY BACKED UP.

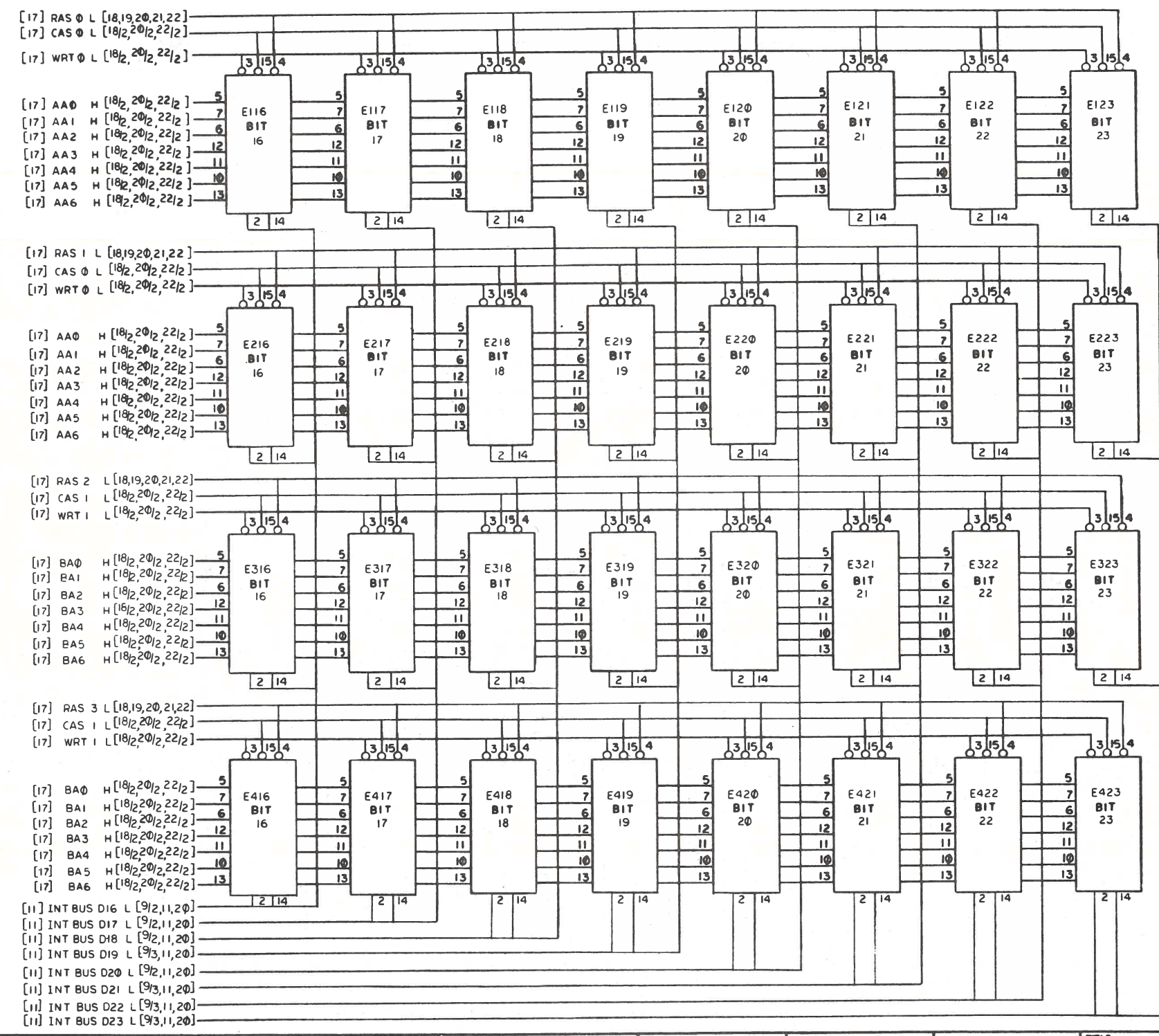
MOS ARRAY (DATA BYTE 1)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS11M)		D	CS M8722-0-1	F
SCALE	SHEET 19 OF 22	DIST.		

ML2

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GND PIN 16
- 5V PIN 1
+ 5V PIN 9
+ 12V PIN 8
FOR 16K
MOS RAM

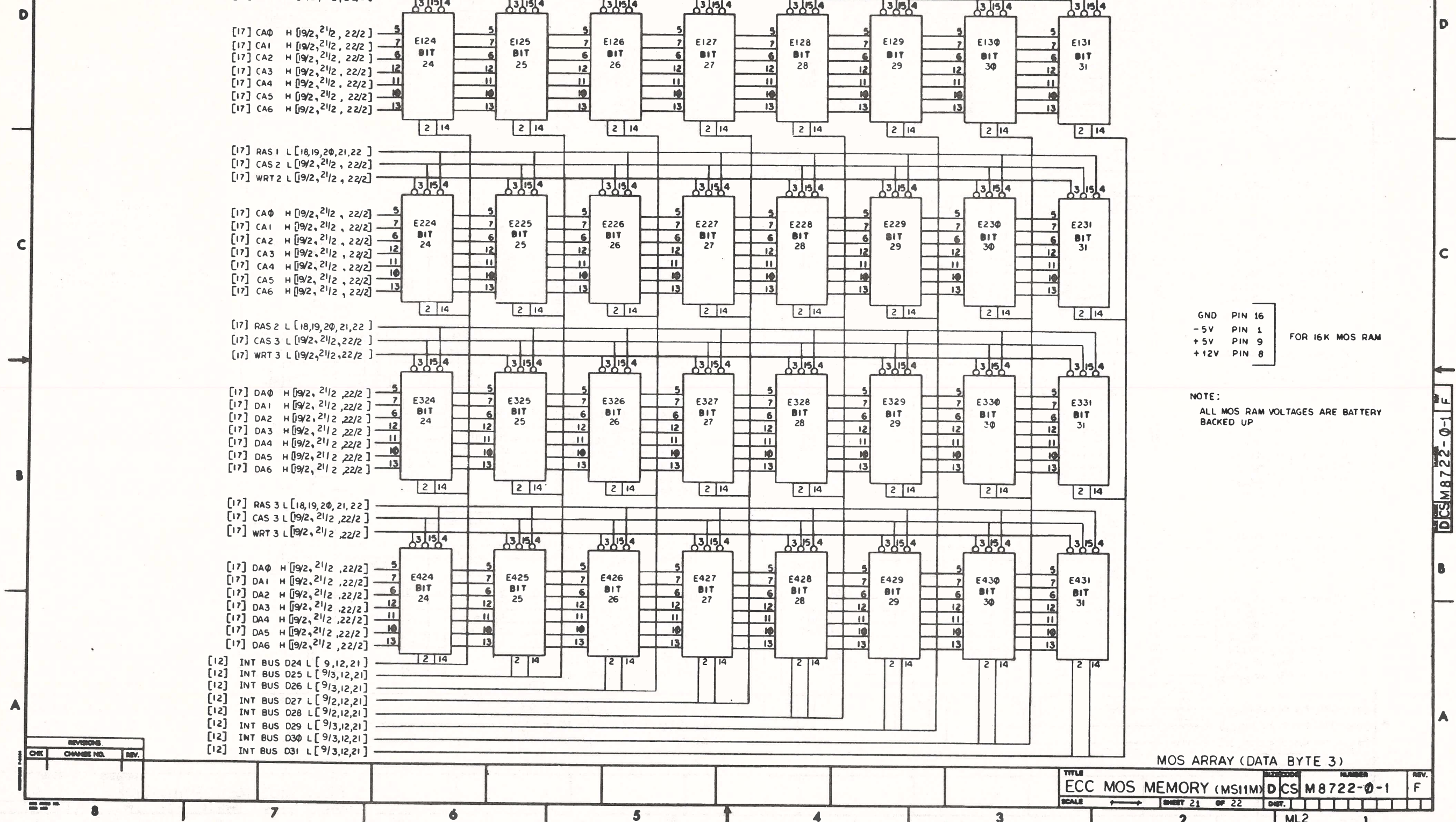
NOTE:
ALL MOS RAM VOLTAGES ARE BATTERY
BACKED UP

REVISIONS		
CHK	CHANGE NO.	REV.

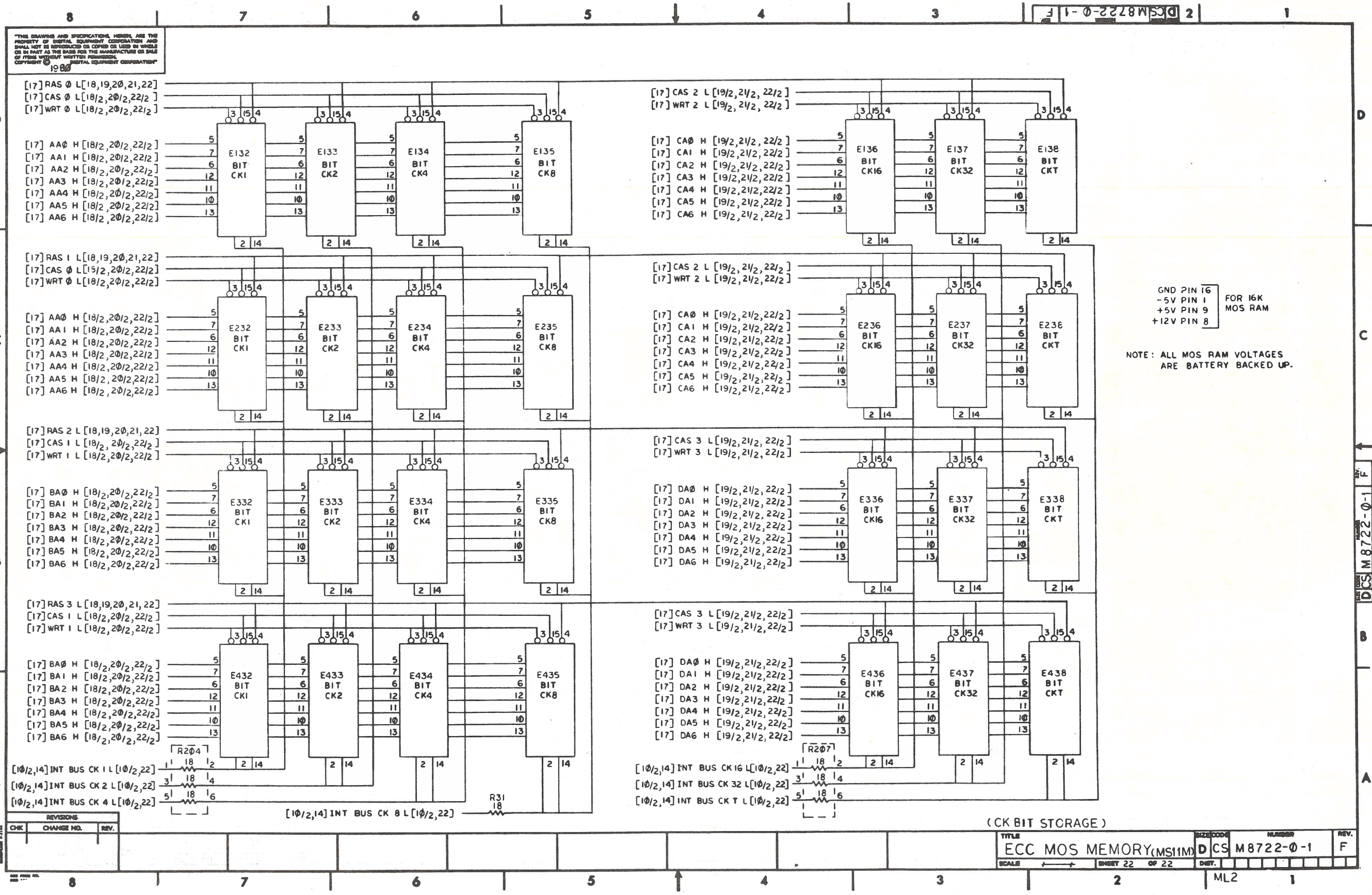
TITLE		SIZE CODE	NUMBER	REV.
ECC MOS MEMORY (MS1M)		DCS	M8722-0-1	F
SCALE		SHEET 20	OF 22	DIST.
ML2				

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DCS M8722-0-1 2



REVISIONS		
CHK	CHANGE NO.	REV.



DIGITAL EQUIPMENT CORPORATION PARTS LIST				QUANTITY / VARIATION												NOTES:		
MADE BY H. DARAKJIAN DATE 28 MAR 79		CHECKED D. HEALY DATE 26 DEC 79		SECTION 1		MS11-MA	MS11-MB	MS11-MC	MS11-MD									
ENG <i>John B. Manton</i> DATE 1-15-80		PROD <i>Bob Schaaf</i> DATE 1-15-80		ISSUED SECTION 1														
ITEM NO.	DRAWING NO.	PART NO.	DESCRIPTION															REF DESIGNATION
1	B-TC-MS11-M-1	MP00742	PRINT SET MS11-M	1	1	1	1											
2		EK-MS11M-UG	MS11-M ECC MOS MEMORY USERS GUIDE	1	1	1	1											
3		AC-F294A-MC	MS11-M & MS11-L DIAGNOSTIC LISTING	1	1	1	1											
4		AK-F293A-MC	PAPER TAPE	1	1	1	1											
E.C.O. NO.																		
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								SHEET 1 OF 1				INSERTION PARTS LIST DATA BASE REV						