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**NOTES:**

The M7942 uses all 512\*4 PROMS or all 256\*4 PROMS selection of the module is to one 4K bank for the 512\*4 part or to one 2K bank for the 256\*4 part. Within a bank any 512 or 256 word combinations (depending on type PROM) of memory may be enabled. Unenabled address groups are available to other devices.

**MODULES**

**JUMPERED ADDRESS SELECTION**

W15	W16	W17	4K RANGE	ADDRESS RANGE
IN	IN	IN	0-4K	00000-017776
IN	IN	OUT	4-8K	020000-037776
IN	OUT	IN	8-12K	040000-057776
IN	OUT	OUT	12-16K	060000-077776
OUT	IN	IN	16-20K	100000-117776
OUT	IN	OUT	20-24K	120000-137776
OUT	OUT	IN	24-28K	140000-167776
OUT	OUT	OUT	28-32K	160000-177776

**512\*4 PART**

W8	W9	W10	W11	W12	W13	W14
IN	IN	IN	OUT	OUT	OUT	OUT

**512\*4 PART**

PROMS OCTAL RANGE*	PHYSICAL ROW	JUMPER IN TO ENABLE RPLY
0 - 1777	CE0	W0
2000 - 3777	CE1	W1
4000 - 5777	CE2	W2
6000 - 7777	CE3	W3
10000 - 11777	CE4	W4
12000 - 13777	CE5	W5
14000 - 15777	CE6	W6
16000 - 17777	CE7	W7

**256\*4 PART**

W8	W9	W10	W11	W12	W13	W14
OUT	OUT	OUT	IN	IN	IN	OUT
OUT	OUT	OUT	IN	IN	OUT	IN

**256\*4 PART (LOWER 2K)**

OCTAL RANGE *	PHYSICAL ROW	JUMPER IN TO ENABLE RPLY
000000-00077	CE0	W0
001000-001777	CE4	W4
002000-002777	CE1	W1
003000-003777	CE5	W5
004000-004777	CE2	W2
005000-005777	CE6	W6
006000-006777	CE3	W3
007000-007777	CE7	W7

**256\*4 PART (UPPER 2K) JUMPER IN TO ENABLE REPLY**

OCTAL RANGE *	PHYSICAL ROW	JUMPER IN TO ENABLE RPLY
010000-010777	CE0	W0
011000-011777	CE4	W4
012000-012777	CE1	W1
013000-013777	CE5	W5
014000-014777	CE2	W2
015000-015777	CE6	W6
016000-016777	CE3	W3
017000-017777	CE7	W7

\*Add one of the following addresses corresponding to the modules jumpered address selection (beginning address) to the octal ranges above to determine the true octal range of a PROM:

ADDRESS RANGE	ADDRESS RANGE
000000	100000
020000	120000
040000	140000
060000	160000

**M7942 PROM BOARD BURNING SUMMARY**

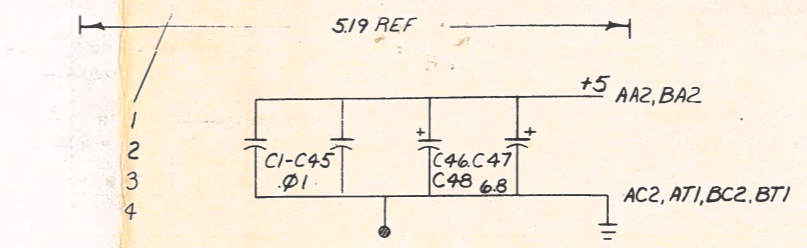
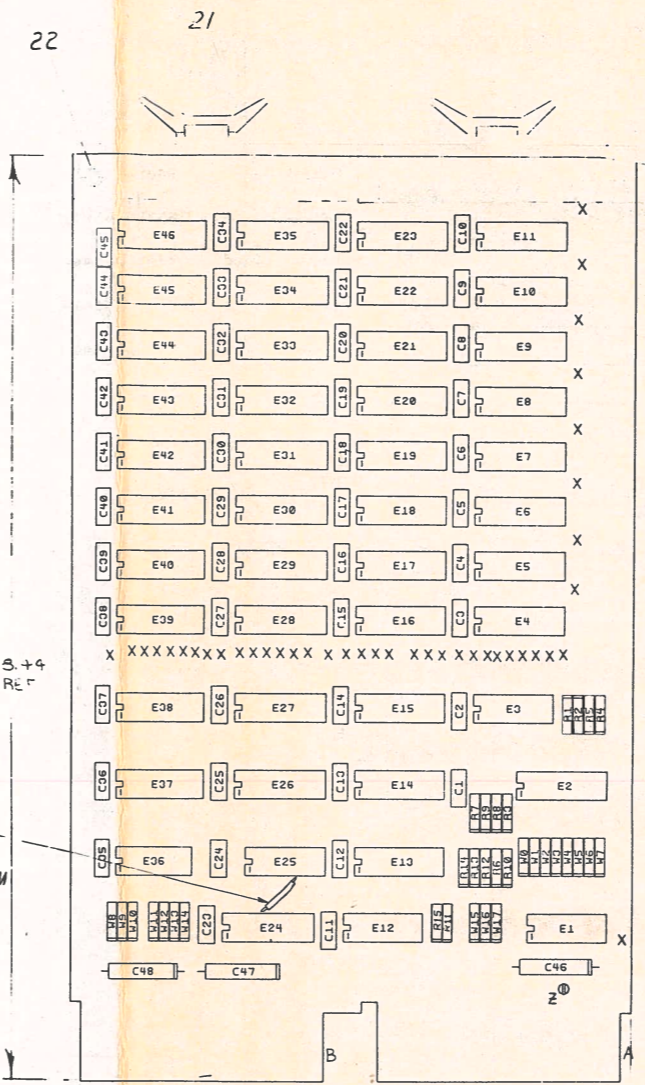
PROM OUTPUT PIN#	PDP-11 BIT #
9	3 7 11 15
10	2 6 10 14
11	1 5 9 13
12	0 4 8 12

A logic 1 data bit (corresponding to a 1 in any PDP-11 literature showing OP Codes or data) should assert high on the PROM output (data in true form). For virgin high parts like MMI do not burn data bits which want to be A1.

Address 0 puts all highs on PROM address pins. (PROM address is in negative logic)

PROM PIN	14	15	1	2	3	4	7	6	5
ADDR0	H	H	H	H	H	H	H	H	H
ADDR1	H	H	H	H	H	H	H	H	L
ADDR377	L	L	L	L	L	L	L	L	L

Varies most rapidly  
 INSTALL JUMPER FROM E24-13 TO E25-5



REF	DESCRIPTION	QTY	REF. DESIGNATION
REF	X-Y COORDINATE HOLE LOCATION	1	M-CO M7942-0-4
REF	ASSY, DRILLING HOLE LAYOUT	2	D-AH-M7942-0-5
REF	MODULE ECO HISTORY	3	B-MH-M7942-0-6
1	ETCHED CIRCUIT BOARD	5011562	
45	C1 THRU C45	CAPACITOR, 01, 100V, 20F DISC	1001610-01
3	C46, C47, C48	CAPACITOR, 6.8 35V, 10% TANT	1005306
13	R3 THRU R15	RESISTOR, 1K, 1/4W, 5%	1300365
1	R2	RESISTOR, 3.3K, 1/4W, 5%	1300439-00
1	R1	RESISTOR, 5.6K, 1/4W, 5%	1301874-00
18	NO THRU W17	JUMPER, INSULATED	9009185
1	E1	IC, DEC 7430	1905578-00
2	E26, E37	IC, DEC 7475	1909050-00
1	E2	IC, DEC 7442	1910046-00
3	E3, E25, E36	IC, DEC 7437	1910091-00
1	E14	IC, DEC 74174	1910652-00
5	E13, E15, E24, E27, E38	IC, DEC 8838	191117-00
1	E12	IC, DEC 8242	1909712
32	E4 THRU E11, E16 THRU E23 E28 THRU E35, E39 THRU E46	DEC 16 PIN SOCKET	1211813
1		SPLIT LUG	9006735
2		HANDLE FLIP CHIP MAGENTA	9008337-6
4		EYELET GS4-7	9006732

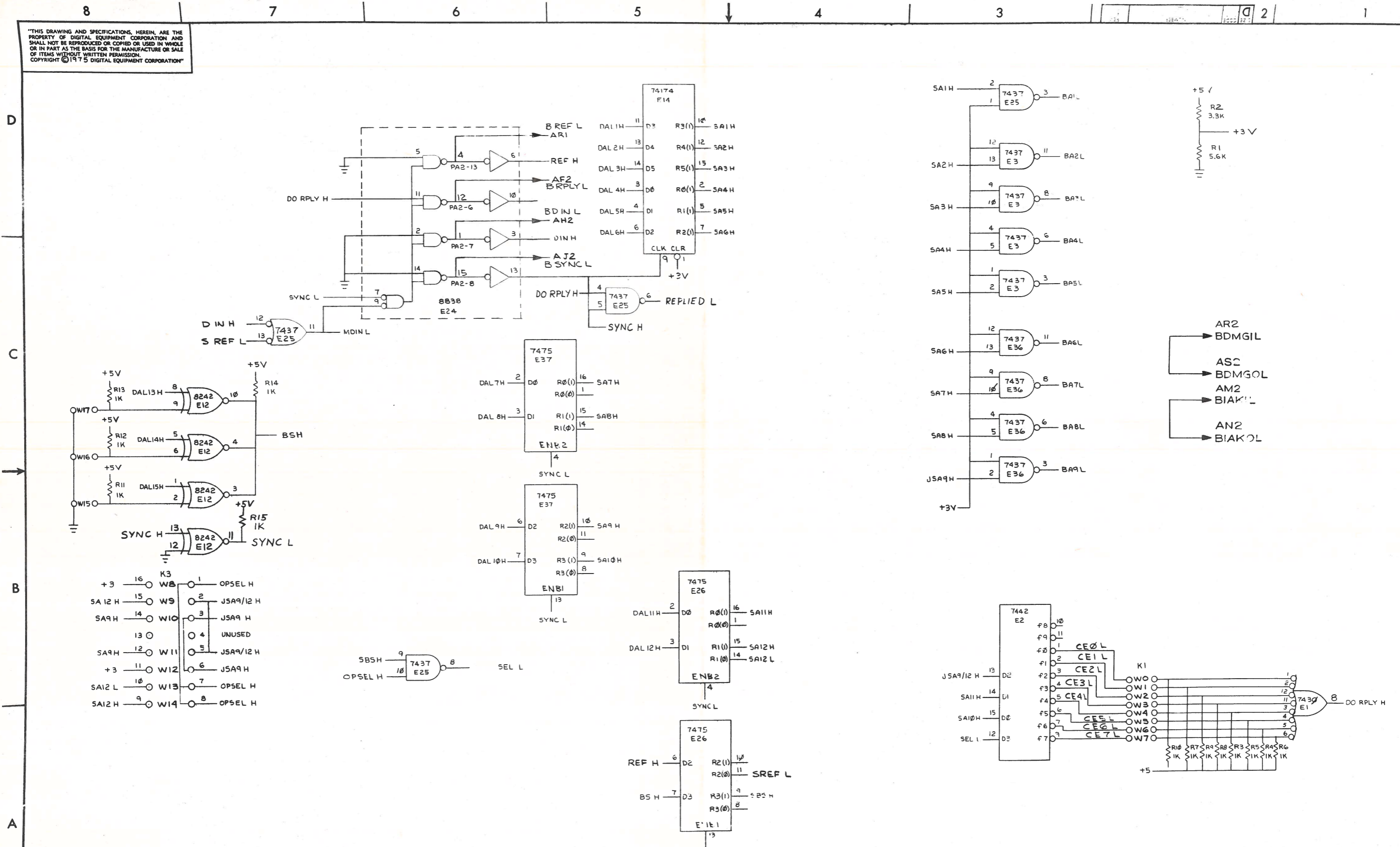
PROM	8	16
7442	8	16
8838	8	16
14174	8	16
1475	12	5
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

**IC PIN LOCATIONS**

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.											
	FIRST USED ON OPTION MODEL	PARTS LIST													
	LST-11	ETCH BOARD REV. D													
<table border="1"> <tr> <td>DRN. J. PHELPS</td> <td>DATE 5/1/77</td> <td rowspan="5"> </td> </tr> <tr> <td>CHK'D. R. FORTANE</td> <td>DATE</td> </tr> <tr> <td>ENG. W. ENGLISH</td> <td>DATE</td> </tr> <tr> <td>PROJ. ENG. A. ERICSON</td> <td>DATE</td> </tr> <tr> <td>PROD. W. ERICSON</td> <td>DATE</td> </tr> </table>					DRN. J. PHELPS	DATE 5/1/77		CHK'D. R. FORTANE	DATE	ENG. W. ENGLISH	DATE	PROJ. ENG. A. ERICSON	DATE	PROD. W. ERICSON	DATE
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ENG. W. ENGLISH	DATE														
PROJ. ENG. A. ERICSON	DATE														
PROD. W. ERICSON	DATE														
NEXT HIGHER ASSY			TITLE: 4K, 2K PROM												
DEC NO.		EIA NO.		SIZE CODE: DCSM7942 0 1											
SEMICONDUCTOR CONVERSION CHART		SCALE		REV. 0											
SHEET		OF													

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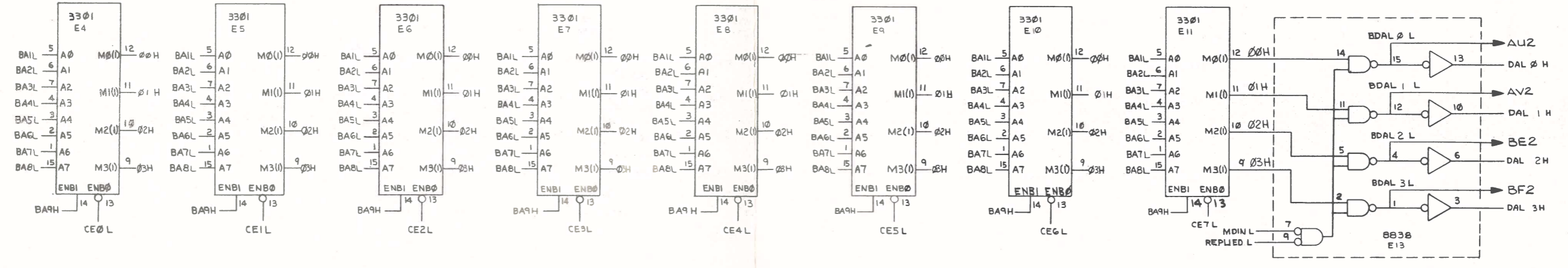
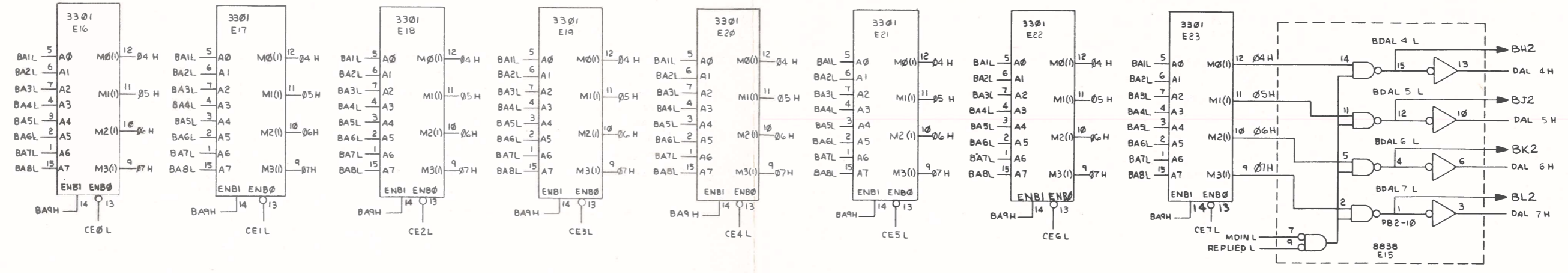


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4K/2K PROM	SIZE CODE	D CS	NUMBER	M7942-0-1	REV.	D
SCALE	++	SHEET	2	OF	4	DIST.	

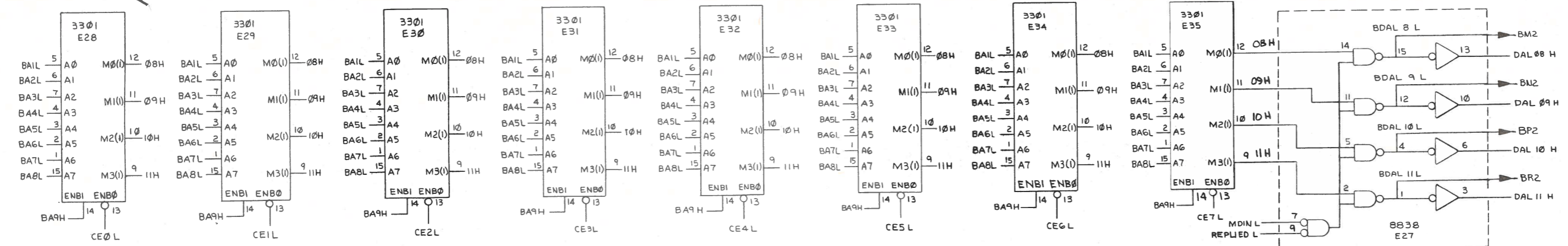
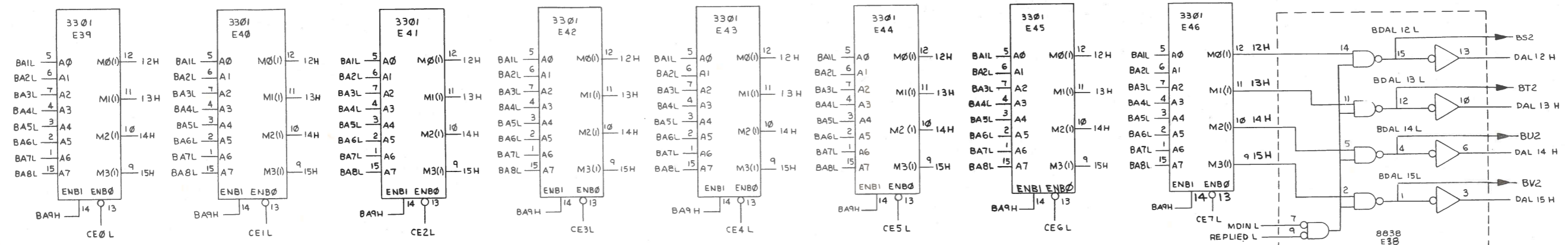
REV. D  
NUMBER M7942-0-1  
SIZE CODE DCS

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REVISIONS		
CHK.	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4K/2K PROM	SIZE CODE	D CS	NUMBER	M7942-0-1	REV.	D
SCALE	++	SHEET	+	OF	4	DIST.	

REV. D  
NUMBER DCS M7942-0-1