MSV11-D,-E
user's manual

MOSTEK
MK4116P-3

Use FRMTDY.SAV on 2-13
to format disks

597-1877

MSV11-D,-E
user's manual

EK-MSV1D-OP-001

digital equipment corporation • maynard, massachusetts

1st Edition, December 1977

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

FIGURES

TABLES

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This manual contains all user information required for installing and using MSV11-D and MSV11-E LSI-11 memory options in LSI-11 microcomputer systems. MSV11-D and MSV11-E models are summarized below.

Model	Memory Capacity (1)	Module	Parity Bits (2)
MSV11-DA	4K by 16 bits	M8044-AA	no
MSV11-DB	8K by 16 bits	M8044-BA	no
MSV11-DC	16K by 16 bits	M8044-CA	no
MSV11-DD	32K by 16 bits	M8044-DA	no
MSV11-EA	4K by 18 bits	M8045-AA	yes
MSV11-EB	8K by 18 bits	M8045-BA	yes
MSV11-EC	16K by 18 bits	M8045-CA	yes
MSV11-ED	32K by 18 bits	M8045-DA	yes

NOTES

1. K = 1024 (e.g., 4K - 4096)

2. Memory models that include parity bits are for future LSI-11 microcomputer models. Sixteen computer word bits plus two parity bits (one for each 8-bit memory byte) compose the 18-bit capacity for each memory location.

1.2 GENERAL DESCRIPTION

All MSV11-D and MSV11-E memory models are LSI-11 bus-compatible "doubleheight" (two sets of backplane pins) modules (printed circuit assemblies) that plug into any LSI-11 bus-structured backplane. An MSV11-DD module is shown in Figure 1-1.

Memory storage is provided by either 4K by 1 bit or 16K by 1 bit integrated circuits, depending on model. The integrated circuits are dynamic metal oxide semiconductor (MOS) types that the LSI-11 microcomputer can access during read and write operations. Memory contents are volatile; that is, when operating power is lost, memory data is lost. However, memory contents can be protected during system power failures by supplying battery backup power.

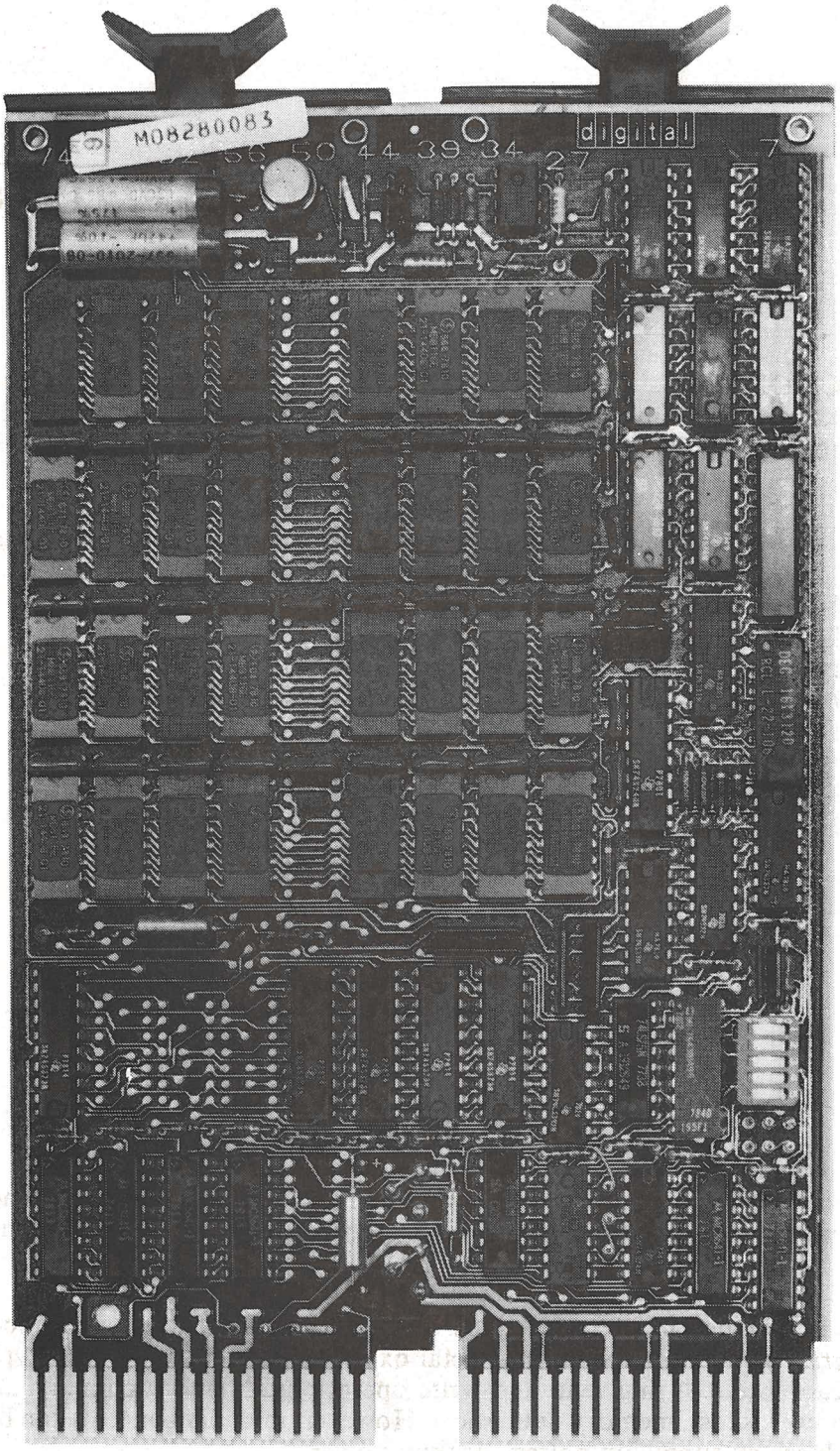


Figure 1-1 MSV11-DD 32K by 16-Bit Read/Write Memory

MSV11-D and MSV11-E memory modules feature:

1. On-board memory refresh, eliminating the need for refresh signals on the LSI-11 bus.
2. The system memory address space to which the module will respond is user-configured via switches contained on the module. An address can start at any 4K bank boundary ranging through the 0–128K address range.
3. Memory modules perform DATI, DATO, DATOB, DATIO, AND DATIOB bus cycles according to LSI-11 bus protocol.
4. No special power is required. Only the normal +5 V and +12 V present on the LSI-11 backplane are necessary. An on-board charge pump circuit produces the necessary –5 V operating voltage for the memory integrated circuits.
5. Jumpers allow the user to implement battery backup power.
6. Memory access is disabled when "Bank 7" is addressed (BBS7 L is asserted) or when "external" memory refresh bus cycles are in progress. The lower 2K of Bank 7 can be enabled by a user-installed jumper. (Bank 7, the upper 4K system address space, is normally reserved for peripheral device addressing.)

1.3 SPECIFICATIONS

1.3.1 Electrical

Power Requirements

Model	Supply Voltage	Operating Power Typical	Operating Power Maximum	Standby Power Typical	Standby Power Maximum
MSV11-DA,-DC (4K or 16K)	+5V System Power	1.7A,8.5W	1.9A,9.5W	1.7A,8.5W	1.9A,9.5W
	+5V Battery Backup	0.7A,3.5W	0.8A,4.0W	0.7A,3.5W	0.8A,4.0W
	+12V System Power or Battery Backup	0.34A,4.0W	0.38A,4.6W	.06A,0.7W	.07A,0.9W
MSV11-DB,-DD (8K or 32K)	+5V System Power	1.7A,8.5W	1.9A,9.5W	1.7A,8.5W	1.9A,9.5W
	+5V Battery Backup	0.7A,3.5W	0.8A,4.0W	0.7A,3.5W	0.8A,4.0W
	+12V System Power or Battery Backup	0.37A,4.5W	0.41A,4.9W	.08A,1.0W	0.1A,1.2W
MSV11-EA,-EB (4K or 16K)	+5V System Power	2.0A,10W	2.2A,11W	2.0A,10W	2.2A,11W
	+5V Battery Backup	1.0A,5W	1.2A,6W	1.0A,5W	1.2A,6W
	+12V System Power or Battery Backup	0.38A,4.6W	0.42A,5.0W	.06A,0.7W	.07A,0.9W
MSV11-EC,-ED (8K or 32K)	+5V System Power	2.0A,10W	2.2A,11W	2.0A,10W	2.2A,11W
	+5V Battery Backup	1.0A,5W	1.2A,6W	1.0A,5W	1.2A,6W
	+12V System Power or Battery Backup	0.41A,4.9W	0.46A,5.5W	.09A,1.1W	.11A,1.3W

Bus Loading

AC load = 2
DC load = 1

Operating Speed

MSV11-D Models

Bus Cycle Type	Access Time (ns) Typ	Max	Notes	Cycle Time (ns) Typ	Max	Notes
DATI	210	225	1,2	500	520	1,4
DATO(B)	100	110	1,2	545	565	1,5
DATIO(B)	630	650	1,3	1075	1100	1,6

MSV11-E Models

Bus Cycle Type	Access Time (ns) Typ	Max	Notes	Cycle Time (ns) Typ	Max	Notes
DATI	250	265	1,2	500	520	1,4
DATO(B)	100	110	1,2	545	565	1,5
DATIO(B)	670	690	1,3	1115	1140	1,6

All Models

Refresh cycle time (7) 575 ns typ., 600 ns max.

NOTES

1. **All operating speeds are in nanoseconds and are based on memory not busy and no refresh arbitration. Refresh arbitration adds 100 ns typical (120 ns maximum) to access and cycle times. Refresh conflicts add 575 ns typical (600 ns maximum) to access and cycle times.**

2. **Access times defined as internal SYNC H to RPLY H with minimum times (25 or 50 ns) from SYNC H to DIN H or DOUT H. The DATO(B) access and cycle times assume a minimum 50 ns from SYNC H to DOUT H at bus receiver outputs. For actual LSI-11 bus measurements, 150 ns should be added to DATO(B) times, i.e., access time (typical) = 100 + 150 = 250 ns.**

3. **Access times defined as internal SYNC H to RPLY H (DATO(B)) with minimum time (25 ns) from SYNC H to DIN H, and minimum time (350 ns) from RPLY H (DATI) asserted to DOUT H asserted.**

4. **Cycle times defined as internal SYNC H to LOCKOUT L negated.**

5. **Cycle times defined as internal SYNC H to LOCKOUT L negated with minimum time (50 ns) from SYNC H to DOUT H.**

6. **Cycle times defined as internal SYNC H to LOCKOUT L (DATO(B)) with minimum times (25 ns) from SYNC H to DIN H and minimum time (350 ns) from RPLY H (DATI) asserted to DOUT asserted.**

7. **Refresh cycle time defined as internal REF REQ L to LOCKOUT L negated.**

1.3.2 Environmental

Operating: 5° to 50° C (41° to 122° F) with a relative humidity of 10% to 95% (no condensation), with adequate airflow across the module. When operating at the maximum temperature (50° C or 122° F), air flow must maintain the inlet to outlet air temperature rise across the modules to 7° C (12.5° F), maximum. During battery backup operation, the temperature must be maintained within the normal operating temperature range.

Storage: –40° to 66° C (–40° to 151° F) with a relative humidity of 10% to 90% (no condensation).

NOTE

Before operating a module that has been stored in an environment outside the specified operating environment, the module must be allowed to stabilize at the operating temperature for 5 minutes (minimum).

1.3.3 Physical Size

Height	13.2 cm (5.2 in)
Length	22.8 cm (8.9 in)
Width	1.27 cm (0.5 in)

NOTE

Length as stated is approximate and includes plastic handles. Actual module length is 21.6 cm (8.5 in).

1.3.4 Backplane Pinning Utilization

MSV11-D and MSV11-E backplane pin utilization is shown in Table 1-1. Blank spaces indicate pins not used.

Table 1-1 Backplane Pin Utilization

A Connector			B Connector		
Side 1	Pin	Side 2	Side 1	Pin	Side 2
	A	+5 V	BDCOK H	A	+5 V
	B			B	
BDAL16 L	C	GND		C	GND
BDAL17 L	D	+12 V		D	+12 V
	E	BDOUT L		E	BDAL02 L
	F	BRPLY L		F	BDAL03 L
	H	BDIN L		H	BDAL04 L
GND	J	BSYNC L	GND	J	BDAL05 L
REF KILL L	K	BWTBT L	-5 V	K	BDAL06 L
	L		-5 V	L	BDAL07 L
GND	M	BIAKI L	GND	M	BDAL08 L
	N	BIAKO L		N	BDAL09 L
	P	BBS7 L		P	BDAL10 L
BREF L	R	BDMGI L		R	BDAL11 L
+12 B	S	BDMGO L		S	BDAL12 L
GND	T		GND	T	BDAL13 L
	U	BDAL00 L		U	BDAL14 L
+5 B	V	BDAL01 L	+5 V	V	BDAL15 L

1.4 RELATED HARDWARE MANUALS

Title	Document No.	Notes
Microcomputer Handbook	EB-07948-53/77	Available on hard copy.
PDP-11V03 System Manual	EK-11V03-TM-002	Available on hard copy.
PDP-11T03 System Manual	EK-11T03-OP-001	Available on hard copy.

These documents can be ordered from:

DIGITAL EQUIPMENT CORPORATION
444 Whitney Street
Northboro, MA 01532

ATTENTION: COMMUNICATIONS SERVICES (NR2/M15)
CUSTOMER SERVICES SECTION

CHAPTER 2
INSTALLATION

2.1 GENERAL

This chapter contains information required for configuring and installing the MSV11-D or MSV11-E in the LSI-11 system backplane. Configuring the module involves selecting the module's address range via switches, and other functional operations implemented or disabled via jumpers. Proper installation will ensure normal operation in the system and eliminate the possibility of physical damage to the module or backplane in which it is installed. Details are provided in the following paragraphs.

NOTES

1. **If the MSV11-D or MSV11-E memory module is installed in a system that contains an LSI-11 processor module etch revision C or D, CS revision H2 or earlier, BDAL16 L and BDAL17 L bus lines (AC1 and AD1, respectively) must be terminated. This is accomplished by installing DEC ECO number M7264-00018.**

2. **Each MSV11-D or -E module contains two factory-installed wire-wrap jumpers that select memory size (4K, 8K, 16K, or 32K,); these jumper configurations normally should not be changed.**

2.2 CONFIGURING MODULE SWITCHES AND JUMPERS

2.2.1 General

Configuring the MSV11-D or MSV11-E will alter its operation for a specific system application. The following items can be configured.

1. Select the starting address for the contiguous memory contained on the module.
2. Battery backup power.
3. Enable/disable 2K word portion of Bank 7.

2.2.2 Address Selection

The MSV11-D or MSV11-E address can start at any 4K bank boundary. The address configured is the starting address for the contiguous portion of memory (4K, 8K, 16K, or 32K) contained on the module. Set the switches, located as shown on Figure 2-1, to the desired starting address as listed in Table 2-1. Note that the module is designated to accommodate a 128K system addressing capability; however, the present addressing capability of the LSI-11 system, including all PDP11/03, PDP-11V03 and PDP-11T03 systems, is 32K. By PDP-11 convention, the upper 4K address space is normally reserved for peripheral device and register addresses. Thus, with the present LSI-11 maximum addressing capability of 32K, Bank 7 (addresses 160000-177777) normally should not be used for system memory.

Factory-configured modules will not respond to Bank 7 addresses. In special applications that permit the use of the lower 2K portion of Bank 7 for system memory, enable the lower 2K portion of Bank 7 by removing the jumper from wire wrap pins 1 and 3 and connecting a new jumper from 1 to 2.

2.2.3 Battery Backup Power

MSV11-D and MSV11-E modules are factory-configured with power jumpers installed for normal system power, only. If the system uses a battery backup power source, remove jumpers W2 and W3. Install new jumpers W4 and W5. (Two jumpers are removed and two new jumpers are installed.)

2.2.4 Parity

One jumper is factory-installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on model. Do not reconfigure this jumper. Standard jumper configurations are listed below for reference purposes.

All MSV11-D models: Jumper installed from pin 7 to pin 5.
All MSV11-E models: Jumper installed from pin 6 to pin 5.

2.2.5 Memory Size

Two jumpers are factory-installed to configure addressing logic for memory size (number and type of memory integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below for reference purposes.

		Jumpers (two installed)	
	Models	**Memory Range Pins**	**Memory Select Pins**
	MSV11-DA, -EA	From 17 to 15	From 17 to 14
	MSV11-DB, -EB	From 17 to 15	From 12 to 14
NOW →	MSV11-DC, -EC	From 16 to 15	From 16 to 14
LATER →	MSV11-DD, -ED	From 16 to 15	From 10 to 14

2.3 MODULE INSTALLATION IN SYSTEM BACKPLANE

Memory modules, including MSV11-D and MSV11-E models, are not priority-dependent; thus, the module can be installed in any option slot in the LSI-11 system backplane.

CAUTION

1. **The memory module and/or backplane connector blocks can be damaged if the module is installed backwards. Ensure that the component side of the module faces in the same direction as other LSI-11 system modules (described in detail in the Microcomputer Handbook, Section 1, Paragraph 6.4).**

2. **DC power must be removed from the backplane during module insertion or removal.**

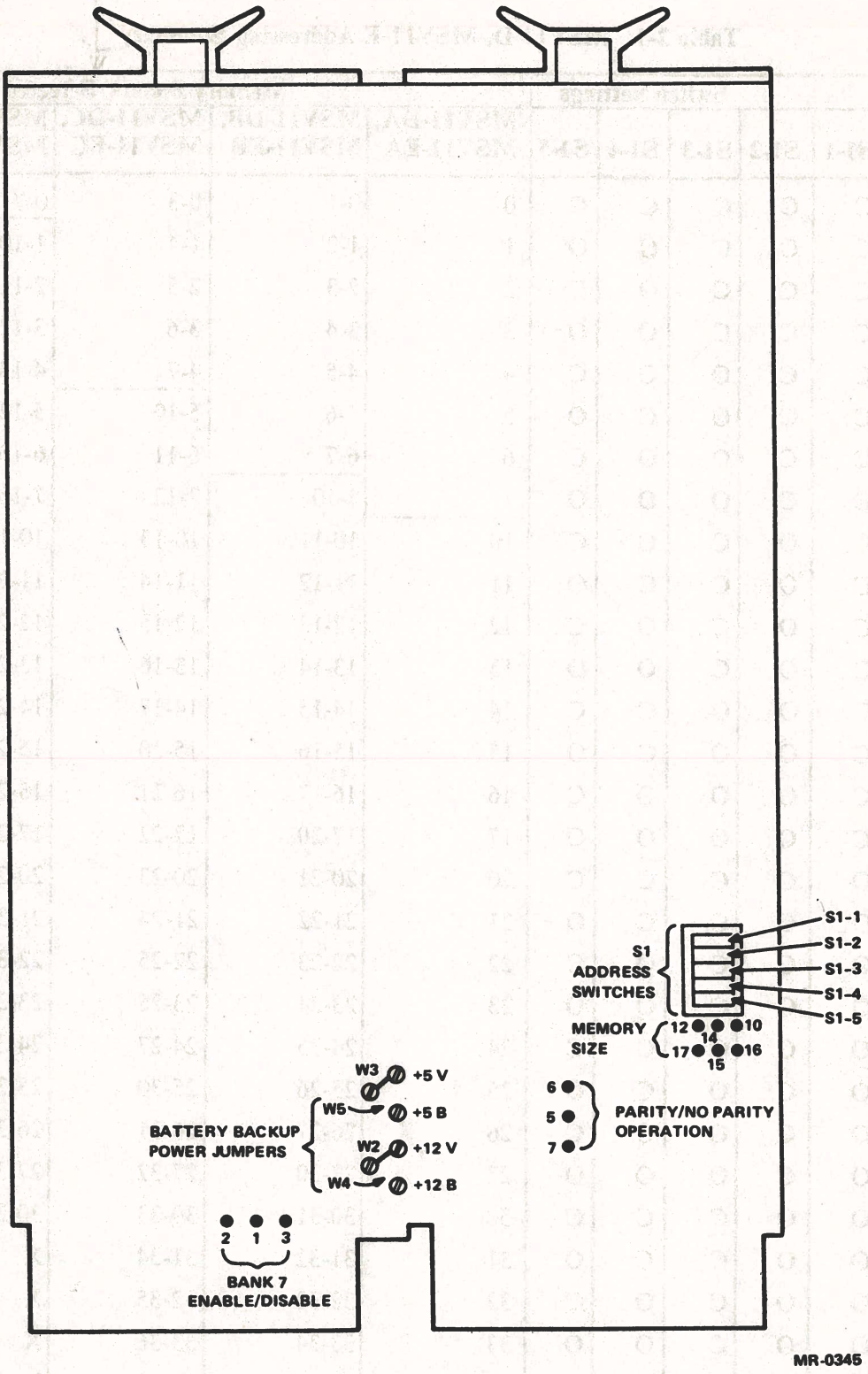


Figure 2-1 MSV11-D, MSV11-E Switch and Jumper Locations

Table 2-1 MSV11-D, MSV11-E Addressing Summary

Starting Address	Switch Settings					Memory Bank(s) Selected			
	S1-1	S1-2	S1-3	S1-4	S1-5	MSV11-DA, MSV11-EA	MSV11-DB, MSV11-EB	MSV11-DC, MSV11-EC	MSV11-DD, MSV11-ED
0	C	C	C	C	C	0	0-1	0-3	0-7
20000	C	C	C	C	O	1	1-2	1-4	1-10
40000	C	C	C	O	C	2	2-3	2-5	2-11
60000	C	C	C	O	O	3	3-4	3-6	3-12
100000	C	C	O	C	C	4	4-5	4-7	4-13
120000	C	C	O	C	O	5	5-6	5-10	5-14
140000	C	C	O	O	C	6	6-7	6-11	6-15
160000	C	C	O	O	O	7	7-10	7-12	7-16
200000	C	O	C	C	C	10	10-11	10-13	10-17
220000	C	O	C	C	O	11	11-12	11-14	11-20
240000	C	O	C	O	C	12	12-13	12-15	12-21
260000	C	O	C	O	O	13	13-14	13-16	13-22
300000	C	O	O	C	C	14	14-15	14-17	14-23
320000	C	O	O	C	O	15	15-16	15-20	15-24
340000	C	O	O	O	C	16	16-17	16-21	16-25
360000	C	O	O	O	O	17	17-20	17-22	17-26
400000	O	C	C	C	C	20	20-21	20-23	20-27
420000	O	C	C	C	O	21	21-22	21-24	21-30
440000	O	C	C	O	C	22	22-23	22-25	22-31
460000	O	C	C	O	O	23	23-24	23-26	23-32
500000	O	C	O	C	C	24	24-25	24-27	24-33
520000	O	C	O	C	O	25	25-26	25-30	25-34
540000	O	C	O	O	C	26	26-27	26-31	26-35
560000	O	C	O	O	O	27	27-30	27-32	27-36
600000	O	O	C	C	C	30	30-31	30-33	30-37
620000	O	O	C	C	O	31	31-32	31-34	X
640000	O	O	C	O	C	32	32-33	32-35	X
660000	O	O	C	O	O	33	33-34	33-36	X
700000	O	O	O	C	C	34	34-35	34-37	X
720000	O	O	O	C	O	35	35-36	X	X
740000	O	O	O	O	C	36	36-37	X	X
760000	O	O	O	O	O	37	X	X	X

NOTES

1. **Switch settings:**

   C = ON
   O = OFF

2. **Dotted lines indicate present upper address limit in LSI-11 systems.**

3. **Bank 7 cannot be selected as factory configured; however, the user can enable the lower 2K portion of bank 7 for use as directed in Paragraph 2.2.2.**

4. **X = Do not use.**

CHAPTER 3
TECHNICAL DESCRIPTION

3.1 GENERAL

Logic functions and circuits that comprise MSV11-D and MSV11-E memory modules are shown on Figure 3-1. Both types of memory modules are identical, with the exception that MSV11-E models include parity logic; MSV11-D models do not include parity.

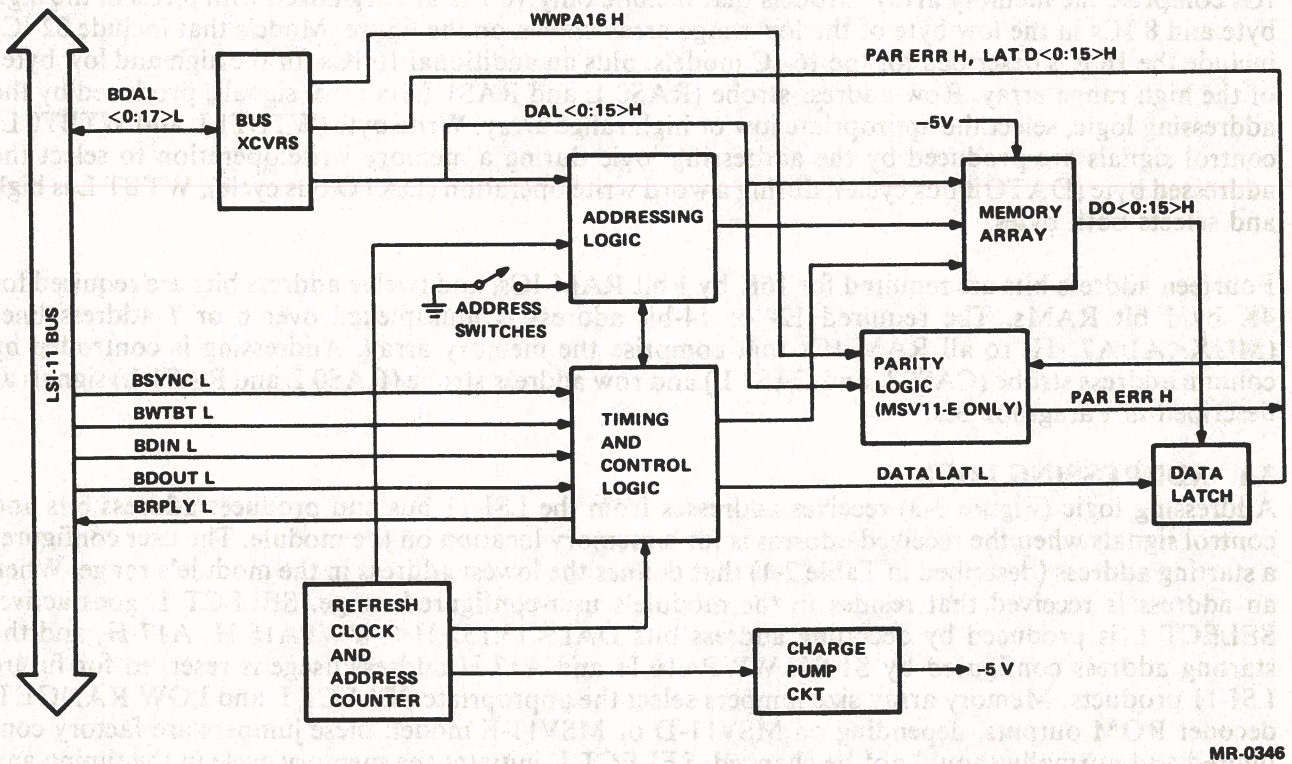


Figure 3-1 MSV11-D and MSV11-E Logic Functions

3.2 MEMORY ARRAY

The memory array is the main function contained on the module. Depending on model, the module will contain 16 or 32 dynamic random access memory (RAM) integrated circuits (ICs); in addition, MSV11-E models include an additional two or four RAM ICs, depending on model, as part of the parity logic. All RAM ICs will be identical types for a given model. Two types are used: 4K by 1 bit and 16K by 1 bit. The number and type of RAMs used are listed for each memory model as follows.

Model	RAM IC Type	Qty RAM ICs In Memory Array	Qty RAM ICs In Parity Logic
MSV11-DA	4K × 1	16	none
MSV11-DB	4K × 1	32	none
MSV11-DC	16K × 1	16	none
MSV11-DD	16K × 1	32	none
MSV11-EA	4K × 1	16	2
MSV11-EB	4K × 1	32	4
MSV11-EC	16K × 1	16	2
MSV11-ED	16K × 1	32	4

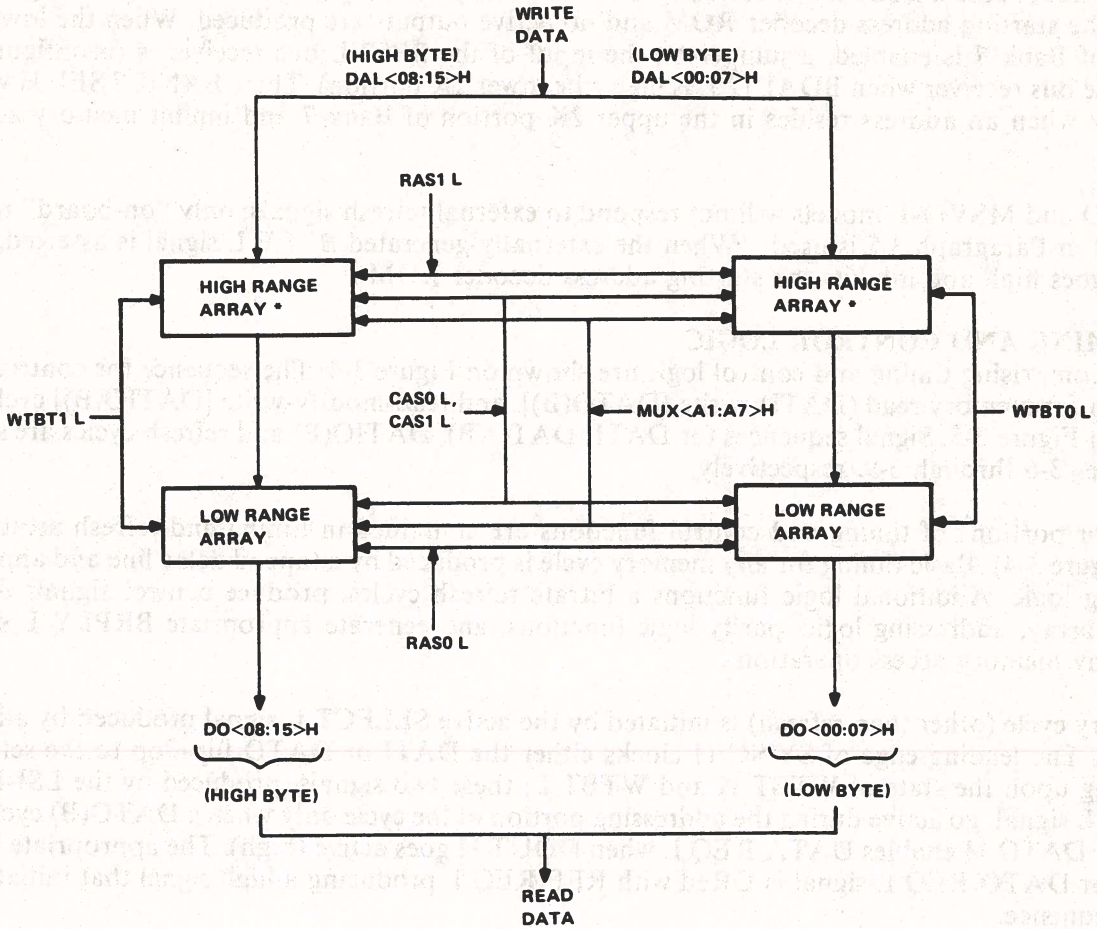
The memory array is organized as shown on Figure 3-2. As previously listed, either 16 or 32 memory ICs comprise the memory array. Models that include only 16 ICs are organized with 8 ICs in the high byte and 8 ICs in the low byte of the low range array shown on the figure. Models that include 32 ICs include the 16 ICs described for the 16-IC models, plus an additional 16 ICs for the high and low bytes of the high range array. Row address strobe (RAS0 L and RAS1 L) control signals, produced by the addressing logic, select the appropriate low or high range array. Write byte (WTBT1 L and WTBT0 L) control signals are produced by the addressing logic during a memory write operation to select the addressed byte (DATOB bus cycle); during a word write operation (DATO bus cycle), WTBT L is high and selects both bytes.

Fourteen address bits are required for 16K by 1 bit RAM ICs, and twelve address bits are required for 4K by 1 bit RAMs. The required 12- or 14-bit address is multiplexed over 6 or 7 address lines (MUX<A1:A7>H) to all RAM ICs that comprise the memory array. Addressing is controlled by column address strobe (CAS0 L and CAS1 L) and row address strobe (RAS0 L and RAS1 L) signals as described in Paragraph 3.3.

3.3 ADDRESSING LOGIC

Addressing logic (Figure 3-3) receives addresses from the LSI-11 bus and produces address bits and control signals when the received address is for a memory location on the module. The user configures a starting address (described in Table 2-1) that defines the lowest address in the module's range. When an address is received that resides in the module's user-configured range, SELECT L goes active. SELECT L is produced by decoding address bits DAL<13:15>H< WWPA16 H, A17 H, and the starting address configured by S1-S5. WWPA16 H and A17 H address usage is reserved for future LSI-11 products. Memory array size jumpers select the appropriate SELECT L and LOW RANGE L decoder ROM outputs, depending on MSV11-D or MSV11-E model; these jumpers are factory configured and normally should not be changed. SELECT L initiates the memory cycle in the timing and control logic. LOW RANGE L controls selection of RAS0 L or RAS1 L signals that select the low range array for all models, or the high range array when addressed on MSV11-DB, -DD, -EB, and -ED models.

The starting address decoder is always inhibited during external refresh operations; EXT REF H goes low during normal memory access operations.



* HIGH RANGE ARRAY IS PRESENT ON THE FOLLOWING MODELS ONLY: MSV11-DB, MSV11-DD, MSV11-EB, MSV11-ED

MR-0347

Figure 3-2 Memory Array

Bank 7, the upper 4K address space in all LSI-11 systems, is normally reserved for peripheral devices. However, the user can enable the use of the lower 2K portion of Bank 7 by installing a jumper. When Bank 7 is not enabled, BBS7 L is inverted by a bus receiver producing BANK 7 SEL H; the high signal inhibits the starting address decoder ROM and no active outputs are produced. When the lower 2K portion of Bank 7 is enabled, a jumper on the input of the BBS7 L bus receiver is reconfigured to inhibit the bus receiver when BDAL12 L is high (the lower 2K portion). Thus, BANK 7 SEL H will go high only when an address resides in the upper 2K portion of Bank 7 and inhibit memory address decoding.

MSV11-D and MSV11-E models will not respond to external refresh signals; only "on-board" refresh described in Paragraph 3.5 is used. When the externally-generated BREF L signal is asserted, EXT REF H goes high and inhibits the starting address decoder ROM.

3.4 TIMING AND CONTROL LOGIC

Circuits comprising timing and control logic are shown on Figure 3-4. The sequence for control logic operation for memory read (DATI), write [DATO(B)], and read-modify-write [DATIO(B)] cycles are shown on Figure 3-5. Signal sequences for DATI, DATO(B), DATIO(B) and refresh cycles are shown on Figures 3-6 through 3-9, respectively.

The major portions of timing and control functions are contained in timing and refresh arbitration logic (Figure 3-4). Basic timing for any memory cycle is produced by a tapped delay line and appropriate gating logic. Additional logic functions arbitrate refresh cycles, produce control signals for the memory array, addressing logic, parity logic functions, and generate appropriate BRPLY L signals during any memory access operation.

A memory cycle (other than refresh) is initiated by the active SELECT L signal produced by addressing logic. The leading edge of SYNC H clocks either the DATI or DATO flip-flop to the set state, depending upon the state of WTBT H and WTBT L; these two signals, produced by the LSI-11 bus BWTBT L signal, go active during the addressing portion of the cycle only when a DATO(B) cycle is in progress; DATO H enables DATA REQ L when DOUT H goes active (high). The appropriate DATI REQ L or DATO REQ L signal is ORed with REF REQ L producing a high signal that initiates the timing sequence.

If a refresh cycle is in progress when the DATI, DATO(B), or DATIO(B) cycle is initiated, the refresh operation is first completed before continuing the memory access operation; LOCKOUT L goes active during any cycle timing sequence and inhibits the new request from starting another cycle until the present cycle has been completed. However, if a memory access cycle is initiated (addressing portion completed) and a refresh cycle request occurs, refresh arbitration logic delays the start of the memory access cycle approximately 100 ns. If a refresh conflict occurs (refresh wins), the refresh cycle will be first completed and add approximately 575 ns to the DATI or DATO(B) cycle time. If memory has been accessed (LOCKOUT L goes passive), a refresh cycle can be initiated although the bus cycle "handshaking" may not have been completed.

A DATIO(B) bus cycle is similar to a DATI cycle followed by a DATO(B) cycle; however, only the addressing portion of the cycle prior to the DATI portion occurs, according to LSI-11 bus protocol.

Write-byte operations (DATOB or the DATOB portion of DATIOB cycles) are controlled by the bus BWTBT L signal and the addressing logic. The timing and control functions are exactly the same for write byte or write word operations.

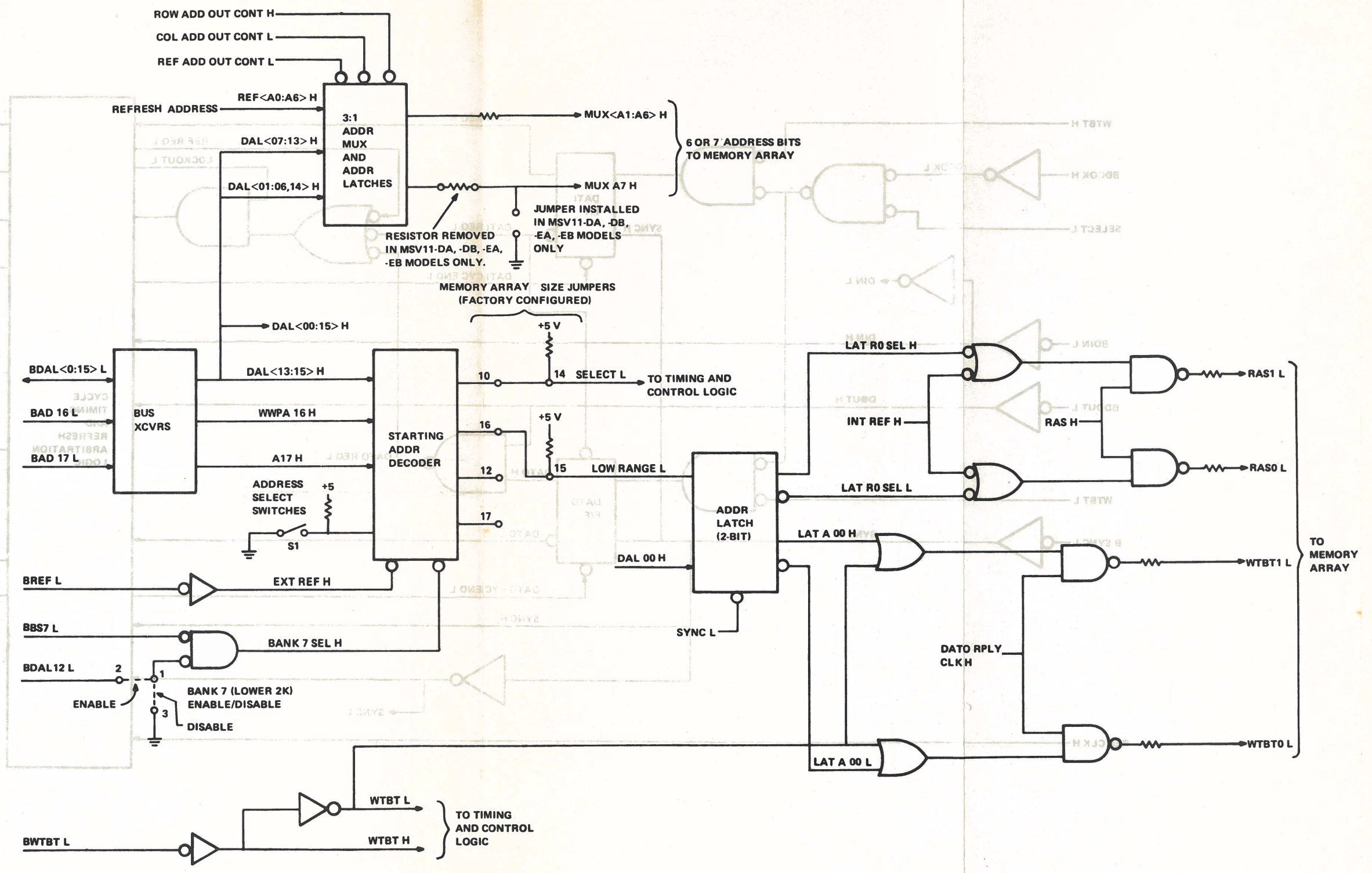


Figure 3-3 Addressing Logic

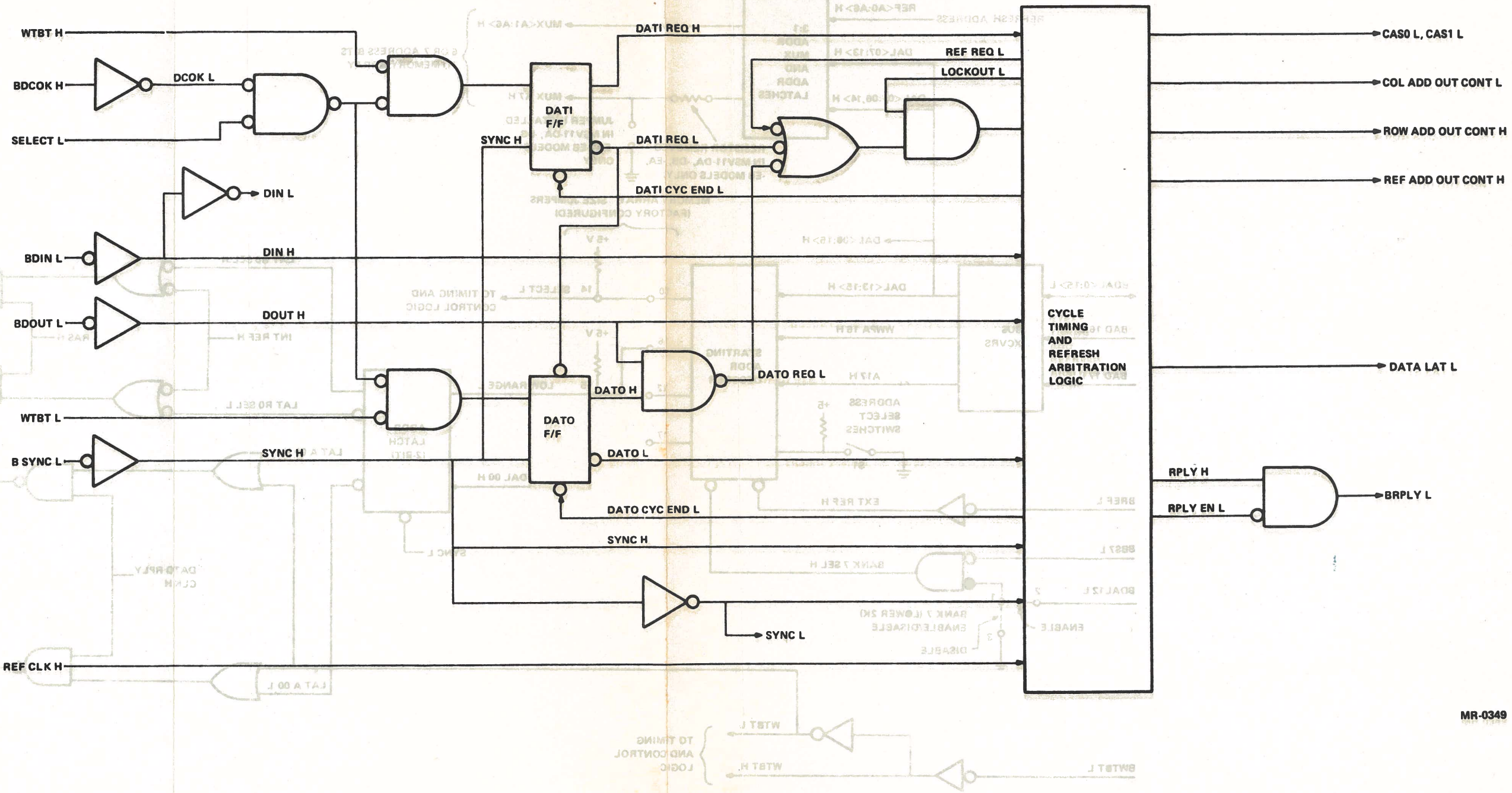


Figure 3-4 Timing and Control Logic

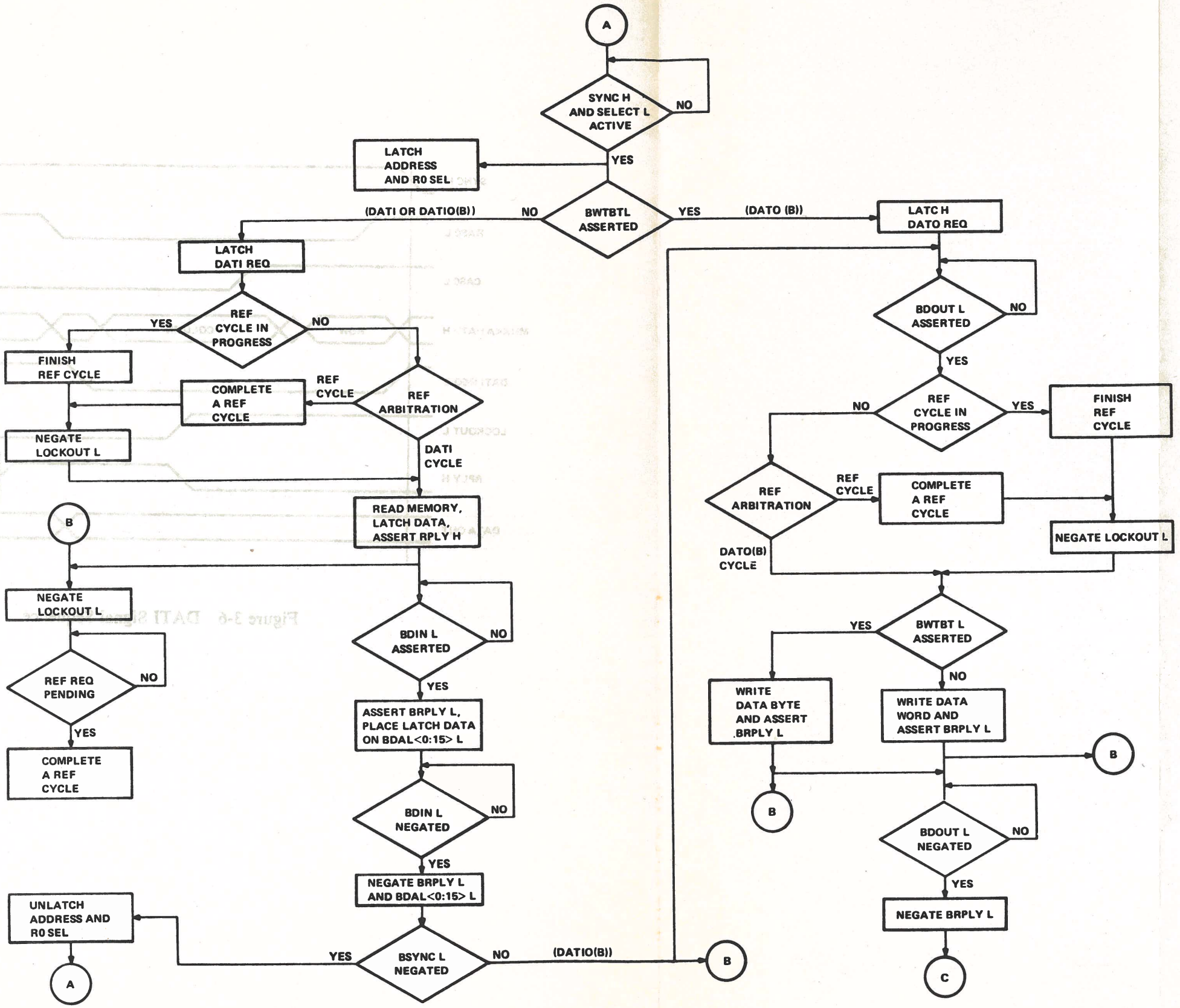


Figure 3-5 Memory Cycle Operation

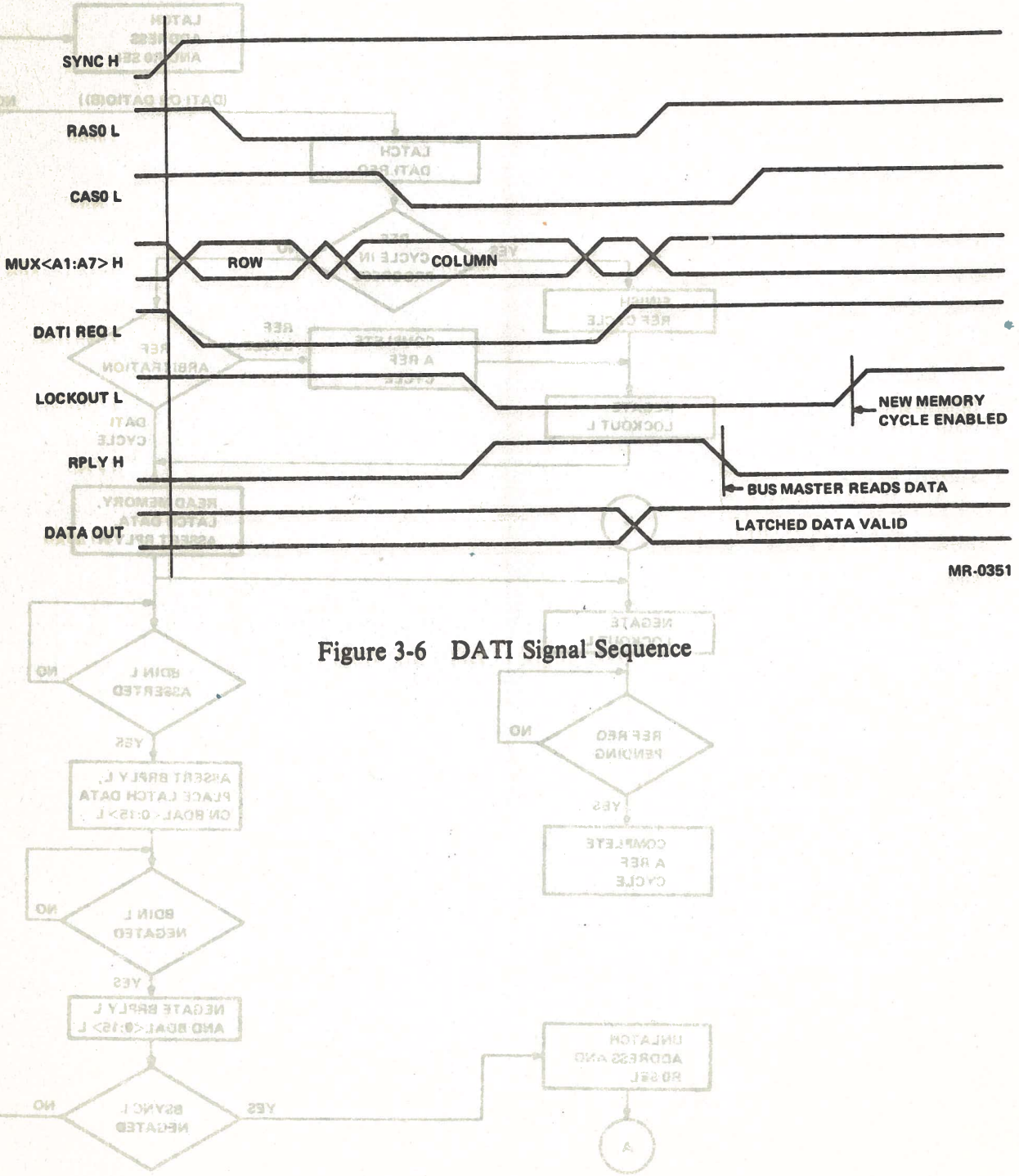


Figure 3-6 DATI Signal Sequence

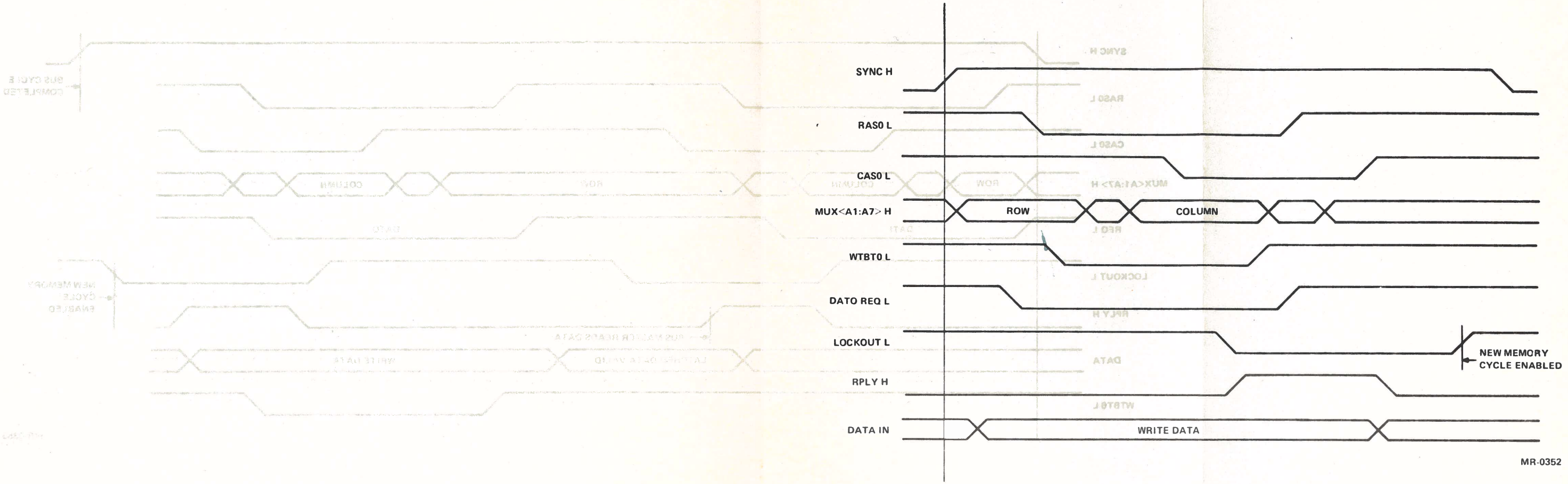


Figure 3-7 DATO(B) Signal Sequence

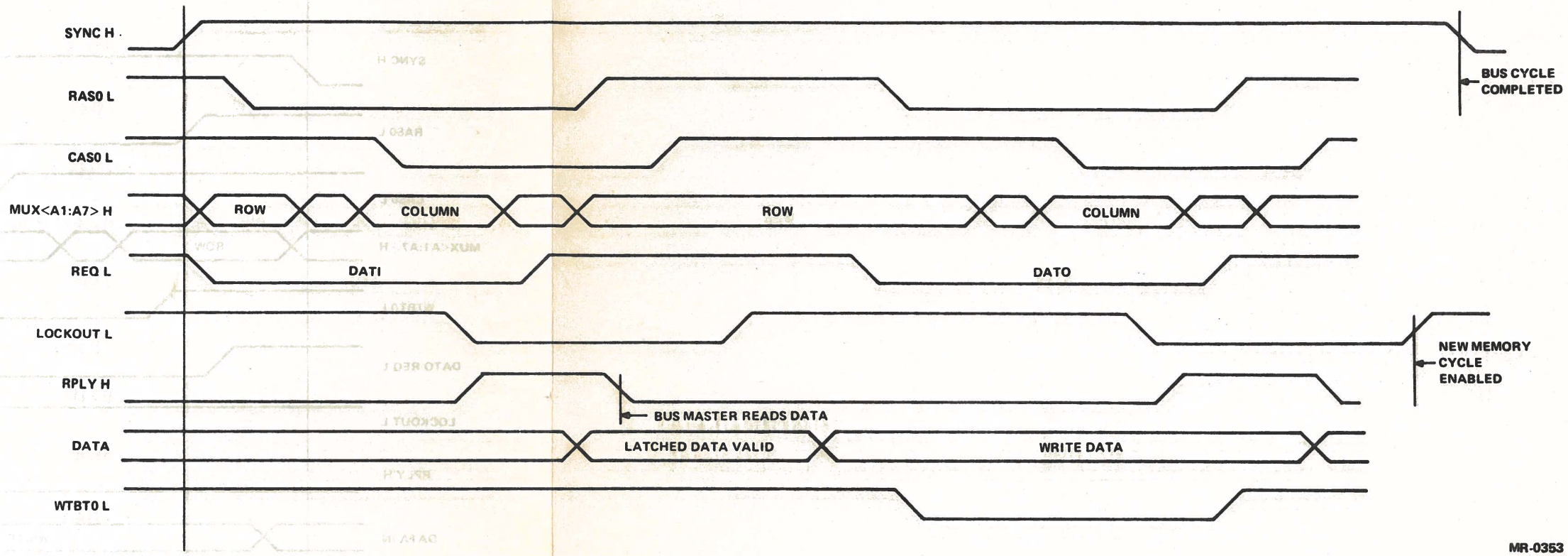


Figure 3-8 DATIO(B) Signal Sequence

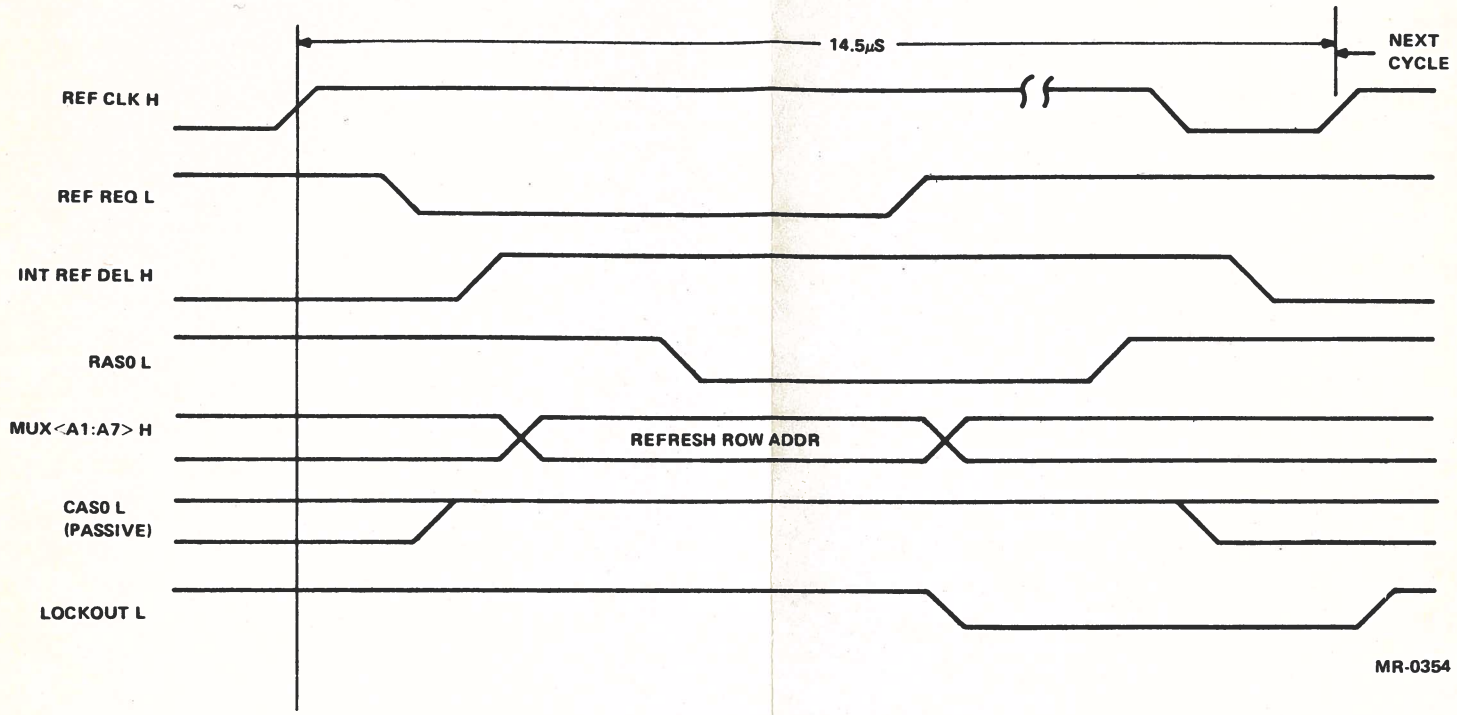


Figure 3-9 Memory Refresh Signal Sequence

3.5 MEMORY REFRESH

Memory refresh request logic is shown on Figure 3-10. A 14.5 μs refresh clock operates the refresh request time to allow completion of 128 refresh cycles during any 2 ms period. A refresh address counter increments once on each refresh cycle producing the current refresh row address. Sequential row addresses are thus refreshed, completing all 128 rows within 2 ms for 16K by 1-bit memory integrated circuits, or 64 rows within 1 ms for 4K by 1-bit memory integrated circuits.

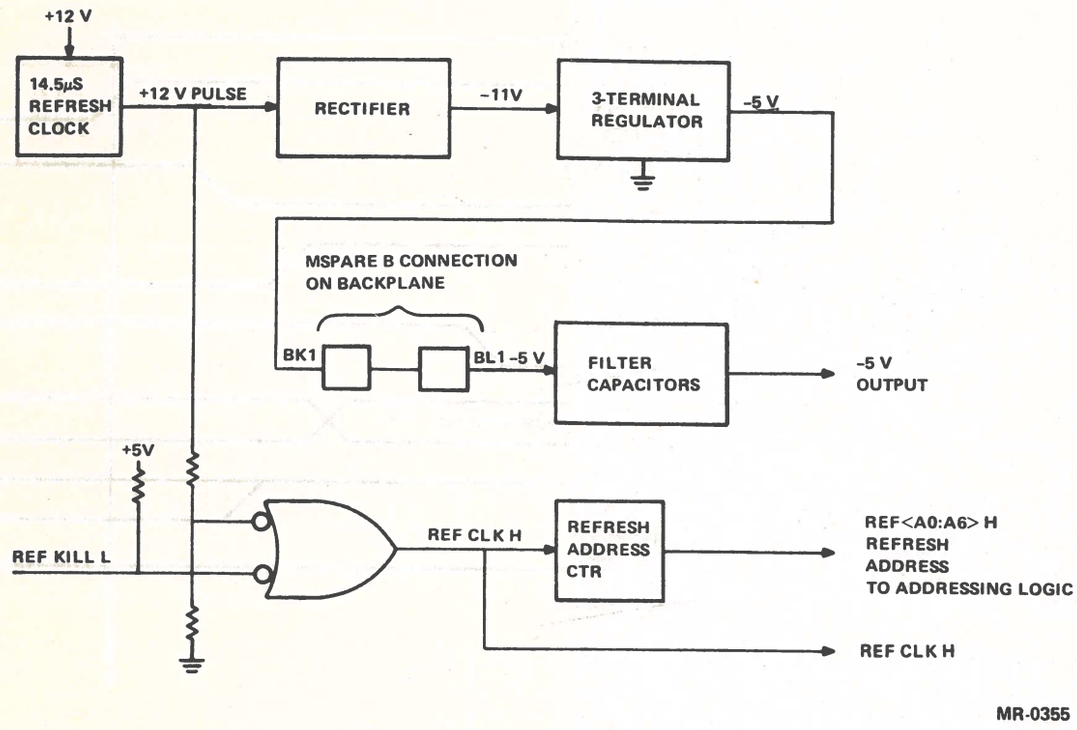


Figure 3-10 Refresh Logic and Charge Pump Circuit

3.6 CHARGE PUMP CIRCUIT

The charge pump circuit (Figure 3-10) produces -5 Vdc for the memory array. Input power is obtained from the +12 V system or battery backup power applied via the refresh clock. The resulting 12 V 14.5 μs refresh clock pulse is applied to a rectifier circuit which produces a -11 Vdc (approximately) output. A three-terminal regulator then produces the required regulated -5 Vdc.

Note that the -5 V is applied to the filter capacitors via MSPAREB backplane pins. This is done for manufacturing test purposes. These pins are connected on all LSI-11 backplanes as shown on the figure. If nonstandard backplanes (user-supplied) are used, be certain that these pins are connected.

3.7 MSV11-E PARITY LOGIC

MSV11-E parity logic functions are shown on Figure 3-11. The basic functions include a parity generator for memory write data, a 2-bit memory array, a parity detector, and a latch circuit. The parity generator produces two parity bits, one for each main memory byte. Address and control signal (not shown) lines are identical to those applied to the main memory array described in Paragraph 3.2. When any main memory location is read, the corresponding parity memory location is read. Parity bits are checked by the parity detector and the result is stored in the output latch. If a parity error is detected (PAR ERROR IND H is active), PAR ERR H is gated onto the BDAL16 L bus line. The processor reads the error during the memory read (DATI) cycle and responds accordingly.

MSV11-E memory modules respond to bus master devices by delaying BRPLY L assertion to accommodate the parity generator and parity detector logic. This timing is jumper-selected (factory configured) and should not be changed.

Parity logic functions are tested when running memory diagnostics by writing incorrect parity bits. The processor forces this condition during a DATO(B) cycle by asserting BDAL16 L during the output data transfer portion of the bus cycle. BDAL16 L is received, inverted to produce "write wrong parity" (WWPA16 H), and applied to the parity generator, forcing it to store incorrect parity bits. The error is then detected by subsequent memory read cycles.

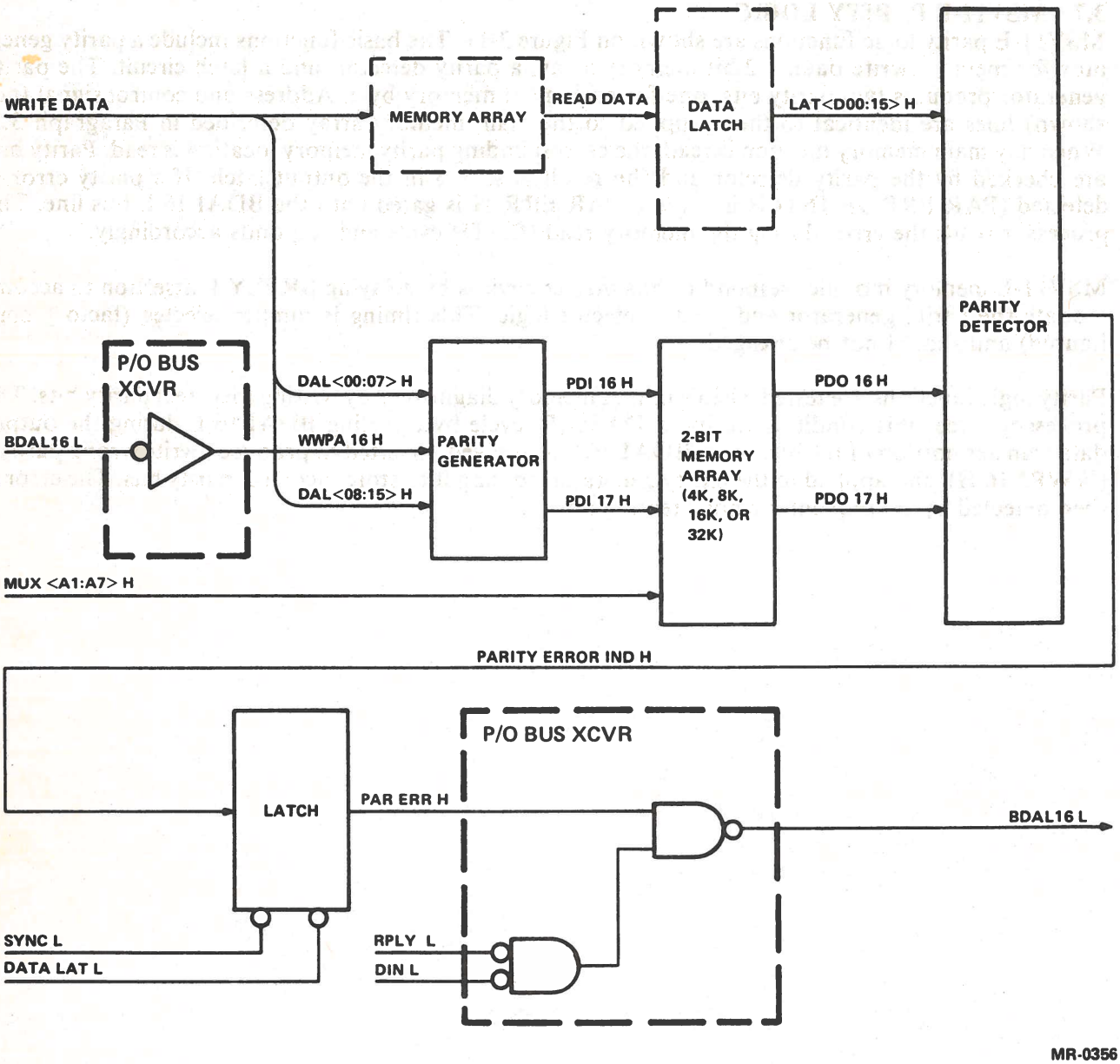


Figure 3-11 Parity Logic

CHAPTER 4
MAINTENANCE

4.1 DIAGNOSTICS

Memory diagnostic programs are available from DIGITAL for testing the MSV11-D and MSV11-E memory modules. Memory diagnostic programs are included in ZJV01-RB paper tape diagnostic software and ZJ215-AY floppy disk software. Detailed operating instructions and program listings are included with each diagnostic software kit. Operating instructions involving the general use of system diagnostics (paper tape and floppy disk) are included in the Microcomputer Handbook, Section 1, Chapter 9.

4.2 DEC SERVICES

Maintenance services can be performed by the user or by DIGITAL, as desired. DIGITAL's maintenance services are described in the Microcomputer Handbook, Section 5, Chapter 3.

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

What features are most useful? _____

What faults or errors have you found in the manual? _____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____
Title _____ City _____
Company _____ State/Country _____
Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Ma 01532
Attention: Communications Services (NR2/M15)
Customer Services Section

Order No. EK-MSV1D-OP-001

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
Maynard, Massachusetts 01754