CDP-16KX16
MAGNETIC CORE MEMORY
TECHNICAL MANUAL

california data processors

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INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides the information needed to understand, install and maintain the CDP-16KX16 Magnetic Core Memory when used with Drawing Package 21518017. The information in this manual is for the use of a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques. A basic knowledge of design principles and circuits used in coincident-current core memories is assumed, hence no tutorial material of this kind is included. An understanding of the computers in which the CDP-16KX16 may be used is also assumed. Detailed information about these computers is available in published manuals.

As a stand-alone publication, this manual has a good functional and physical description of the CDP-16KX16, providing the information needed to understand the capabilities and optional features of the memory and to plan a system using it. The maintenance coverate of this manual is commensurate with the prerequisite skills and knowledge of the defined user, characteristics of the product and maintainability requirements established by Cal Data.

Users holding controlled copies will be provided with revisions and additions to this manual.

1.2 DOCUMENTATION

Modules and assemblies covered in this manual include:

80010 Standard CDP-16KX16.
80011 Interleaved CDP-16KX16.
80012 CDP-16KX16 with 15K option.

The following paragraphs define publications and conventions that support this manual.

1.2.1 Publications

Two manuals are available describing the Cal Data MACROBUS^{TM}. The first manual listed below is provided with CDP-XI computer systems:

21518003 CDP-XI/00 Processor Maintenance Manual
21518008 MACROBUS User Manual

For maintenance purposes, this manual is supported by Drawing Package 21518017, which contains theory of operation, schematic diagrams, assembly drawings and other required engineering drawings.

TM - MACROBUS is a trademark of Cal Data.

1.2.2 Abbreviations and Conventions

Table 1-1 lists the abbreviations found in this manual. Conventions used in the text of this manual include:

a. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.
b. Signal names are capitalized for easy identification.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data or CDP	California Data Processors
cm	Centimeter
kg	Killogram
I/O	Input/output
K	1,024 memory locations
ns	Nanosecond
lfm	Linear feet per minute
lmm	Linear meters per minute
A	Ampere
mA	Milliampere
µA	Microampere
V	Volt
dc	Direct current

SECTION 2
DESCRIPTION

2.1 GENERAL

The CDP-16KX16 Magnetic Core Memory, shown in Figure 2-1, is a plug-compatible storage element for the CDP-XI and PDP-11* series of computers. The CDP-16KX16 offers several outstanding features and advantages. These include:

High speed. The 300-ns access and 850-ns cycle times offer a fast core memory system for the PDP-11 series.

Full compatibility. The CDP-16KX16 can be installed internally in all CDP-XI and PDP-11 computer models, thus eliminating the need for different versions or expensive, space-consuming auxiliary mounting boxes, power supplies and interface cables.

Reduced bus loading. The Cal Data memory has a low MACROBUS (and UNIBUS) load specification, permitting expansion in large system configurations.

Low power consumption. The dc power consumption of the CDP-16KX16 is lower than comparable memory modules available.

15K word option. This option permits CDP-XI and PDP-11 systems to be expanded to 31K words (versus 28K words) without addition of a memory management unit. Only 1K (rather than 4K) word locations are reserved for I/O device addresses. (The system can be expanded to 127K words of memory with memory management.)

2.2 FUNCTIONAL DESCRIPTION

The CDP-16KX16 is a random-access, coincident-current ferrite core memory, arranged in a "three-wire, 3-D" configuration. The capacity is 16,384 words of 16 bits each. The CDP-16KX16 consists of:

a. A single full-sixe printed circuit board containing the memory electronic circuitry.
b. A plug-in magnetic-core-plane board.

The CDP-16KX16 can be operated in one of four modes:

a. Read/restore (equivalent to PDP-11 DATI).
b. Hald-cycle read (equivalent to PDP-11 DATIP).
c. Clear/write (equivalent to PDP-11 DATO).
d. Clear/write byte (equivalent to PDP-11 DATOB).

The full memory cycle (clear/write or read/restore) time is 850 ns for the worst case, measured at the memory interface connector. The worst case read-data access time is 300 ns.

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*The following are trademarks of Digital Equipment Corporation: PDP-11, UNIBUS, DEC.

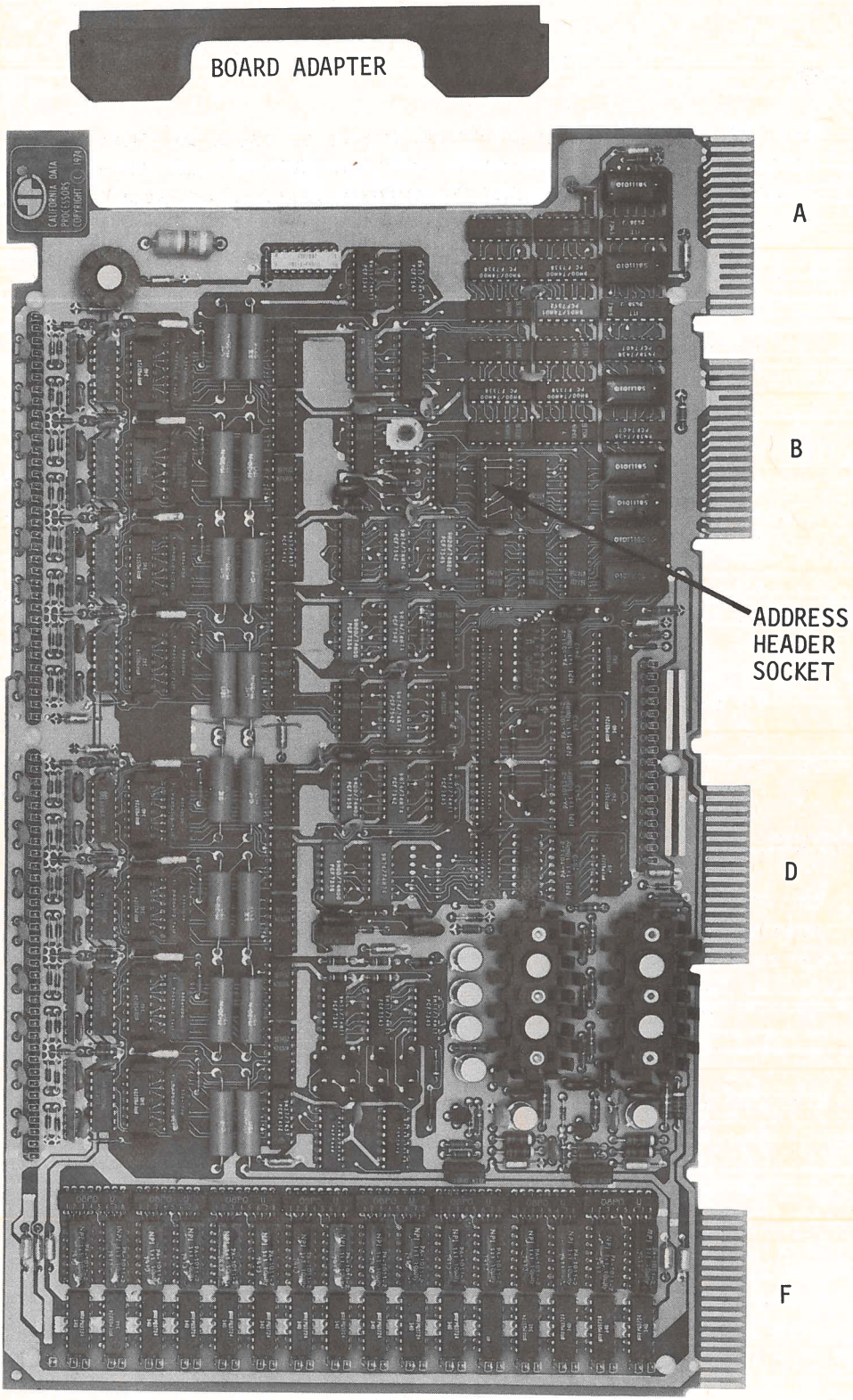


Figure 2-1. CDP-16KX16 Magnetic Core Memory, Component Side

Since the CDP-16KX16 is directly compatible with the PDP-11 computer series, the memory interface follows all rules of the standard UNIBUS.

The CDP-16KX16 is a functionally complete module and requires no additional supporting electronics (other than dc power) for operation in a MACROBUS (or UNIBUS) interface environment.

The CDP-16KX16 is addressed by a set of 18 address lines. In the standard configuration, each CDP-16KX16 module in a system uses the least-significant 15 bits of the address for byte or word selection. The least-significant bit (A00) selects either the more-significant (even) or less-significant (odd) data byte for modification during a clear/write-byte operation (DATOB). The most-significant three address bits select one of eight possible module starting addresses, which can be between 0 and 112K in 16K increments. A plug-in address header assembly provided with each CDP-16KX16 patches the desired starting address.

In addition to the standard configuration described above, two optional configurations are available:

a. Interleaved modules.
b. 15K option.

2.2.1 Operating Modes

2.2.1.1 Read/Restore (DATI)

In a read/restore operation, the CDP-16KX16 reads information from a selected core location, transfers it to the MACROBUS and then writes the information back into the core location. Restoring is necessary since the process of reading a core location erases the contents. During the restore cycle of the operation, the CDP-16KX16 writes the information held in the register back into the selected location.

2.2.1.2 Half-Cycle Read (DATIP)

In a half-cycle read operation, the CDP-16KX16 reads information from a selected core location, transfers it to the MACROBUS and then pauses.

During the read cycle, the CDP-16KX16 loads the accessed information into a register while applying it to the MACROBUS. Data is provided to a master device for modification prior to being restored at the same location. The half-cycle read operation should be followed by a write operation (DATO or DATOB), since any other subsequent operation leads to a memory error and can prevent proper operation of the MACROBUS.

2.2.1.3 Clear/Write (DATO) and Clear/Write Byte (DATOB)

During a clear/write operation, the CDP-16KX16 reads information from a selected core location, discards the information and then writes into the selected location theinformation provided on the MACROBUS. The read cycle of the operation is necessary to clear the specified location prior to writing new data. If the clear/write operation is specified after a half-cycle read operation, the read cycle of the

operation is not performed, reducing the operation time by about 50 percent. Regardless of whether the clear/write operation is commanded independently or after a half-cycle read operation, the data to be stored is loaded into a register immediately on receipt of the command. Any information previously sorted in the register is lost. During the write cycle of the operation, the CDP-16KX16 writes the information held in the register into the selected location.

A clear/write byte operation is identical to a clear/write operation, except that only the byte to be stored is loaded into a register immediately on receipt of the command. Any information previously stored in that half of the register is lost. The other half of the register always contains the retained byte previously read from the selected location. The write cycle of the operation is identical for both clear/write operations.

2.2.2 Interleaved Modules

A pair of CDP-16KX16 modules can be set for interleaved operation in which words at even and odd word addresses are written into or read from alternate modules. A clear or read operation can begin in one module while a write or restore operation is being completed in the alternate module, giving a higher effective memory-transfer rate. This configuration is prepared by interchanging the least-significant word-address bit (A01) with the least-significant module-address bit (A15).

Interleaving is always associated with a pair of CDP-16KX16 modules, and the interleaved pair is effectively treated as a contiguous series of 32K word (64K byte) locations. Interleaved CDP-16KX16 modules must be ordered in this configuration.

2.2.3 15K-Word Option

The basic CDP-XI and PDP-11 computer systems limit, by convention, the number of memory locations addressable by the processor to 28K. The last 4K locations (out of a maximum of 32K) are reserved for I/O device addresses other than core memory. Memory expansion from 28K to 124K requires addition of a memory management unit (available only for DEC computer models 35, 40 and 45).

In some systems, 1K addresses is adequate for nonmemory I/O devices. The Cal Data 15K-word option permits memory expansion to 31K (versus the usual maximum of 28K) without requiring the addition of a memory management unit.

2.2.4 Other Features

The CDP-16KX16 permits retention of previously stored contents during a power-up or a power-down sequence. A dc power status signal (DCLO) indicating availability of properly regulated dc power is supplied to theCDP-16KX16 via one of the interface pins. A low signal disables the select current drives to all memory locations and prevents erasure of data by spurious current pulses during a transient power condition. This dc power status signal is generated by the power supply when the CDP-16KX16 is used in a compatible computer environment.

Voltages required for memory operation are +5 Vdc and -15 Vdc. No special sequencing of these voltages is required by the CDP-16KX16, although certain PDP-11 power supplies sequence the two voltages to the memory.

2.3 PHYSICAL DESCRIPTION

The CDP-16KX16 (Figures 2-1 and 2-2) is contained on a drive electronics board having overall outline dimensions of 15.69 inches (39.85 cm) by 8.94 inches (22.70 cm). The drive board contains AMP Mod. 1 receptacles into which the core plane assembly plugs from the back side of the board (Figure 2-3). The core plane assembly is shown in Figure 2-4. The overall depth of the CDP-16KX16 assembly with core plane installed in 0.87 inch (2.21 cm).

The drive board contains all electrical circuits of the memory except the stering diodes associated with the core X and Y drive lines. The core plane assembly is a planar array of magnetic cores mounted on a substrate, plus a protective cover place. The core plane board also contains the X and Y drive-line steering diodes and current-probe test loops. The core plane assembly is electrically connected by AMP pins into the drive board.

On the top right-hand edge of the board, a 0.18 by 5.30 inch (.044 by 13.46 cm) identation permits a flat I/O cable to exit the rear of the chassis over the top of the board.

CDP-16KX16 modules should normally be mounted nearest to the processor inside the chassis, since w/O device cables are most easily routed outside from the rear of the chassis.

The right-hand edge of the board has a 1.0 by 5.5 inch (2.5 by 14.0 cm) cut out as clearance for the side-mounted cooling fans in the CDP-XI, PDP-11/15 and PDP-11/20 computers, as well as the DEC BA11-EC, DEC BA11-ES and CDP-XI/EB extension mounting boxes. When the CDP-16KX16 is installed in a PDP-11 model 05, 10, 35, 40 or 45, a board adapter can be inserted into the cut-out area to provide a continuous edge for mating with the card guides of these computers.

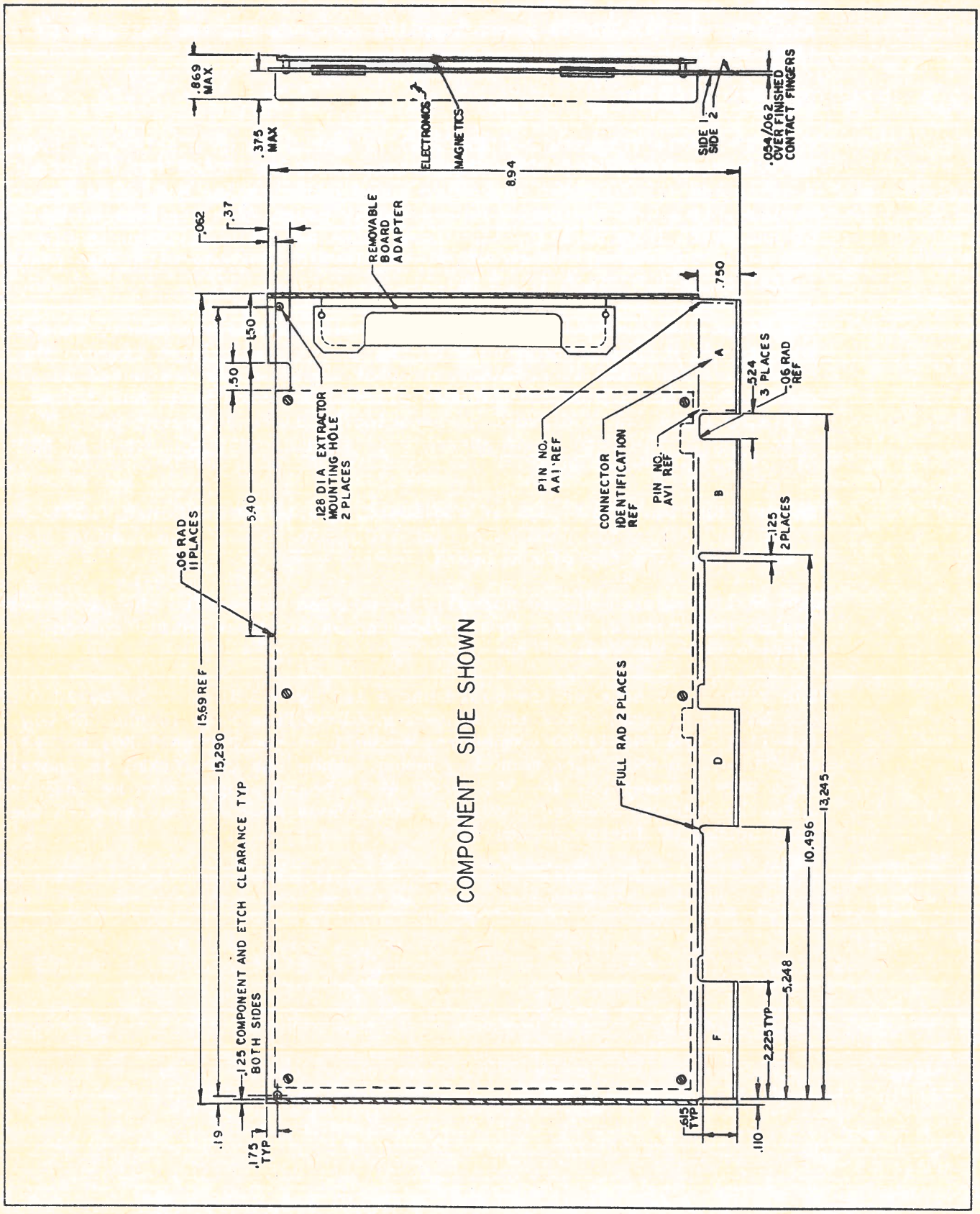


Figure 2-2. CDP-16KX16 Magnetic Core Memory, Mechanical Outline

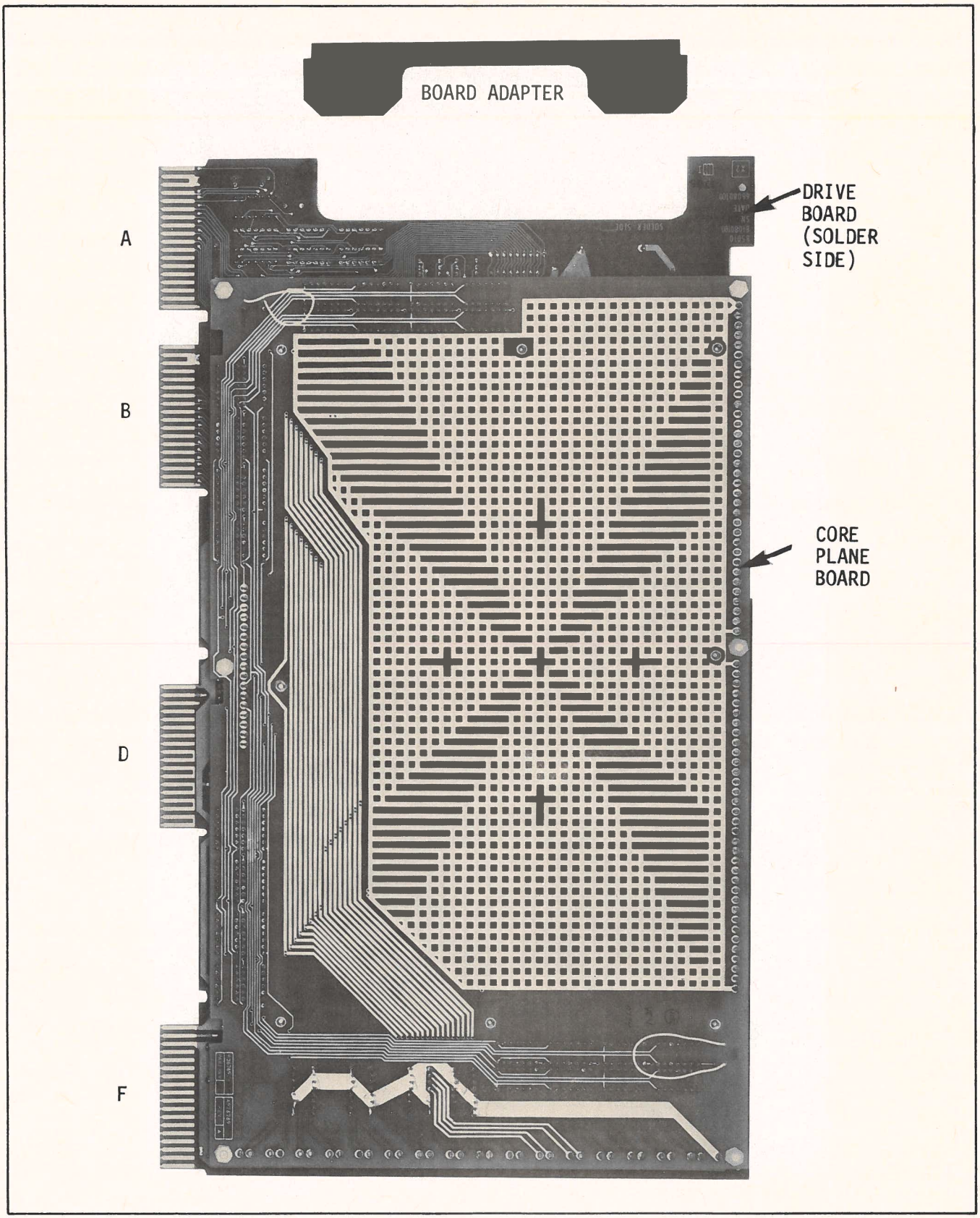


Figure 2-3. CDP-16KX16 Magnetic Core Memory, Core Plane Side

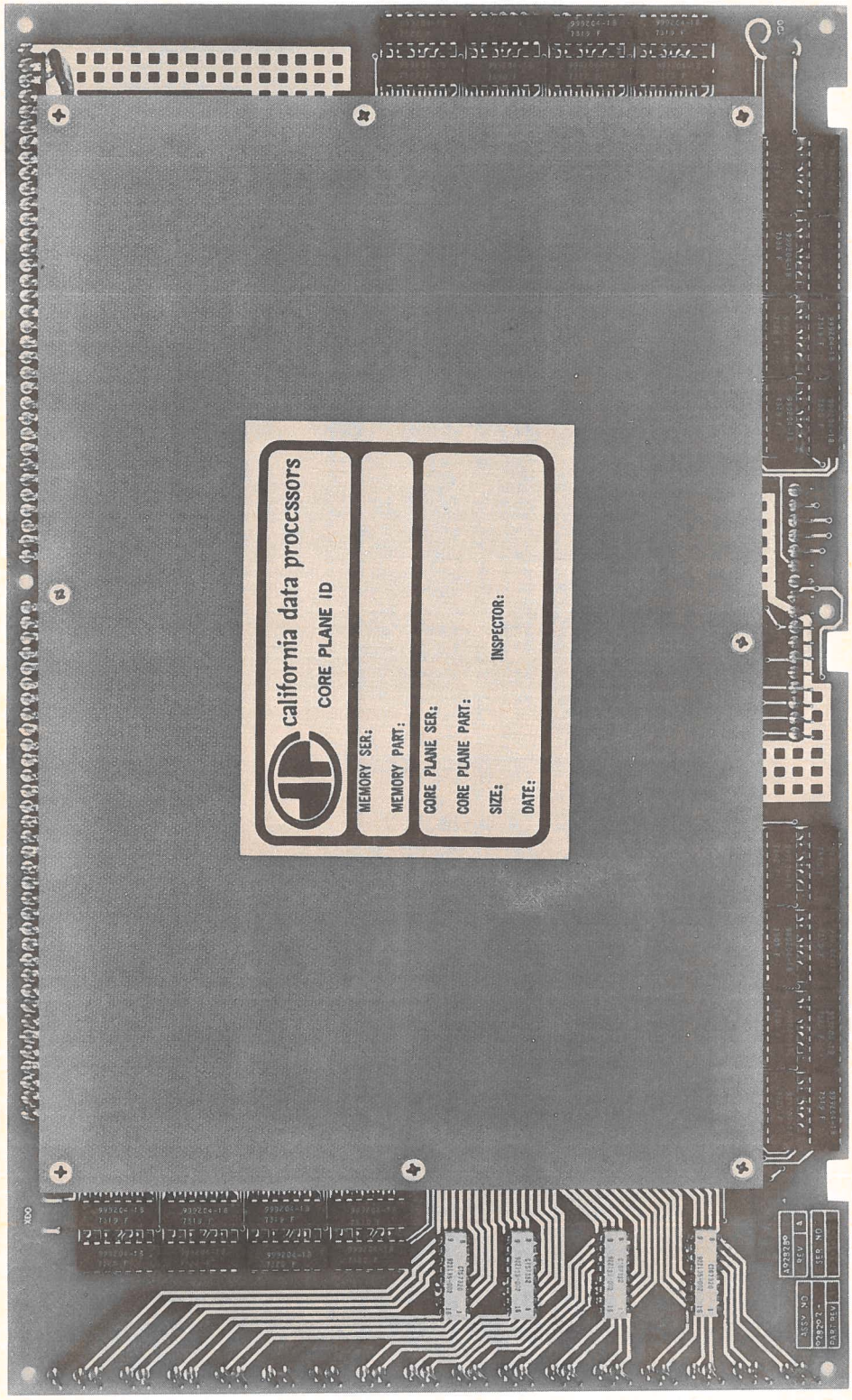


Figure 2-4. CDP-16KX16 Magnetic Core Memory, Core Plane Assembly

2.4 SPECIFICATIONS

General specifications for the CDP-16KX16 are given in Table 2-1.

Table 2-1. CDP-16KX16 Memory Module General Specifications

Characteristic	Specification		
Type	Ferrite magnetic core, random access, coincident current.		
Organization	3-wire, 3-D planar core array.		
Word length	16 bits.		
Storage capacity	16,384 words (32,768 bytes).		
Operating times:	Cycle Time (1)		Access Time (1)
	Noninterleaved	Interleaved (2)	
Read/restore (DATI)	850 ns	450 ns	300 ns
Read (DATIP)	340 ns	340 ns	300 ns
Clear/write (DATO)	850 ns	425 ns	-
Half-cycle write	560 ns	560 ns	-
Interface signals:	Input	Bidirectional	Output
High (False)	+2.5 V min.	+2.5 V min.	
Low (True)	+1.4 V max.	+1.4 V max.	+0.5 V max. at 50 mA
Input current	+120 A max. 2.5 V	+120 A max. at 2.5 V	+120 A max. at 2.5 V
Power:	Operating (3) Amperes	Standby (3) Amperes	Voltage Tolerance
+5 Vdc	3.2	2.4	±5%
-15 Vdc	4.7	0.44	±5%
Ambient temperature	0° to +50° with 200 lfm (61 lmm) airflow.		
Ambient humidity	0 to 90 percent without condensation.		
Dimensions	8.94 by 13.25 by 0.87 inches (22.70 by 33.64 by 2.21 cm).		
Mounting centers	1 inch (2.5 cm) recommended minimum.		

Notes:

1. Worst case, measured at the CDP-16KX16 module interface connector.
2. Effective cycle time for sequenctial access to contiguous interleaved memory locations.
3. Maximum current drain for continuous operations. For noninterleaved operation, only one memory module in the system is operating at a time. The others are on standby. If two CDP-16KX16 modules are interleaved, both should be considered as operating for maximum power calculations.

SECTION 3
INTERFACE

3.1 GENERAL

This section describes the functional circuit design of the CDP-16KX16. The CDP-16KX16 conforms to all standard PDP-11 interfacing rules and interfaces with the standard CDP-XI MACROBUS as well as with the PDP-11 UNIBUS. This section assumes an understanding of these I/O structures. Detailed bus information is available in other technical publications.

3.2 INTERFACE DESCRIPTION

The CDP-16KX16 connects to either the MACROBUS or UNIBUS as a standard peripheral device. It always operates as a slave device (i.e., the CDP-16KX16 never takes control of the bus as a master device). Thus, all transfers are controlled by a bus master, such as the CDP-XI processor or a direct-memory-access controller.

The memory is designed to plug into a single standard hex-height connector row; however, the unit plugs into only connectors A, B, D and F. All functional interface signals used by the memory terminate on the A and B connectors, with standard pin assignments used. Bus Grant signals are not used by the memory module; however, these signals are jumpered through the D connector via etched lines on the board so that these lines are automatically propagated with the memory installed.

If a memory is removed from a location and no new board is installed, the Bus Grant lines must be jumpered on the connector if other I/O devices are operating on any of the priority interrupt lines. The D and F connectors are used for power and ground connection to the memory module.

The CDP-16KX16 decodes the 18-bit address transmitted on the MACROBUS when a Master Synchronization signal (MSYN) is asserted by the device in control of the MACROBUS (bus master). If the address corresponds to the CDP-16KX16 module address, the CDP-16KX16 responds by executing the operation specified by the mode Control lines (C0, C1) and asserting a Slave Synchronization signal (SSYN) on the MACROBUS to indicate acceptance or availability of data.

3.2.1 Interface Signals

Table 3-1 lists the mnemonic, name and description of each MACROBUS signal used by the CDP-16KX16. Signals not required for memory operation are ignored (open circuit); however, there are cetain signals associated with chained priority operations on the bus that require physical line continuity through the interface connectors, whether or not the interface device uses the signals. The CDP-16KX16 ensures continuity of these signals, when installed, by propagating the necessary signal lines via etched conductors on the circuit board. If a memory module is removed from the system, these signal lines must

Table 3-1. MACROBUS Signal Definitions

Mnemonic	Name	Description	Memory Use
A17 to A00	Address	Selects slave device.	Most-significant 3 bits select module; least-significant 15 bits select word/byte.
D15 to D00	Data	Word or byte transferred.	Data in or out.
C0 and C1	Control	Selects mode.	Operation performed.
MSYN	Master Synchronization	Initiates operation.	Gates Ann, Dnn and Cn signals.
SSYN	Slave Synchronization	Response to MSYN.	Signals acceptance or availability of data.
PA			Reserved.
BP			Reserved.
NPR	Nonprocessor Request	Highest-priority bus request.	Ignored.
BR7 to BR4	Bus Request	Interrupt request.	Ignored.
NPG	Nonprocessor Grant	Grant bus control.	Ignored.
BG7 to BG4	Bus Grant	Grant bus control.	Propagated, ignored.
SACK	Selection Acknowledgement	Acknowledges bus grant.	Ignored.
BBSY	Bus Busy	Asserts bus mastership.	Ignored.
INTR	Interrupt	Retains bus control.	Ignored.
INIT	Initialize	Clear and reset.	Initializes memory.
ACLO	AC Low	Impending power failure.	Ignored.
DCLO	DC Low	DC voltages out of tolerance.	Protects memory contents.

be closed by jumper wiring or other means if another board is not physically located in the vacated connector slot.

Appendix A lists interface pin assignments.

3.2.2 Control Modes

The CDP-16KX16 operates in one of four modes (Table 3-2) specified by bus Control lines C0 and C1. In modes requiring a byte operation (DATOB), address bit A00 specifies the byte affected.

CDP-16KX16 logic forces the operation immediately following DATIP to be a half-cycle write operation. The bus master initiates DATO or DATOB after DATIP, and these commands are interpreted by the memory logic to half-cycle write operations.

3.3 INTERFACE TIMING

Figure 3-1 shows interface timing for the basic CDP-16KX16 operations. The direction of data transfer is given with respect to the bus master rather than to the CDP-16KX16. Thus data input implies a transfer to the master (output from the CDP-16KX16) and vice versa.

3.3.1 Read/Restore (DATI)

The CDP-16KX16 reads a 16-bit word from the location designated by the input address and places the word on the MACROBUS. The word is also restored automatically by the CDP-16KX16.

As shown in Figure 3-1, the Address and Control lines (A17 to A00, C0 and C1) must be settled at the CDP-16KX16 at least 50 ns prior to receipt of MSYN to permit decoding of these signals. Data (16-bit word) read from memory and SSYN are placed on the bus within a maximum of 300 ns from receipt of MSYN. The addressed word is restored during the next 500 ns. Address and Control signals received at time 800 ns, followed by a MSYN at 850 ns, result in a minimum repetitive read/restore cycle of 850 ns.

Table 3-2. CDP-16KX16 Operating Modes

A00	C1	C0	Command	Operation
x	0	0	DATI	Read/restore
x	0	1	DATIP	Half-cycle read
x	1	0	DATO	Clear/write
0	1	1	DATOB 0*	Read/restore byte 1, Clear/write byte 0
1	1	1	DATOB 1*	Read/restore byte 0, Clear/write byte 1

*Byte 0 = less significant; byte 1 = more significant.

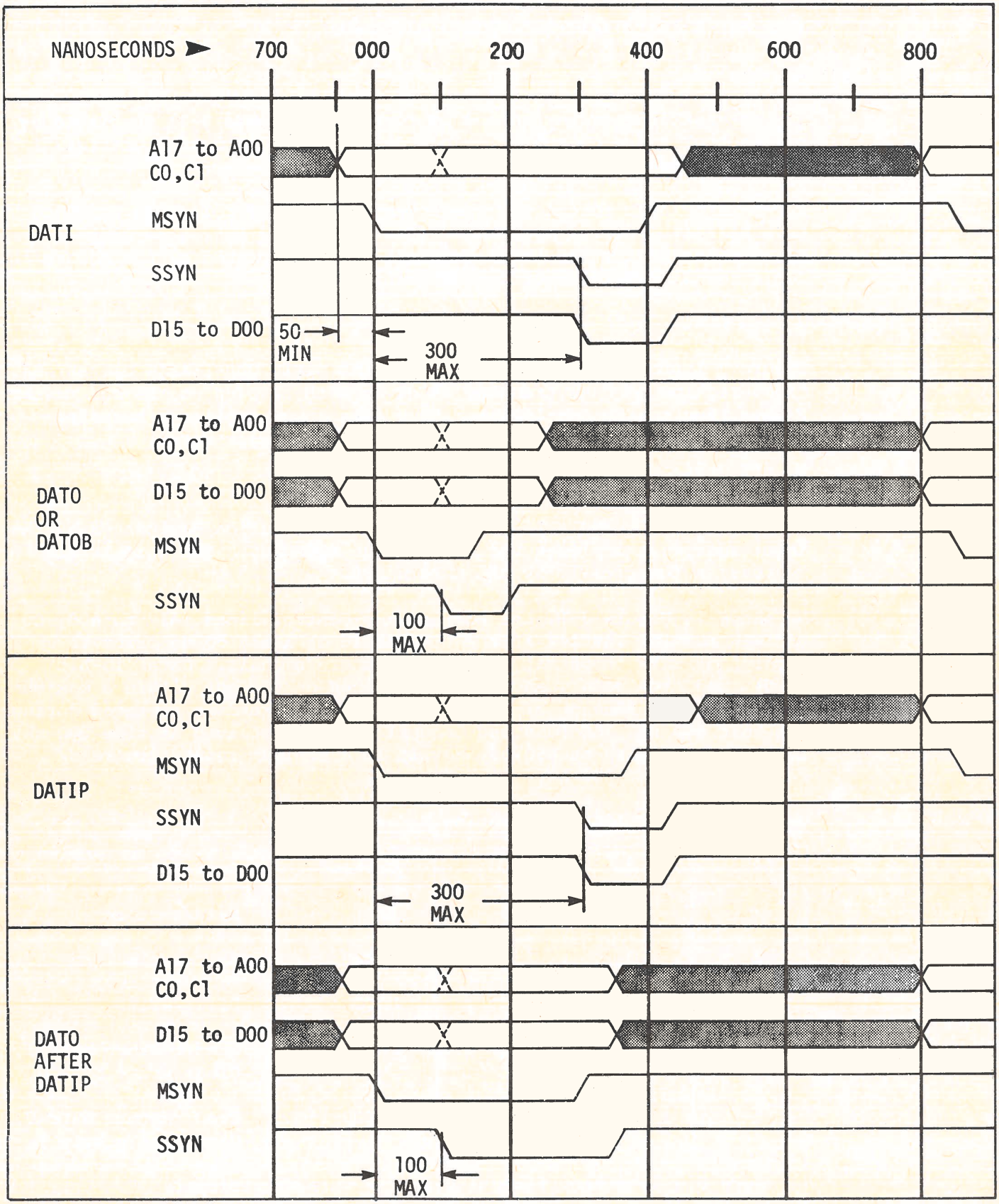


Figure 3-1. CDP-16KX16 Memory Interface Timing

The CDP-16KX16 provides internal storage for the Address and Control signals, hence it is not necessary to retain information on these lines throughout the cycle. The earliest recommended time for removing the Address and Control signals is 100 ns after MSYN is received. Because of the asynchronous nature of the MACROBUS, the bus master has no indication that the memory operation has actually started until SSYN is received. Early removal of Address and Control signals is not useful in this case, but other applications could make use of this feature.

The operation timing shown represents the guaranteed worst-case and, in general, the CDP-16KX16 operates faster than specified. MSYN can be reasserted within 150 ns after it has been removed in response to SSYN, provided that the Address and Control signals have been established at least 50 ns earlier.

3.3.2 Clear/Write (DATO) and Clear/Write Byte (DATOB)

For DATO, the CDP-16KX16 clears the location designated by the address lines and writes into that location the 16-bit word received on the MACROBUS.

As shown in Figure 3-1, the Address, Control and Data signals must be settled at the interface connector at least 50 ns prior to receipt of MSYN to permit decoding of the Address and Control signals, and storing of the data. SSYN is asserted on the MACROBUS within 100 ns after MSYN is recognized. The clear/write operation internal to the memory required 850 ns, maximum.

MSYN can be reasserted within 150 ns after it is removed in response to SSYN, provided Address and Control signals are settled at least 50 ns earlier. The CDP-16KX16 generally operates at a speed higher than specified.

Timing for the clear/write byte operation (DATOB) is identical to that for DATO. Functionally, the CDP-16KX16 clears and writes only the designated byte (upper or lower). A read/restore operation is performed on the other byte.

3.3.3 Half-Cycle Read (DATIP)

The CDP-16KX16 reads a 16-bit word from the location designated by the input address and places the word on the MACROBUS along with SSYN. The word read out is not restored, but is held in the memory data register. Access timing at the interface is identical to that for DATI (Figure 3-1).

DATIP permits the word read out to be modified by the bus master and the modified word restored in the same location. The bus master must retain bus mastership until the modified word is restored. To ensure that proper design rules are followed, DATO and DATOB are the only commands permitted to follow DATIP. These operations can be initiated within 150 ns (by reassertion of MSYN) after MSYN has been removed following the assertion of SSYN by the CDP-16KX16, provided that Address and Control signals are settled at least 50 ns earlier. Figure 3-1 shows the timing.

The CDP-16KX16 automatically performs a half-cycle write operation in response to the next MSYN after a DATIP, regardless of the states of C1 and C0.

3.4 INTERFACE CIRCUITS

Because memory modules are attached to the same interface bus as peripheral devices, the bus loading introduced by the CDP-16KX16 is an important system consideration for configurations containing a large amount of memory or numerous peripheral devices. The CDP-16KX16 minimizes the loading of receivers and the leakage current of drivers in the high state (these being the critical bus-loading parameters). This is accomplished in two ways:

a. The driver leakage load is limited to that of one gate instead of two (as is common in other designs).
b. A CDP proprietary bus receiver circuit improves speed and reduces drive requirements.

3.4.1 Line Driver

The line driver is a TTL buffer. The critical bus specifications for the device are:

Output low voltage at 50 mA sink (V_{OL})	+0.5 V, max.
Output high leakage current at 2.5 V (I_{OH})	+60 µA, max.

3.4.2 Line Receiver

The CDP-16KX16 uses a CDP line receiver, the critical bus specifications for this device are:

Input high threshold (V_{IH})	+2.5 V min.
Input low threshold (V_{IL})	+1.4 V max.
Input current at +2.5 V (I_{IH})	+60 µA max.
Input current at 0.0 V (I_{IL})	±25 µA max.

3.4.3 Bus Loading

The limiting bus loading occurs on the bidirectional Data lines that have one receiver and one driver for each CDP-16KX16 memory module. Worst-case module bus load specifications are:

V_{IH}	+2.5 V min.
V_{IL}	+1.4 V max.
I_{IH}	+120 µA max. at +2.5 V.
I_{IL}	±25 µA max. at 0.0 V.

SECTION 4
INSTALLATION

4.1 GENERAL PROCEDURES

When used as part of a CDP-XI system, the CDP-16KX16 will have been installed and tested by Cal Data prior to shipment. Thus, the following procedures describe the installation of modules received individually for addition to an existing installation.

The CDP-16KX16 core memory module is designed for direct installation in the CDP-XI computer, in a CDP-XI/EB Extension Box, a DEC BA11-EC or DEC BA11-ES extension box, or in any model of the PDP-11 series computers.

Before installing the CDP-16KX16 in a PDP-11 computer, the user should be familiar with physical details of the applicable system, particularly the backplane (system-unit signal wiring and power distribution). The CDP-16KX16 interfaces with the standard UNIBUS signals carried in the A and B connector columns of all PDP-11 series computers. The specific installation procedures vary with each model in the series, since the physical signal connector and power distribution schemes differ from model to model.

The signal, power and ground connections to the CDP-16KX16 are made via the A, B, D and F connectors as given in Appendix A. For any given installation, compare this signal list against that of the backplane or system unit for the intended installation.

The general installation procedure consists of inserting the CDP-16KX16 into the appropriate connectors so that the A and B plugs interface with the UNIBUS connectors. The component side of the CDP-16KX16 drive board faces the same direction as the component side of the standard PDP-11 circuit boards. The CDP-16KX16 core plane, which plugs into the rear of the drive board, blocks the next connector slot, since standard PDP-11 connector rows are on half-inch centers and the CDP-16KX16 requires 0.87 inch (2.21 cm).

4.1.1 Unpacking and Inspection

Each CDP-16KX16 is shipped in an individual, padded shipping container for protection during transportation. This container can be saved for future use if the unit is returned for repair or reshipped separately from the associated computer system.

The following steps are recommended for unpacking and initially inspecting the memory:

1. Prior to opening, inspect the box for obvious damage.
2. Cut the packing tape, open the box and remove the module. Next remove the plastic wrapper and inspect the module for physical damage.

3. Inspect the board connector pins for any foreign matter and clean if necessary for reliable contact with the connectors.

It is important to note immediately any physical damage that might have resulted from shipment. The carrier should be notified of such damage and given the opportunity to inspect the unit and container. This helps establish the validity of any claims for shipping insurance.

4.1.2 Handling

The CDP-16KX16 can withstand all normal shock and vibration encountered in shipping and when installed in a computer system. While not a fragile device, the module should be handled with reasonable care to avoid damage that might result in operational failure. The following are some general pointers on handling the module during inspection, installation and maintenance operations:

a. The core stack plugs into the rear of the electronics drive board and is held in place by safety nuts at several points on the stack assembly. These nuts should always be on and tight when the module is installed in a system.
b. When installed on the drive board, the magnetic core array is protected by the etched core plane board. This cover is rigit and provides adequate protection for normal handling. NEVER EXERT PRESSURE ON THE CORE PLANE BOARD.
c. Avoid bending components when handling the drive board assembly. To prevent oxides from forming on the gold plating, do not touch the connector pins.
d. Always insert and remove modules with the system power OFF.
e. When inserting or removing the CDP-16KX16, be sure that the component side faces the correct direction and that the board is aligned in the card guides (if present).
f. Insert and remove the module slowly and carefully so that it does not make contact with adjacent boards.
g. Never use components as finger grips. Use the grip areas at the corners of the board.

4.1.3 Addressing Strapping

Each memory module in a system must have a different block starting address to prevent more than one module from responding to the same address from the processor or DMA device (except for interleaved pairs, which have a common block starting address).

The standard CDP-16KX16 can be set to any starting address from 0 to 112K in 16K increments. Interleaved modules can have starting addresses of 0, 32K, 64K or 96K.

Cal Data provides a memory address header assembly with each CDP-16KX16. This assembly can be delivered either prewired to a specified starting address or unwired, according to user specification. The assembly plugs into a socket on the board.

Prior to system installation, set up the CDP-16KX16 for the proper block starting address strapping. Strapping is accomplished by jumpers placed between pins in a 16-pin dual-in-line socket mounted on the board for this purpose (Tables 4-1, 4-2 and 4-3).

Table 4-1. Jumpers for Block Starting Addresses, Standard CDP-16KX16

Block Starting Address	Cal Data Part Number	Pin Numbers									
		From	To	From	To	From	To	From	To	From	To
None	85300068	NO JUMPER WIRES PROVIDED									
0	85300069	16	2	15	4	14	6	10	7	9	8
16K	85300070	16	2	15	4	14	5	10	7	9	8
32K	85300071	16	2	15	3	14	6	10	7	9	8
48K	85300072	16	2	15	3	14	5	10	7	9	8
64K	85300073	16	1	15	4	14	6	10	7	9	8
80K	85300074	16	1	15	4	14	5	10	7	9	8
96K	85300075	16	1	15	3	14	6	10	7	9	8
112K	85300076	16	1	15	3	14	5	10	7	9	8

Table 4-2. Jumpers for Block Starting Addresses, CDP-16KX16 with 15K Option

Block Starting Address	Cal Data Part Number	Pin Numbers											
		Fr	To	Fr	To	Fr	To	Fr	To	Fr	To	Fr	To
16K (to 31K)	85300085	NC	NC	NC	NC	14	5	10	7	9	8	13	11
112K (to 127K)	85300086	16	1	15	3	14	5	10	7	9	8	13	11

Note: NC = no connection.

Table 4-3. Jumpers for Block Starting Addresses, Interleaved CDP-16KX16 Modules

Block Starting Address	Cal Data Part Number	Pin Numbers									
		From	To	From	To	From	To	From	To	From	To
0 even	85300077	16	2	15	4	14	8	10	5	9	6
0 odd	85300078	16	2	15	4	14	7	10	5	9	6
32K even	85300079	16	2	15	3	14	8	10	5	9	6
32K odd	85300080	16	2	15	3	14	7	10	5	9	6
64K even	85300081	16	1	15	4	14	8	10	5	9	6
64K odd	85300082	16	1	15	4	14	7	10	5	9	6
96K even	85300083	16	1	15	3	14	8	10	5	9	6
96K odd	85300084	16	1	15	3	14	7	10	5	9	6

If the system contains a 4K-word memory unit, this unit must be set to the highest block starting address in the system (i.e., 16K-word modules occupy block starting addresses 0, 16K, 32K, etc.).

4.2 INSTALLATION IN THE PDP-11/05 OR PDP-11/10

CDP-16KX16 modules can be installed directly in the PDP-11/05 or PDP-11/10 chassis with or without an 8K MM11-L memory. The information presented in this subsection is also applicable to installations in the PDP-11/35 expansion chassis.

There are two standard DEC configurations of the 05 and 10, each with a different backplane:

a. Configuration 1 is wired for 16K of memory with one small-peripheral controller slot (Figure 4-1).
b. Configuration 2 is wired for 8K of memory with four small-peripheral controller slots (Figure 4-2).

The following apply to those installations:

a. The CDP-16KX16 is installed with components toward the top of the cabinet and the core plane toward the bottom of the cabinet. The keyed connectors prevent reversing the board.
b. Check the CDP-16KX16 for proper orientation (components up, core plane down) before attempting to insert the board. Excessive force applied to a reversed board can result in damage to the backplane connectors.
c. Always install and remove boards with the system power OFF.
d. A UNIBUS terminator is placed at the end of the UNIBUS, either inside or outside the computer chassis.
e. The Cal Data board adapter assembly should be installed on the CDP-16KX16 to make proper contact with the card guides of the cabinet.

CDP-16KX16 modules can be installed in various combinations with or without an MM11-L. No modification of the computer backplane is necessary and no electrostatic shield is required. The following subsections describe typical memory configurations.

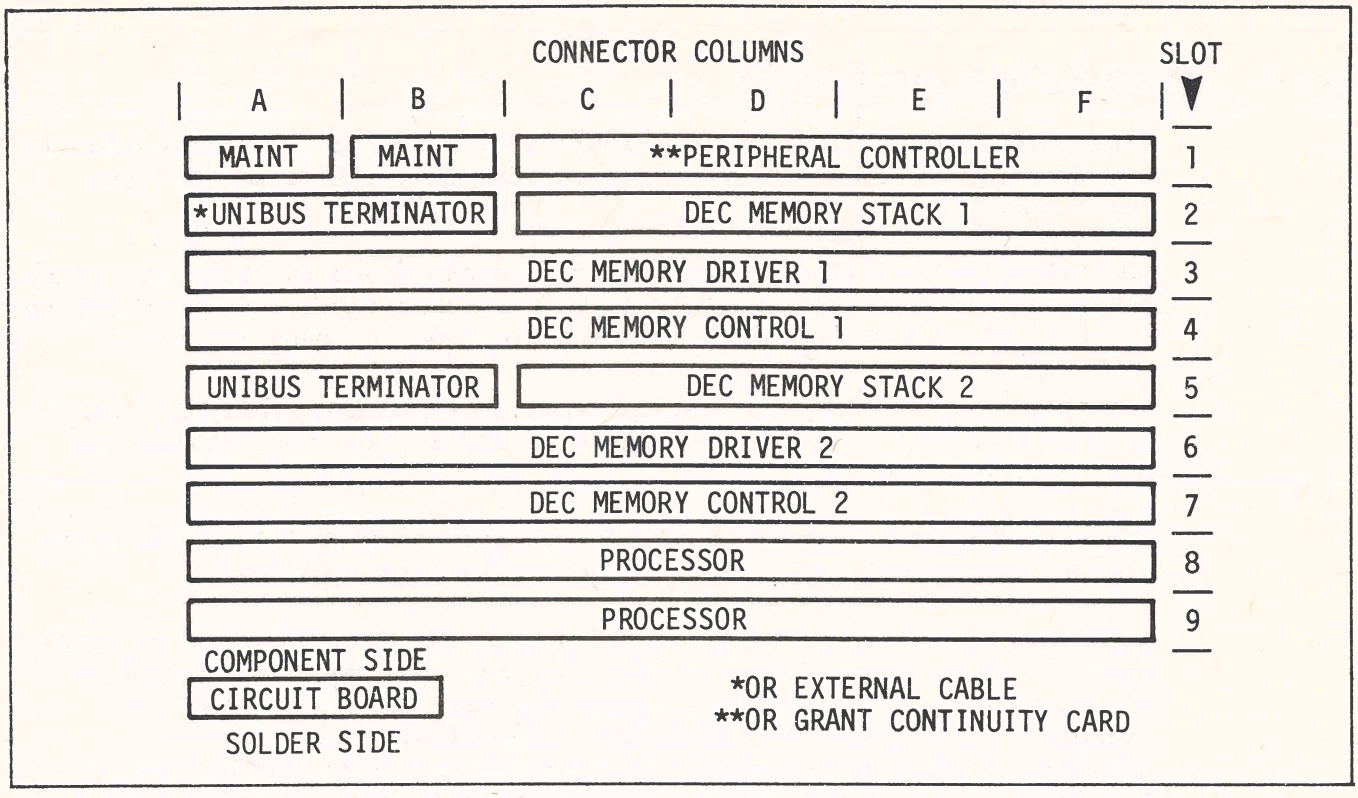


Figure 4-1. DEC PDP-11/05 and PDP-11/10 Standard Module Utilization - Configuration 1 (16K)

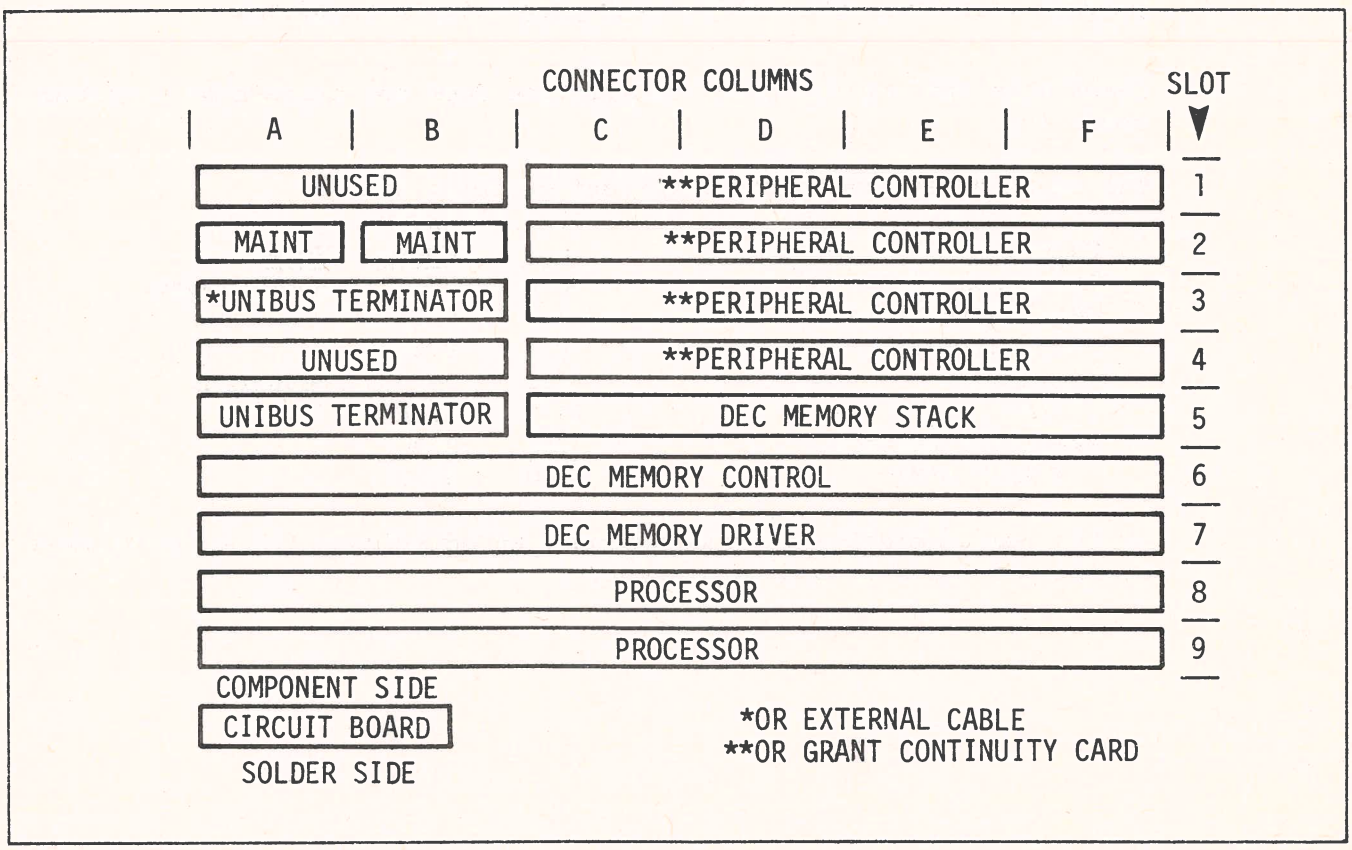


Figure 4-2. DEC PDP-11/05 and PDP-11/10 Standard Module Utilization - Configuration 2 (8K)

4.2.1 32K-Word Configuration 1A

The 32K-word configuration 1A (Figure 4-3) uses two CDP-16KX16 modules and no MM11-L. (The processor can address only the first 28K core locations.)

The CDP-16KX16 modules are installed in slots 3 and 5. The core plane board blocks the adjacent slots (4 and 6, respectively) even though no connections to the CDP-16KX16 modules are made in these locations.

For this installation, the UNIBUS terminator board normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installation of the memory modules.

The UNIBUS signals are available in connectors 2A/2B. A UNIBUS terminator or external cable can be inserted in this location.

Note that empty slot 2 is wired to contain the MM11-L core stack and memory driver boards. This wiring does not conform to that used by a peripheral controller board, hence the slot cannot be used for standard DEC quad-height controller assemblies. This slot can, however, contain user-designed controllers on hex-height boards, Such boards obtain all UNIBUS communication from the A and B connectors, and power and ground inputs from the other connectors. Cal Data offers various hex-height controllers, including a general-purpose wire-wrap HEXBOARD™, that plug into these slots.

Check that the overall power consumption does not produce an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
Processor	8.0	-	Approximate.
One 16KX16 running	3.2	4.7	
One 16KX16 standby	2.4	0.44	
Terminator	1.2	-	Required.
LOAD	14.8	5.14	
Available reserve	2.2	0.86	
SUPPLY LIMIT	17.0	6.00	

If the bus terminates in this cabinet, an additional 1.2 A (+5 V) must be allowed for a second terminator.

TM - HEXBOARD is a trademark of California Data Processors.

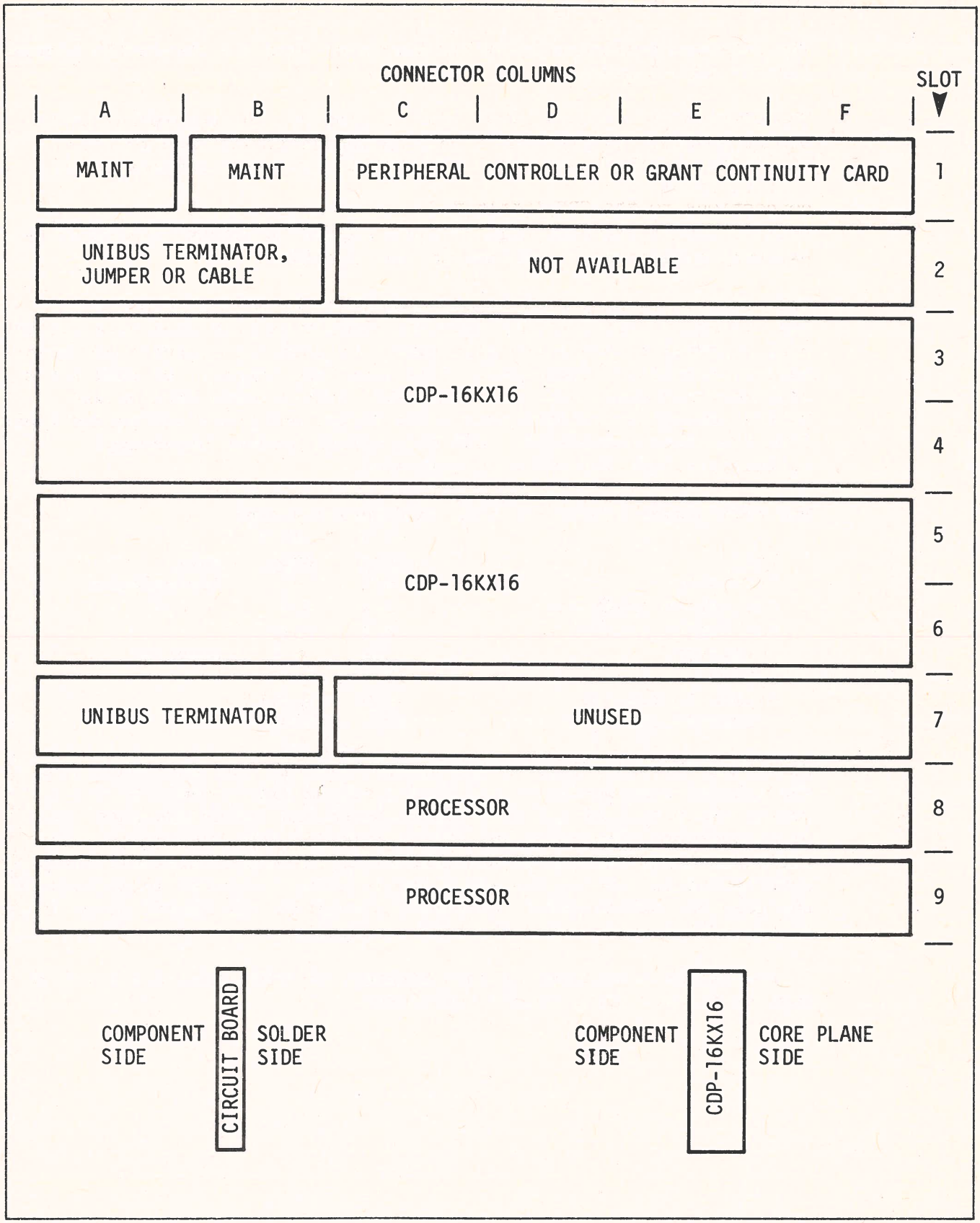


Figure 4-3. 32K-Word Configuration 1A

4.2.2 24K-Word Configuration 1B

The 24K-word configuration 1B (Figure 4-4) uses one CDP-16KX16 module and one MM11-L module.

The CDP-16KX16 module is installed in slot 3. The core-plane board blocks adjacent slot 4 even though no connection is made to the CDP-16KX16 in this location. The UNIBUS terminator remains in connectors 5A/5B.

UNIBUS signals are available in slots 2A/2B. A UNIBUS terminator or external cable can be inserted in this location.

Note that empty slot 2 is wired to contain the MM11-L core stack. The wiring in this location does not conform to that used by a peripheral controller, hence the slot cannot be used for standard DEC quad-height controller assemblies. This slot can, however, be used for a user-designed controller on a HEXBOARD. Such a board obtains all UNIBUS communication from connectors 2A/2B, and power and ground inputs from the other connectors. Cal Data offers various hex-height controllers that interface in this slot.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
Processor	8.0	-	Approximate.
One MM11-L operating	3.4	6.0	
One 16KX16 standby	2.4	0.44	
Terminator	1.2	-	Required.
LOAD	15.0	6.44	
Available reserve	2.0	-(0.44)	
SUPPLY LIMIT	17.0	6.00	

Note that the -15 V is over the supply limit in this configuration. The standby consumption on -15 V of a second MM11-L would be 0.5 A versus the 0.44 A of the CDP-16KX16, hence the latter presents *less* of an overload than using two MM11-L memories (the CDP-16KX16 power rating given is for worst-case conditions). Should difficulties be experienced in running the -15 V supply above the rated load, consult the computer manufacturer concerning provisions for normal operation of two MM11-L units under the same conditions.

If the UNIBUS terminates in this cabinet, an additional 1.2 A (+5 V) must be allowed for a second terminator.

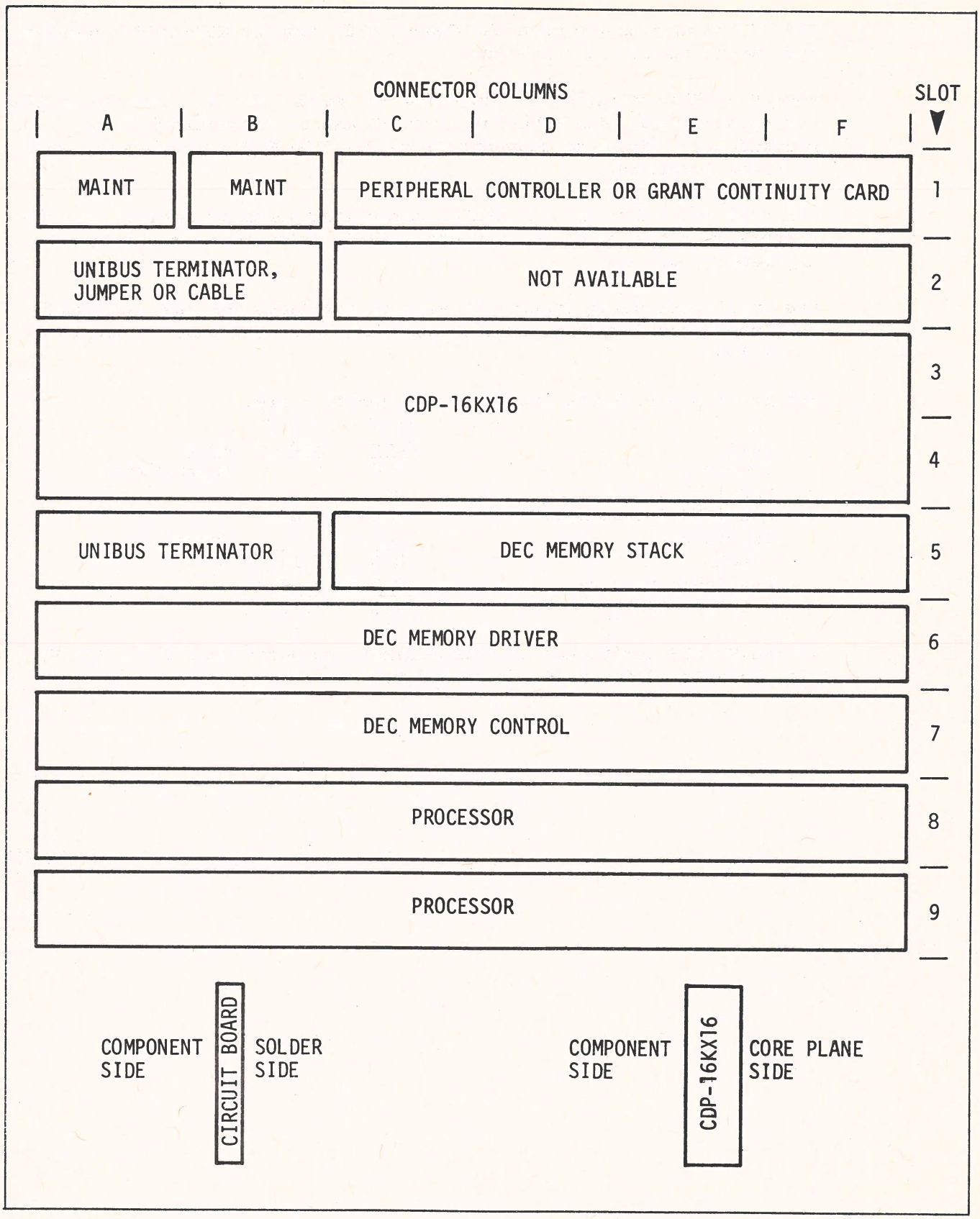


Figure 4-4. 24K-Word Configuration 1B

4.2.3 32K-Word Configuration 2A

The 32K-word configuration 2A (Figure 4-5) has two CDP-16KX16 modules and two peripheral controllers.

The CDP-16KX16 modules are installed in slots 3 and 5. Because of the core-plane board, the adjacent slots (4 and 6, respectively) are blocked even though no connections to the CDP-16KX16 modules are made in these locations.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installation of any memory modules.

One small-peripheral controller slot is available for use, provided that the overall system power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
Processor	8.0	-	Approximate.
One 16KX16 operating	3.2	4.7	
One 16KX16 standby	2.4	0.44	
Terminator	1.2	-	Required.
LOAD	14.8	5.14	
Available reserve	2.2	0.86	
SUPPLY LIMIT	17.0	6.00	

If the UNIBUS terminates in this cabinet, an additional 1.2 A (+5 V) must be allowed for a second terminator.

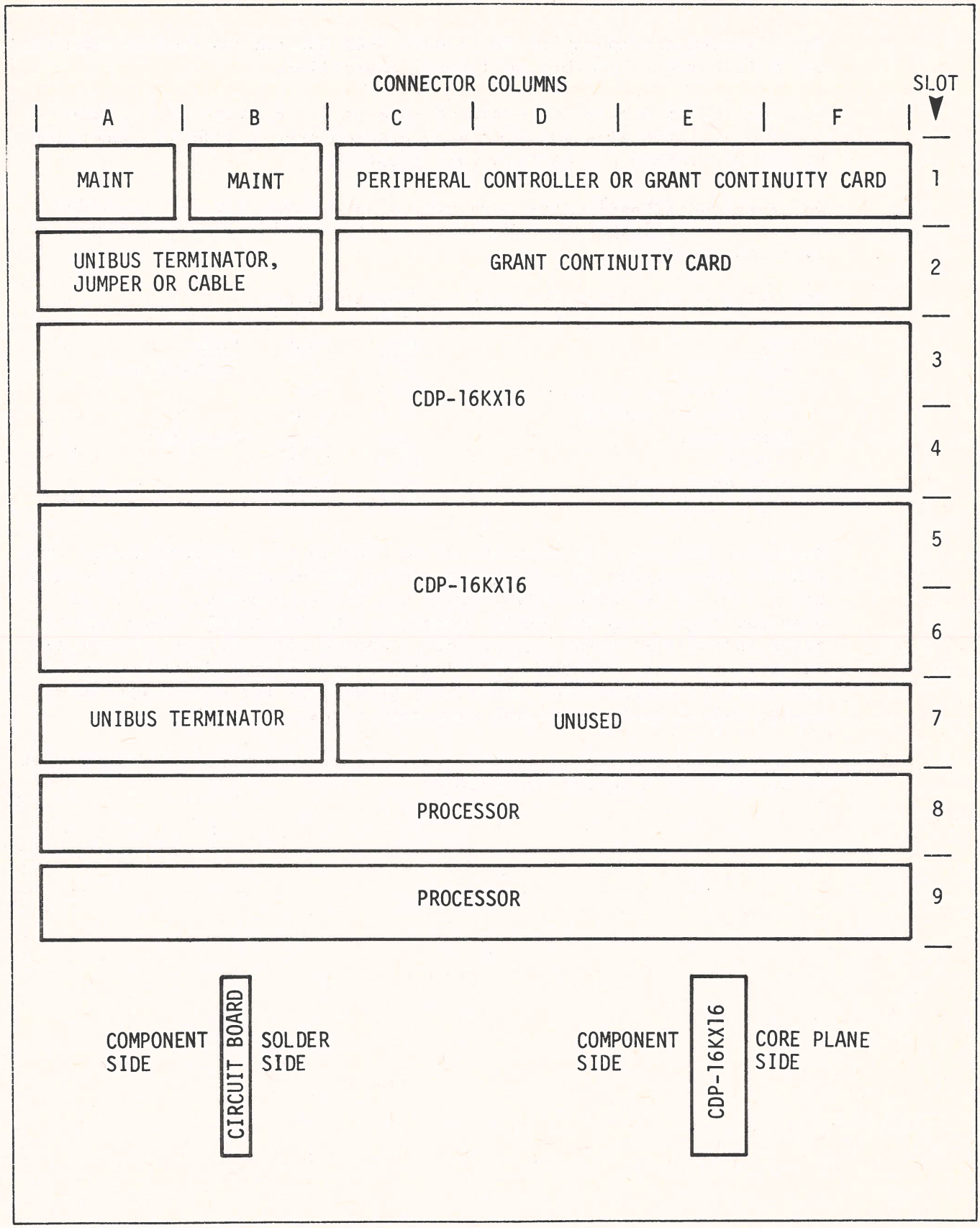


Figure 4-5. 32K-Word Configuration 2A

4.2.4 24K-Word Configuration 2B

The 24K-word configuration 2B (Figure 4-6) has one CDP-16KX16 module, one MM11-L module and one peripheral controller.

The CDP-16KX16 module is installed in slot 3. Because of the core-plane board, the adjacent slot 4 is blocked even though no connections to the CDP-16KX16 are made in this location.

One small-peripheral controller slot is available for use, provided that the overall system +5 V power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
Processor	8.0	-	Approximate.
One MM11-L operating	3.4	6.0	
One 16KX16 standby	2.4	0.44	
Terminator	1.2	-	Required.
LOAD	15.0	6.44	
Available reserve	2.0	-(0.44)	
SUPPLY LIMIT	17.0	6.00	

Note that the -15 V is over the rated load in this configuration. The standby consumption on -15 V of a second MM11-L would be 0.5 A versus the 0.44 A of the CDP-16KX16, hence the latter presents *less* of an overload than using two MM11-L memories (the CDP-16KX16 power rating given is for worst-case conditions). Should difficulties be experienced in running with the -15 V supply above the rated load, consult the computer manufacturer concerning provisions for normal operation of two MM11-L units under the same conditions.

If the UNIBUS terminates in this cabinet, 1.2 A additional (+5 V) must be allowed for a second terminator.

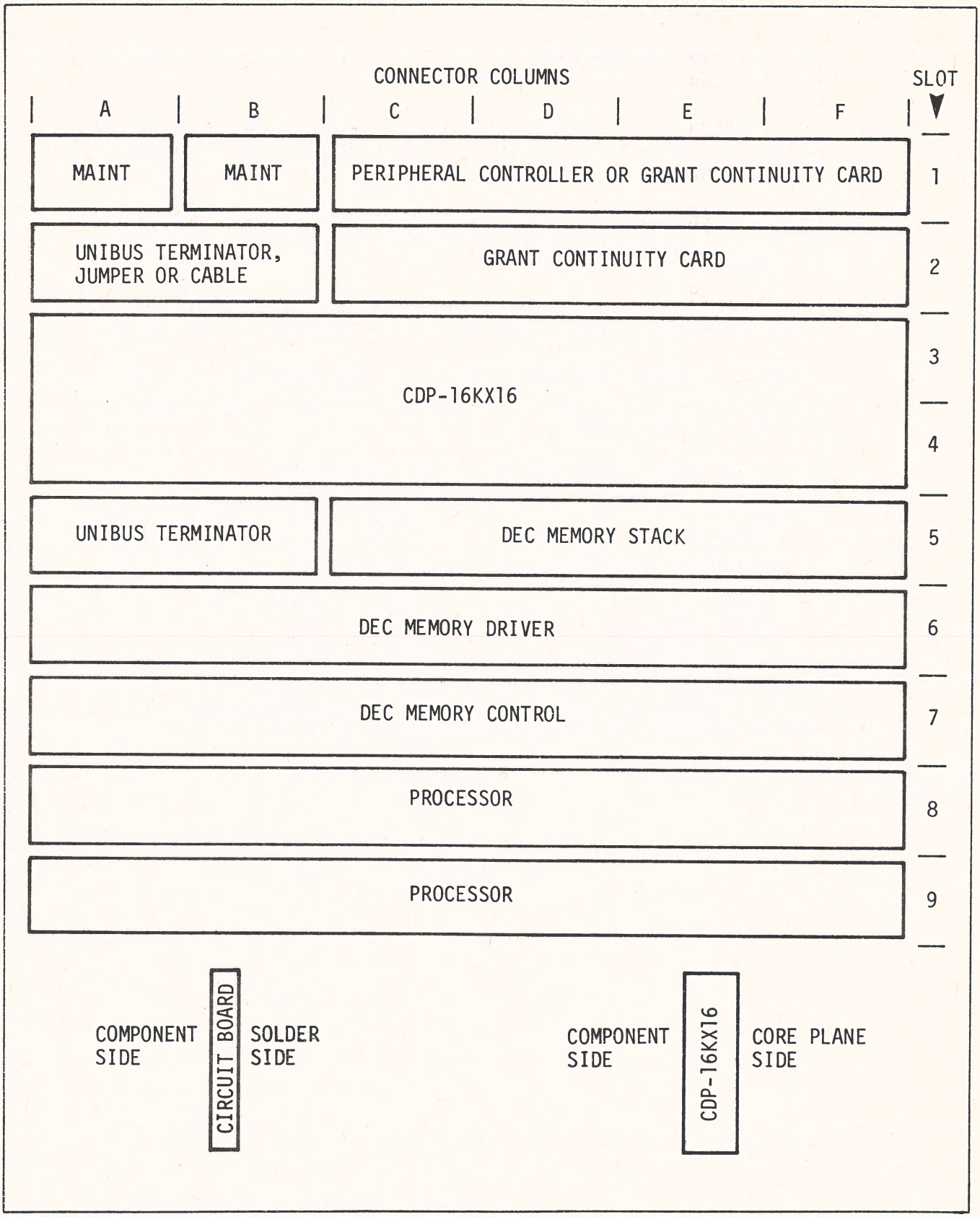


Figure 4-6. 24K-Word Configuration 2B

4.2.5 16K-Word Configuration 2C

The 16K-word configuration 2C (Figure 4-7) has one CDP-16KX16 module and four peripheral controllers.

The CDP-16KX16 is installed in slot 5. Because of the core-plane board, the adjacent slot 6 is blocked even though no connections to the CDP-16KX16 are made in this location.

For this installation, the UNIBUS terminator normally located in connectors 5A/5B is moved to connectors 7A/7B prior to installing the memory.

Connectors 3A/3B and 4A/4B (labeled UNIBUS) are available for installing either the second terminator or the external UNIBUS cable.

Three small-peripheral controller slots are available for use, provided that the overall system power consumption does not cause an overload condition.

The rated power limits for this configuration are:

Unit	+5 V Amps	-15 V Amps	Note
Processor	8.0	-	Approximate.
One 16KX16 operating	3.2	4.7	
Terminator	1.2	-	Required.
LOAD	12.4	4.7	
Available reserve	4.6	1.3	
SUPPLY LIMIT	17.0	6.0	

If the UNIBUS terminates in this cabinet, an additional 1.2 A (+5 V) must be allowed for a second terminator.

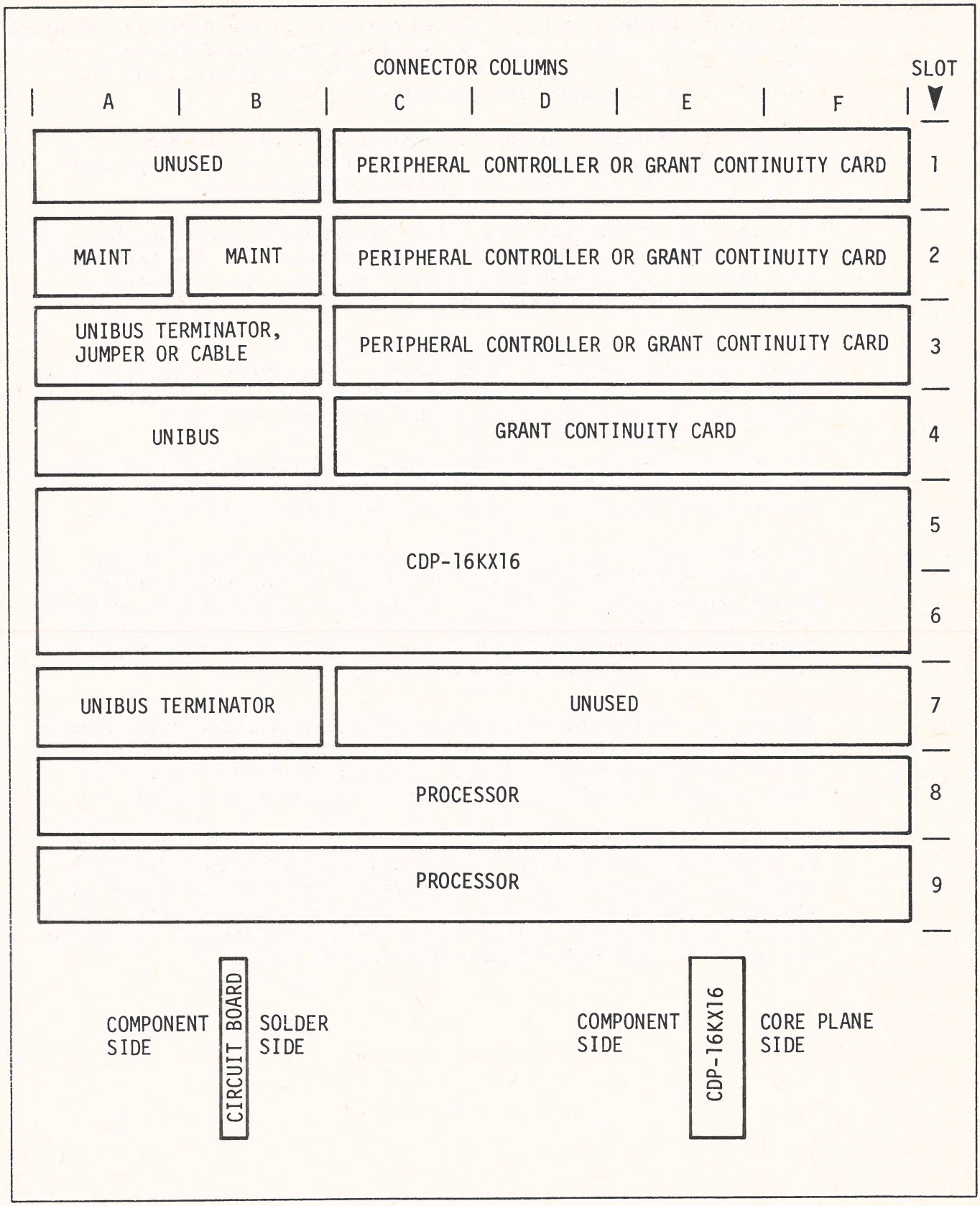


Figure 4-7. 16K-Word Configuration 2C

4.3 INSTALLATION IN THE PDP-11/35, PDP-11/40 OR PDP-11/45

CDP-16KX16 modules can be installed directly in the PDP-11/40 mounting box (BA11-FC). Figure 4-8 shows a view of the module side of the cabinet, Figure 4-9 shows a multiple-module installation and Figure 4-10 shows the backplane connectors.

Although the material in this subsection is a specific description of CDP-16KX16 installations in the PDP-11/40, it is also applicable to the PDP-11/35 and PDP-11/45, with minor differences.

The basic system contains two double system units for board installation, each unit containing nine rows of connectors. The first nine-slot unit contains the processor and associated option boards and is not used for memory installation.

The second double system unit is prewired for one to three MM11-L memory modules. Each MM11-L module is a three-board assembly consisting of a stack, memory driver and control board. Thus, this double system unit generally contains 8K to 24K of MM11-L memory.

The remainder of the BA11-FC box can be used for single or double system units for additional memory or peripheral interfaces. Each double system unit is equivalent to five single system units.

This section presents typical installation details for mounting CDP-16KX16 modules in the assembly with or without MM11-L memories. Memory expansion beyond the basic double unit for memory is identical when other MM11-L backplanes are installed. The user can use the information provided to determine the installation method required for other types of system mounting units.

Figure 4-11 shows slot allocation for a fully-expanded 24K assembly using MM11-L memories. The MM11-L memory driver and control/data boards are hex height and use all six connectors of a slot. The stack board is quad height and occupies columns C to F only.

The A and B connectors in slots 1 and 9 are used either to extend or to terminate the UNIBUS. The standard UNIBUS jumper is used to extend the bus from system unit to system unit. The terminator is placed in the last system unit at or near the end of the bus. These requirements, and the number of MM11-L modules installed, determine the number of CDP-16KX16 modules that can be used.

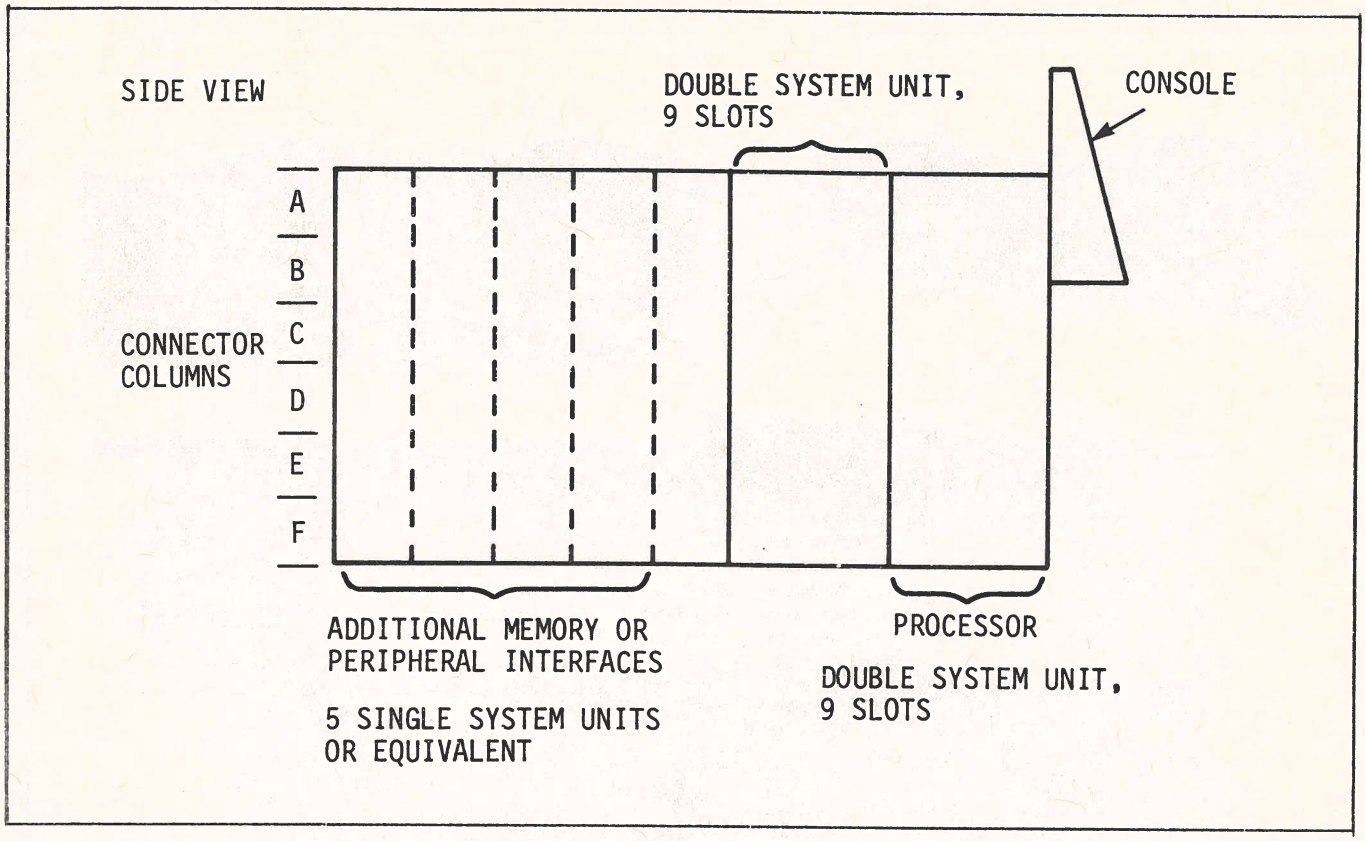


Figure 4-8. PDP-11/40 Mounting Box

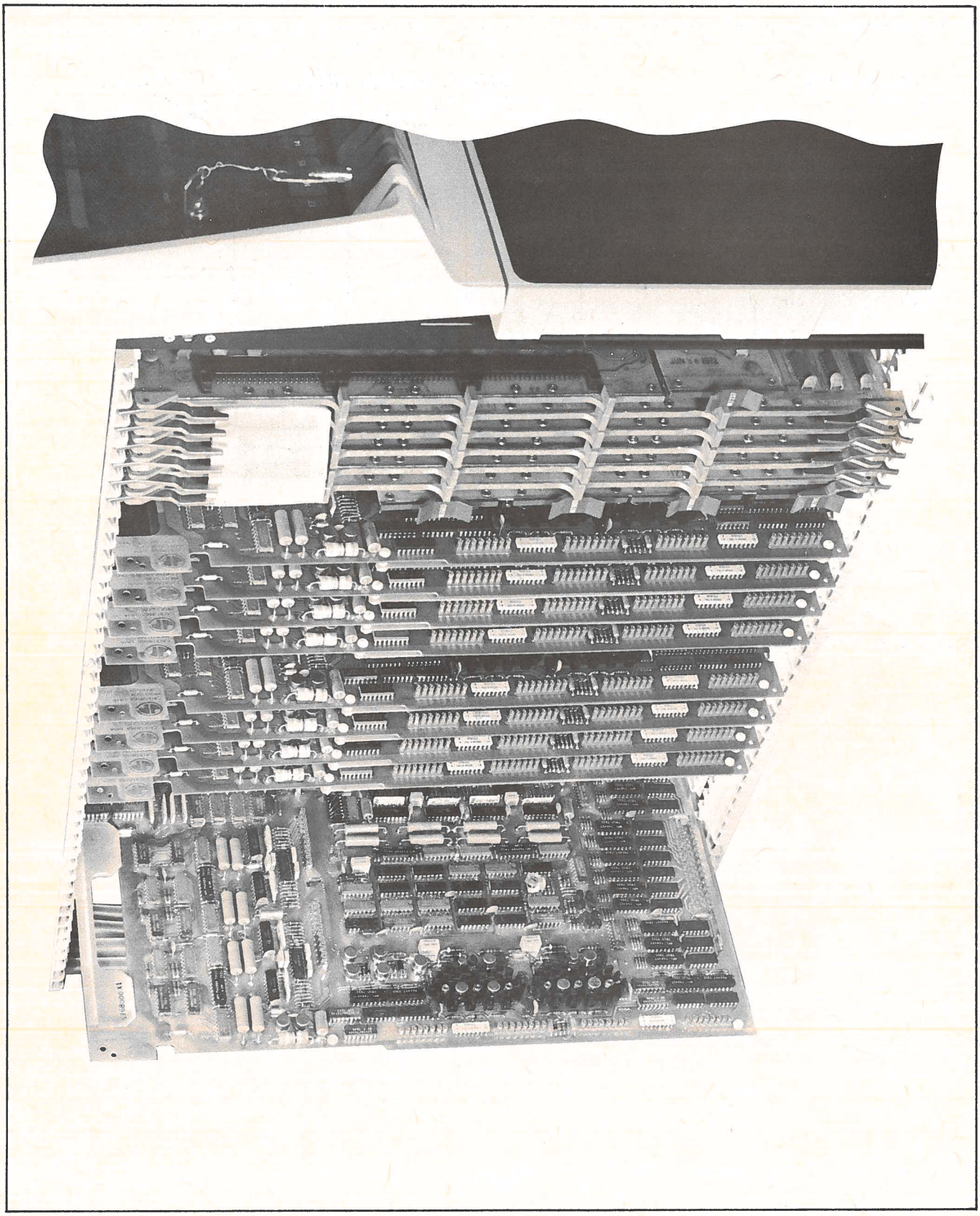


Figure 4-9. PDP-11/40 Multiple-Module Installation

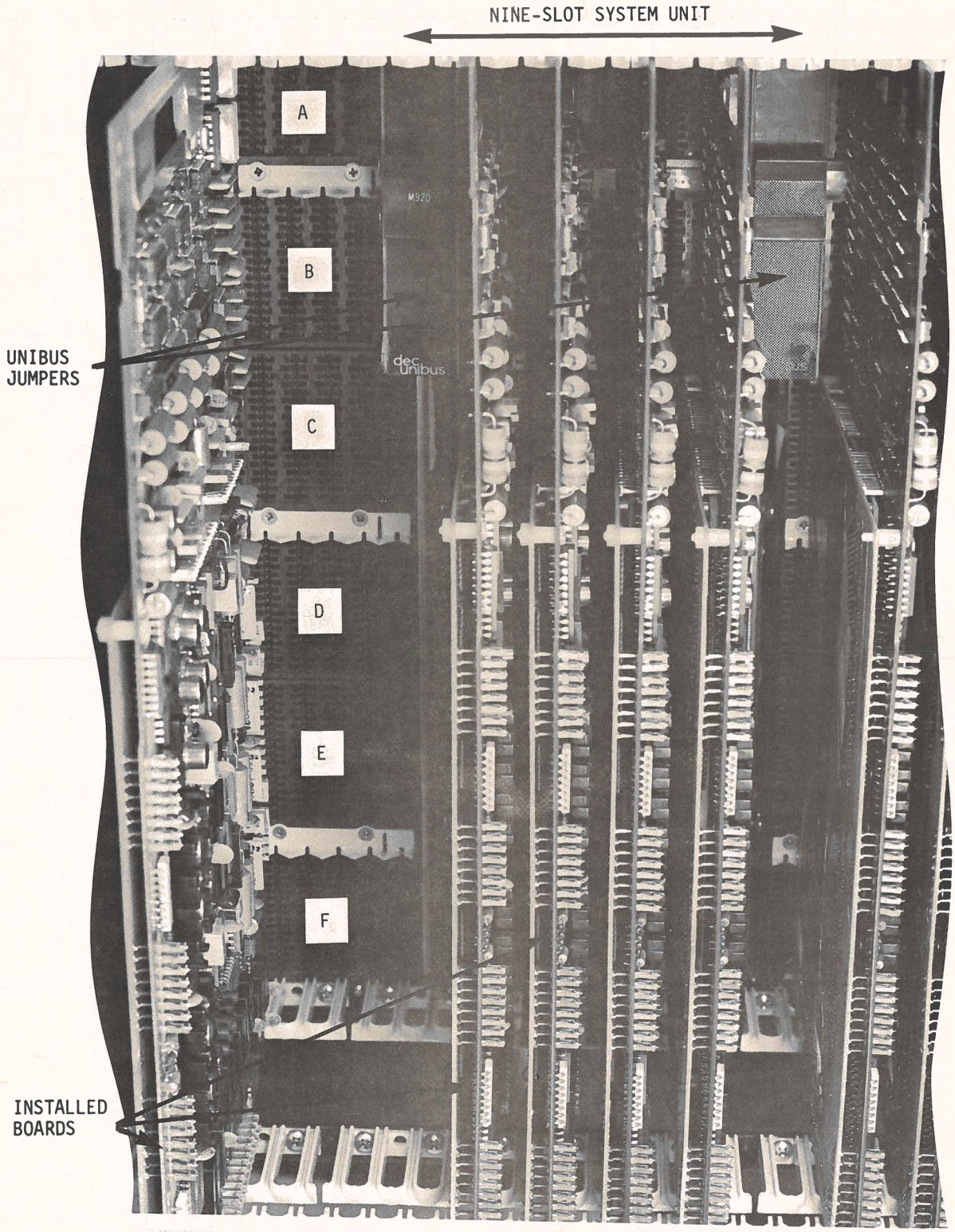


Figure 4-10. PDP-11/40 Backplane Connector Scheme

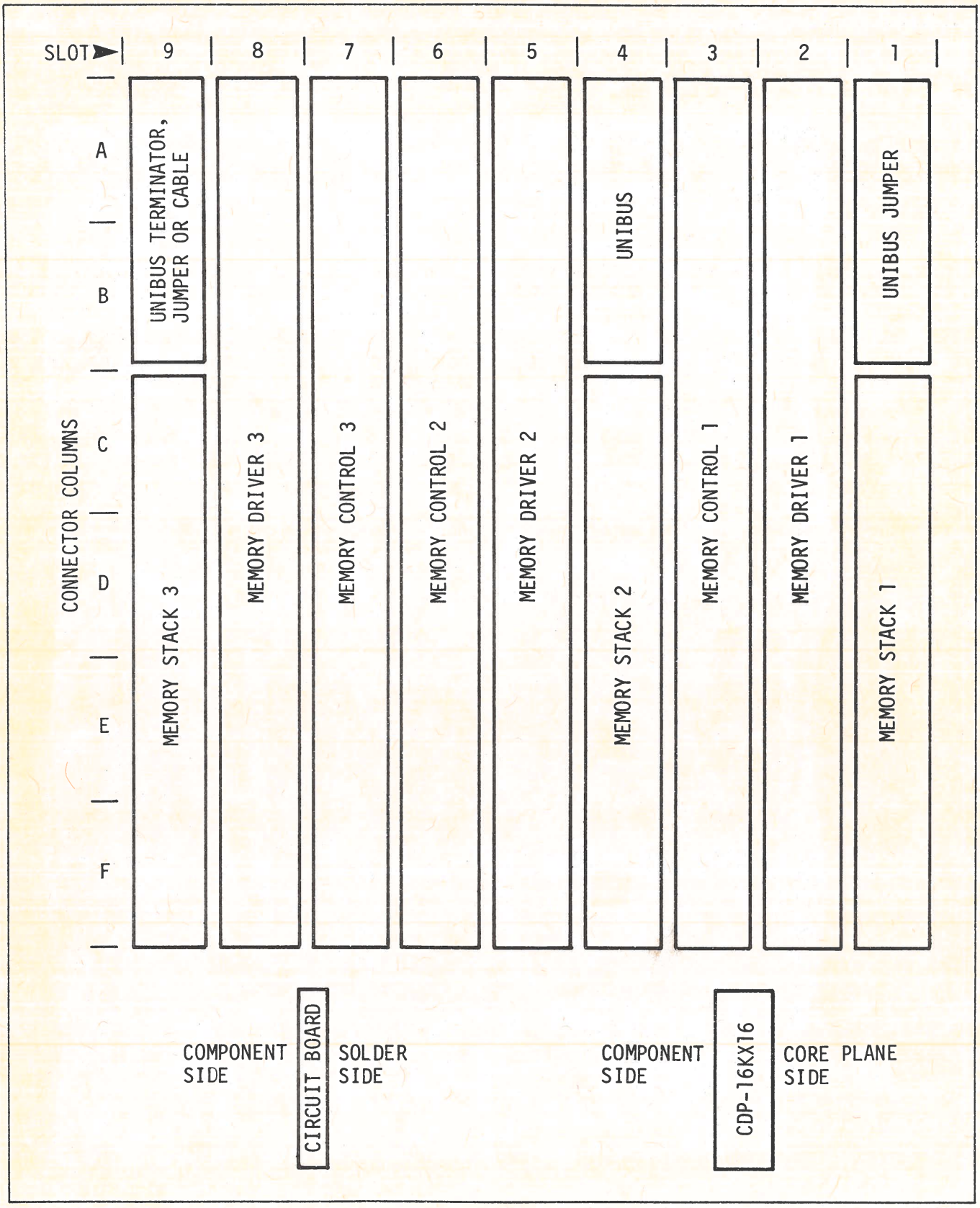


Figure 4-11. DEC Assembly Utilization (24K)

The following are general rules for using the CDP-16KX16:

a. The component side cannot be adjacent to a board that occupies connector columns C to F, because CDP-16KX16 components in this area can make contact with the adjacent board.
b. The component side of a CDP-16KX16 can be adjacent to a board that occupies connector columns A and B only (e.g., the standard UNIBUS jumper and terminator boards).
c. The component side of a CDP-16KX16 always faces the same direction as the components of all other boards in the system.
d. Always have power OFF when inserting or removing boards. Check the memory board for proper component orientation before insertion. Excessive force applied to a reversed board can result in damage to the backplane connectors.
e. Memory management is required for configurations that total more than 32K of memory.
f. The core plane side blocks the adjacent higher-numbered slot. The second higher slot can be occupied by another CDP-16KX16 module, or by any other board whose maximum height does not exceed that of the CDP-16KX16 components.
g. The Cal Data board adapter assembly should be installed on the CDP-16KX16 to make proper contact with the card guides of the computer cabinet.

Installations in PDP-11/35 extension box are analagous to those in PDP-11/05 computers (subsection 4.2).

4.3.1 48K-Word Configuration

The 48K-word configuration (Figure 4-12) has three CDP-16KX16 modules in a nine-slot system unit with no MM11-L installed. For this configuration, memory management is required.

The CDP-16KX16 modules are installed in slots 2, 4 and 6. A UNIBUS terminator board is installed in connectors 9A/9B if the bus is to be terminated at that point. If the bus is to be extended, a UNIBUS jumper or extension cable is used rather than the terminator.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One 16KX16 operating	3.2	4.7	
Two 16KX16 standby	4.8	0.88	
MINIMUM LOAD	8.0	5.58	
Terminator	1.2	-	If required.
TOTAL LOAD	9.2	5.58	Noninterleaved.
Interleaved	0.9	4.3	Optional.
INTERLEAVE LOAD	10.1	9.88	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

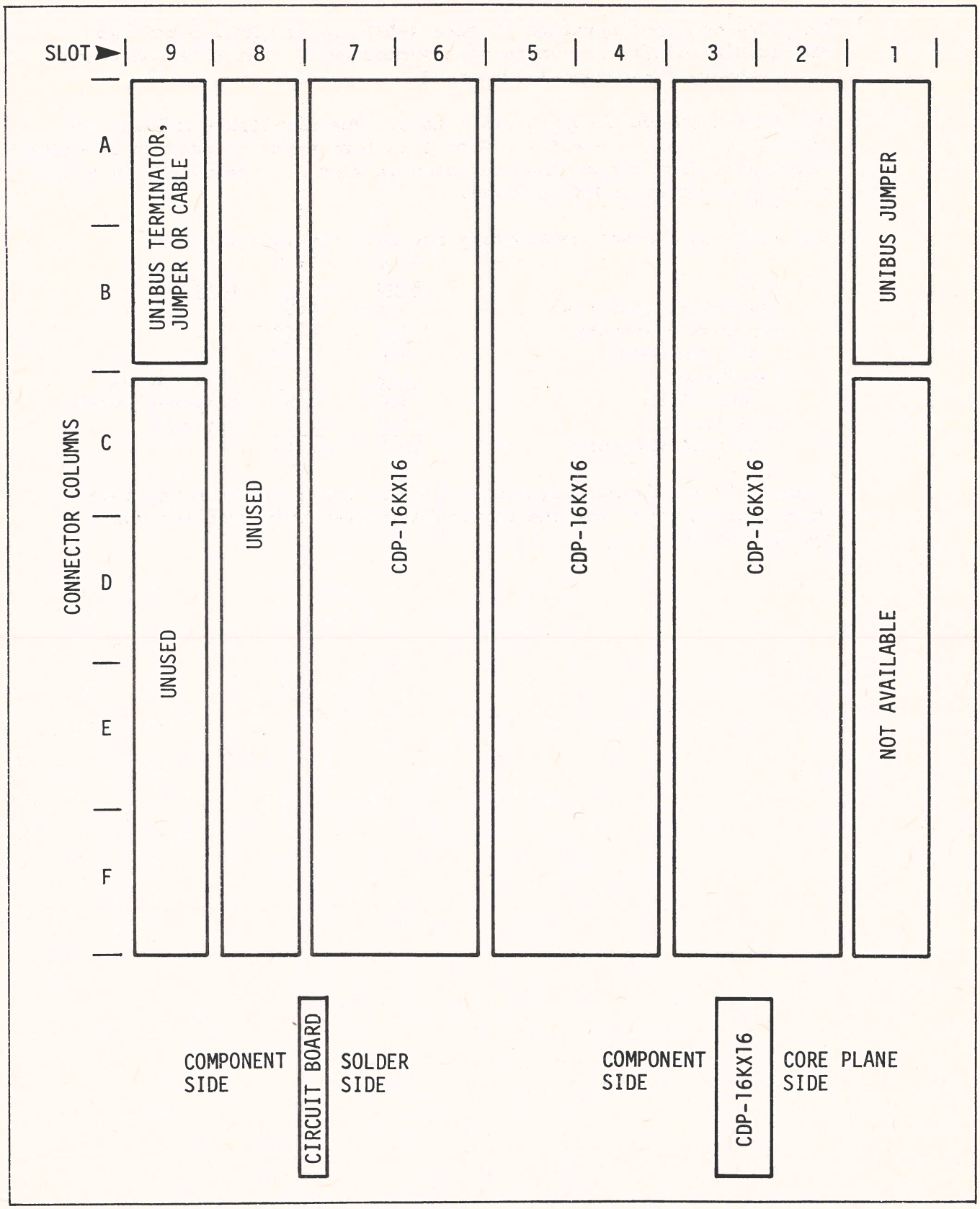


Figure 4-12. 48K-Word Configuration

4.3.2 40K-Word Configuration

The 40K-word configuration (Figure 4-13) has one MM11-L and two CDP-16KX16 modules in a nine-slot system unit. For this configuration, memory management is required.

The MM11-L boards occupy slots 1 to 3. The CDP-16KX16 modules are installed in slots 5 and 7. Slot 4 is left empty to prevent CDP-16KX16 components from contacting the board in slot 3. The UNIBUS is either terminated or extended at 9A/9B.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One MM11-L operating	3.4	6.0	
Two 16KX16 standby	4.8	0.88	
MINIMUM LOAD	8.2	0.88	
Terminator	1.2	-	If required.
TOTAL LOAD	9.4	6.88	Noninterleaved.
Interleaved	0.9	4.3	Optional
INTERLEAVED LOAD	10.3	11.18	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

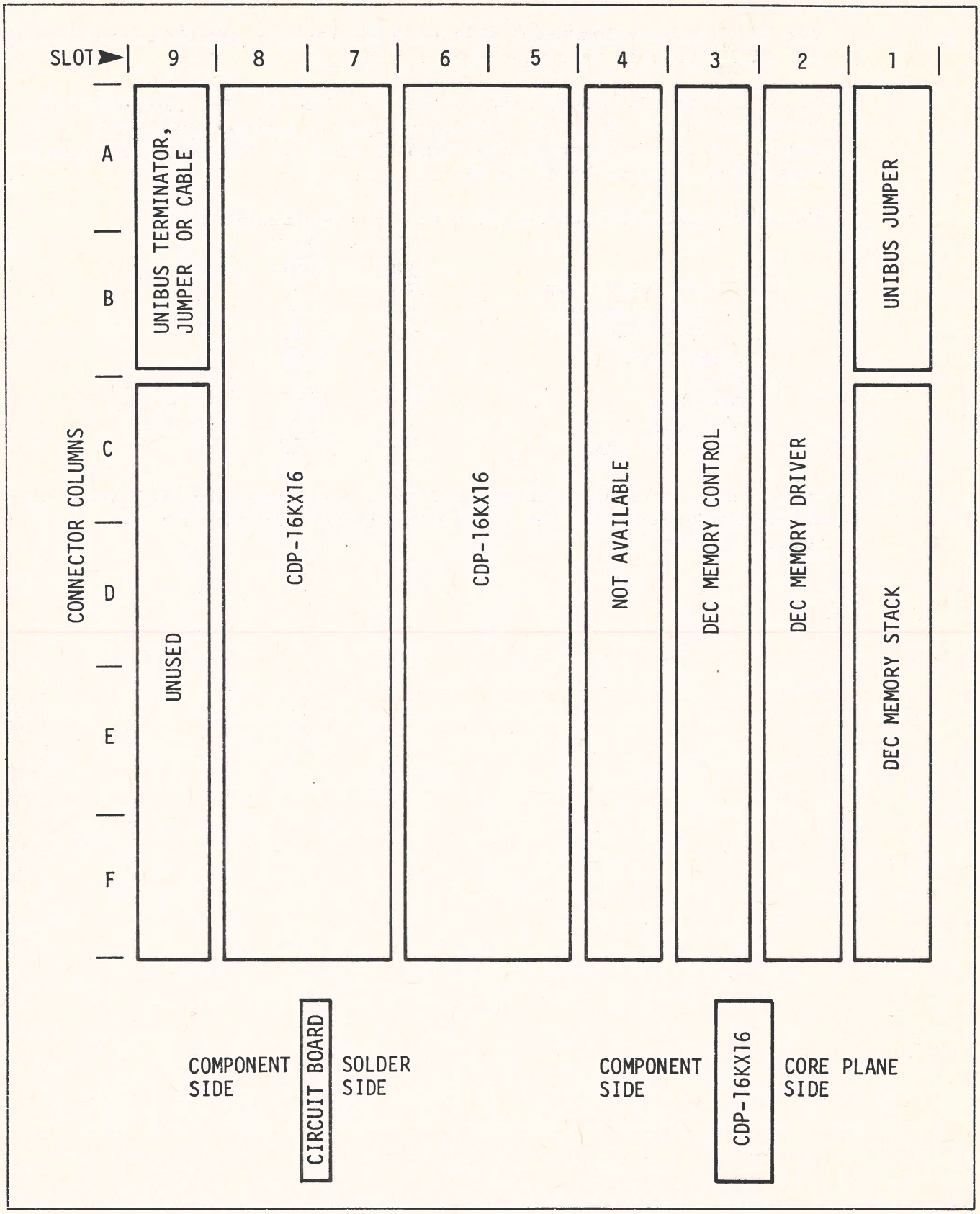


Figure 4-13. 40K-Word Configuration

4.3.3 32K-Word Configuration

The 32-K word configuration (Figure 4-13) has one CDP-16KX16 and two MM11-L modules in a nine-slot system unit.

The MM11-L boards occupy slots 1 to 3 and 7 to 9. The CDP-16KX16 is installed in slot 5. Slot 4 is left empty to prevent CDP-16KX16 components from contacting the board in slot 3. The UNIBUS is either terminated or extended at 9A/9B.

The worst-case power consumption for this configuration is:

Unit	+5 V Amps	-15 V Amps	Note
One MM11-L operating	3.4	6.0	
One MM11-L standby	1.7	0.50	
One 16KX16 standby	2.4	0.44	
MINIMUM LOAD	7.5	6.94	
Terminator	1.2	-	If required.
TOTAL LOAD	8.7	6.94	Noninterleaved.
Interleaved	0.9	4.10	Optional
INTERLEAVE LOAD	9.6	11.04	

Check this requirement against the power available from the power distribution panel for the particular system unit used for the memory modules.

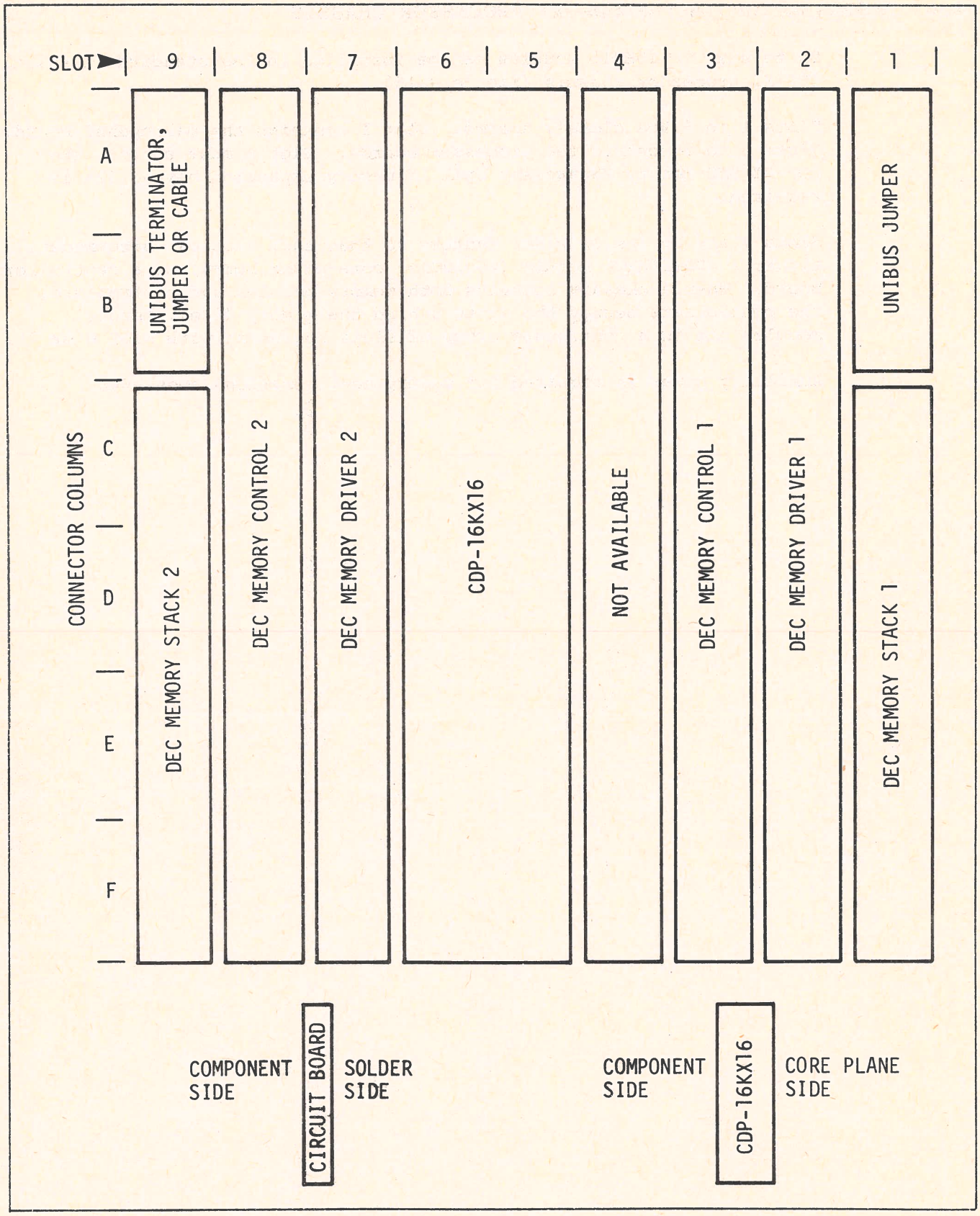


Figure 4-14. 32K-Word Configuration

4.4 INSTALLATION IN THE CDP-XI PROCESSOR CHASSIS

Up to six CDP-16KX16 modules can be installed in the standard (12-slot) CDP-XI processor chassis (Figure 4-15).

Slots 1 to 6 are closely spaced. Slot 1 contains the macropanel board. Slots 2 to 5 contain the processor boards. Slot 6 must contain the CDP-XI/MMU Memory Management Unit if memory expansion beyond 32K is required.

Slots 7 and up are on wider centers so that each slot can accommodate either a CDP-16KX16 module (*including* core-plane board) or a controller board. When a chassis contains both memory modules and controllers, the controllers occupy the slots behind the memory (i.e., memory modules are in a contiguous group of slots beginning with slot 6 or 7).

Auxiliary power is required for memory configurations above 64K.

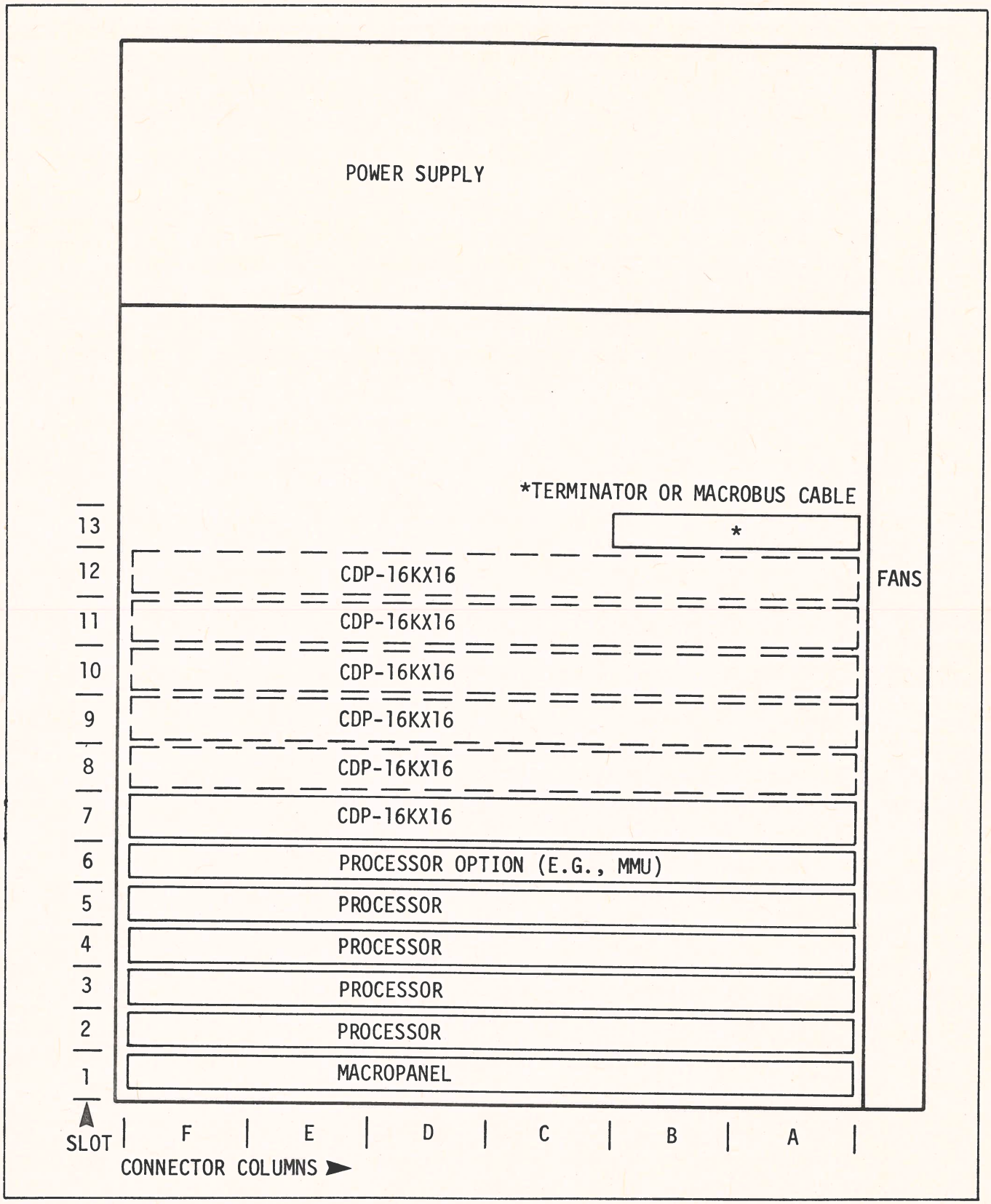


Figure 4-15. CDP-XI Chassis Layout

SECTION 5
MAINTENANCE

(In work.)

APPENDIX A
INTERFACE PIN ASSIGNMENTS

Table A-1 gives interface pin assignments for A and B connectors that interface all active signal lines used by the CDP-16KX16. Table A-2 gives ground and power inputs and propagated Bus Grant line pins associated with the D and F connectors. Figure A-1 is a drawing of the connector layout.

Table A-1. CDP-16KX16 Interface Pin Assignments

Signal	Connector		Signal
INIT L	AA1	AA2	* +5 V
* INTR L	AB1	AB2	GND
D00 L	AC1	AC2	GND
D02 L	AD1	AD2	D01 L
D04 L	AE1	AE2	D03 L
D06 L	AF1	AF2	D05 L
D08 L	AH1	AH2	D07 L
D10 L	AJ1	AJ2	D09 L
D12 L	AK1	AK2	D11 L
D14 L	AL1	AL2	D13 L
* PA 1	AM1	AM2	D15 L
GND	AN1	AN2	* PB 1
GND	AP1	AP2	* BBSY L
GND	AR1	AR2	* SACK L
GND	AS1	AS2	* NPR L
GND	AT1	AT2	* BR7 L
* NPG H	AU1	AU2	* BR6 L
* BG7 H	AV1	AV2	GND
* BG6 H	BA1	BA2	* +5 V
* BG5 H	BB1	BB2	GND
* BR5 L	BC1	BC2	GND
GND	BD1	BD2	* BR4 L
GND	BE1	BE2	* BG4 H
* ACLO L	BF1	BF2	DCLO 1
A01 L	BH1	BH2	A00 L
A03 L	BJ1	BJ2	A02 L
A05 L	BK1	BK2	A04 L
A07 L	BL1	BL2	A06 L
A09 L	BM1	BM2	A08 L
A11 L	BN1	BN2	A10L
A13 L	BP1	BP2	A12 L
A15 L	BR1	BR2	A14 L
A17 L	BS1	BS2	A16 L
GND	BT1	BT2	C1 L
SSYN L	BU1	BU2	C0 L
MSYN L	BV1	BV2	GND

*Pins assigned in the UNIBUS, but not used by the CDP-16KX16.

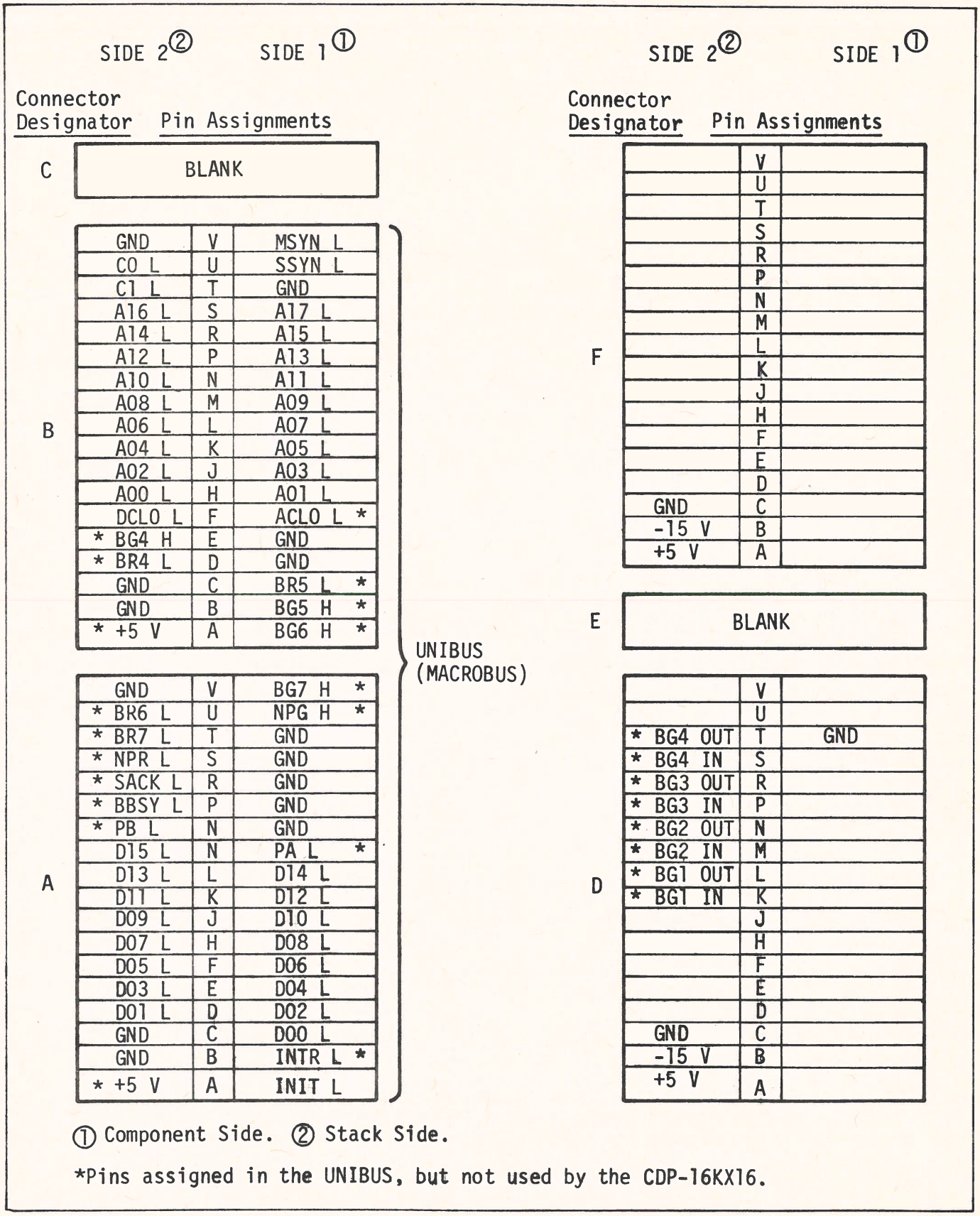
Table A-2. CDP-16KX16 Power and Bus-Grant Pin Assignments

Power	
Signal	Connector
+5 V	DA2
+5 V	FA2
-15 V	DB2
-15 V	FB2
GND	DC2
GND	FC2
GND	DT1
GND	FT1

Bus Grant	
Signal	Connector
*BG1 IN	DK2
*BG1 OUT	DL2
*BG2 IN	DM2
*BG2 OUT	DN2
*BG3 IN	DP2
*BG3 OUT	DR2
*BG4 IN	DS2
*BG4 OUT	DT2

*Pins assigned in the UNIBUS, but not used by the CDP-16KX16.

These signals are properly jumpered in the CDP-16X16 to provide bus-grant continuity.



① Component Side. ② Stack Side.

*Pins assigned in the UNIBUS, but not used by the CDP-16KX16.

Figure A-1. CDP-16KX16 Interface Connector Layout

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