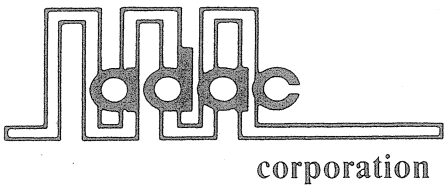
1953, 1903CT, 1903BC

INSTRUCTION MANUAL



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1953, 1903CT, 1903BC

INSTRUCTION MANUAL

IM- 784
A2-10675, Rev. 0F

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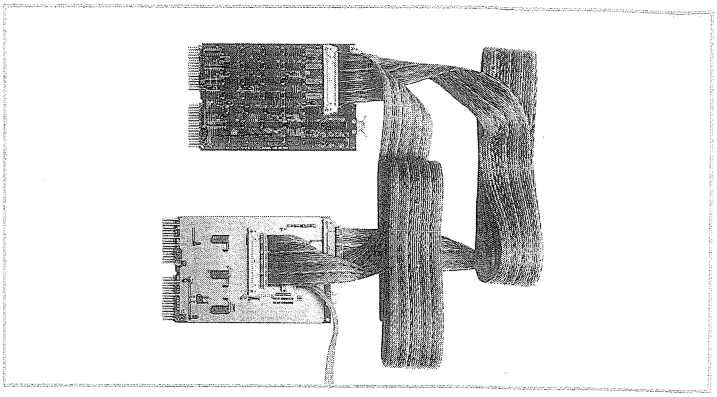
adac corporation

	ADAC MODELS	COMPATIBLE WITH
BUS REPEATER	1953	DEC LSI-11/2, LSI-11/23, and ADAC Series 1200, 2200, 3200
CABLE TERMINATOR	1903CT	
BUS CABLE SET	1903BC	

FEATURES

- High Noise Immunity, Controlled Rise-Time Transceivers
- On-board Arbitration for DMA and Multi-level Interrupts
- Repowered Data and Control Signals
- Coordinated Power Up-Down Sequencing
- Block Mode DMA — 2 Million wps
- Q-Bus Memory Parity and Bus Parity
- Up to 21 Slave Backplanes, 462 Slots
- 16, 18 and 22 Bit Addressing



GENERAL DESCRIPTION

Model 1953 is an active bus repeater designed to provide fully transparent multiple backplane operation in systems having a single CPU. By receiving Q-Bus signals and generating an almost identical set of signals for the slave backplane, Model 1953 repowers the slave bus to maintain bandwidth performance within Q-Bus specifications. Propagation delay of only 57 nanoseconds is typical, including transit time of two backplanes and a 10′ cable.

Provided with on-board arbitration and multiple levels of interrupt, Model 1953 supports all commonly used Q-Bus facilities as well as the recently defined DEC block mode DMA and bus parity. Cards and/or peripherals in the multiple backplane topography appear as if they were adjacent to the CPU. LSI-11/23 expanded memory 22 bit addressing is fully supported, including memory parity and DMA, to allow up to 4 megabytes of memory to be plugged into master or slave. Removable jumpers facilitate 16 or 18 bit operation.

Each Model 1953 contains on-board arbitration logic to handle DMA grants and to detect the highest level of priority requested by the slave buses. For LSI-11/2 and SBC-11/21 CPU's, a single interrupt structure grants interrupt priority based on the relative proximity of the requesting card to the CPU. When operating with an LSI-11/23 CPU, multiple level interrupt is employed at levels 4, 5, 6 and 7, with level 7 having highest priority.

Orderly up-down power sequencing protects system status, with each Model 1953 sensing both AC input and 5V power supply output for its slave. The slaves can be turned on simultaneously or in any order with the last one "on" asserting status signals and controlling the re-boot or restoration of the system. In the event of impending slave failure, the 1953 will initiate orderly system shutdown.

In supporting the recently defined DEC block mode DMA and bus parity features, Model 1953 permits memory transfers at 3 times or more normal Q-Bus bandwidth or up to 2 million words per second. This block mode DMA capability may permit systems expanded with Model 1953's to exceed the throughput rates of non-expanded, non-block mode DMA Q-Bus systems.

SYSTEM CONFIGURATION

The ideal system employs the "star" configuration with all Model 1953's positioned in the master backplane and cable-connected to their respective slave units. In this configuration, all slave boards and peripherals operate as if located in the master backplane without signal skewing and propagation delays. On-board arbitration resident in each 1953 detects interrupt request by priority level and passes control to the highest level request. Requests of equal priority level go the 1953 located closest to the CPU.

The maximum system configuration (with the ADAC Series 1200 enclosure) can be one CPU with 21 bus repeaters in the master enclosure. Each of the slaves can hold up to 22 cards for a maximum system card count of 462. Model 1953 has two cable terminator connectors on it for hook-up to its slave.

SYSTEM INTERCONNECT

When operating with ADAC Series 1200 or 2200 master and slave bus enclosures, cable connection is directly to the 40-pin and 50-pin headers on each ADAC backplane by means of the Model 1903BC bus cable set. Connection to non-ADAC master and slave units is facilitated by use of Model 1903CT cable terminator boards.

Model 1903CT is an LSI-11 half-quad cable terminator board for use with other than ADAC slave LSI-11 backplanes. When located in a slave unit, Model 1903CT is positioned in the first slot. Removable jumpers facilitate operation with 16 and 18 bit addressing. In a "star" configured system of other than ADAC backplanes, a Model 1903CT is installed in each slave unit, connected to its corresponding 1953 bus repeater through a 1903BC bus cable set.

Model 1903BC bus cable set is a pair of twisted-pair, shielded flat cables with strain-relieved connectors at each end to mate with ADAC LSI-11 backplanes, Model 1953 and Model 1903CT. Available in lengths from 10′ to 40′, Model 1903BC meets FCC Class A emission standards when connected to proper chassis grounds.

SPECIFICATIONS
MODEL 1953
BUS REPEATER

Function	Provides bi-directional drive capability for all DEC LSI-11 bus signals. Allows master backplane (with CPU) to drive up to 21 slave backplanes (without CPU). Can be used with any system structured around LSI-11 bus.
Point of Insertion	Unit is inserted in master backplane.
Method of Expansion	Connection from 1953 to expansion chassis made by means of Model 1903BC bus cables. The cables plug into headers on the 1953 and into the Model 1903CT cable terminator on the other end. The 1903CT plugs into one card slot of the expansion backplane. When used with the ADAC Series 1200 or 2200, the 1903BC plugs directly into the backplane without need for the 1903CT.
Bus Loading	One bus load for each line on master side.
Drive Capability	20 bus loads for each line on slave side.
Configuration	Back to back bi-directional open-collector transceivers.
Bus Terminators	Sockets for 120 ohm or 240 ohm terminator resistor packs on both sides of repeater. Normally supplied with networks on expansion side only.
Communications Method with Slave Peripherals	Program control, program interrupt, DMA and block mode DMA.
Interfacing Technique	Completely asynchronous, interlocking handshake interface between buses.
Effects on LSI-11 Programming	None. All LSI-11 instructions can operate across the repeater. Operation is transparent to programmer.
Max. Delay Through Repeater	57 ns, including 10′ of cable.
Service Request Methods	Levels 4, 5, 6 and 7 program interupt and DMA.
Addressing	16, 18 and 22 bit.
Parity	Q-Bus memory and bus parity.
Direct Memory Access	A DMA device plugged into expander bus can request bus mastership by asserting its BDMR line. Once granted mastership, the requesting device can then transfer data directly to any device on either side of the repeater.

PHYSICAL & ENVIRONMENTAL

Size	8½″ × 5″ × 0.375″ (standard DEC half quad)
Power	+5V ±5% @ 1.5 amps
Termperature Range of Operation	0°C to +55°C

SPECIFICATIONS
MODEL 1903CT
CABLE TERMINATOR

Function	Provides plug-in cable termination for 40-pin and 50-pin 1903BC bus cable set when utilizing Model 1953 in other than ADAC LSI-11 backplanes.
Bus Terminators	Sockets provided for optional bus terminators — none (standard), or 120 ohm.
Connectors	One 40- and one 50-pin header to receive 1903BC bus cable set. One 10-pin connector for power interlock between master and slave.
Size	8½″ × 5″ (half quad size)

SPECIFICATIONS
MODEL 1903BC
BUS CABLE SET

Function	Connects 1953 bus repeater in master to slave LSI-11 backplanes. One cable set used for each 1953 in system.
Lengths	10′, 15′, 20′, 30′, 40′.
Cable Type	Twisted-pair, flat ribbon cables. 40-Pin and 50-pin connectors at each end.
Ground	Common on 10′ and 15′; twisted with each signal on longer cables.

HOW TO ORDER

Model 1953 — [ ]

BUS TERMINATORS
0 = None (standard)
1 = 120 ohm

Model 1903CT-[ ]

BUS TERMINATORS
0 = None
1 = 240 ohm (standard)
2 = 120 ohm

Model 1903BC-[ ]

FLAT CABLE LENGTHS

10 = 10 ft.	10S = 10 ft. shielded
15 = 15 ft.	15S = 15 ft. shielded
20 = 20 ft.	20S = 20 ft. shielded
30 = 30 ft.	30S = 30 ft. shielded
40 = 40 ft.	40S = 40 ft. shielded

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PRINTED IN U.S.A.

CHAPTER 1

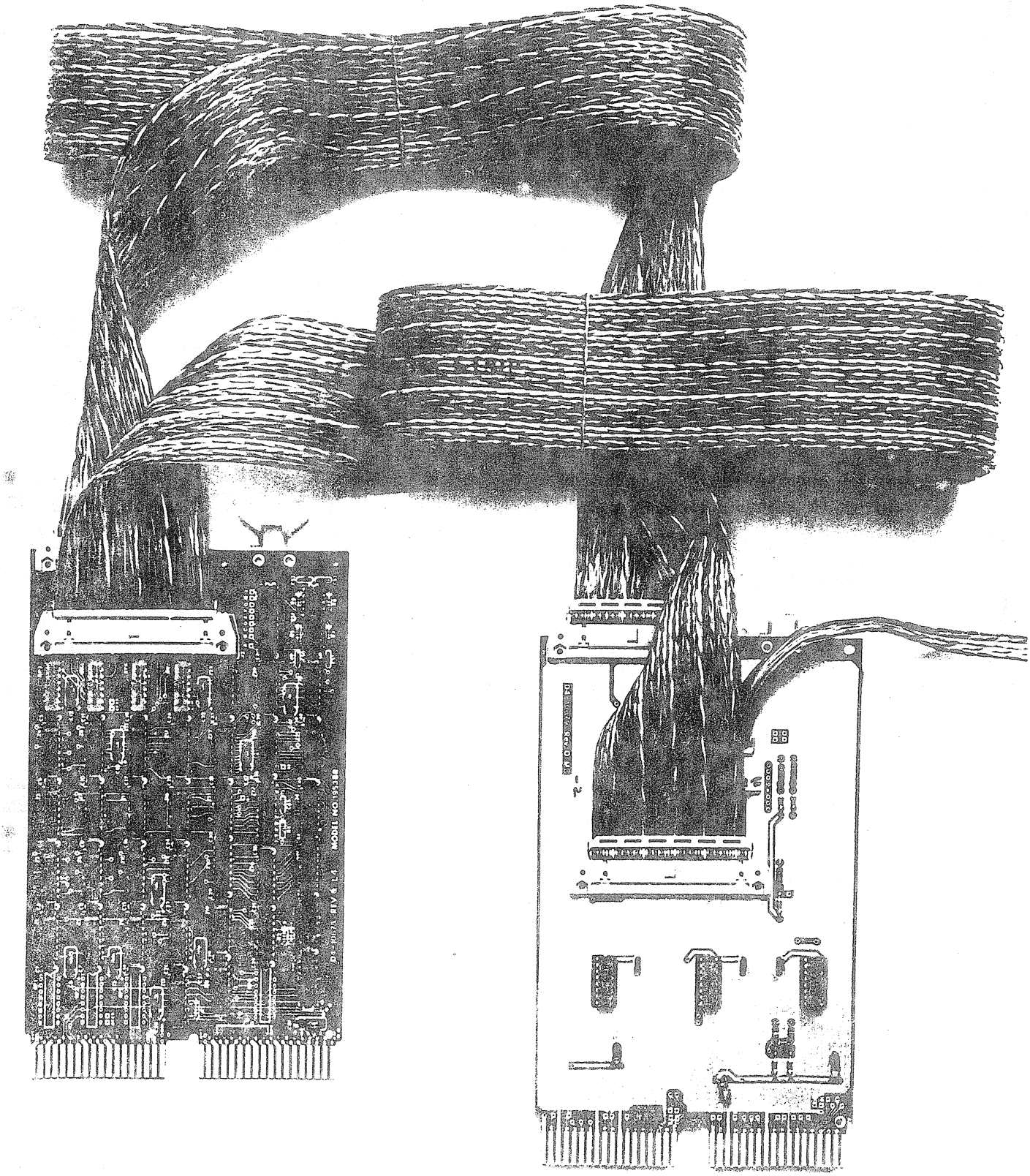
INTRODUCTION

This manual treats ADAC Corporation's latest system expanding products, the 1953 bus repeater, the 1903CT cable terminating card and the 1903BC interconnecting cable sets. It is intended as a guide to system implementers to help them make the tradeoffs in constructing a multiple backplane system from Q-BUS components.

The ADAC 1953 is an active bus repeater to be installed into a master Q-BUS backplane. The card then receives Q-BUS signals and creates a new but nearly identical set of signals to operate a "slave" Q-BUS backplane to which the card is attached. All Q-BUS transactions are supported and cards in the slave box(es) operate as though they were adjacent to the processor in the master box.

The ADAC 1953 supports all of the commonly used Q-BUS facilities and incorporates features contained in the Q-BUS definition and some new features which are defined in the specification but not yet widely available.

This manual describes the features of the 1953, compatibility issues, how to configure the board for special cases, how to apply the repeater into a variety of system configurations and, last, why it works. Our intention is to provide enough information in this manual to enable a system engineer to make informed choices in constructing very high performance Q-BUS systems.



1953, 1903CT,
1903BC Family

1.1 FEATURES OF THE 1953 BUS REPEATER

DESIGNED WITH:

1. HIGH NOISE IMMUNITY, HIGH QUALITY, CONTROLLED RISE-TIME Q-BUS TRANSCEIVERS (more Q-BUS compatible than the DEC parts)

2. ON-BOARD ARBITRATION FOR BOTH DMA AND INTERRUPTS (allows extraordinary capability for designing hierarchical priorities among DMA and INTERRUPTING devices)

3. REPOWERED DATA AND CONTROL SIGNALS into and out of the slave chassis's (unlike other passive "bus extenders")

4. COMPLETE COMPATIBILITY with a variety of ADAC, DEC, and other backplanes for the Q-BUS

SUPPORTS:

1. COORDINATED POWER SEQUENCING - Power on signals from all slave boxes are coordinated and redistributed from the master to allow proper "booting" and orderly shut-down on power turn-off.

2. COMPLETE PROCESSOR TRANSPARENCY (all attached backplanes and peripherals appear to the processor as though they are in the "master" chassis)

3. ALL ADDRESSING MODES - including 16-BIT, 18-BIT, 22-BIT

4. 4-LEVEL PRIORITY INTERRUPT using levels 4, 5, 6, and 7

5. STANDARD Q-BUS DMA transferring one word or byte using BDMR, BDMGI/O BSACK and device generated BSYNC, BDIN/BDOUT/BWTBT, address and data

6. MULTI-WORD Q-BUS DMA in which a device master transfers two or more words per mastership arbitration

7. Q-BUS MEMORY PARITY TRANSACTIONS (MSV11 - 11/23) using BDAL16/17 during the data phase of Q-BUS transactions

ALSO SUPPORTS THE RECENTLY ANNOUNCED (by DEC) capabilities:

1. BLOCK-MODE DMA (over 2 million words per second) in which the master performs one memory address selection followed by multiple data transfers at higher than normal Q-BUS rates

2. Q-BUS BUS PARITY in which the BDAL<18-21> lines are used to transmit bus parity information, both data and control.

With this combination of features, a user can expand a system today, using the 1953 and fully expect his system to support exciting new processors and peripherals about to be announced by DEC and by other third party vendors.

The 1953 bus repeater, as shipped, is compatible with nearly all currently manufactured Q-BUS products. By definition, nearly any system which contains a 1953 is a large system with large numbers of cards and with a large number of activities and operations to be coordinated. The benefits from resolving the relatively minor system engineering issues involved with a 1953 based system are quite numerous. The advantages of using the 1953 are:

1. at least one less processor to program and run
2. no additional program memory
3. avoid the cost of additional peripheral devices (disks, terminals)
4. no interprocessor links (serial or parallel)
5. avoid the cost of developing interprocessor linking software
6. avoid the cost and complication of system-engineering a multi-processor topology
7. up to 463 cards in a system (21 X 22 cards + cpu in a practical system)

The aggregate financial savings to a 1953 user can be in the 12,000 to 20,000 dollar range, depending on the nature of the application.

1.2 COMPATIBILITY

The 1953 is compatible with virtually all devices intended for integration into Q-BUS systems (both backplanes and card products). In some cases, especially where devices have not been designed exactly to specification, the compatibility issues are likely to be resolved by relocation of the offending device or controller.

In any proposed system configuration in which the subject of compatibility is an issue, the topics to be considered are:

1. priority and placement conflicts (unbuffered DMA devices placed farther from the processor than fully buffered DMA devices)

2. incompatible device requirements (block mode DMA in combination with older style 4K word memories which require CPU refresh signals)

3. backplanes (some backplanes either do not bus all required signals or use some signal lines instead for the transmission of special signals/voltages for specialized applications)

4. power supplies (current requirements in a given box and the presence or absence of all required voltages)

5. power sequencing (some systems do not have DEC compatible pin-outs in the initializing signals from the power supply)

6. device addressing (must be correctly resolved on even the smallest of systems)

7. device timing (interfaces which are marginal on a Q-BUS system may actually not work in an extended system)

CHAPTER 2

CONFIGURATION

2.1 CONFIGURING THE 1953

The 1953 is shipped by ADAC configured to operate in any STANDARD DEC or ADAC backplane (such as the ADAC 1200, 2200, or 3200 master or slave backplanes).

There are are a few circumstances under which a customer might want to reconfigure the 1953.

1. Expanding with a non-standard or specialized backplane

2. Incorporating an older non-self-refreshing memory

3. Terminating a non-ADAC backplane

First, the extended (22-bit) addressing bits, BDAL(18-21) have sometimes been used for special purposes by some manufacturers of Q-BUS systems. In those cases, remove the four jumpers on the 1953 near the BC1-BF1 fingers. If that 1953 is ever subsequently required for use in a 22-bit addressing system, simply replace the jumpers.

Second, DEC's original 4K word memory board, the MSV-11, did not contain any refresh circuitry, but relied on either the processor or an external DMA controller (BDV-11) to refresh the dynamic memory chips. The refresh transaction used a bus signal called "BREF/L" to accomplish this function simultaneously for all such memories in a given system. That function has been obsoleted by subsequent announcements of first 16K word then 128K and 256K memories at nearly the same price. All of the newer memories have on board refresh circuitry, eliminating the function previously provided by the BREF/L signal.

The next set of Q-BUS offerings will allow a feature called BLOCK MODE DMA which will nearly triple the rate at which data is transferred on the Q-BUS. That new feature redefines the function of the BREF/L signal to function as an enabling signal during the BLOCK MODE DMA read and write function.

The 1953 is configured to allow BLOCK MODE DMA. It must be customer reconfigured to support refresh of obsolete memories. The reconfiguring is accomplished by cutting the etch at E7 to E8 and E9 to E10 and inserting jumpers from E7 to E9 and E8 to E10.

Third, ADAC master backplanes are preterminated with 220 ohm thevenin equivalent terminators to 3.4 volts as defined in the Q-BUS definition. When a processor such as the 11/23 is inserted in the backplane with it's own on-board 220 ohm terminators, the proper 120 ohm lumped termination is created on the backplane. ADAC "slave" backplanes are preterminated with 120 ohms. Most DEC backplanes are unterminated. Other manufacturers provide a variety of configurations, some of which meet and some of which do not meet the Q-BUS specification.

To help a user navigate through this maze, sockets are contained on both the 1953 and the 1903CT to allow a user to install resistor packs (120 ohm or 220 ohm as appropriate to his situation). The cable connection between systems is always terminated at 120 ohms at each end. Since the 1903CT is a passive device, either it or the backplane into which it's inserted must be terminated with 120 ohms.

The following chart is included as an aid in determining the compatibility and configuration issues for specific backplanes.

1953 BACKPLANE CONFIGURATION AND COMPATIBILITY CHART

MASTERS: \ SLAVES:	1200	2200	3200	DEC	1000	2000	OTHER
1200	Q22	Q22	Q22,6	1,5	1,2,5	1,2,5	1,5
2200	Q22	Q22	Q22,6	1,5	1,2,5	1,2,5	1,5
3200	Q22	Q22	Q22,6	1,5	1,2,5	1,2,5	1,5
DEC	4	4	6,4	1,4,5	1,2,4,5	1,2,4,5	1,4,5
1000	3,4	3,4	6,3,4	1,3,4,5	1,2, 3,4,5	1,2, 3,4,5	1,3,4,5
2000	3,4	3,4	6,3,4	1,3,4,5	1,2, 3,4,5	1,2, 3,4,5	1,3,4,5
OTHER	4	4	6,2,4	1,2,4,5	1,4,5	1,4,5	1,4,5

NOTES:

---- Q22 means fully Q-BUS compatible.

1- Use 1903CT's in the slave box.
2- Modify the 1903CT to avoid +/-15vdc conflict.
3- Modify the 1953BR to avoid +/-15vdc conflict.
4- May necessitate master backplane rewiring to accomodate Q-BUS features.
5- May necessitate slave backplane rewiring to accomodate Q-BUS features.
6- Use 3200CT in 3200 slave box.

CHAPTER 3

APPLICATIONS

The 1953 and it's companion ADAC products can be used to configure very high performance Q-BUS based computer systems. This section describes the do's and don'ts of connecting repeaters, peripherals, cpu's, arithmetic processors, communications equipment and the like.

3.1 GENERAL ASPECTS

The most successful applications of the 1953 will always use the "STAR" configuration instead of a series backplane connection. This means that all 1953 cards in a system will be placed in the master chassis. The alternative, the serial topology, involves repeating master signals into a first slave and then repeating the first slaves's signals into a second slave.

With the serial topology, given that there is some differences among the loading of various signals among cards in a backplane, signal skews become aggrevated beyond Q-BUS specifications and, under certain circumstances, unreliable performance results. Therefore, the serial topology is not recommended by ADAC.

Placement of cards is dicussed below but, in general, only the maintainence of daisy-chains indigenous to the Q-BUS restricts card placement in a 1953 based system. Placement is determined by the desired arrangement of interrupt and DMA priority.

Some performance advantage (1% to 5%) can be gained by placing memory, CPU, and some DMA devices all in the master backplane. The performance gain is extremely sensitive to both the application and to the specific devices employed (memory and DMA) and is usually negligible.

3.2 BACKPLANE CONSIDERATIONS

The 1953 supports all features used by Q-BUS peripherals. Success in using those features involves careful selection and integration of not only the cards and the 1953's in the system but also the backplane. Q-BUS processors support a wide variety of applications involving large and small numbers of cards. Addressing modes include 16-bit, 18-bit and 22-bit support. Not all DEC backplanes support all addressing modes and most DEC backplanes provide no bus termination. Some processors do no terminate all required lines used in address decoding by some memories.

The 1953 has features installed to accomodate all of the varieties of systems which can be configured around the Q-BUS. The solutions are pre-engineered in the current line of ADAC products and they are only slightly more difficult to activate using a mix of equipment from various vendors. What is crucial however is that the user be cognizant of all of the details about not only the interface cards but also the backplane(s) he is planning to integrate.

For example, locations are provided at which the BEVENT clock source can be rerouted from master to slave. In a similar way, BSRUN can be redirected or ignored.

3.2.1 ADAC 22-BIT BACKPLANES

ADAC produces a series of high performance, properly terminated, properly cooled, overtemperature protected enclosures for use in Q-BUS applications. They not only support 22-bit but 18-bit and 16-bit applications as well.

The ADAC enclosures are fully engineered to support the full range of Q-BUS high performance features now finding their way into implemented products.

3.2.2 MODEL 1200 SERIES

The Model 1200 series is the most powerful of the three families of ADAC system enclosures. It includes the 1200M master data acquisition system, the 1200S slave system, and the 1200TU master system with a dual drive cartridge tape unit.

Each system consists of a 7" high rack-mountable enclosure, a 22 slot Q bus configured backplane, and a power supply unit. The enclosure design features a front-loading card cage/backplane unit that is accessible after the top cover is removed. The card cage can be tilted upwards and locked at a 45 degree angle to allow easy access to all of the system cards. A high pressure, high velocity fan is mounted to the card cage to allow cooling of

the cards even when the cage is tilted upwards.

Cable egress and clamping is facilitated with a cable clamp assembly mounted on the rear panel. The power supply unit, mounted in the rear of the enclosure, has a second fan mounted to it. The front panel assembly consists of a beige molded plastic piece mounted to a solid steel plate, in order to minimize RFI problems. A vertical row of four back-lighted pushbuttons and indicators provide the CPU and power controls.

The backplane assembly consists of 11 quad wide slots. Slot 1 is on the top. Viewed from the front, the four connectors in each slot are labeled A,B,C,D from left to right. Each pair of connectors, AB and CD, contain all of the Q bus signals. Therefore, any dual height Q bus card can be inserted into any of the 22 dual slots. However, it is recommended that slot 1-AB be reserved for the CPU board since this slot has one extra wire connected to it to allow the CPU to drive the front panel RUN light.

The Model 1200 backplane can also accomodate quad size cards in any of the 11 slots. The card cage contains a plastic center card quide mounted vertically in the center of the cage. The quide provides positive retention for dual size cards. It can be held rigidly to the cage by two screws through the top or (and) bottom plates of the cage. If only dual height boards are used throughout the backplane, the entire guide is used. If a combination of quad and dual height boards are used, the boards should be clustered by size. As an example, all dual boards could be mounted in the top portion of the cage, with quad boards mounted below. The guide is designed to be easily cut for customization. This approach solves the problem of how to mechanically support two different size cards in the same backplane.

In placing cards in the backplane, the systems engineer must keep in mind two factors - maintaining daisy chain continuity, and relative interrupt priority. The daisy chain consists of two Q bus signals that wind their way through the backplane, going in and out of each board in sequence. These signals are labeled BIAK for Bus Interrupt Acknowledge, and BDMG for Bus DMA Grant. These two signals are not continuous on the bus, but enter each card on the input pin and exit on the output pin. In the Model 1200, these two signals originate at the CPU in slot 1-AB. From there, they go to 1-CD, 2-CD, 2-AB, 3-AB, 3-CD, and so forth, throughout the backplane, forming an inverted S pattern. It is the responsibility of the system engineer to ensure the integrity of these daisy chain signals. Dual height cards must be inserted in sequence, keeping the inverted S pattern in mind. If a dual slot is left vacant, the system will not boot or run properly. Quad size cards, of course, complete the chain for both AB and CD positions of a slot.

For LSI-11/2 and SBC-11/21 Falcon CPUs, a single interrupt structure is employed. Priority over other cards is gained by

relative proximity to the CPU in the inverted S pattern. Therefore a card located in slot 1-CD has priority over a card in 2-AB if simultaneous interrupt requests occur. For LSI-11/23 CPUs, a multiple level interrupt structure is employed, levels 4, 5, 6 and 7. Level 7 is the highest priority. All boards with single level priorities are on level 4. There are two schemes for incorporating boards of mixed priorities in the same backplane - position independent and position dependent.

The position independent configuration allows devices that use the 4-level interrupt scheme to be placed in the backplane in any order. These devices must send out interrupt requests and monitor higher level request lines. The level 4 request is always asserted by a requesting device, regardless of priority, to allow compatibility with the LSI-11/2 processor. If two or more devices of the same priority request an interrupt, the device physically closest to the processor (in the S pattern) will win arbitration. Devices that use the single-level interrupt scheme must be placed at the end of the inverted S pattern for arbitration to function properly.

The position-dependent scheme is easier to implement. A constraint is that peripheral devices must be inserted with the highest priority device located closest to the processor in the S pattern, and the remaining devices placed in the backplane in decreasing order of priority, with the lowest priority devices farthest from the processor. With this configuration each device has to assert only its own level and level 4 (for LSI-11/2 compatibility). Monitoring higher level request lines is unnecessary. Arbitration is achieved through the physical positioning of each device on the bus. Single level interrupt devices on level 4 should be positioned last on the bus.

The backplane in the 1200 is structured for full 22 bit addressing, as supported by the LSI-11/23 CPU. This means that up to 4 megabytes of memory can be inserted in the backplane. The 22 bit structure starts in slot 1-AB and is carried throughout the backplane. As such, it is fully compatible with the LSI-11/23 and SBC-11/21 processors. However, caution must be employed when using the DEC LSI-11/2 CPU.

THE LSI-11/2 is an old design that supports a 16 bit addressing structure. As such, it works well in the Model 1200 (as well as DEC and other third party 22 bit backplanes) AS LONG AS ALL OTHER DEVICES PLUGGED INTO THE SAME BACKPLANE ARE STRUCTURED FOR 18 BITS ONLY. Originally, the 4 extra address bits were defined by DEC as User Spares. DEC used these four bit positions on the LSI-11/2 for diagnostic and maintenance purposes. Therefore, the LSI-11/2 will interfere with bus transactions if other devices plugged into the bus have active connection to these 4 pins. It is possible to have DMA devices accessing 22 bits of address even though the CPU has only 16 bits.

ADAC has written an application note (AN-13) describing this problem and offering two solutions. AN-13 is included in the appendix of this manual.

If more cards are needed in the system than can be accomodated in one backplane, the Model 1953 can be used to expand the bus. There are two bus connectors (one 50 pin and one 40 pin) mounted directly on the backplane of each 1200 system. The 1953 is mounted in the master enclosure (as described earlier) and the 1903BC bus cable set is used to connect between the 1953 and the bus connectors on the backplane of the slave unit. No card slot is taken up in the slave in this configuration.

3.2.3 MODEL 2200 SERIES

The Model 2200 series consists of a family of half-rack enclosures that can be used independently as bench-top units or that can be bolted together in pairs for rack-mounting applications. The family includes the 2200M master data acquisition system, the 2200S slave system, the 2200TU dual drive tape cartridge unit, the 2200CR system monitor, and the 2200E empty enclosure. Each unit is 7" high, 8.5" wide, and 22" deep. In the rack-mounted configuration, any two units can be bolted together and be supplied with slides.

The enclosure design features a pop-off front panel that allows front access to the system boards without removing covers. A fan is mounted on the rear panel to allow cooling of the rear-mounted power supply assembly as well as to pull air from the card cage. Air intake is from the bottom of the enclosure.

The system cables are routed from the edge of the boards, through the right side of the assembly, and through a cable clamp assembly mounted on the rear panel. The front panel assembly consists of a beige molded plastic piece mounted to a steel plate to minimize RFI problems. A vertical row of four back-lighted pushbuttons and controls provide the CPU and power controls.

The backplane assembly consists of 13 dual wide slots. Slot 1 is on the right, as viewed from the front. The pair of connectors in each slot contain all of the Q bus signals. Any dual height Q bus board can be inserted into any of the 13 slots. However, it is recommended that slot 1 be reserved for the CPU since it has one extra wire connected to it to allow the CPU to drive the front panel RUN light.

When placing cards in the backplane, the systems engineer must keep in mind the same two factors described in Sec. 3.2.2. The daisy chain continuity must be maintained, and the relative interrupt priority must be considered. In the 2200M and 2200S systems, the daisy chain starts in slot 1 and propogates through the backplane to slot 13. As in the 1200 system, the daisy chain continuity must not be broken for proper system operation. See Sec. 3.2.2 for interrupt priority considerations.

As in the 1200, the 2200 supports fully the 22 bit addressing structure of the LSI-11/23. As such, it has the same constraints when operating with the LSI-11/2 as detailed in the previous section.

Like the 1200, expansion of the 2200 series from master to slave is accomplished in an identical fashion. Two bus connectors are provided on each backplane to allow the 1903BC to connect from the 1953 directly to the backplane of the slave 220.

3.2.4 MODEL 3200 SERIES

The Model 3200 series is the smallest and most economical of the three families of system enclosures. It includes the 3200M master data acquisition system., the 3200S slave system, the 3200TU dual drive tape cartridge system, the 3200CR system monitor, and the 3200E empty enclosure.

Each system is 8" high, 8.5" wide, and 3" deep. In the rack-mounted configuration, two units are fastened together and include mounting rails.

As in the 2200 series, the enclosure features a pop-off front panel of the same design, to allow front access to the system boards as well as the power supply. In the 3200, the cards are mounted horizontally. A fan is mounted on the right side of the system enclosure to push air across the cards. Air exit is through the left side of the enclosure.

The system cables are routed over the top of the card cage and out through a cable clamp assembly mounted on the rear panel. The front panel assembly is identical to that of the 2200 family.

The backplane assembly consists of six horizontal slots containing two connectors per slot. Each slot can house one dual height bus board. Quad boards cannot be accommodated in the 3200. Any Q bus board can be inserted into any of the six slots. However, again, slot 1, the top slot, should be used only for the CPU for proper operation of the RUN light.

One of the key features of the 3200 is the plug-in power supply assembly. Above slot 1 is a seventh connector, of different design, that allows the power supply module to be easily accessible from the front of the system.

When placing cards in the backplane, the same considerations mentioned for the 1200 and 2200 systems must be adhered to.

As in the 1200 and 2200 series, full 22 bit addressing structure is carried throughout the 3200 backplane.

Unlike the 1200 and 2200 series, the 3200 does not contain bus connectors on its backplane. Expansion from a master unit to a slave requires the use of the model 1953 bus repeater mounted in the master, the 3200CT cable terminator mounted on the rear backplane pins of the slave, and the 1903BC bus cables connecting the two. A small flat ribbon cable between 3200PS and 3200CT must also be used to provide automatic power sequencing.

3.2.5 OLDER ADAC BACKPLANES

Older ADAC backplanes (1000 series and 2000 series) are 18 bit systems which used three of the four additional 22 bit address lines for +/-15VDC power distribution. Therefore, the 1953 that is used in these systems must have the four jumpers near BC1-BF1 removed. If an older ADAC backplane is used as a slave, a 1903CT card is required in the first slot to be compatible with the 1903BC cables.

3.2.6 DEC BACKPLANES

The major obstacle to using DEC backplanes in Q-BUS systems is that many of the DEC products do not adhere to the Q-BUS specification.

In the case of the RL support backplanes, a local C-D interconnect in the middle of the backplane is reserved specifically for the 2-board RLV-11 controller set, rendering the backplane incapable of expansion to 22-bit support without very detailed system engineering. Other backplanes provided by DEC have uncommitted slots in which the Q-BUS signals are not bussed.

Also, the DEC backplanes are not terminated but rather derive their terminating impedances from the cards inserted into the backplane. This is especially important since not all signals required among 22-bit peripherals are terminated by all DEC terminators and processors.

In general, however, one can expect to install in an ADAC backplane, nearly any combination of cards which support 22-bit addressing, whether they be from DEC or other vendors, and expect them all to work together with 1953's.

Further, one can reasonably expect to expand a system into a DEC backplane using non-DMA peripherals and expect that system expansion to work well. System engineering issues begin to surface only when 22-bit and non-22-bit components are intermixed in a system. At that point, some care, caution and attention to detail in system engineering is the usual remedy.

3.2.7 THE MINC

Expanding the MINC is a subject in itself. The MINC is a product developed by DEC's laboratory products group to meet what they perceived as unique reqirements in the lab area. As a result of that perception, inter-card spacing, C-D interconnection, and power supplies to the cards are non-standard in the MINC. The 1953 can be engineered into a MINC but the user bears a very large responsibility of system engineering in selecting the appropriate slot and either lowering his expectations from the expansion or being prepared to rewire parts of the backplane to support the new and exciting Q-BUS features which have been excluded from the design of the MINC.

CHAPTER 4

SPECIAL CONSIDERATIONS

4.1 POWER SEQUENCING

Power sequencing in a chassis is normally controlled by the power supply with signals generated to notify the processor of both a successful turn-on and an impending shut-down (someone pulled the plug).

Two signals, BDCOK H and BPOK H are generated by the power supply or power controller and are sensed by the processor (which generates the third signal BINIT L). When multiple chassis's are involved in a system, a means of coordinating backplane activity needs to be employed. This is required due to potential loading differences, timing differences, and energy source differences among the system power supplies in the system. The most obvious timing discrepancy occurs when only one of several chassis's are turned on or off.

The 1953 manages this operation by receiving all such signals from all slave power supplies and logically combining them in the master backplane, from where the three signals are transmitted nearly simultaneously to all slave chassis's. In this way, the LAST bus to be correctly powered-on, controls the rebooting or restoring of the previous state of the system.

The underlying assumption behind this method is that all busses are unreliable until all are correctly powered. Using this organization, a user may power-up his system from either a master switch or by turning-on individual chasses. In either case, the system boots normally and behaves as a complete system as though all cards were in one chassis, powered by one power supply.

4.2 LOCATION OF CPU

The CPU in a 1953-based system is always the first card in the master chassis. There is no practical way around this due to the processor-generated interrupt and DMA grants through the backplane daisy chain.

Also, the processor generates a signal called SRUN which is picked up from the first slot and used to light the "RUN" lamp on the front panel of a master chassis.

In the attached slave chassis's, if a 1903CT is required, it is placed in the first slot and it behaves as a processor. If an ADAC 1200, or 2200 is used as the slave, the no 1903 is required and signals on the backplane connector are routed automatically to the "0th" slot. The card in the first slot behaves, then, as though it is next to the processor.

4.3 LOCATION OF MEMORY

All 22-bit compatible 22-bit memories pass DMA and interrupt grants through jumpers on the card although they do not use or sense those signals themselves. As a result, memory cards may be placed in any position in any chassis in any 1953 based system. They may even be placed at the last slot, with intervening empty slots between memory and the end of the grant daisy chains.

4.4 LOCATION OF DMA DEVICES

DMA devices may be positioned into a 1953 based system with regard only to the buffering and speed capabilities of each device. Keep in mind, however, that each 1953 in the master backplane performs arbitration. This means that the devices in slave chassis number two will incur a lower positional priority than devices in slave chassis number one.

4.5 LOCATION OF INTERRUPTING DEVICES

The comments on DMA devices apply here as well. However, the Q-BUS and the 1953 support multiple level priority interrupts so in the slave chasis number one/two situation, contention arises only among devices interrupting on the same priority level.

The user should be aware that single level interrupt cards (priority 4) can act like higher priority cards located further away from the CPU because they will "grab" an interrupt acknowledge caused by a card set at a higher priority, located further away from the CPU.

4.6 OTHER BACKPLANES

In general, any backplane which is truly Q-BUS compatible is a candidate for inclusion in a 1953 connected system. However, it is the customer's responsibility to assure that compatibility and to resolve the terminating issues that arise in specially engineered large systems.

CHAPTER 5

THEORY OF OPERATION

This section of the manual deals with the details of operation of the bus repeater. Here we shall treat both the electrical and functional requirements of the DIGITAL EQUIPMENT CORPORATION Q-BUS as implemented both in DEC and ADAC products.

The Q-BUS is a high-speed, high quality computer bus whose design evolved out of the several generations of computer development at DEC. It uniquely combines precisely controlled and defined electrical characteristics with a reliable, versatile and proven architecture. The versatility of the Q-BUS and its supporting instruction set processors, allow a system implementor to make a balanced compromise between performance and cost in his application.

The ADAC 1953 subsystem was designed to preserve that philosophy and to allow a system designer to make his own trade-offs in selecting and intermixing processors and peripherals without precluding growth upward in performance or growth upward in cost effectiveness. The 1953 supports all the features and functions required for the processors and controllers available today and supports features not yet implemented in processors available from DEC for the Q-BUS.

5.1 GENERAL

The 1953 because of it's on-board arbitration of both DMA grants and interrupt acknowledge signals, provides some new and sophisticated opportunities for arranging priorities among peripherals in a system. Unlike other repeaters, the 1953's are never series connected. Instead, intelligent on-board arbitration is designed into the unit. Multiple 1953's are all placed in the master chassis in any positional relation to the other peripheral devices in the master chassis.

Systems designed with the 1953 will nearly always use a CPU, memory, some interrupting devices (such as terminal interfaces), some DMA devices (such as disks), and some program I/O devices (such as hardware non-interlocked discrete digital I/O). All 1953 cards in a system are placed in the master backplane. Each expansion chassis is connected to the master through it's respective 1953. In this way, up to 21 backplanes of up to 22 Q-BUS cards each may be interconnected (although 462 peripherals on a single CPU would represent an unusual software load).

The delays seen by each of the "slave" backplanes for nearly all signals amounts to only the propogation delays of two bus transceivers plus the electrical propogation delay of signal down a terminated transmission line. The total combined transceiver delay is on the order of 40 nano-seconds and the cable delay, at 1.7 nano-seconds per foot times say ten feet, is an additional 17 nano-seconds for 57 total.

Q-bus transactions are normally on the order of 1200 nano-seconds. The interposing of a 1953 extends that to about 1440 nano-seconds for normal reads or writes across one repeater. Block mode transactions take place in about 550-700 nano-seconds with appropriate peripherals and memory. Propogation delays through the 1953 are felt by the processor only in four cases and affect the transaction by extending the following intervals.

Those intervals are:-

1. master asserts BDIN/BDOUT and the slave receives that signal

2. slave asserts BREPLY and the master receives that signal

3. master negates BDIN/BDOUT and the slave receives that signal

4. slave negates BREPLY and the master receives that signal

All other timing signals remain virtually unchanged. The net result is that each of the slave backplanes run at bus bandwidths which are very close to the Q-bus maximums.

Maximum cable lengths using the 1953 card and cable set are designed to be a maximum of 40 feet. This limit is imposed by both D.C. resistance of the cable and by signal skew considerations. Of course, the best performing overall system design will use the shortest cable lengths consistent with good packaging and service access.

The 1953 card thus arranged into a system will all support:

1. normal memory reads and writes
2. multi-level priority bus interrupts
3. dma transactions amongst competing devices in any of the attached backplanes
4. memory parity coordinated among cpu memory and DMA devices
5. burst mode DMA transactions
6. correct power sequencing among all chasses
7. Q-BUS parity (as yet not provided by DEC devices)
8. BLOCK MODE DMA (as yet not provided by DEC devices)
9. remote refresh of older style memories (but not in the same system as contains block mode dma devices)

Thus it is that with the 1953, a system implementer has virtually unlimited capability to configure devices into a series of low cost or high performance chasses and cabinets, using any of the available or yet to be announced Q-BUS instruction set processors.

5.2 MEMORY AND DEVICE TRANSFERS

"Normal" data transfer operations along the Q-BUS (byte and word moves) can take on any of several forms, but the basic transaction remains the same. In that context, we need to discuss several kinds of data transfer operations and to examine the similarities and differences.

Those transfer operations involve:

1. CPU to memory
2. CPU to device register
3. memory to CPU
4. device register to CPU
5. device to memory
6. memory to device

All of the above data transfer operations are treated identically in the PDP-11 family of computers. The computers use memory

mapped I/O in which all device registers accessed by the CPU appear as memory location. In addition, the DMA devices in the system perform I/O to memory using the same bus and the same control signals as does the processor so READS or WRITES in any direction among any points in the system are handled identically, no matter what the data source and sink.

Given the flexibility of transfers in Q-BUS PDP-11's, the next subject of discussion is the actual protocols involved. For data transfer, bytes or words may be passed on the bus and the transfer cycle can be either READ, WRITE, or READ-MODIFY-WRITE.

All transactions begin with an addressing phase followed by a data phase. During the addressing phase, the bus starts off idle with all data lines released (or deasserted) and all data control lines deasserted. The current bus master then places the address on the bus and if the "slave" device in the operation is an I/O device, BBS7 L is asserted (to select the region of I/O addresses) since it is considered part of the address. Also, if a write operation follows, then BWTBT L is asserted as part of the address. After a stabilization time which allows the address to settle on the bus, BSYNC L is asserted. After an address holding time, the address is removed from the bus and the data phase of the operation begins.

During the data phase, if a BYTE operation is to be performed, then BWTBT L is again asserted to allow byte strobing to take place internal to whatever cards are involved. BDIN L or BDOUT L is asserted by the master to cause a READ or WRITE operation respectively into or out of the master. The slave device detects the command and when it is able to either accept data into itself or when it has placed onto the data lines, the requested data from itself, the slave device asserts BRPLY L. The master then negates BDIN L or BDOUT L and the slave (detecting that) negates BRPLY L. The master then negates BSYNC L idling the bus and preparing for the ensuing address phase.

READ-MODIFY-WRITE operations are a simple extension of this protocol. They begin with an addressing phase and perform a read, then a short delay (during the modify) and after the slave negates BRPLY L, the master places data on the bus and asserts BDOUT L. The slave senses that BSYNC L has not been negated and is therefore still selected. The slave then accepts the modified data and asserts BRPLY L a second time and then transactions continues on as a READ.

The role that the 1953 plays in data transfer operations is to sense the impending direction of data flow and to switch its bus transceiver pairs before the data flow actually takes place. In this way, delays through the 1953 are brought to an absolute minimum. In other words, the 1953 monitors the control signals which it is also transmitting and anticipates the nature of the transaction ABOUT to happen and then conditions itself to accommodate the transaction with virtually no lost time.

5.3 INTERRUPT TRANSACTIONS

Interrupt transactions on the Q-BUS allow a device to alter program flow by directing the processor to "immediately" execute an "interrupt service routine" specific to the device which is requesting the service. This is a function which is common to most computers and to many micro-processors.

On the Q-BUS, the function is implemented with hardware on the processor and on each of the cards which can request service. The hardware in each location, coordinates interrupt activity through a protocol or dialogue using predefined signals on the Q-BUS. The signals involved are:

1. INDEX BIRQ4 L BIRQ4 L (bus interrupt request on level 4)
2. BIRQ5 L (bus interrupt request on level 5)
3. BIRQ6 L (bus interrupt request on level 6)
4. BIRQ7 L (bus interrupt request on level 7)
5. BSYNC L (bus sync, deasserted for vector transactions)
6. BDIN L (asserted during 'rupt transactions to synchronize arbiters)
7. BIAKO L (output side of daisy chain "acknowledge out"; asserted by each card which determines that the acknowledge is at a higher priority than this card is requesting)
8. BIAKI L (input side of daisy chain "acknowldge in")
9. BRPLY L (bus reply; asserted by the device which places the vector on the Q-BUS)

The interrupt transaction begins when a device which is enabled for interrupts, achieves a ready or done status and requests service by asserting a request (BIRQ<4-7> L). When the processor is running at a priority level lower than the requested interrupt, it pauses between bus cycles and while BSYNC L is deasserted, it asserts BDIN L to cause all devices to stabilize their arbitration circuits. The processor next asserts BIAKO L to start the acknowledge signal through the daisy chain.

Each interrupting device on the bus had been monitoring the current request level and froze it's decision at DIN time. If a given device was requesting an interrupt and if it's priority was equal to or greater than the current request level, then if it receives an assertion of BIAKI L, instead of passing the grant, it places its vector on the Q-BUS and asserts BRPLY L. The processor responds by storing the vector and deasserting BDIN L and BIAKO L. The device next responds by removing the vector

from the bus and deasserting BRPLY L. The processor then detects the deassertion of BRPLY L and proceeds to store the old state of the computer an enters the interrupt service routine defined by the device vector.

Each 1953 in the master bus performs such interrupt arbitrations with one difference. The 1953 detects the highest priority requested on the slave bus and if that meets or exceeds the priority on the master bus, then the 1953 passes the acknowledge to the slave bus, expecting a device there to complete the transaction. Otherwise, the 1953 passes the acknowledge along the master bus, expecting that a higher priority device on either the master or on another 1953 slave is requesting service.

The interrupt acknowledge arbitration chart below describes the request states which can occur on the buses and the action taken by the 1953 as a result.

1953 INTERRUPT ARBITRATION BIAK(I/O) CHART

MSTR-LEVEL	MASTER BUS PRIORITY LEVEL IRQ 4	5	6	7	SLAVE LEVEL	SLAVE BUS PRIORITY LEVEL IRQ 4	5	6	7	IAK TO MASTER	IAK TO SLAVE
0	-	-	-		-	-	-	-	-	Y	-
	Y	-	-	-	4	Y	-	-	-	-	Y
	Y	Y	-	-	5	Y	Y	-	-	-	Y
	Y	-	Y	-	6	Y	-	Y	-	-	Y
	Y	-	Y	Y	7	Y	-	Y	Y	-	Y
4	Y	-	-		-	-	-	-	-	Y	-
	Y	-	-	-	4	Y	-	-	-	-	Y
	Y	Y	-	-	5	Y	Y	-	-	-	Y
	Y	-	Y	-	6	Y	-	Y	-	-	Y
	Y	-	Y	Y	7	Y	-	Y	Y	-	Y
5	Y	Y	-		-	-	-	-	-	Y	-
	Y	Y	-	-	4	Y	-	-	-	Y	-
	Y	Y	-	-	5	Y	Y	-	-	-	Y
	Y	Y	Y	-	6	Y	-	Y	-	-	Y
	Y	Y	Y	Y	7	Y	-	Y	Y	-	Y
6	Y	-	Y		-	-	-	-	-	Y	-
	Y	-	Y	-	4	Y	-	-	-	Y	-
	Y	Y	Y	-	5	Y	Y	-	-	Y	-
	Y	-	Y	-	6	Y	-	Y	-	-	Y
	Y	-	Y	Y	7	Y	-	Y	Y	-	Y
7	Y	-	Y		-	-	-	-	-	Y	-
	Y	-	Y	Y	4	Y	-	-	-	Y	-
	Y	Y	Y	Y	5	Y	Y	-	-	Y	-
	Y	-	Y	Y	6	Y	-	Y	-	Y	-
	Y	-	Y	Y	7	Y	-	Y	Y	-	Y

The interrupt arbitration capability of the 1953 enables a system designer to take advantage of the resulting priority "compartments" by positioning 1953's into the master backplane in a special order. As an example, if several priority 6 devices are all placed into the same slave backplane, all of these devices can enjoy a position in the daisy chain either before or after some or all other devices of similar priority. Simply by changing the position of the connecting 1953 in the master backplane, a user can tailor the balance of interrupt performance among the devices in his system. The same kind of positional priority can be used in configuring the system's DMA devices.

5.4 DMA TRANSACTIONS

DMA operations in the Q-BUS consist of two parts, arbitration and transfer. The transfer part is exactly as described in a previous section on data transfers and will not be repeated here. This section will therefore concern itself with how a device becomes bus master to enable it to perform transfers.

The abribration phase is conducted using four signals for control and completes by monitoring two more signals (6 total are involved). The signals are:

1. BDMR L (bus direct memory request, to gain the processor's attention)

2. BDMGO L (bus direct memory grant out, from the processor to a requesting device)

3. BDMGI L (bus direct memory grant in, the input line sensed by DMA devices)

4. BSACK L (bus sychronous acknowledge, the master device's signal that it has accepted a grant and that arbitration should cease)

5. BSYNC L (bus sync)

6. BRPLY L (bus reply)

When a device becomes ready to transfer data under its own control (generating addresses and sending or receiving words or bytes), it first asserts BDMR L. As the current bus master (usually the proccessor) completes its last transaction, the arbitration logic responds in a way that if BSACK L is not asserted, then BDMGO L is asserted from the processor. That signal is daisy chained through DMA devices and jumpered through non-DMA units. Eventually it arrives at a requesting device which does not pass it along but instead waits for the negation of BRPLY L and BSYNC L.

When the bus has gone idle and a grant has been presented to the requester, then that device asserts BSACK L, indicating that it is the new bus master. It then proceeds with its data transfer operations and negates BDMR L. During its last data transfer as master, the DMA releases BSACK L to allow arbitration to proceed for any other requesting DMA devices.

The 1953 contains arbitration logic to send BDMGO to the attached slave backplane whenever the 1953 senses a DMA request from the slave and a grant reaches it along the master bus. Again, the 1953 contains logic which anticipates the next direction of control and has the bus turned-around in advance of the required change of direction.

5.5 MEMORY PARITY

Memory parity generation and checking involve the use of BDAL16 and BDAL17 during the data phase of transfer operations. The detailed operation will not be described here. The 1953 provides the capability for completing this transaction between busses by altering the direction of flow on these lines as appropriate during the data phase of memory transfer.

5.6 Q-BUS PARITY

Although not yet implemented in commercially available products, bus parity is defined in the Q-BUS specification and is provided for in the 1953 design. The feature, as relates to the 1953, simply required that the data source be allowed to transmit parity data to the sink on BDAL<18-21> during the data phase of any transaction.

5.7 BURST MODE DMA

Burst mode DMA transactions are nearly identical to simple DMA transfers except that the master device retains control longer and executes more than one transfer without arbitrating for mastership. Although the master device must honor a 10 uSEC limit on it's period of control, the 1953 sees this transaction without any unusual perturbations.

5.8 BLOCK MODE DMA

Block mode DMA transactions are a recently defined capability on the Q-BUS. In block mode DMA operations, arbitration and initial addressing take place as in normal DMA transactions. However, during each data-in or data-out step, the master asserts BBS7 L to indicate to the memory that more data will follow and if the slave is able to accomodate such extended transfer, it asserts BREF L during BRPLY L.

The consequence is that for as long as both devices coordinate the transfers, no further address information need be transmitted. Instead, the slave accepts responsibility for maintaining it's address information. In the case of memories as slaves, they must internally increment their address. In the case of disks or other master devices which will conduct later transfers starting at an updated memory address, they must also maintain updated address information through block mode DMA transfers.

Of course, the benefit of using block mode DMA transfer among memory, cache, and peripherals is that transfers take place at an average rate which can exceed three times the normal Q-BUS bandwidth. The 1953 supports this mode of transfer. As a result, a 1953 expanded system can actually exceed in throughput, the results obtained with Q-BUS systems not expanded but not supporting block mode transfers.

5.9 POWER SEQUENCING

Power sequencing using the 1953 can be accomplished in a few ways. The manner recommended by ADAC is designed into the 1953, 1903CT and 1903BC but can be circumvented easily to meet other requirements such as testing.

Q-BUS PDP-11 processors such as the 11/23, 11/2, SBC11/21 Falcon all sense the signals BDCOK H and BPOK H to restore a system to a working state upon power turn-on. These signals are also used to alert the processor to save the system state upon power fail detection.

Using ADAC enclosures, or DEC enclosures and the 1953 components, these signals (generated by the power supplies in all chasses) are all transmitted to the master backplane where they are "wire-or'ed". The method used operates such that any chassis may be powered-up in any order with respect to the others. The last one turned-on will assert DCOK and POK and will control the reboot or restoration of the entire system. This arrangement works using individual power switches and it also works using a common or "master" power-on switch. Jumpers and cables described in the application section of this manual can be arranged to defeat orderly system power-on.

The foregoing theory of operation is intended as a primary reference for a system engineer applying the 1953 into a complex system.

APPENDIX
Q-BUS SIGNAL
PIN-LIST

CARD-EDGE SEQUENTIAL LIST:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
---	AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
---	AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
---	AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
---	AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in some
---	AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
J1 - 17	AN1	BDMR L	DMA REQUEST
J1 - 15	AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 11	AR1	BREF L	REFRESH ADDRESS MODE / SLAVE ASSERTS DATBIO CONTINUE
---	AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP
---	AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AU1	PSPARE1	SPARE - NOT ASSIGNED
---	AV1	+5B	+5 Vdc BATTERY BACK-UP
J2 - 39	BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave signal)
J1 - 01	BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J2 - 37	BB1	BPOK H	AC POWER OK (master drives slave signal)
J2 - 01	BB1	BPOK H	SPOK (slave pwr supply drives master signal) <J3-01 on 1903CT>
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
---	BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
---	BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in some
---	BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
---	BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
---	BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BU1	PSPARE2	SPARE - NOT ASSIGNED
---	BV1	+5	LOGIC VOLTAGE SUPPLY

CARD-EDGE SEQUENTIAL LIST (continued)

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
---	AA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	AB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AD2	+12VDC	LOGIC VOLTAGE SUPPLY
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
J1 - 07	AT2	BINIT L	INITIALIZE HARDWARE DEVICES
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
---	BA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	BB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BD2	+12	LOGIC VOLTAGE SUPPLY
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15

FUNCTIONALLY GROUPED SIGNAL LIST:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
INTERRUPT HANDLING SIGNALS:			
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
DMA TRANSACTION SIGNALS:			
J1 - 17	AN1	BDMR L	DMA REQUEST
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
TRANSFER CONTROL SIGNALS:			
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
DATA AND ADDRESS LINES:			
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER

FUNCTIONALLY GROUPED SIGNAL LIST:

BUS PIN	MNEMONIC	DESCRIPTION
SYSTEM CONTROL SIGNALS:		
J1 - 15 AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 11 AR1	BREF L	REFRESH ADDR MODE / SLAVE ASSERTS DATBIO CONTINUE
J2 - 39 BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave bus signal)
J1 - 01 BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J2 - 37 BB1	BPOK H	AC POWER OK (master drives slave bus signal)
J2 - 01 BB1	BPOK H	SPOK (slave pwr supply drives master signal) <J3-01 on 1903CT>
J1 - 07 AT2	BINIT L	INITIALIZE HARDWARE DEVICES
SPARE AND RESERVED LINES:		
--- AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
--- AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
--- AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
J2 - 47 BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45 BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43 BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41 BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
--- BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
--- AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in some
--- AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
--- BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in some
--- BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
--- AU1	PSPARE1	SPARE - NOT ASSIGNED
--- BU1	PSPARE2	SPARE - NOT ASSIGNED
--- BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
POWER LINES:		
--- AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BV1	+5	LOGIC VOLTAGE SUPPLY
--- AA2	+5VDC	LOGIC VOLTAGE SUPPLY
--- BA2	+5VDC	LOGIC VOLTAGE SUPPLY
--- AD2	+12VDC	LOGIC VOLTAGE SUPPLY
--- BD2	+12	LOGIC VOLTAGE SUPPLY
--- AB2	-12VDC	LOGIC VOLTAGE SUPPLY
--- BB2	-12VDC	LOGIC VOLTAGE SUPPLY
--- AV1	+5B	+5 Vdc BATTERY BACK-UP
--- AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP

SIGNALS FROM THE Q-BUS FOUND ON I/O CONNECTOR J1:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J1 - 01	BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 07	AT2	BINIT L	INITIALIZE HARDWARE DEVICES
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
J1 - 11	AR1	BREF L	REFRESH ADDRESS MODE / SLAVE ASSERTS DATBIO CONTINUE
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER
J1 - 15	AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 17	AN1	BDMR L	DMA REQUEST
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5

SIGNALS ON THE 1953 I/O CONNECTOR J2:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J2 - 01	BB1	BPOK H	SPOK (slave pwr supply drives master signal)
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 37	BB1	BPOK H	AC POWER OK (master drives slave signal)
J2 - 39	BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave signal)
J2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4" <J3-01 on 1903CT>

SIGNALS FROM THE Q-BUS NOT FOUND ON 1953 I/O CONNECTORS:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
---	AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
---	AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
---	AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
---	AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in some
---	AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP
---	AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AU1	PSPARE1	SPARE - NOT ASSIGNED
---	AV1	+5B	+5 Vdc BATTERY BACK-UP
---	BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
---	BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in some
---	BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
---	BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BU1	PSPARE2	SPARE - NOT ASSIGNED
---	BV1	+5	LOGIC VOLTAGE SUPPLY
---	AA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	AB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AD2	+12VDC	LOGIC VOLTAGE SUPPLY
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
---	BA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	BB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BD2	+12	LOGIC VOLTAGE SUPPLY

APPLICATION NOTE

AN-13

22 BIT ADDRESSING CONSIDERATIONS

Consistent with Digital Equipment Corporation's announcement of the use of 22 bit addressing, the Model 1200 was announced as a system that contains the full 22 bit addressing scheme. The Model 1200 contains 22 Q-BUS positions arranged in a configuration that allows two dual height boards to be plugged in side by side. The relative positions in the backplane are identified as the AB and CD sides. In the Model 1200 all 22 slots are connected for the full 22 bit addressing. This is fully consistent with the use of the LSI-11/23.

A problem arises if a user is planning to employ an LSI-11/2 processor intermixed with other cards that are structured for 22 bit addressing. Digital Equipment Corporation had used the lines now configured for the four extra address bits for internal maintenance functions on the LSI-11/2. Therefore, it is mandatory that the extension address bits be disconnected on the individual controller cards. This is generally done with the use of jumpers on boards such as the controller card for the Model 830 floppy disk.

In instances where it is desirable to use the LSI-11/2 with 22 bit controllers, a solution has been implemented. ADAC has assigned Mod 204 to handle this rather unique combination. The essence of the Mod is to disconnect both the AB and the CD connections in slot 1 from the rest of the backplane. This is accomplished with seven etch cuts and three jumpers on the backplane. In the Mod 204 configuration position AB of slot 1 is reserved for the LSI-11/2 processor. The CD position of slot 1 can be used by any board that has a maximum of 18 bit addressing. All other 20 slots can be used by either 18 or 22 bit devices.

MOD 204

Cut etch between the following pins:	Add wire wrap jumpers between:
1B-C1 to 2B-C1	2B-C1 to 2D-C1
1B-D1 to 2B-D1	2B-D1 to 2D-D1
1B-E1 to 2B-E1	2B-E1 to 2D-E1
1B-F1 to 2B-F1	
1D-C1 to 2D-C1	
1D-D1 to 2D-D1	
1D-E1 to 2D-E1	

WARRANTY

ADAC Corporation warrants all data acquisition systems it manufactures to be free from defects in material and factory workmanship, and agrees to repair or replace any system that, under normal use, reveals such a defect within 90 days after shipment to customer.

This warranty shall not apply to any system that has been:

1. repaired, worked on, or altered by persons unauthorized by ADAC, in such a manner as to injure, in ADAC's sole judgment, the performance, stability, or reliability of the system.

2. subject to misuse, negligence, or accident; or

3. connected, installed, adjusted, or used otherwise than in accordance with the instructions furnished by ADAC.

This warranty is in lieu of any other warranty, expressed or implied, including the warranty of merchantability and fitness for particular purposes, and is applicable to any system bearing the "ADAC data conversion systems Warranty", and so designated in the literature pertaining to that system.

ADAC reserves the right to make any changes in the design or construction of its systems at any time, without incurring any obligation to make any change whatever in units previously delivered.

ADAC's sole liabilities, and the buyer's sole remedies, under this agreement shall be limited to a refund of the purchase price, or, at ADAC's sole discretion, to the repair or replacement of any system that proves, upon ADAC's examination, to be defective when returned to the ADAC factory, transportation prepaid by the buyer, within 90 days from the date of original shipment.

ADAC shall in no way be liable for damages consequential or incidental to defects in any system, for failure of delivery in whole or in part, for injuries resulting from its use, or for any other cause.

The warranty and the writing attached constitute the full understanding of the manufacturer and buyer, and no terms, conditions, understanding, or agreement purporting to modify or vary the terms hereof shall be binding unless hereafter made in writing and signed by an authorized officer of the ADAC Corporation.

REV	ECO	DESCRIPTION	DWN	APP'D	DATE
ØH	776	CHANGED JUMPER CONFIGURATION AT BC1-BF1 (NOTE 5)	NJL	RAP	7/31/84
ØJ	930	DELETED TEXT ZONE I6 AND AT H7.	EMM	RAP	8/3/84
ØE	752	ADDITION FOR SYSTEM 1000 COMPATIBILITY SEE NOTE 5	WDC	RAP	9-9-83
ØF	766	SYST. 1000 CAPABILITY WAS AN OPTION DELETE NOTE 5. SEE ZONE E10	WDC	RAP	11/15/83

REV	ECO	REVISIONS DESCRIPTION	DWN	APP'D	DATE
ØA		REVISED	WDC		
ØB	0691	REVISED	WDC	RAP	3-5-84
ØD	0710	ADDED E11-E14	EMM	RAP	30 JAN 84

D 5-10675 ØJ

SEE ZONE H13

SLAVEMASTER/L

SLAVMASTER/H

SLAVEMASTER/L

SEE NOTE 5.

BT OR CT

BT1	BT	CT
RP9	RP1	RP2
	RP3	RP4
	RP5	RP6
	RP8	RP7

NOTES:
1. ALL FINGERS ON BUS CONNECTOR ARE REQUIRED. IF NOT CONNECTED USE FEEDTHROUGH HOLE TO TERMINATE ETCH.
2. E1-E14 ARE TERMINATED WITH FEEDTHROUGHS.
3. C1-C5, C7-C11, C14-C17, 19, 21, C23-C26, C28-C31, C33-C36, C38-C40, C42-C49, 46, 48, 50.
4. Z24, NOT USED
5. JUMPERS AT BC1, BD1, BE1, AND BF1 (E11-E14) ARE NOT INSTALLED FOR THE 1950 CONFIGURATION.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN D. DiRocco	DATE 3 JUN 82	adac corporation
APPLICATION		MATERIAL	CHECKED K.D.	11 FEB 83	1953/1950 BUS REPEATER SCHEMATIC
		FINISH	ENGINEER V.P.	11 Feb 83	
		APPLICABLE SPECIFICATIONS	APPROVED	RELEASED	CODE IDENT NO D 5-10675 REV ØJ
				WEIGHT	SCALE ACCOUNT NO SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
ØB	859	CHANGED JUMPER CONFIGURATION AT BC1, BD1, BE1, BF1. ADDED NOTE 1.	MJL	RHP	4/25/84

D 10679 ØB

SOCKET Z1 SOCKET Z2 Z3 SOCKET J1

+5V

C4 .01μF 50V C1 10μF 10V C2 10μF 10V C3 15μF 10V C6 .01μF 50V C5 .01μF 50V

R1 180 R3 390 R2 180 R4 390 R5 180 R6 390 R7 180 R8 390 R9 390

BDAL07L BL2
BDAL08L BM2
BDAL09L BN2
BSACKL BN1
BDAL10L BP2
BIRQ7L BP1
BDAL11L BR2
BDAL14L BU2
BDAL15L BV2
BDCOKH BA1
BEVNTL BB1
BDAL12L BD2
BDAL13L BT2
BIAKIL AM2
BIAKOL AN2
BDAL06L BK2
BDAL05L BJ2
BDAL04L BH2
BDAL03L BF2
BDAL02L BE2
BPOKH BB1

GND BJ1
GND BM1
GND BT1
GND BC2

AS2 BDMGOL
AP1 BHALT L
AP2 BBS7 L/ BCONTINUE/L
AR1 BREF L/ BKILL
AR2 BDMGIL
AT2 BINITL
AU2 BDAL00L
AV2 BDAL01L
AN1 BDMRL
AL2 BIR4L
AK2 BWTBTL
AJ2 BBYTCL
AM2 BDINL
AP2 BRPLY L
AE2 BDOUT L
AD1 BDALITL
AC1 BDAL18L
AB1 BIRQ6L
AA1 BIRQ5L

+5V E10 E10
AA2 +5V DC
BV1 +5V DC
BA2 +5V DC
BC1 BDAL18L
BD1 BDAL19L
BE1 BDAL20L
BF1 BDAL21L
SEE NOTE 1.
AJ1 GND
AM1 GND
AT1 GND
AC2 GND

E11 E13 E12 E14 E15

J2 J3 2 9 1 10 SENITL SHALTL SPOKH SDCOKH

E1 AE1 SSPARE 1 (+5VBB)
E2 AF1 SSPARE 2 (SRUN)
E3 AH1 SSPARE 3
E4 AU1 PSPARE 1
E5 AV1 +5V B BATT BACK-UP

E6 AK1 MSPARE 1
E7 AL1 MSPARE 2
E8 BH1 SSPARE 2
E9 BU1 PSPARE 2

E16 BK1 MSPARE 3
E17 BL1 MSPARE 3

E18 AS1 +5V B / +12V B BATTERY BACK-UP
E19 AR1 -12V DC
E20 AP1 +12V DC
E21 BC1 -12V DC
E22 BD1 +12V DC
E23 BE1 +12V B

NOTES:
1. JUMPERS INSTALLED AT BC1, BD1, BE1, AND BF1 FOR 1903CT-Q-1, AND -Y ONLY.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±	DRAWN RSP	DATE 2/13/83	adac corporation
APPLICATION		MATERIAL	CHECKED MARION	10/28/83	SCHEMATIC BUS CABLE CARD MODEL 1903 CT
		FINISH	DESIGNED		
		APPLICABLE SPECIFICATIONS	ENGINEER RHP	4/9/84	
			RELEASED		
			WEIGHT		
			CODE IDENT NO	SIZE D	5-10679 ØB
			SCALE	ACCOUNT NO.	SHEET 1 OF 1