Multiparameter ID Module
TMR
Revisions & Operation

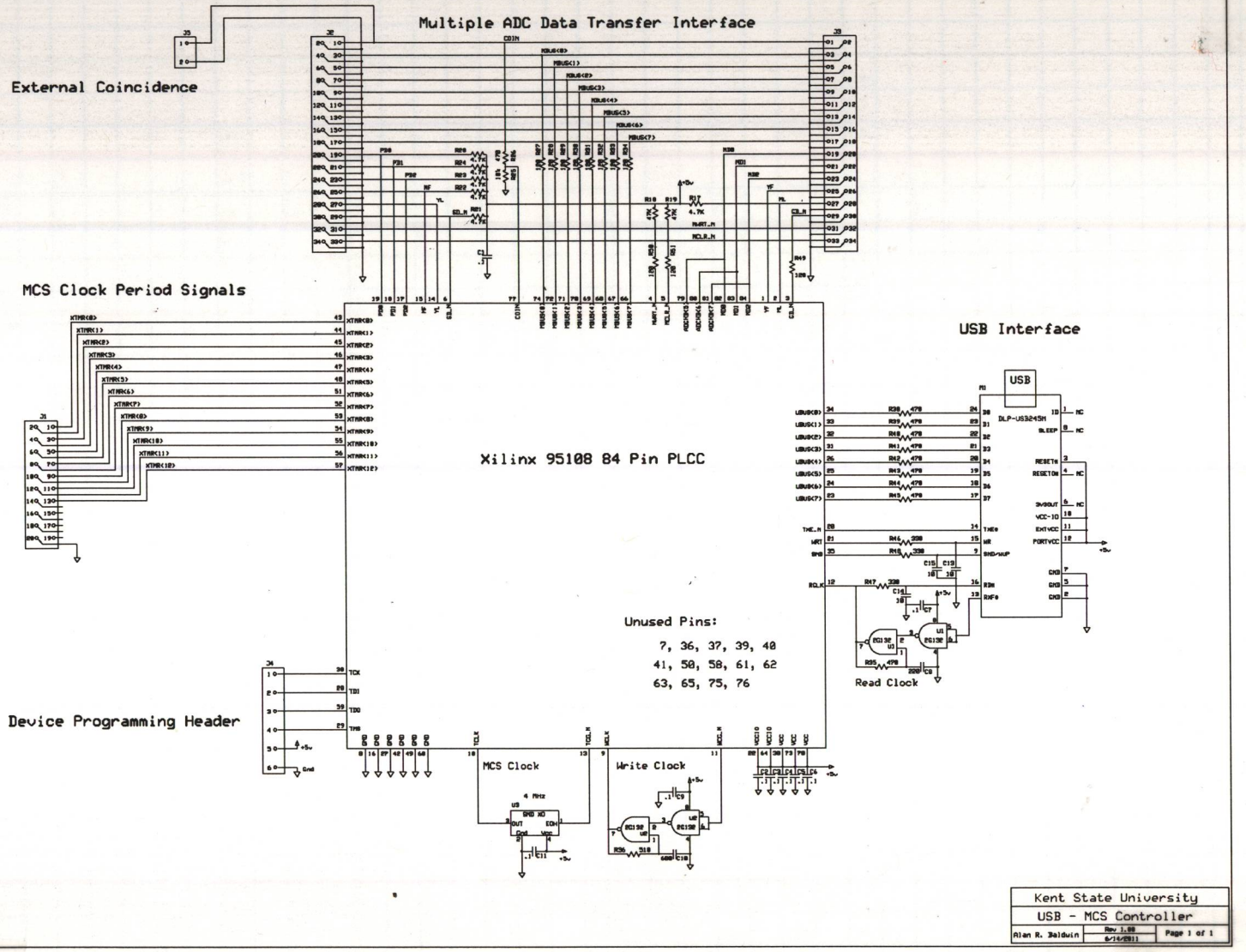
After extensive timing testing it was determined that the 10 MHz readout clock was too fast for reliable readout timing. Component C10 (270pf for a 10 MHz clock) has been changed to 680 pf (a 4 MHz clock).

The timer clock chain has been completely redesigned to be completely synchronous, the timers' 13 bit register bank hold logic is changed to prevent updating during the ID cycle, and changes were made to the Readout and BUS control modules.

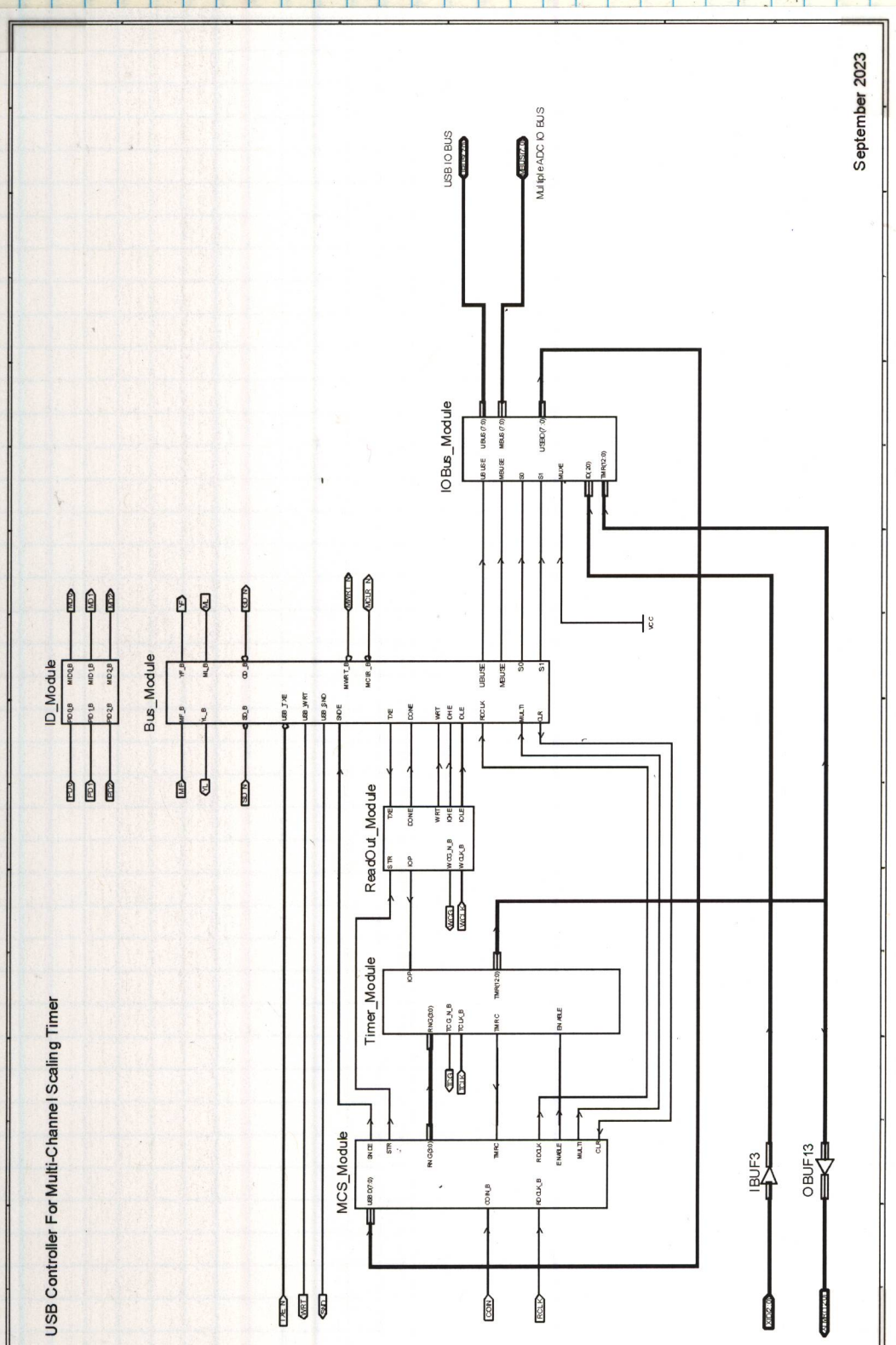
A complete set of schematics is included due to the large number of changes. Additionally descriptions of the Readout and BUS modules have been added.

20 Oct 2023
ABS

PC Board Schematic

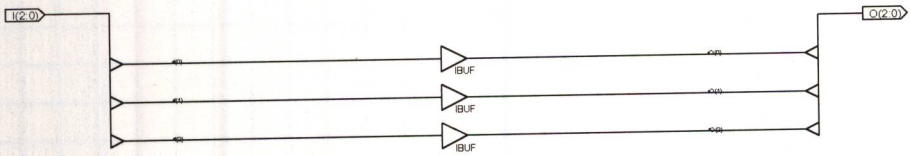


95108 CPLD Block Diagram



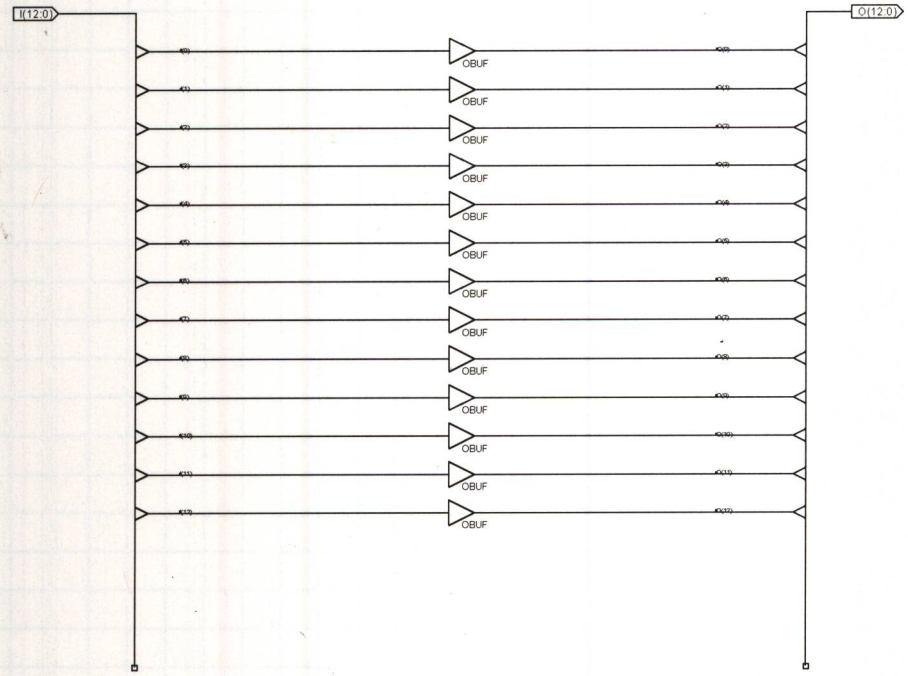
20 Oct 2023
ABB

IBUF3



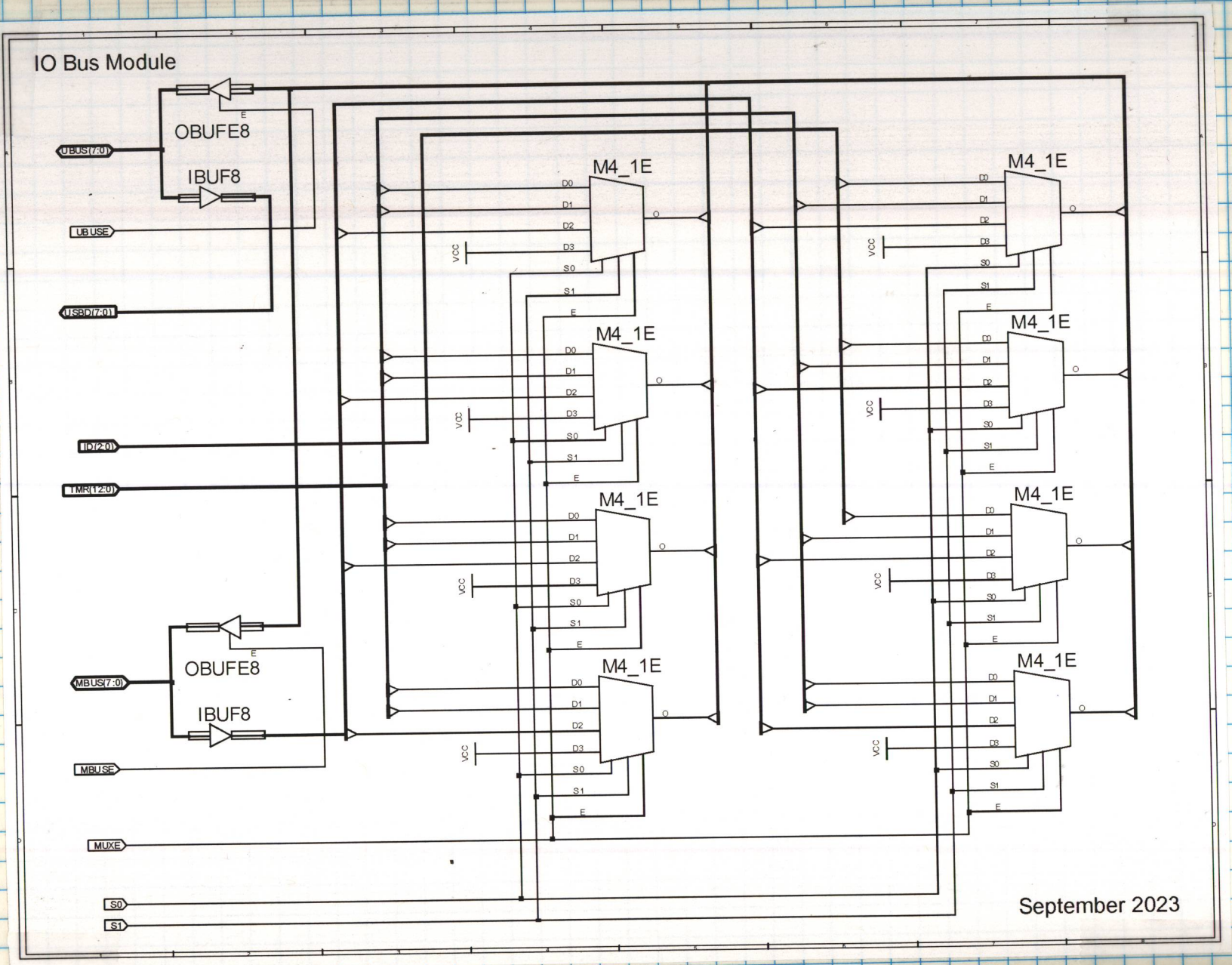
October 2011

OBUF13

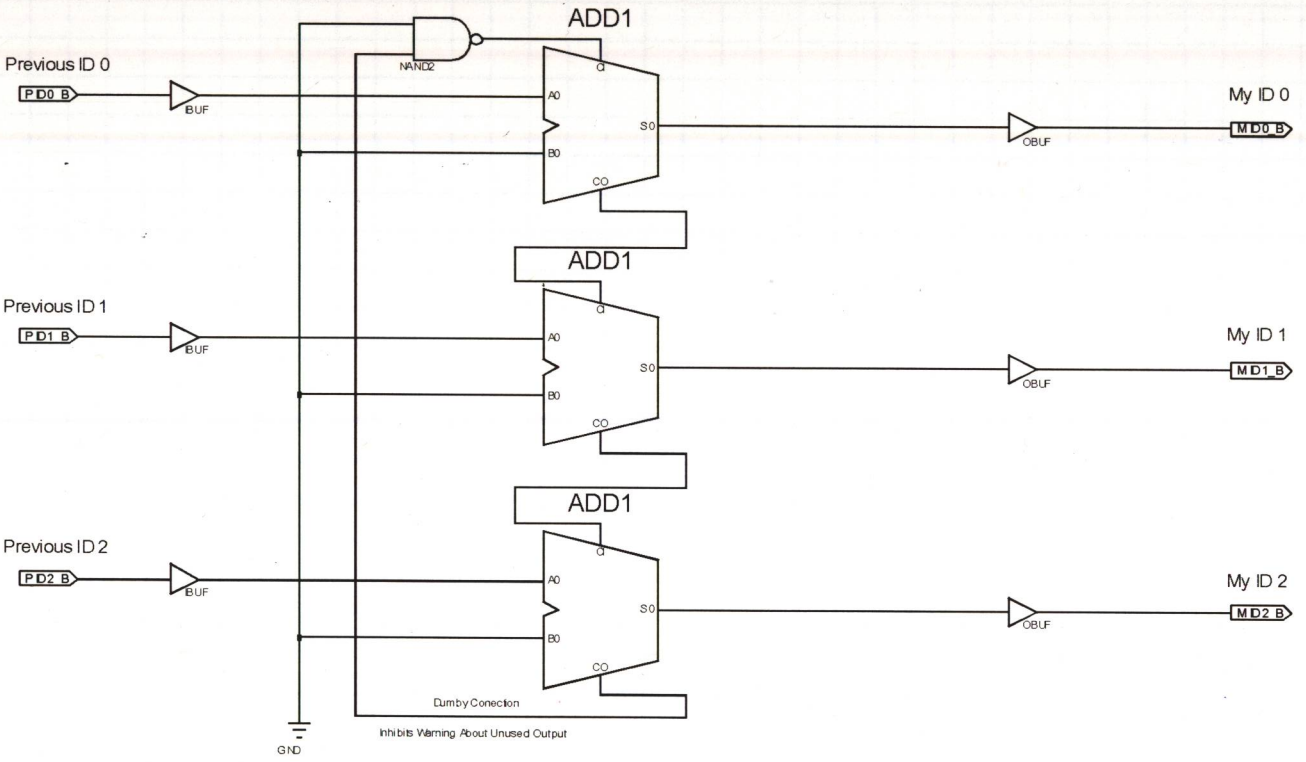


October 2011

2 Oct 2023
ARB

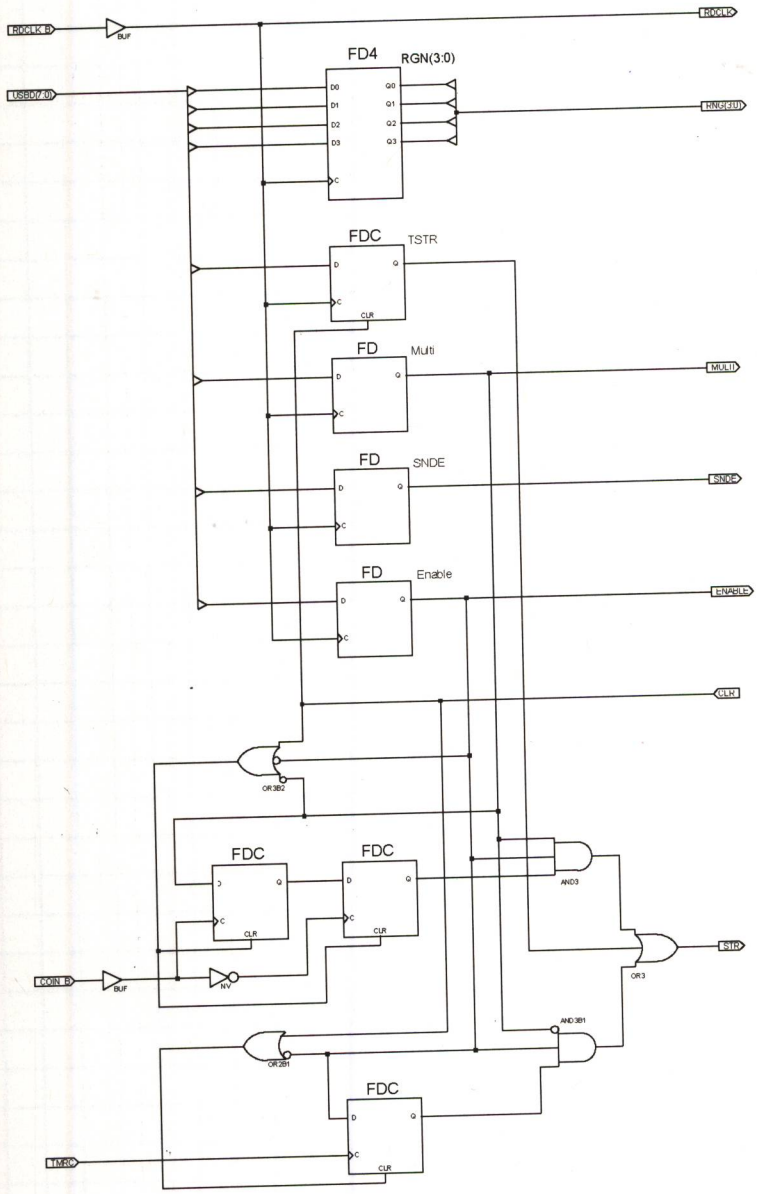

IO Bus Module
OBUFE8
IBUF8
UBUS(7:0)
UBUSE
USBD(7:0)
IDT(2:0)
TMR(12:0)
OBUFE8
IBUF8
MBUS(7:0)
MBUSE
MUXE
S0
S1
M4_1E
D0
D1
D2
D3
S0
S1
E
O
VCC
September 2023

Interface ID Module

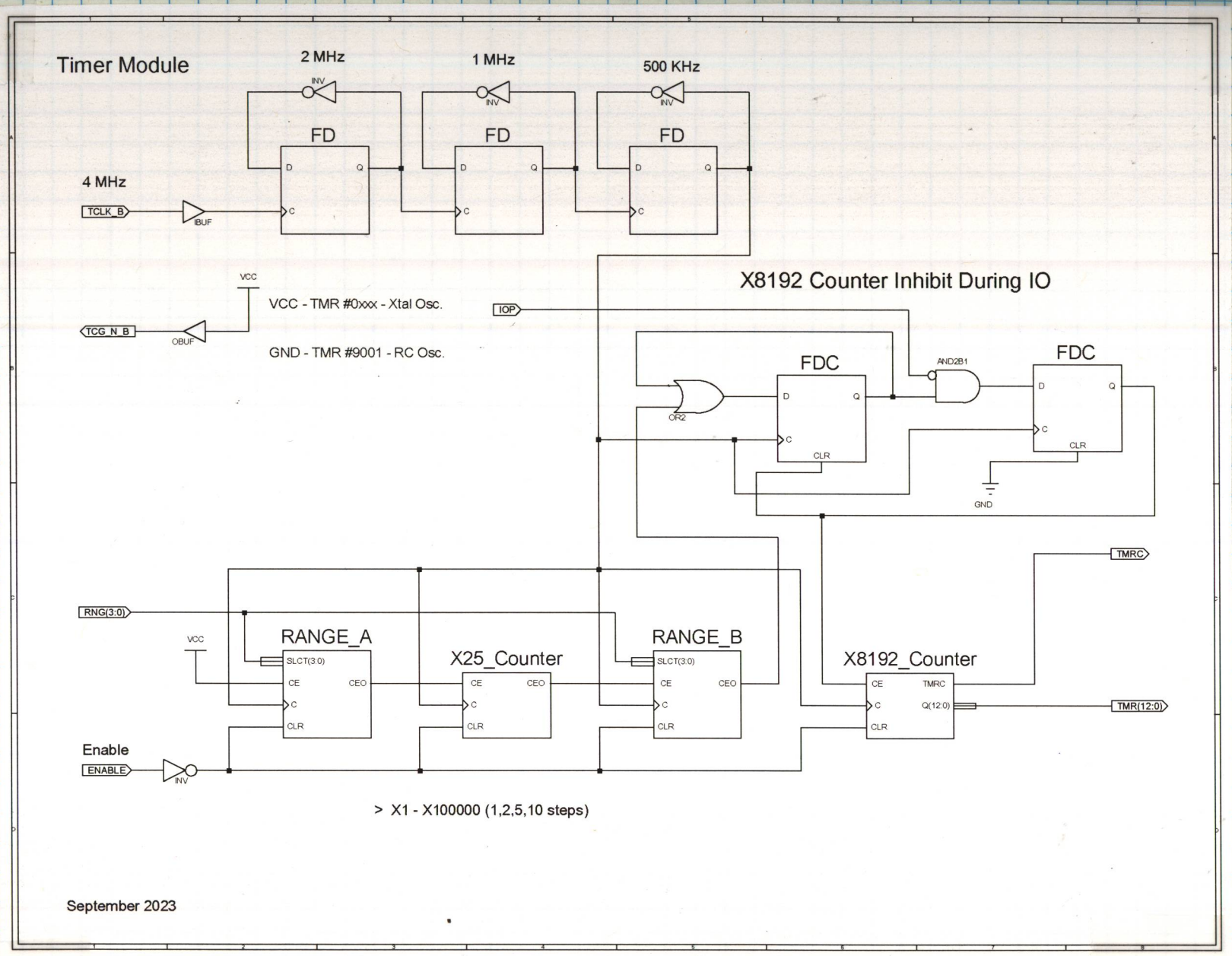


September 2023

MCS Module



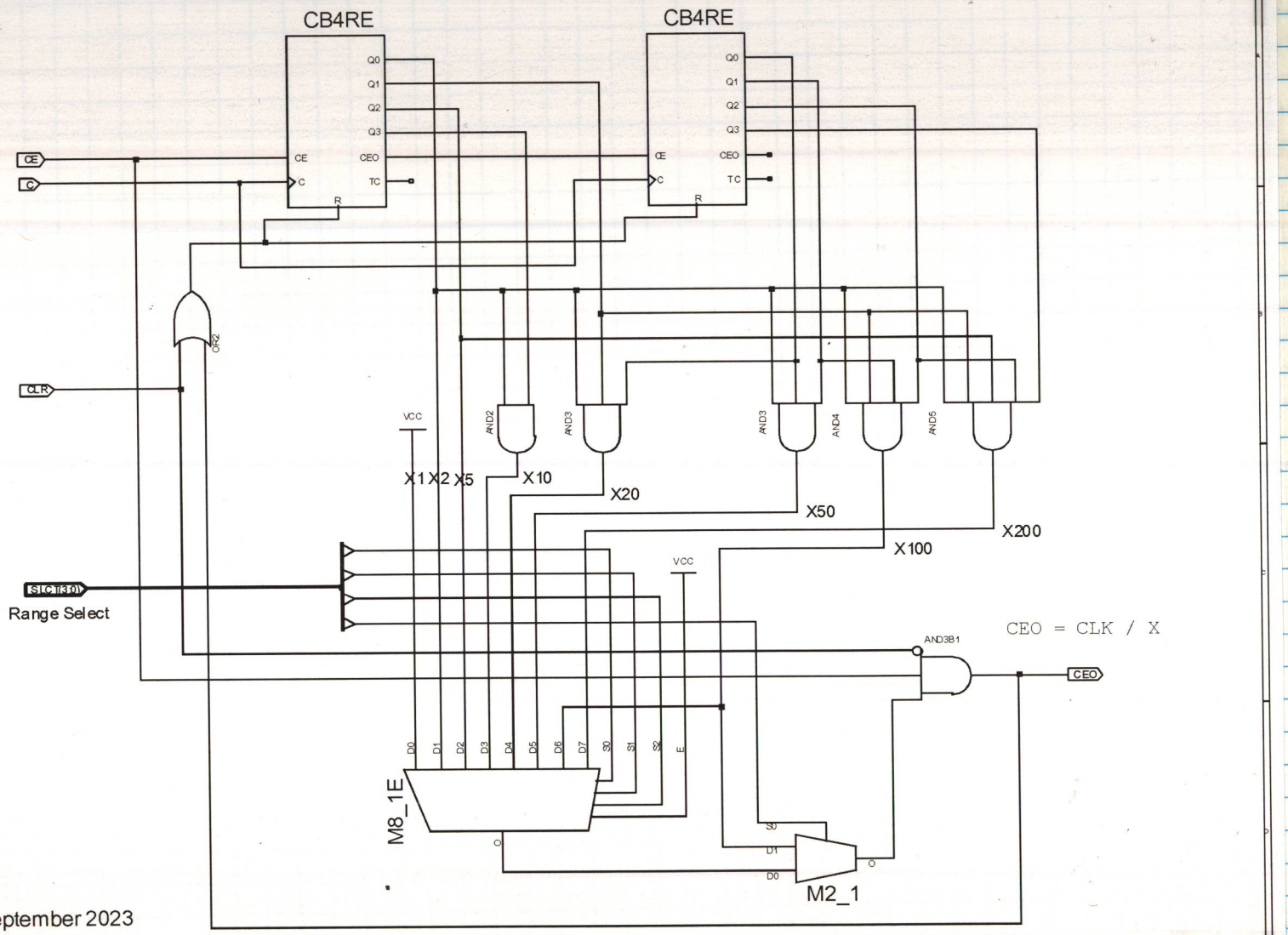
October 2011


Timer Module
2 MHz
1 MHz
500 KHz
INV
FD
D
Q
C
4 MHz
TCLK_B
IBUF
VCC
TCG_N_B
OBUF
VCC - TMR #0xxx - Xtal Osc.
GND - TMR #9001 - RC Osc.
X8192 Counter Inhibit During IO
IOP
FDC
CLR
OR2
AND2B1
GND
TMRC
RNG(3:0)
RANGE_A
X25_Counter
RANGE_B
X8192_Counter
SLCT(3:0)
CE
CEO
TMRC
Q(12:0)
TMR(12:0)
Enable
ENABLE
> X1 - X100000 (1,2,5,10 steps)
September 2023

20 Oct 2023

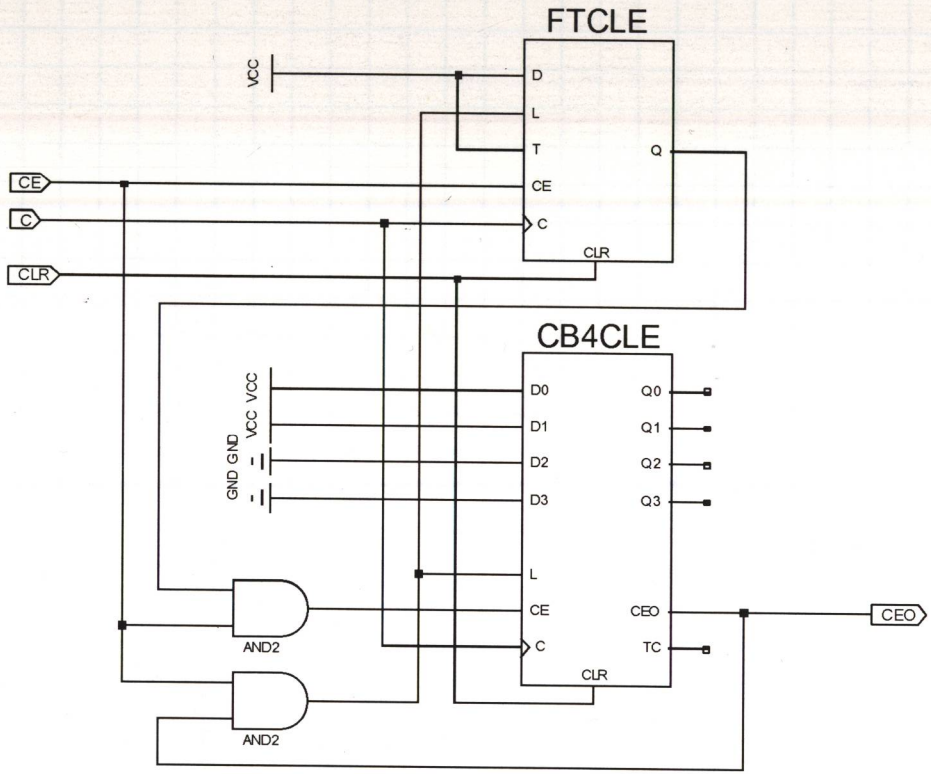
RANGE_A

2 1/2 - Decade 1/2/5/10 Counter



September 2023

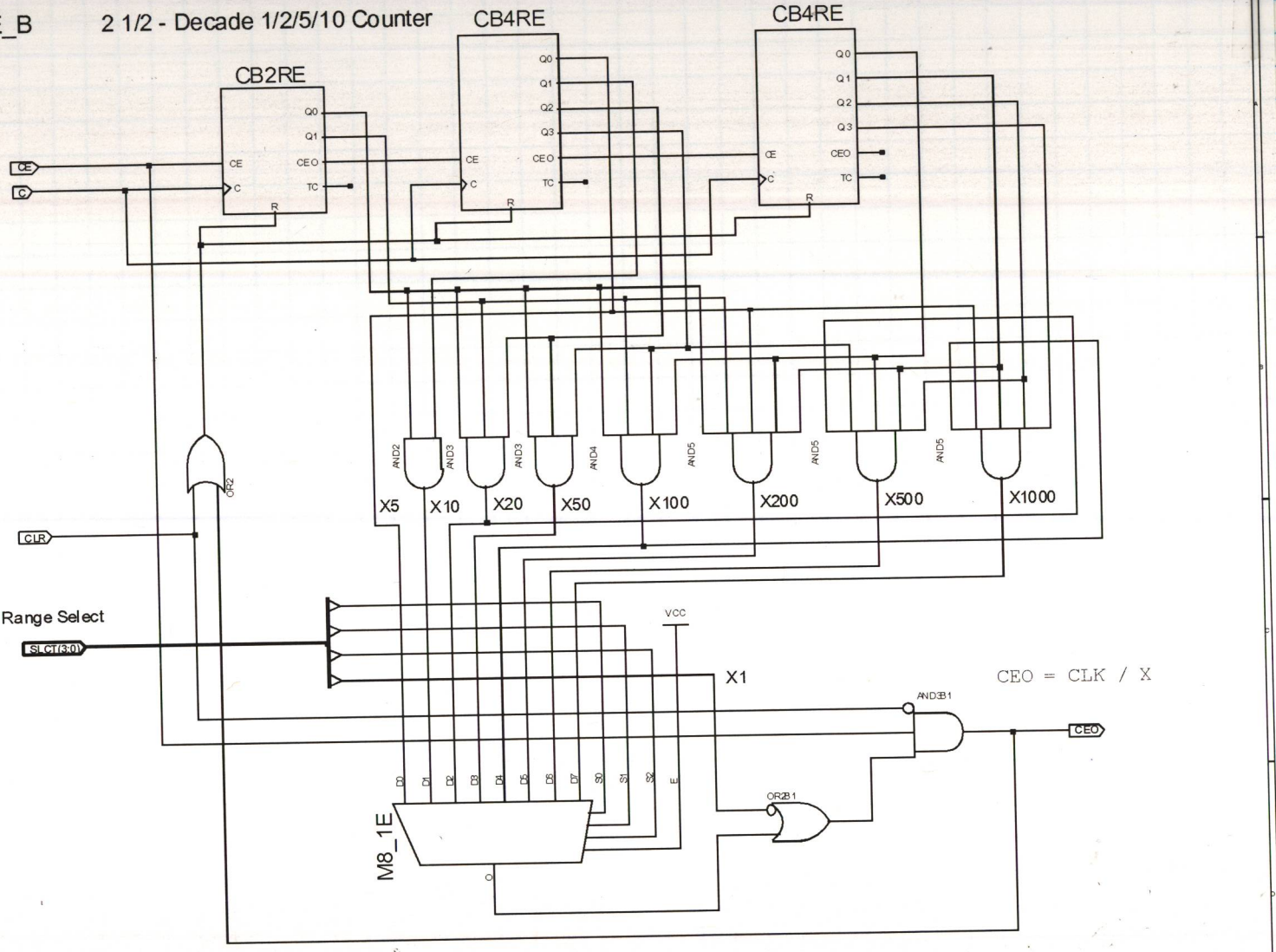
X25 Counter



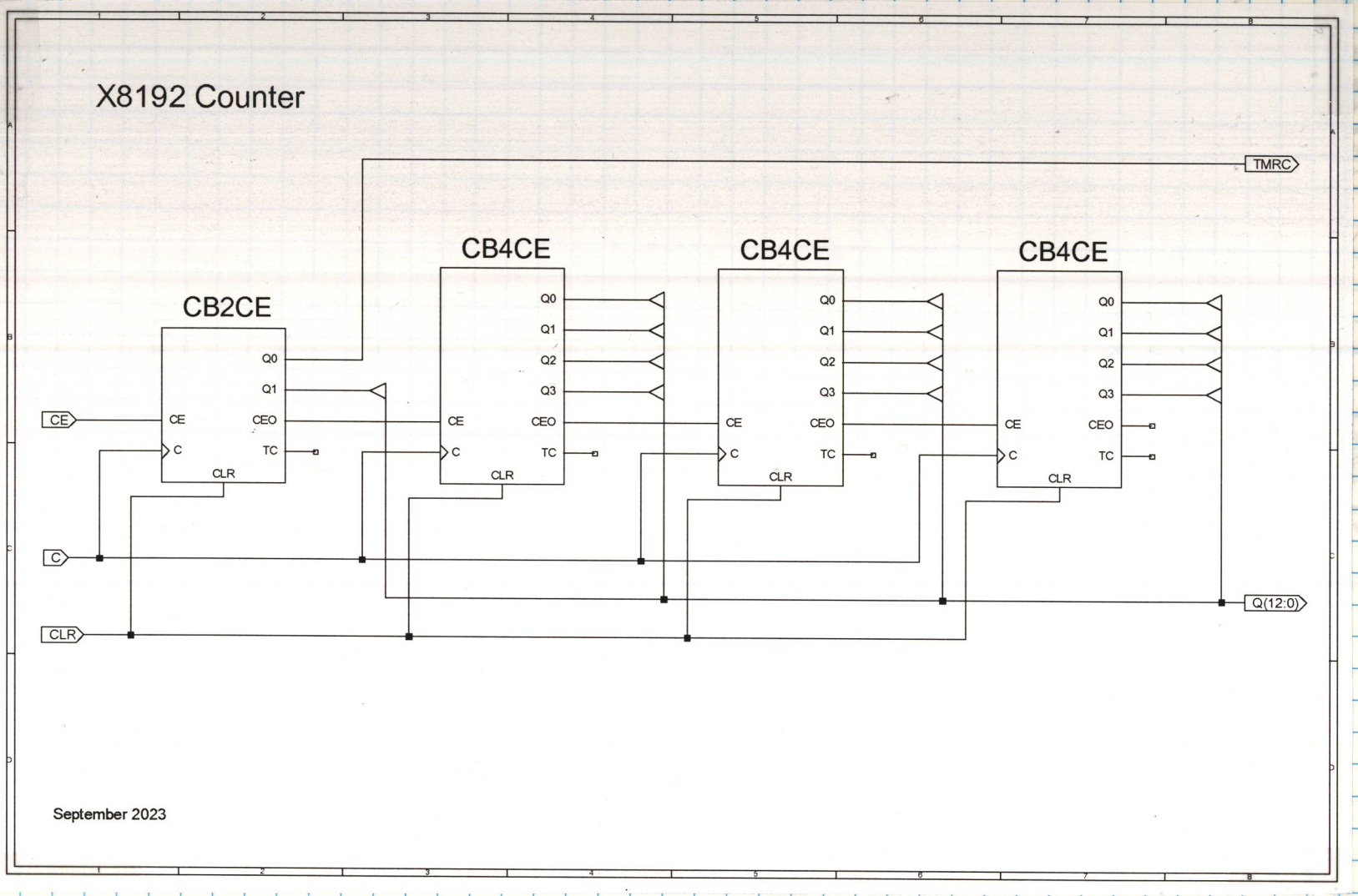
September 2023

2 Oct 2023
RBB

RANGE_B 2 1/2 - Decade 1/2/5/10 Counter



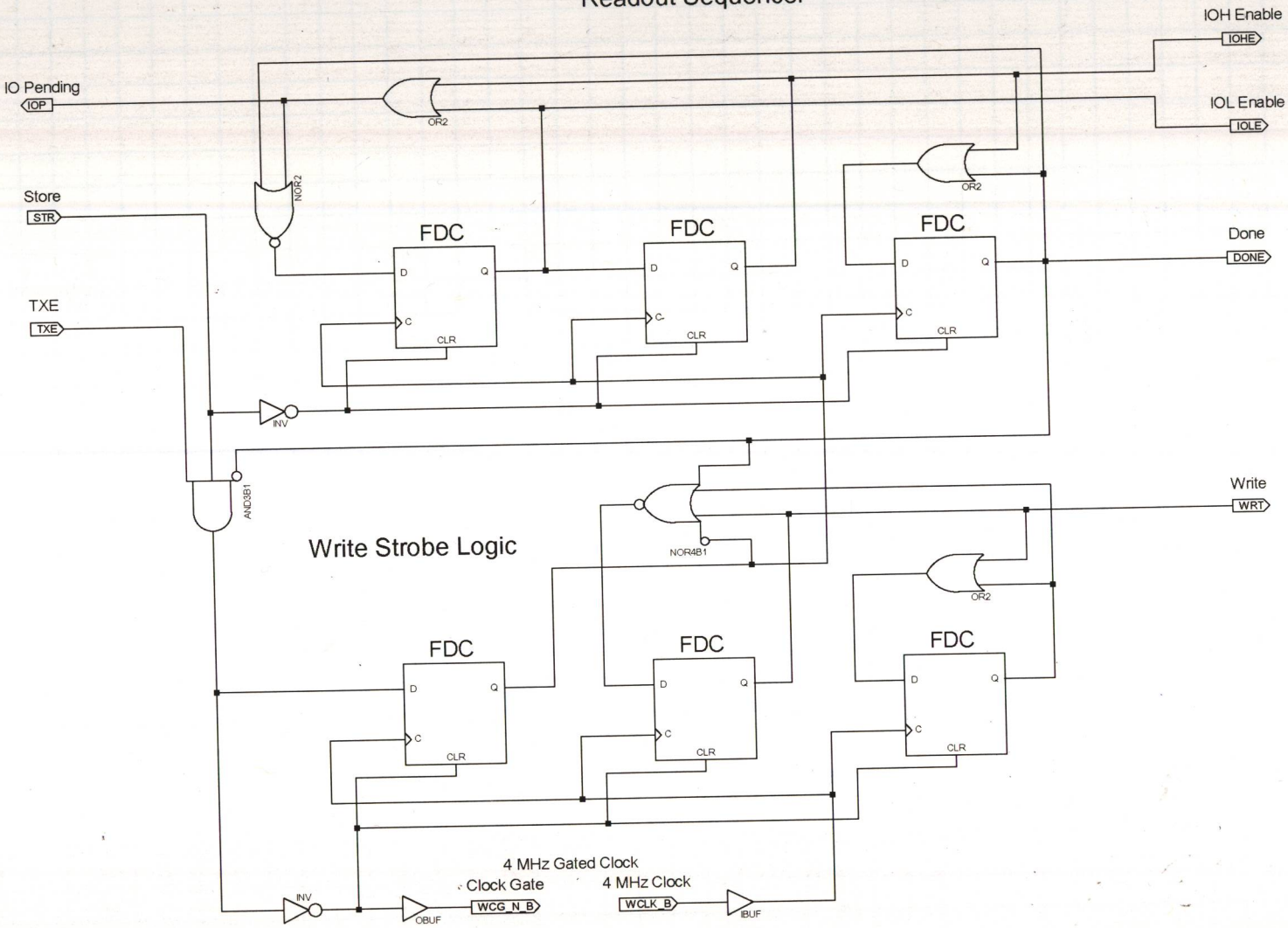
Septemberr 2023



20 Oct 2023
ARB

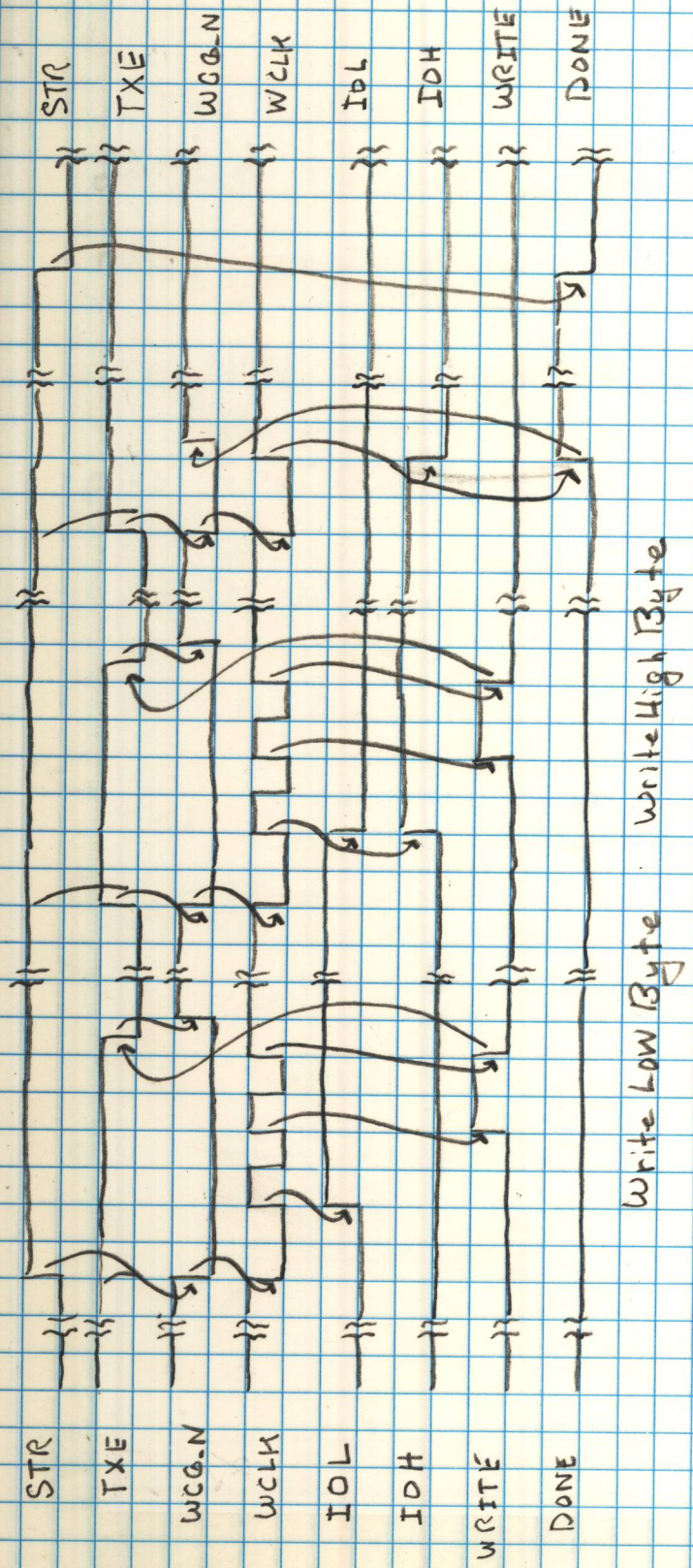
ReadOut Module

Readout Sequencer



September 2023

Readout Sequencer Details



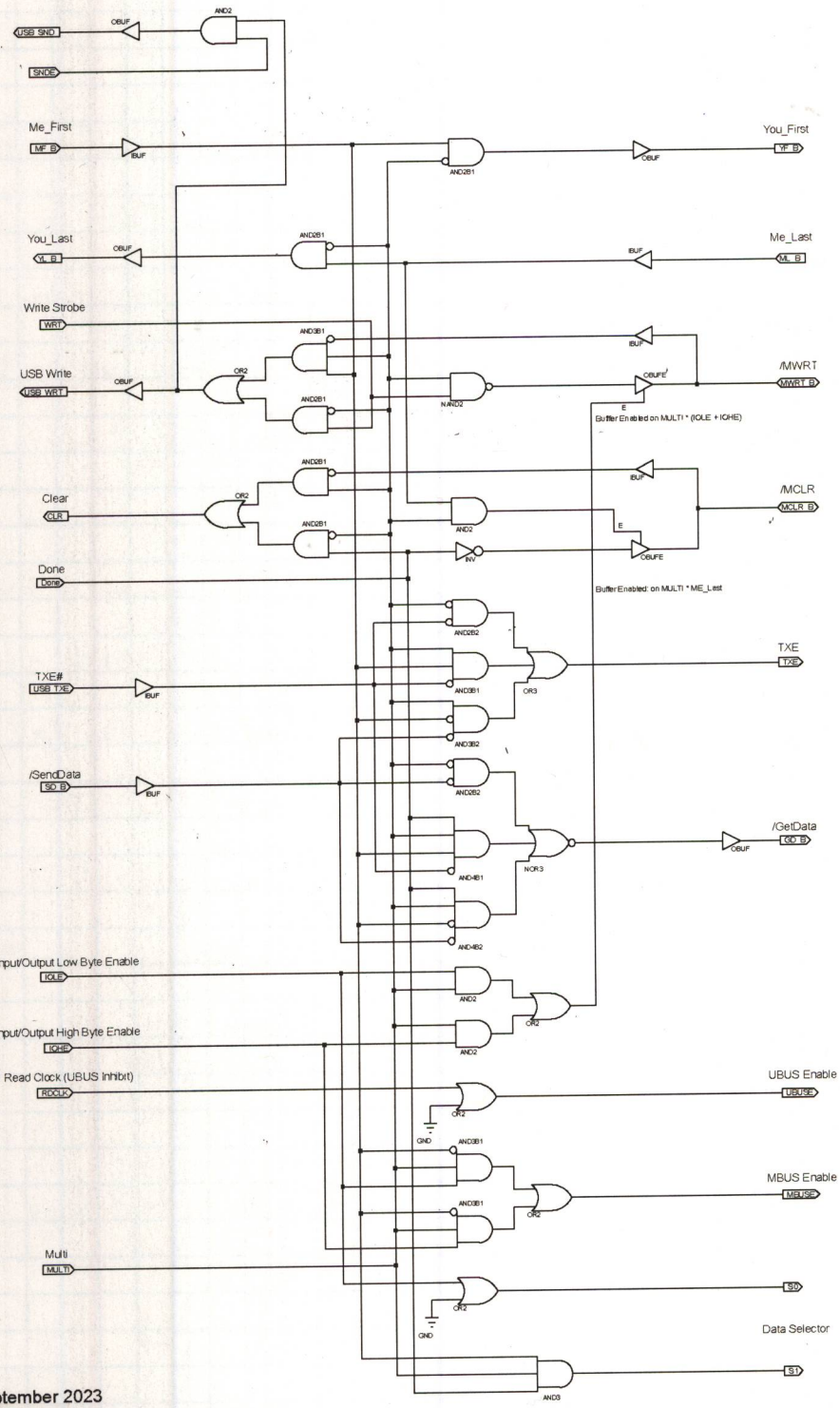
The combination of STR and TXE becoming active triggers the transfer of Two bytes to the USB Controller.

The sequencer waits in the DONE state (ignores the TXE state) until the STR signal Negates which initializes the sequencer for the next transfer.

Typical Transfer Rate:
~3.5 µs for 2 Bytes

2 Oct 23
ARB

Multiple ADC/TMR Bus Control Module



September 2023

The BUS Module

The BUS module controls the transfer of Data from modules in single and multiparameter modes. These modes are:

1) NON Multiparameter Mode (Single)

2) First Module of a Multiparameter Chain

3) Middle Module of a MultiparameterChain

4) Last Module of a Multiparameter Chain

and

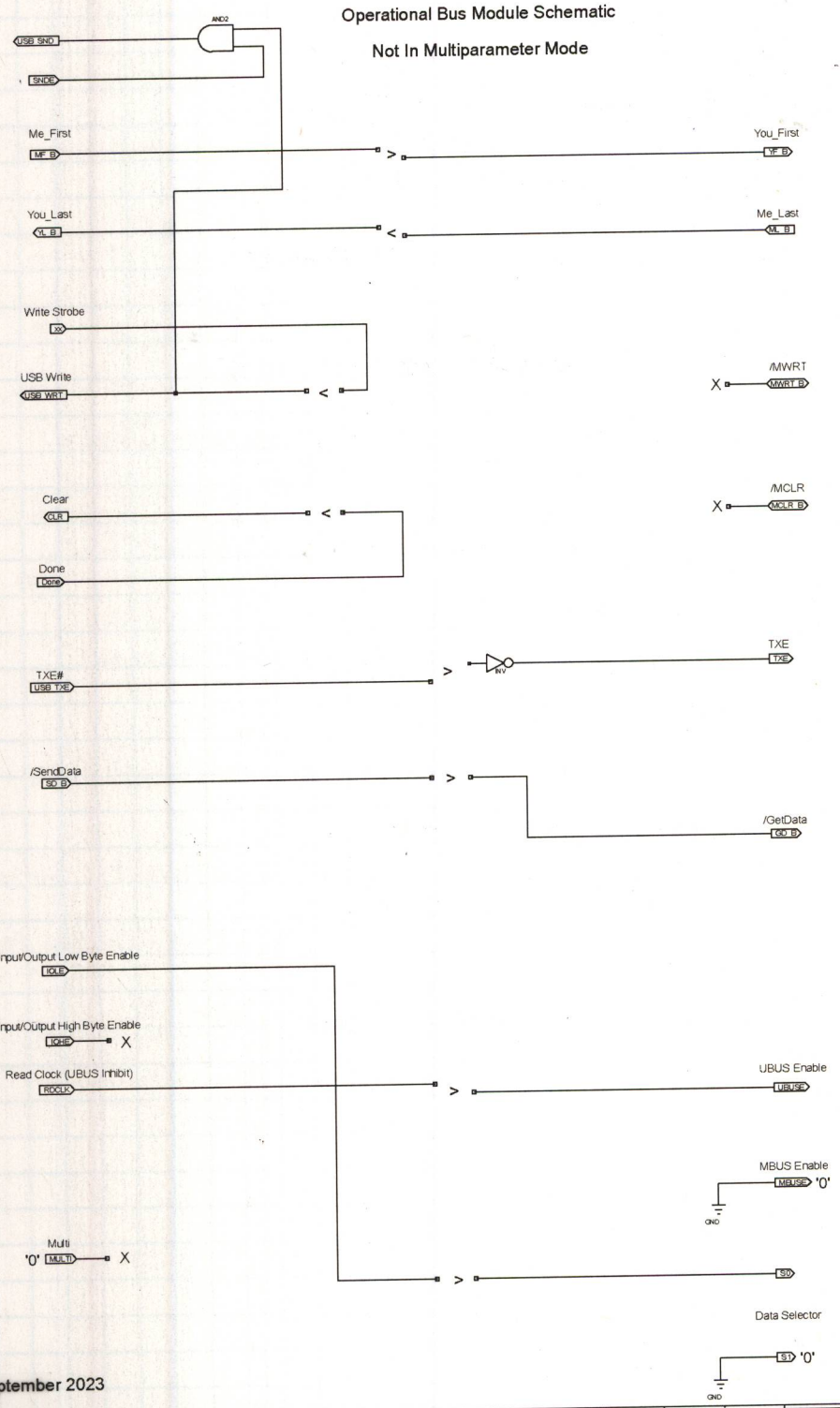
5) First and Last Module of a Multiparameter Chain
   ie - the only module in Multiparameter Mode
   (allows coincidence operation)

20 Oct 2023
ARB

Multiple ADC/TMR Bus Control Module

Operational Bus Module Schematic

Not In Multiparameter Mode



September 2023

NOT in Multiparameter Mode

This is a simplified schematic of the signal flow in the BUS Module when NOT in the multiparameter mode.

The multimode control signals are set pass through signals

Me_First → You_First

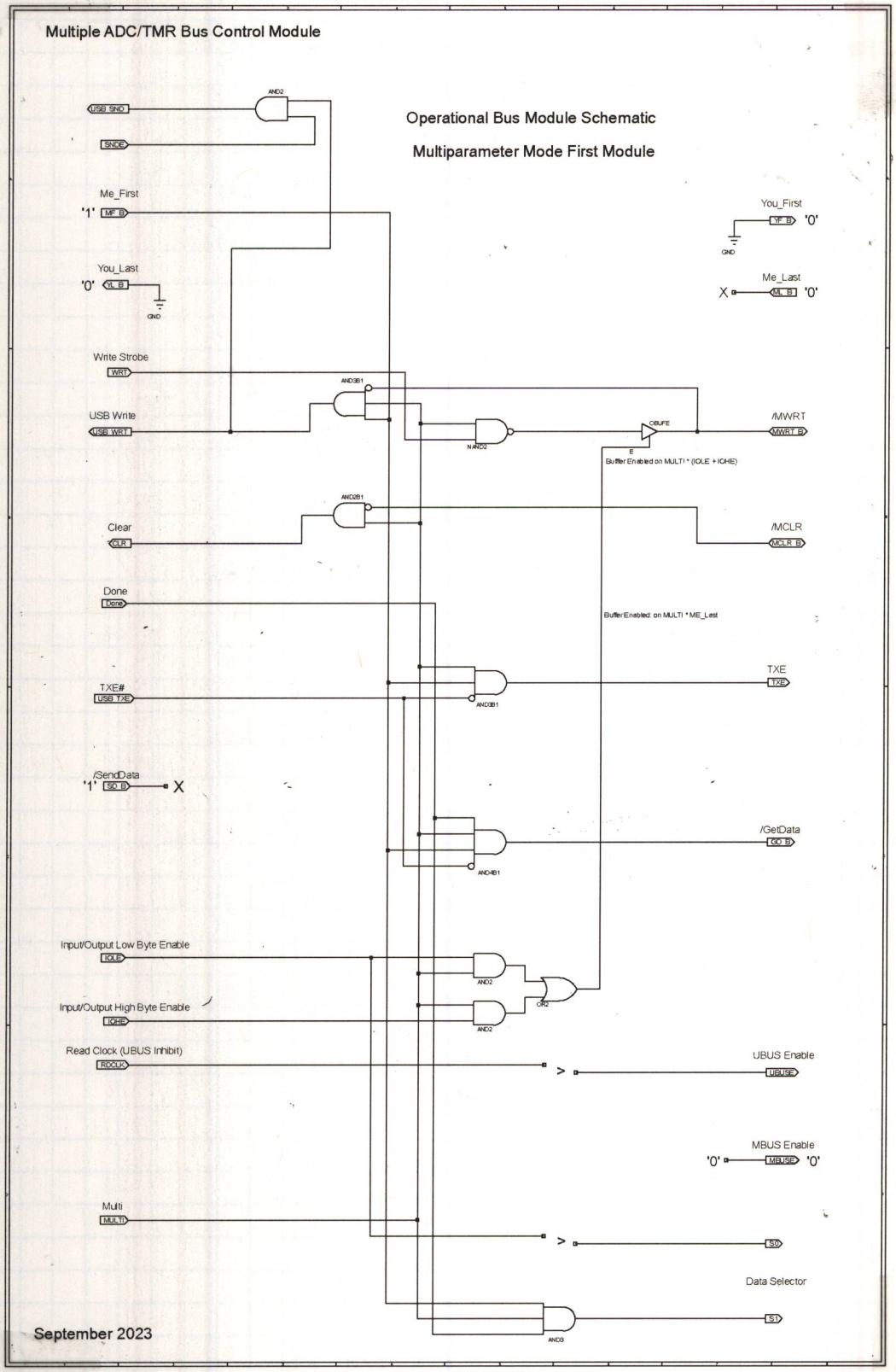
You_Last ← Me_Last

(SendData) SD_B → GD_B (GetData)

This allows single mode modules to be placed between Multiparameter Mode modules.

All other relavent signals are internally controlled independently of multimode operation.

2 Oct 2023
ARB


Multiple ADC/TMR Bus Control Module
Operational Bus Module Schematic
Multiparameter Mode First Module
AND2
USB_SND
SNDE
Me_First
'1'
MF_B
You_First
'0'
GND
YF_B
You_Last
'0'
YL_B
Me_Last
X
ML_B
'0'
Write Strobe
WRT
AND3B1
USB Write
USB_WRT
NAND2
OBUFE
/MWRT
MWRT_B
E
Buffer Enabled on MULTI * (IOLE + IOHE)
AND2B1
Clear
CLR
/MCLR
MCLR_B
Done
Done
Buffer Enabled on MULTI * ME_Last
TXE
TXE#
USB_TXE
AND3B1
/SendData
'1'
SD_B
X
/GetData
GD_B
AND4B1
Input/Output Low Byte Enable
IOLE
AND2
Input/Output High Byte Enable
IOHE
AND2
OR2
Read Clock (UBUS Inhibit)
RDCLK
UBUS Enable
UBUSE
MBUS Enable
'0'
MBUSE
'0'
Multi
MULTI
S0
Data Selector
S1
AND3
September 2023

First Multimode Module in a chain

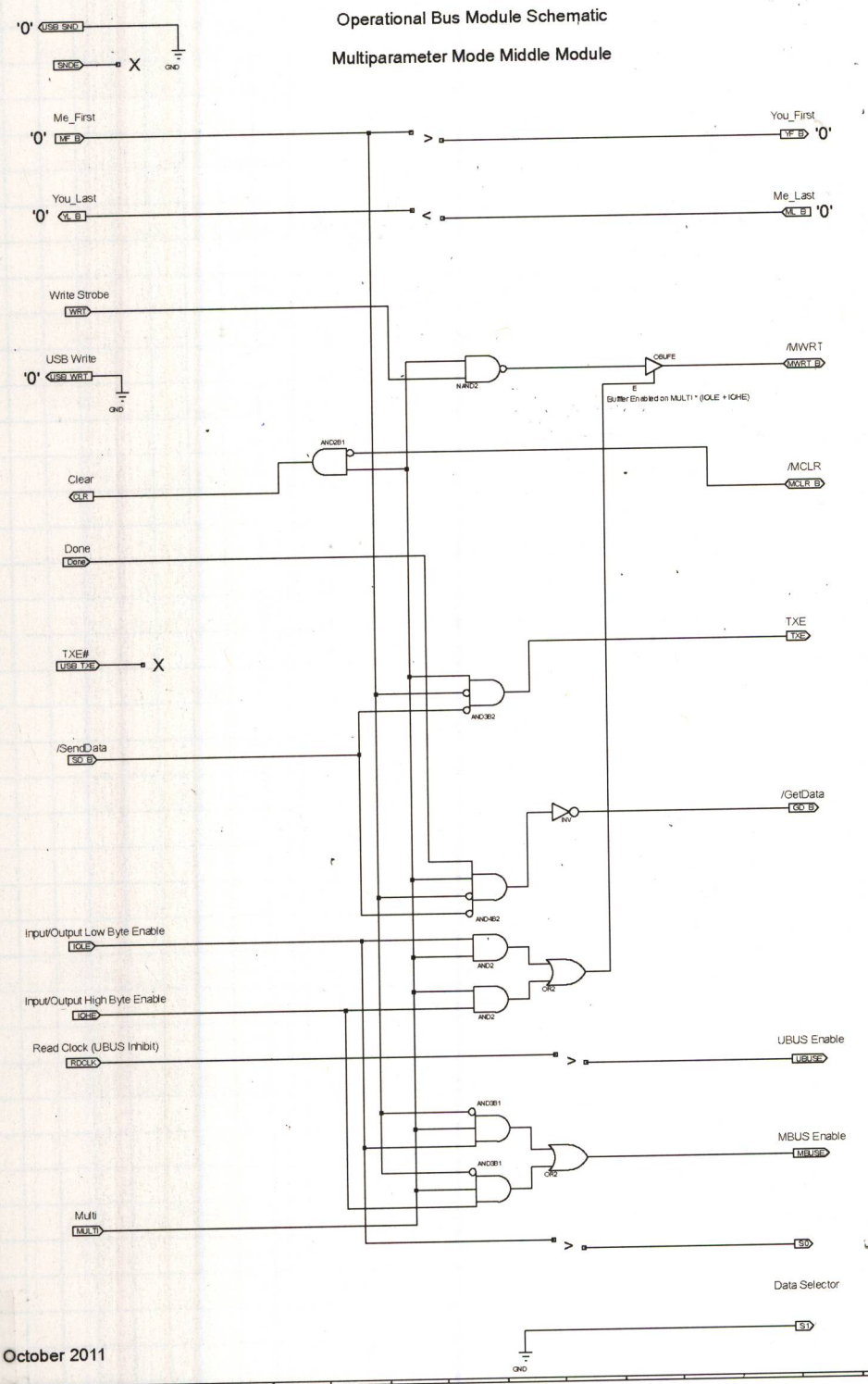
The first multimode enabled module in a chain performs all data transfers for the remaining multimode enabled modules in a chain.

The first module has the Me_First signal at the '1' level. This signal configures the BUS Module to perform all data transfers, internal and external, for the multiparameter chain.

First Module		Next Module (BUS signals)
USB Write (WRT) (WRT before DONE)	←	MWRT_B
CLR	←	MCLR_B (from Last Module)
TXE# (TXE before DONE)	→	GD_B (at DONE)
multi enable	BUS Data to USB	(at DONE)

2 Oct 2023
ARB

Multiple ADC/TMR Bus Control Module



Multiparameter Enabled Module in the Middle of a Chain

A multiparameter enabled module is not the first or last multiparameter enabled module. Data transfer is initiated by the assertion of the SD-B (/Send Data) signal which produces the pseudo TXE signal. Transfer proceeds when the TXE and STR signal within this module becomes active.

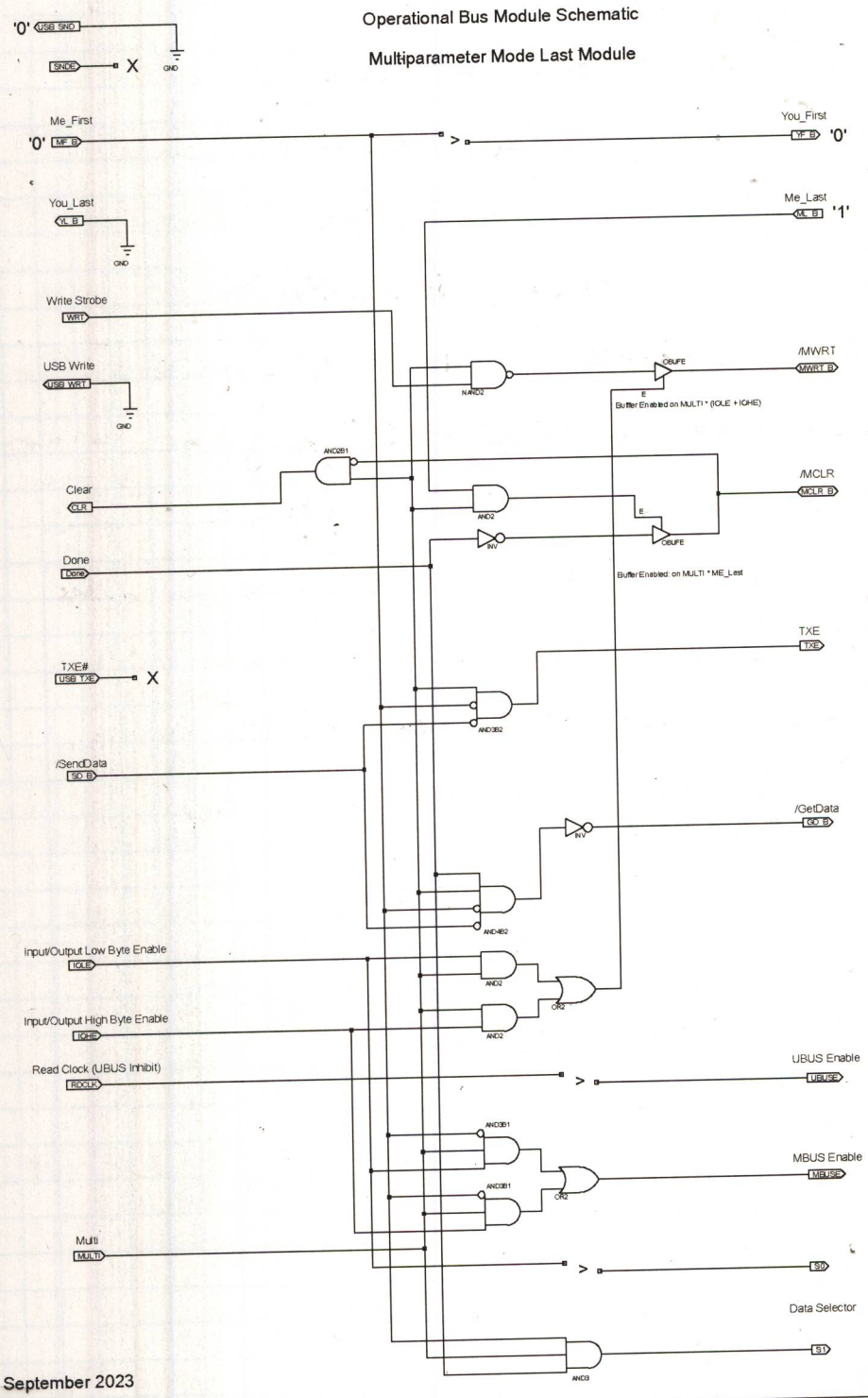
The BUS signals

— from — Previous module		Middle module		— to — Next module
Me_First (Ø)	→	'Ø'	→	You_First
You_Last	←	'Ø'	←	Me_Last (Ø)
GD-B (/Get Data)	→	SD-B (→TXE) (/Send Data)	→	SD-B (at DONE) (/Send Data)
MCLR-B (→CLR)	←	MCLR_B (→CLR)	←	MCLR-B (at DONE) (/MCLR) CLR

MWRT-B
(/MWRT)
from IOL & IOH
& WRT
before DONE

2 Oct 2023
ARB

Multiple ADC/TMR Bus Control Module



The Last Multiparameter Enabled Module in a Chain

The last enabled multiparameter module in a chain controls the completion of the final module's data transfer and terminates the multiparameter transaction. The receipt of the SD-B signal (/Send Data) generates the pseudo TXE signal. When the TXE and the modules' STR signal become active the dat transfer begins. At the completion of the data transfer the DONE signal generates the MCLR-B BUS signal (/MCLR) which then clears all the modules in the multiparameter chain. This readys the chain for another event.

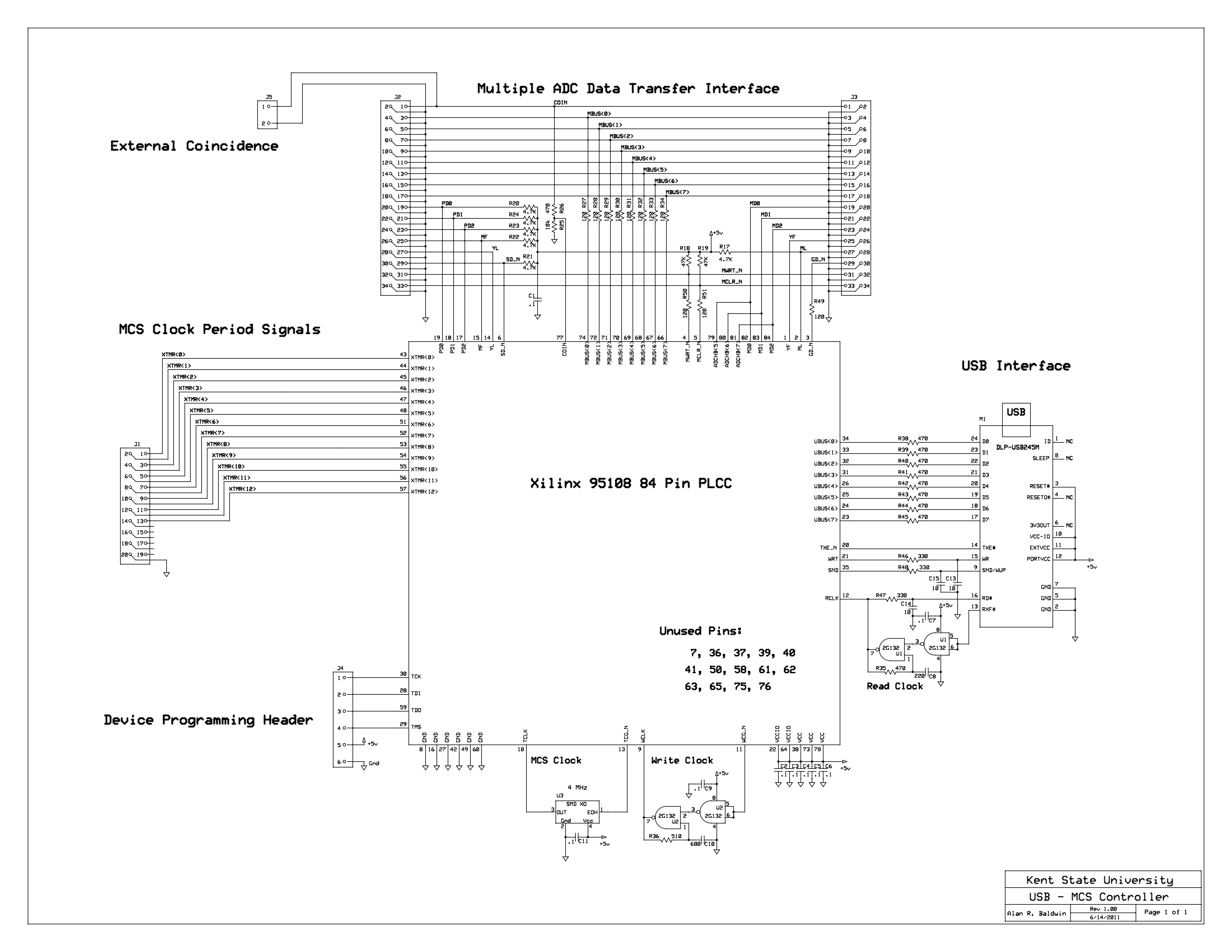
2 Oct 23
ABB

A Single Enabled Multiparameter Module

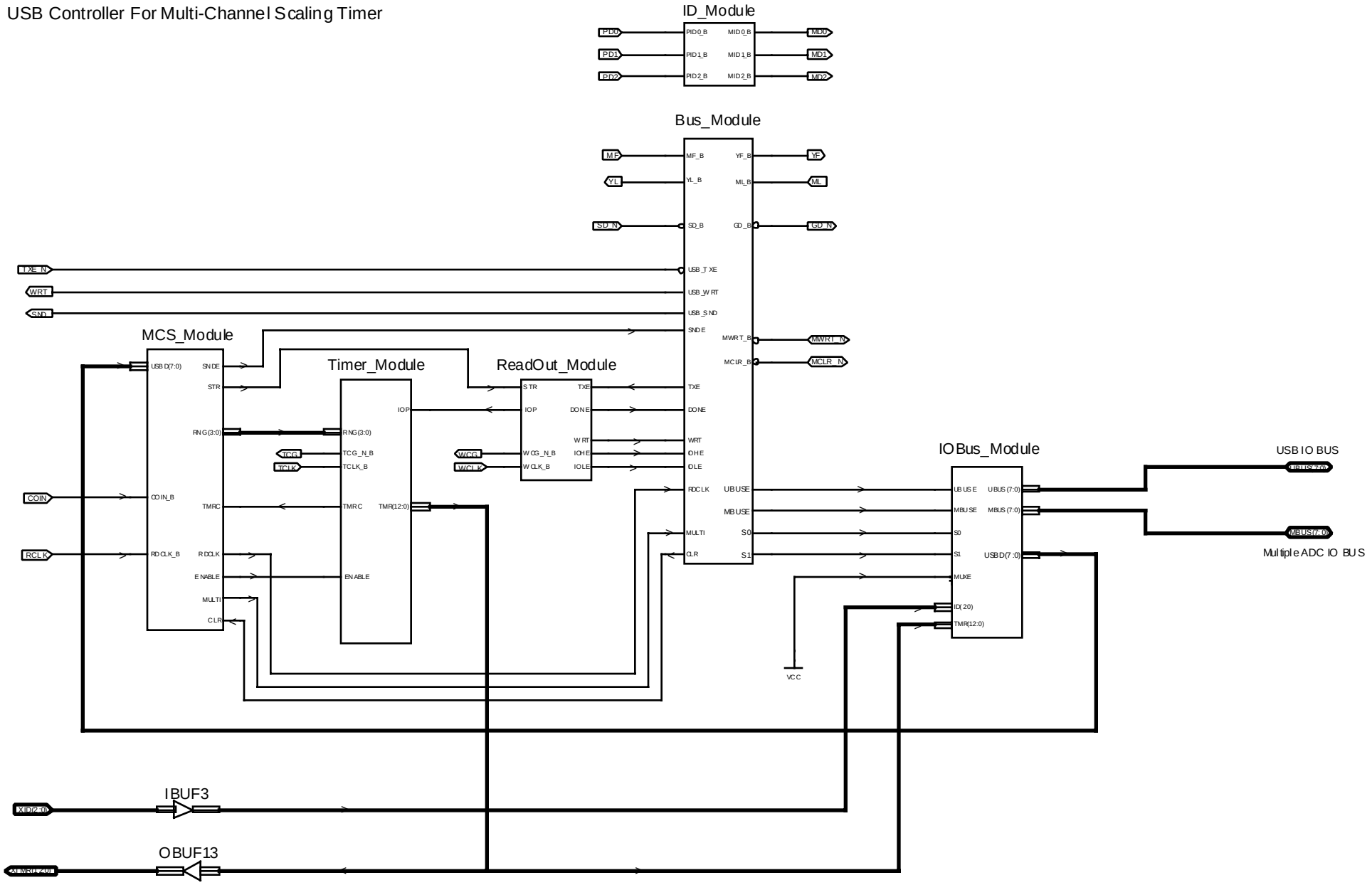
When a module is enabled as a multiparameter module and is the only such module it operates as the first and last module simultaneously.

This mode is useful if acquisition uses the COIN signal to enable the processing of an ADC signal with specific requirements.

2 Oct 2023
ABD

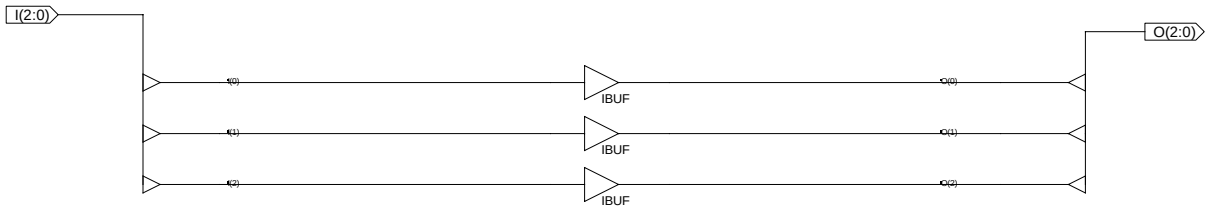

Multiple ADC Data Transfer Interface
External Coincidence
MCS Clock Period Signals
Xilinx 95108 84 Pin PLCC
USB Interface
USB
DLP-USB245M
Read Clock
Unused Pins:
7, 36, 37, 39, 40
41, 50, 58, 61, 62
63, 65, 75, 76
Device Programming Header
MCS Clock
Write Clock
4 MHz
Kent State University
USB - MCS Controller
Alan R. Baldwin
Rev 1.00
6/14/2011
Page 1 of 1

USB Controller For Multi-Channel Scaling Timer



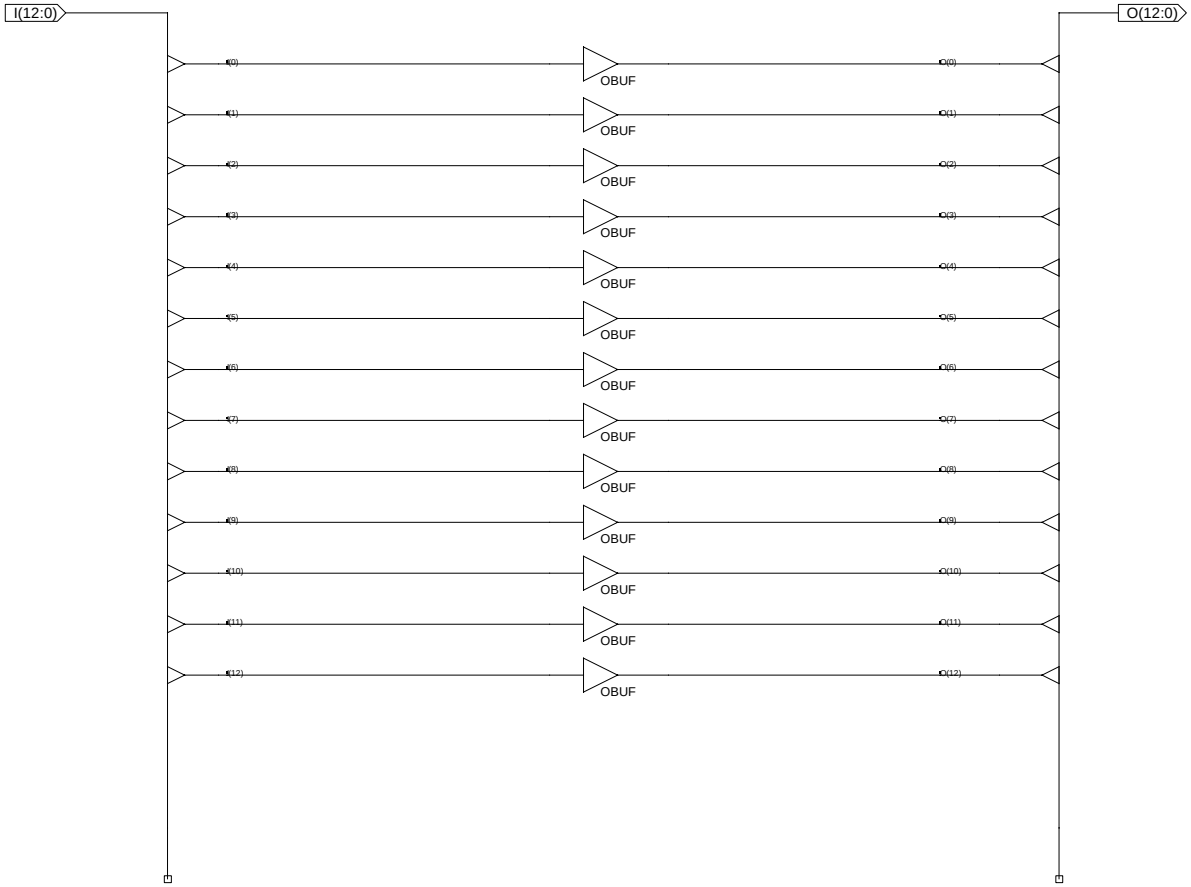
September 2023

IBUF3



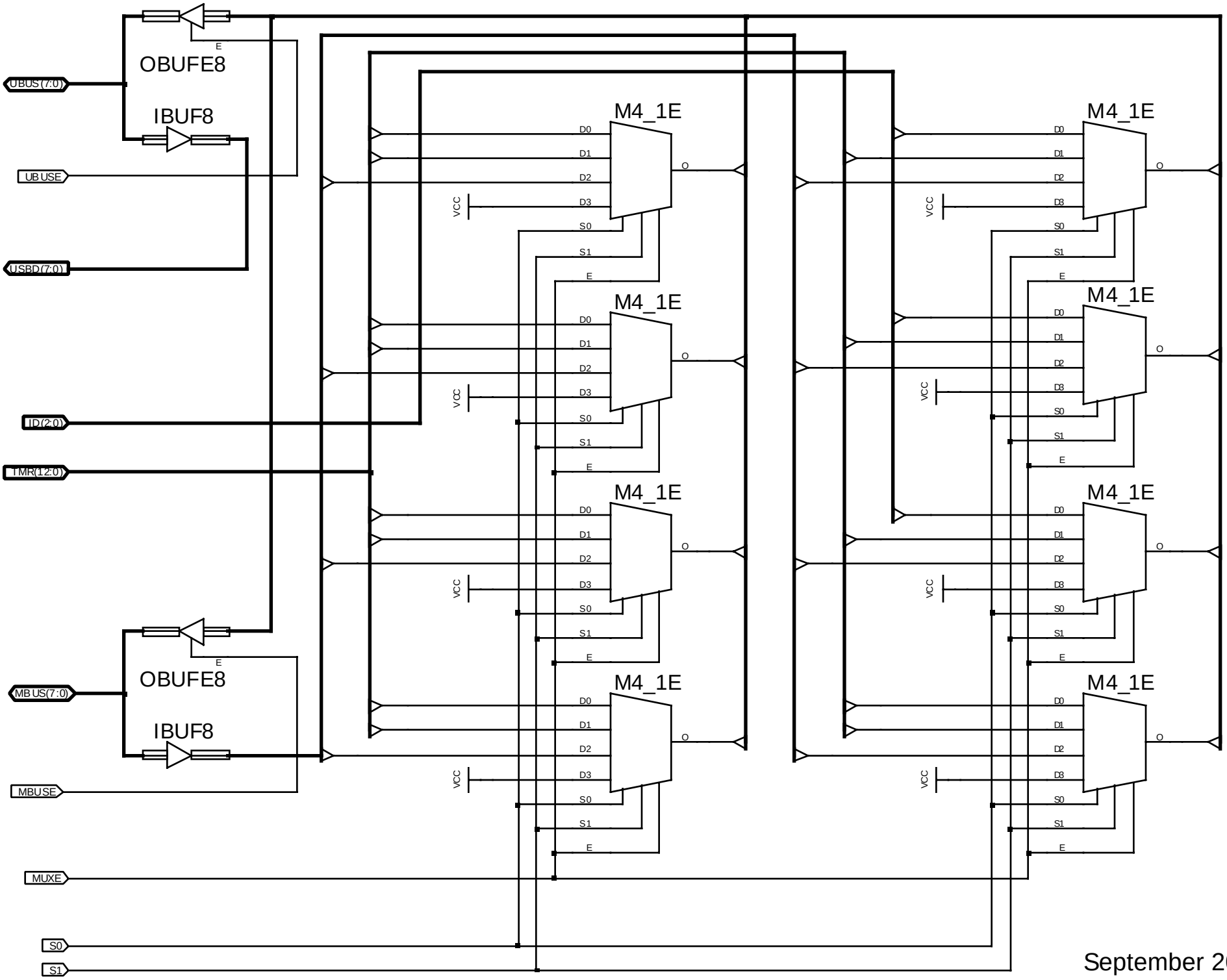
October 2011

OBUF13



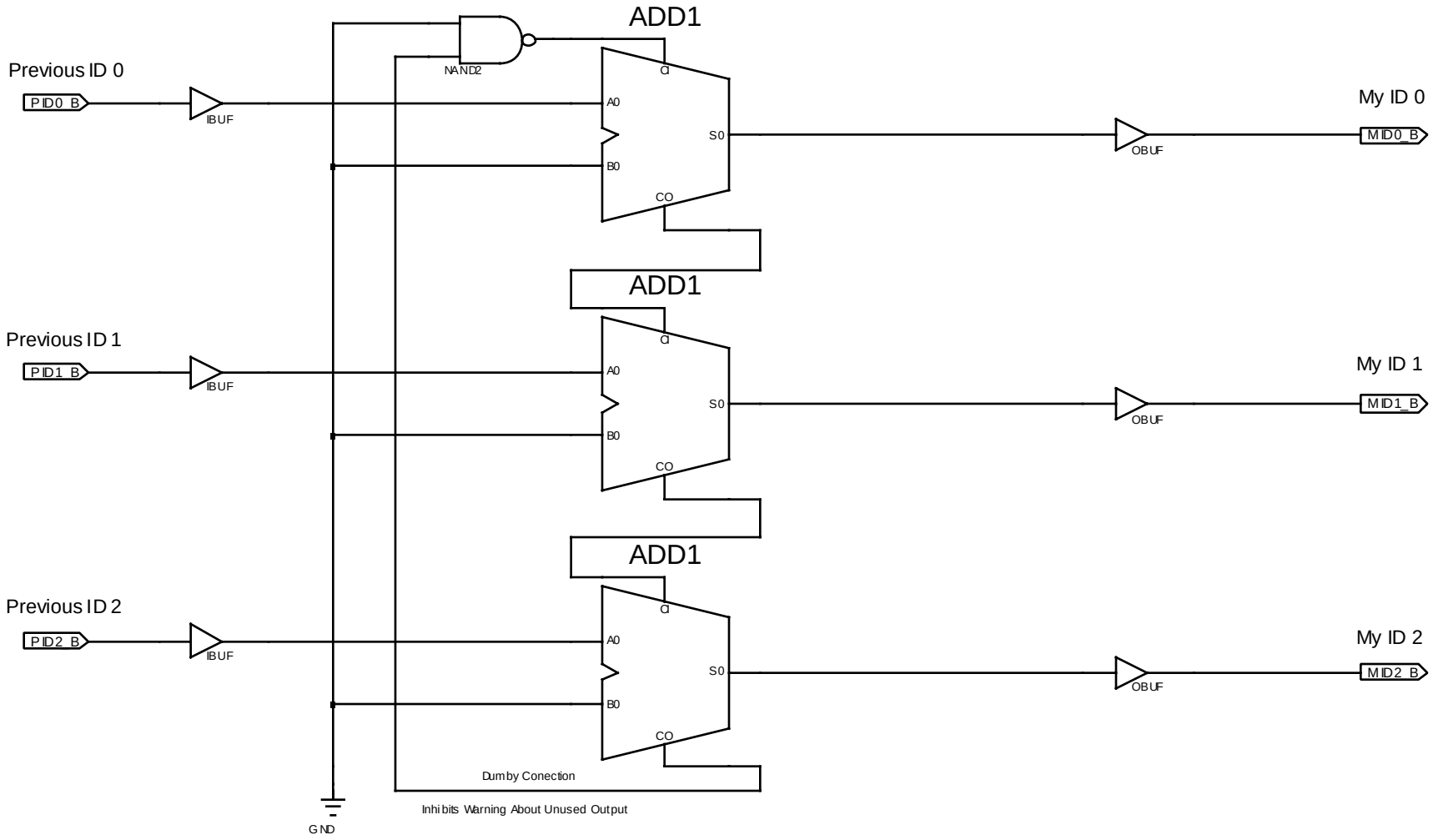
October 2011

IO Bus Module

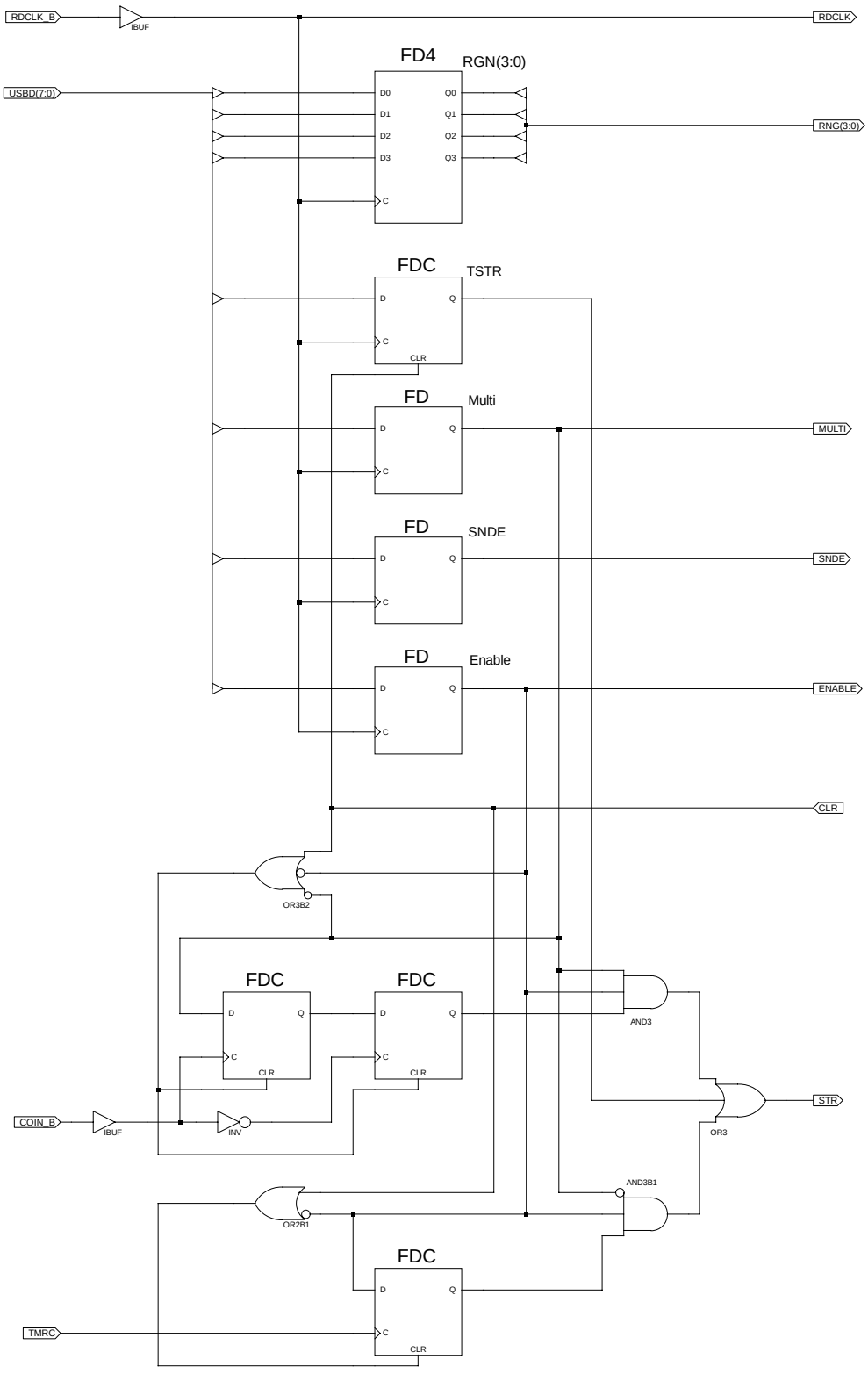


September 2023

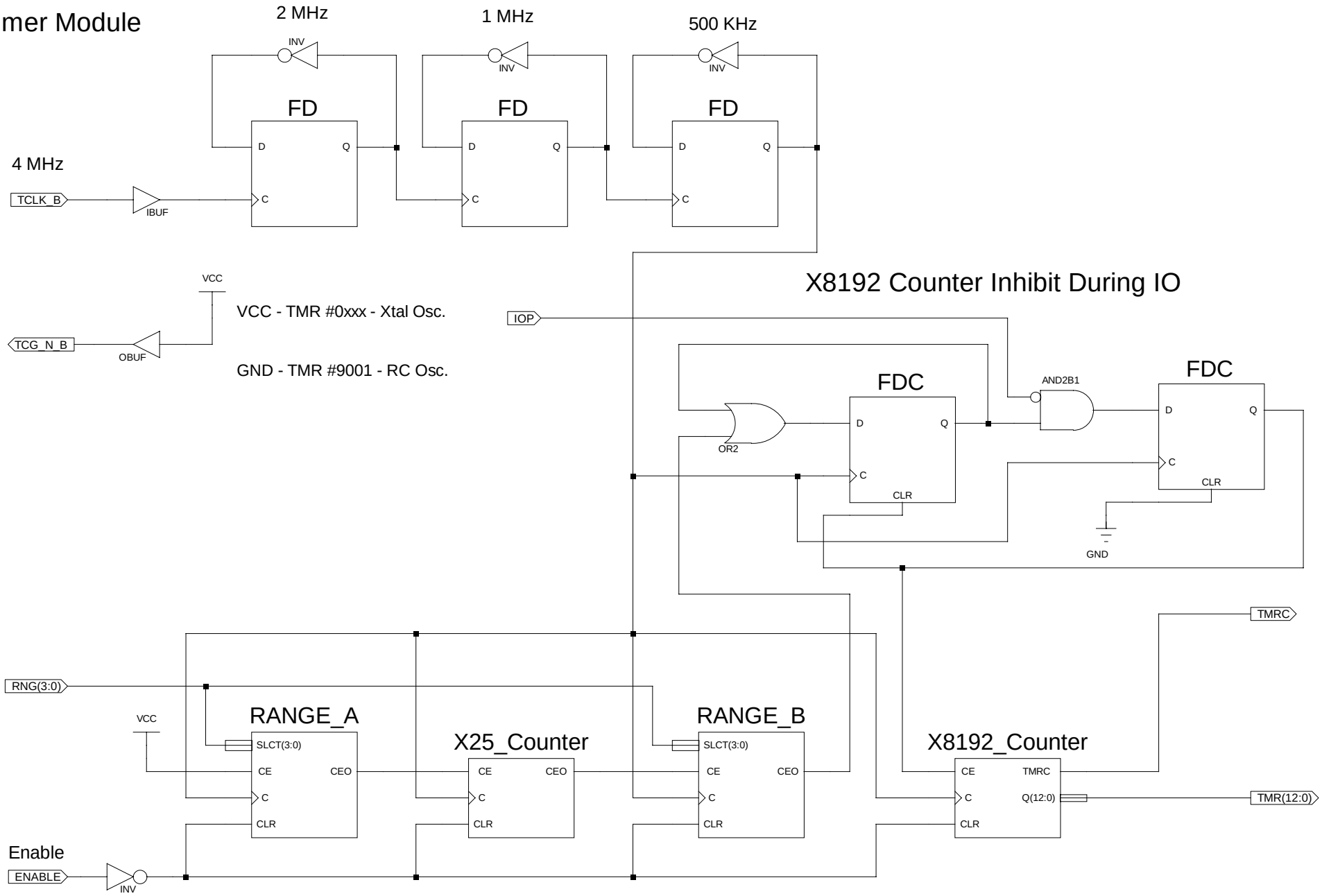
Interface ID Module



September 2023


RDCLK_B
IBUF
RDCLK
FD4
RGN(3:0)
USBD(7:0)
D0
D1
D2
D3
Q0
Q1
Q2
Q3
RNG(3:0)
C
FDC
TSTR
D
Q
C
CLR
FD
Multi
MULTI
SNDE
ENABLE
Enable
CLR
OR3B2
AND3
STR
COIN_B
INV
OR3
AND3B1
OR2B1
TMRC

Timer Module

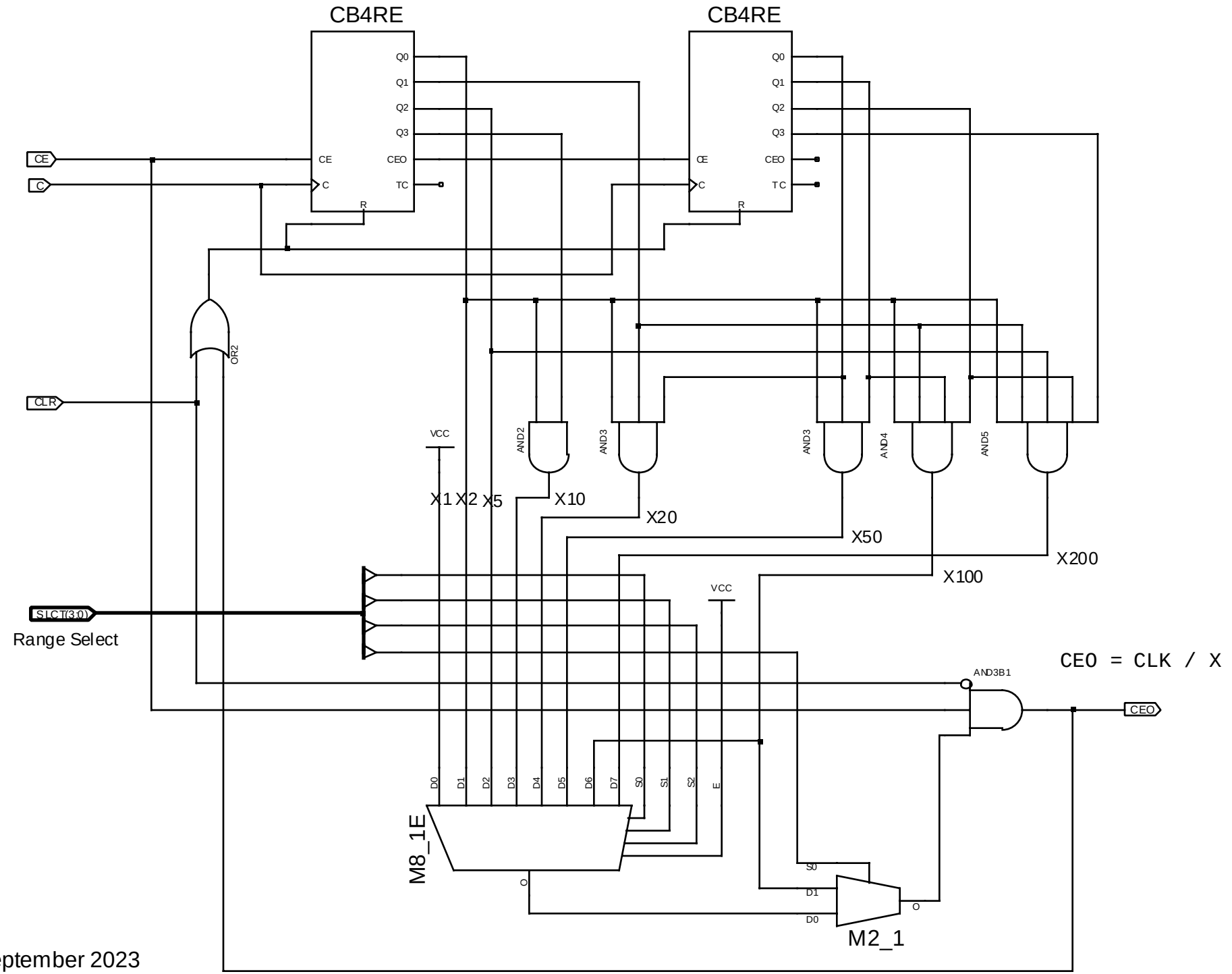


> X1 - X100000 (1,2,5,10 steps)

September 2023

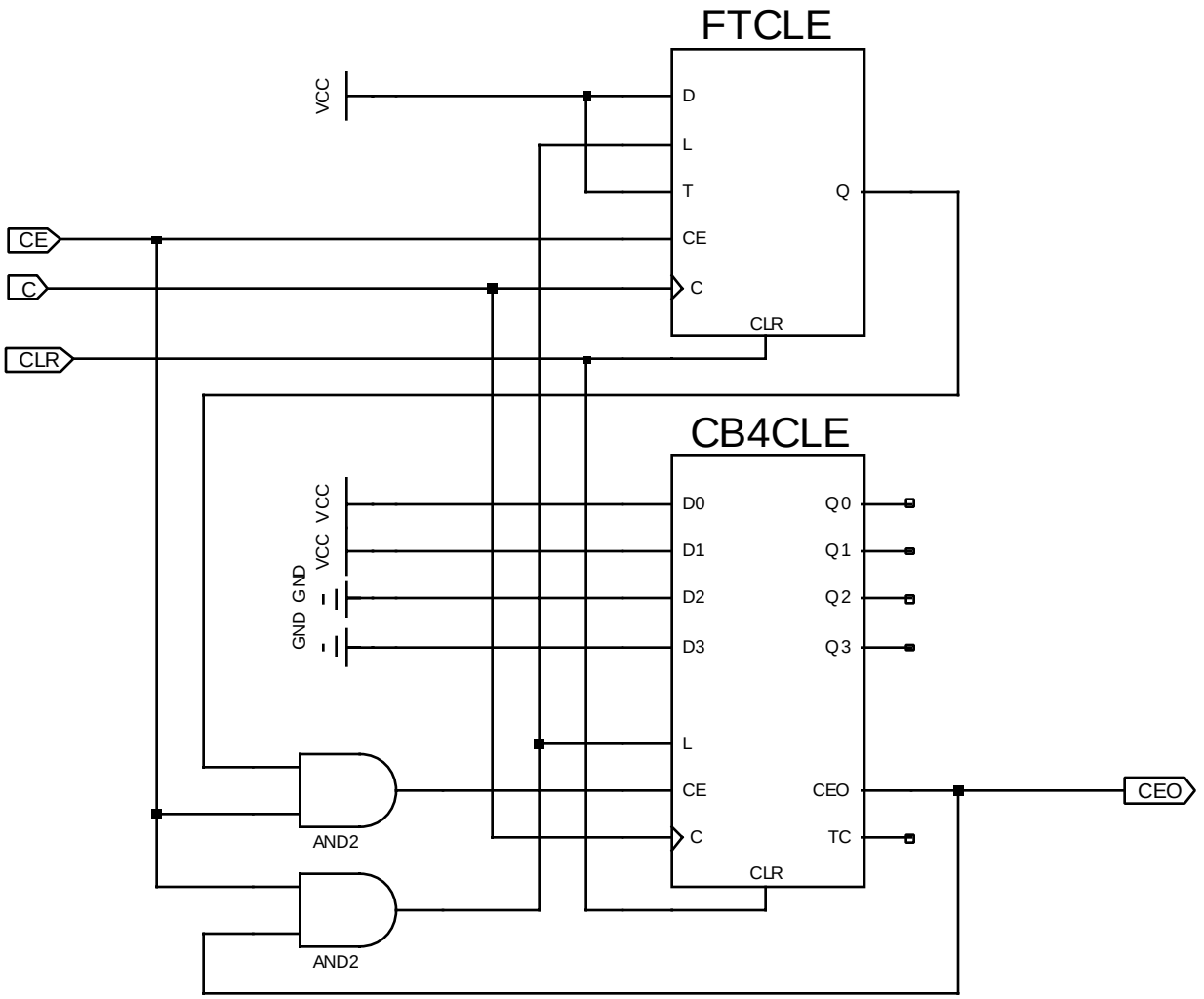
RANGE_A

2 1/2 - Decade 1/2/5/10 Counter



September 2023

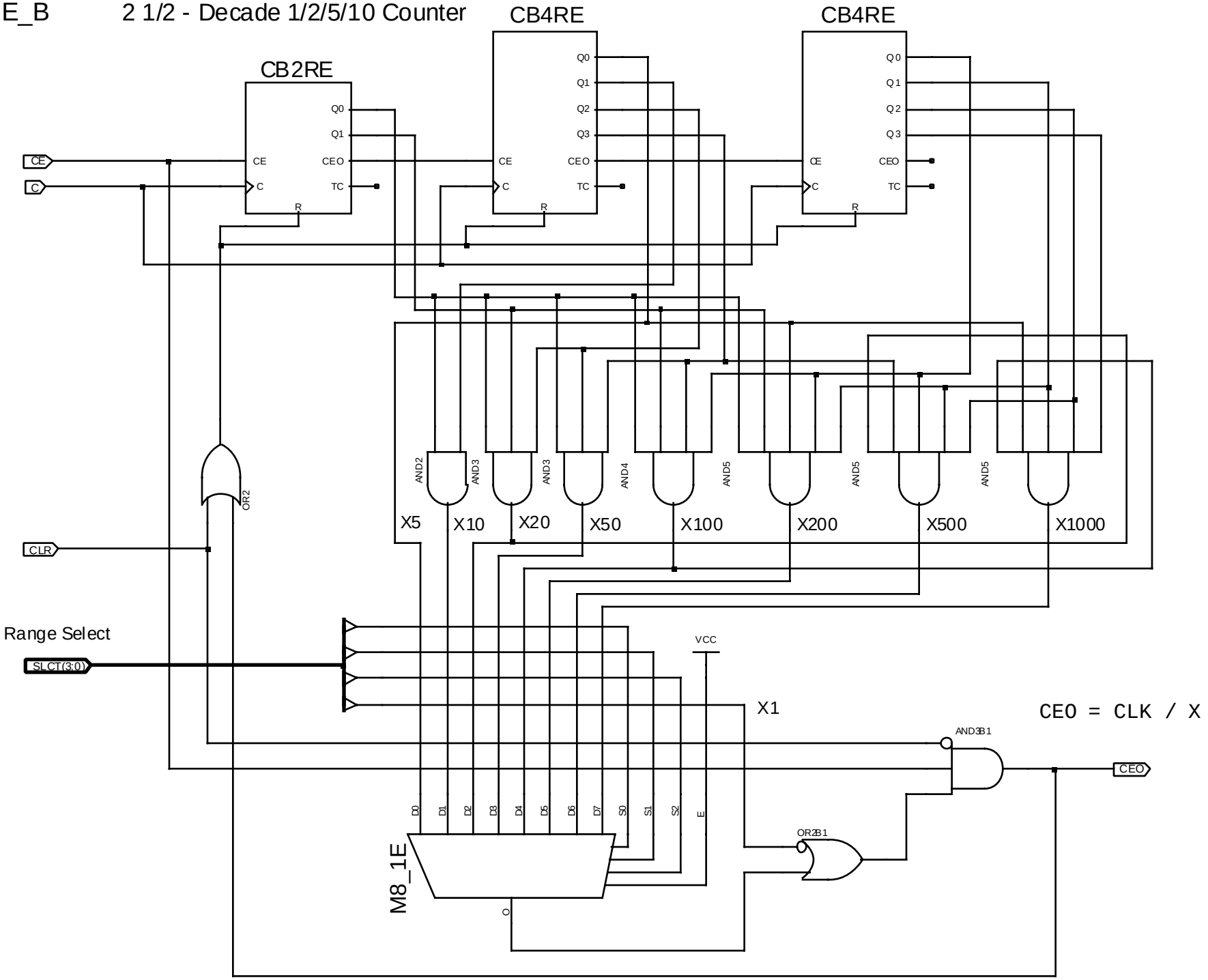
X25 Counter



September 2023

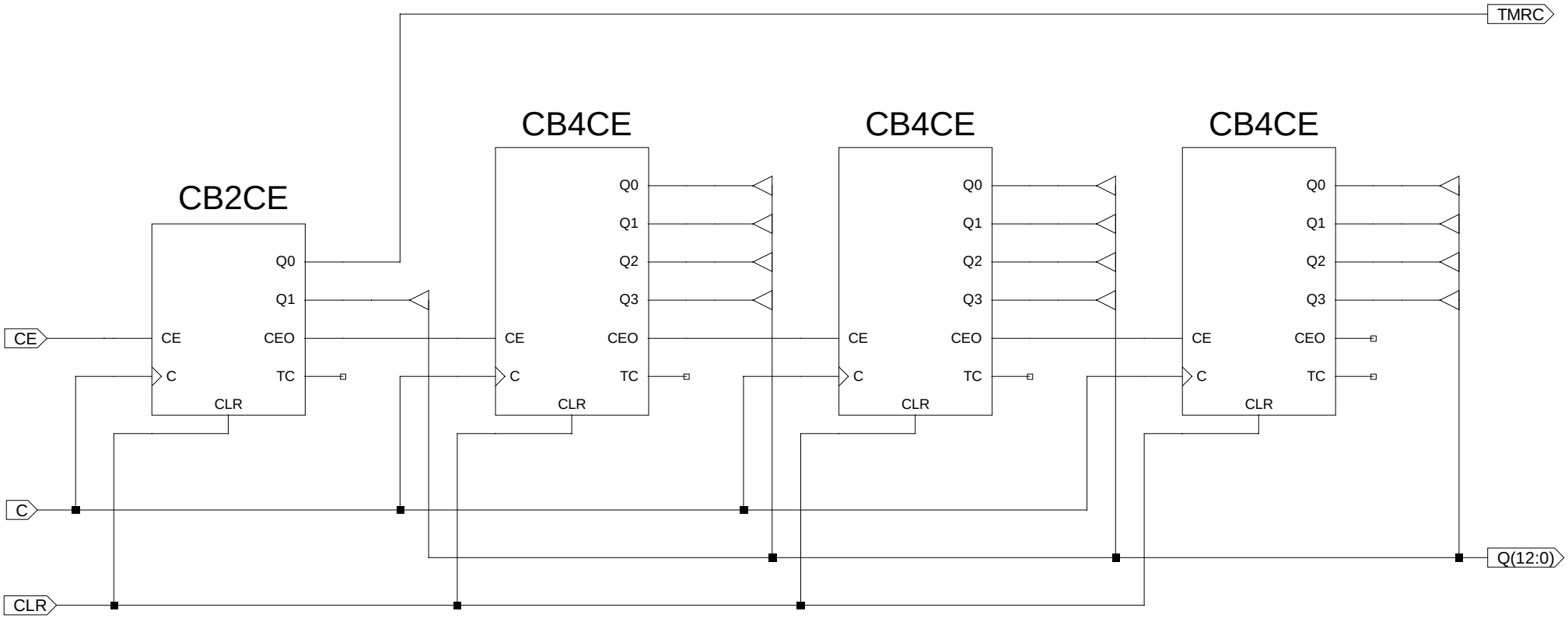
RANGE_B

2 1/2 - Decade 1/2/5/10 Counter



Septemberr 2023

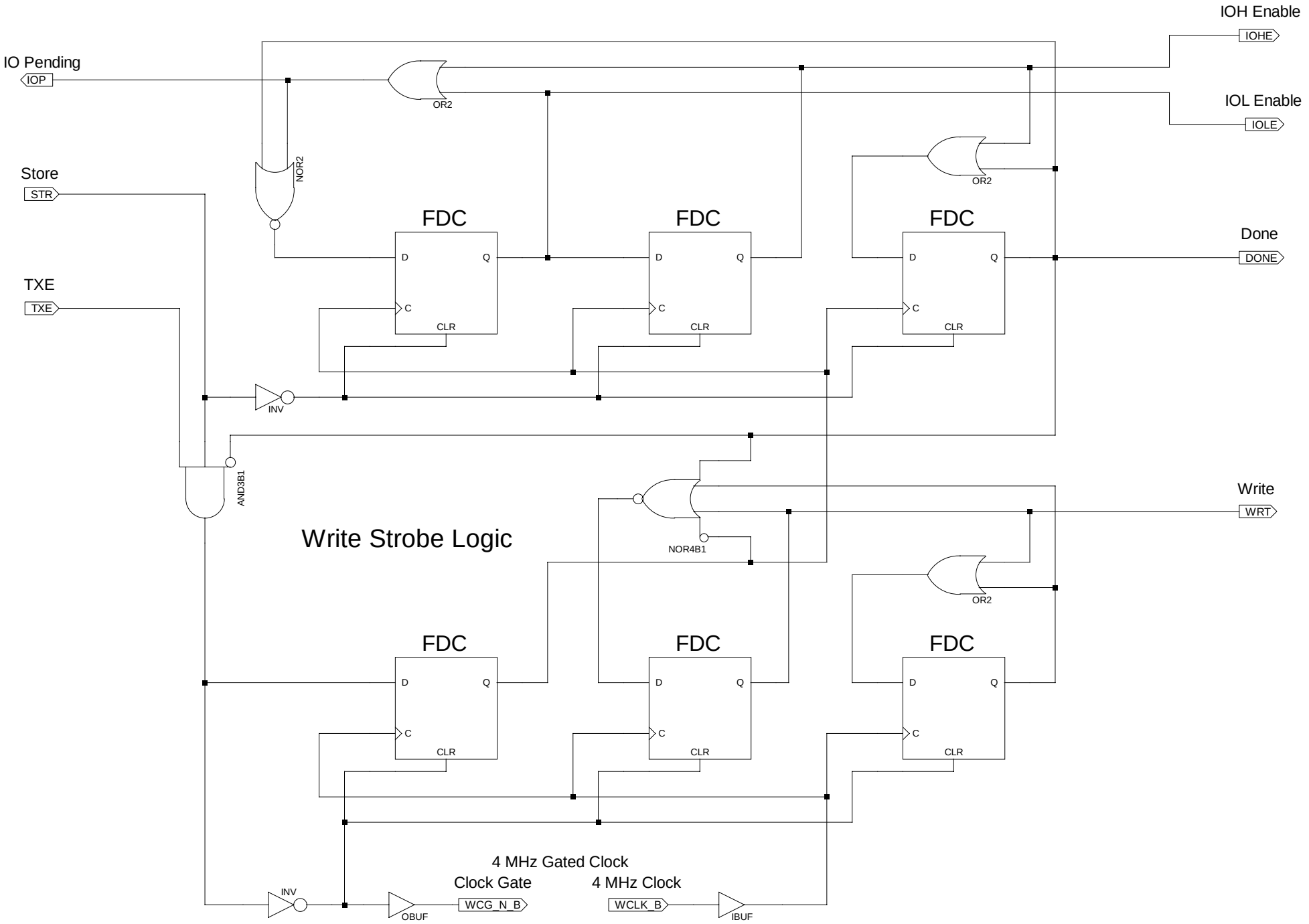
X8192 Counter



September 2023

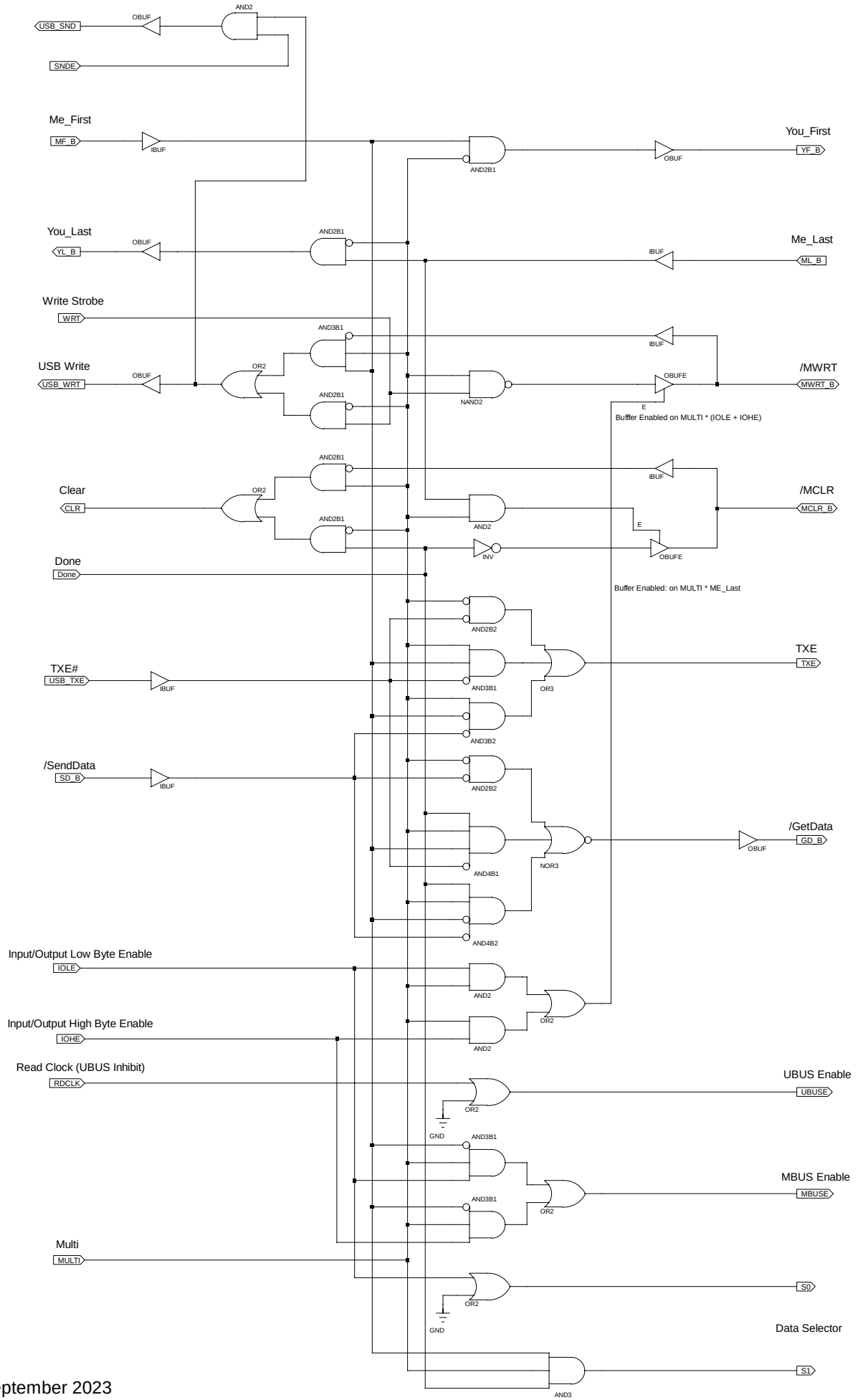
ReadOut Module

Readout Sequencer



September 2023

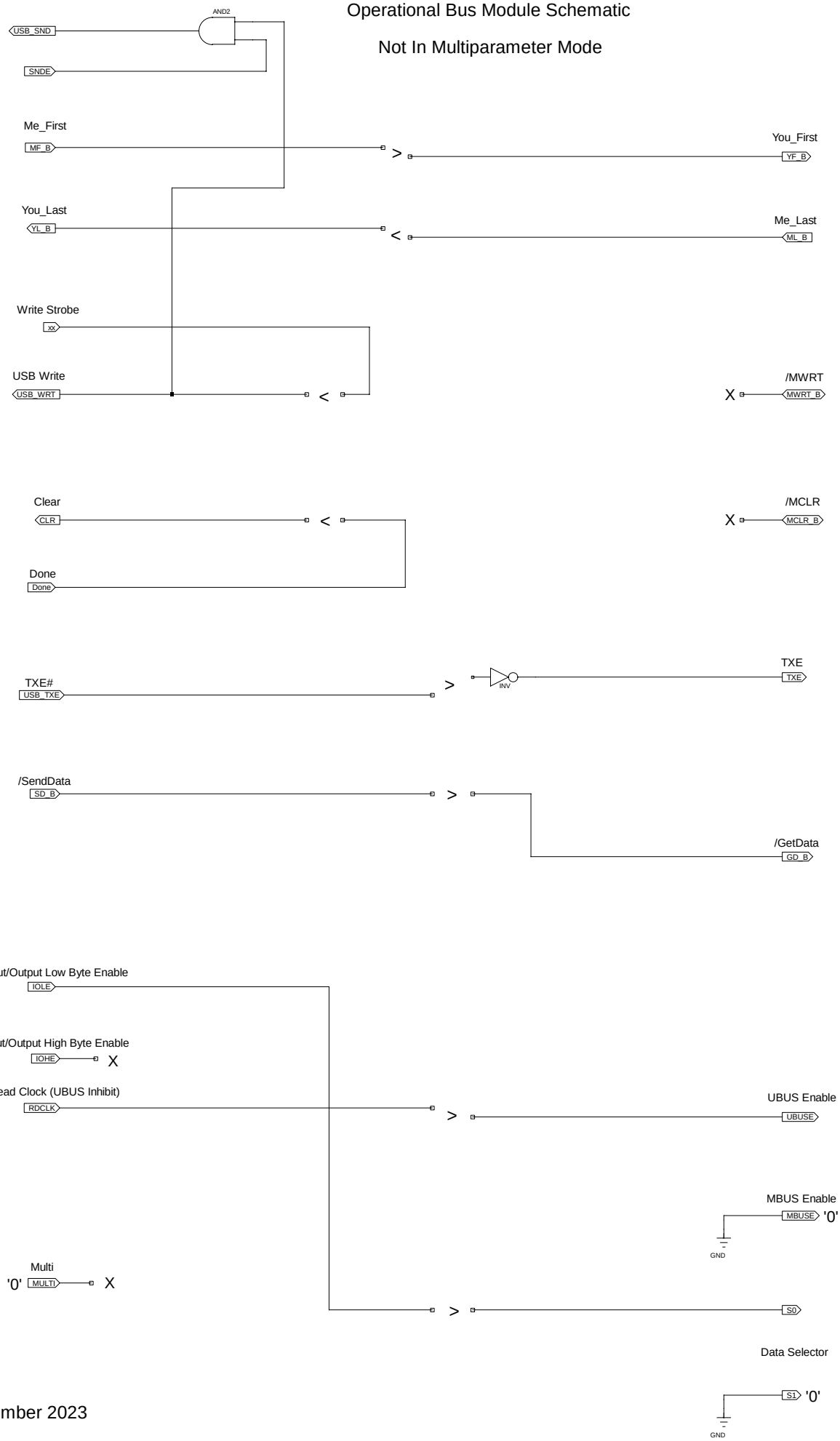
Multiple ADC/TMR Bus Control Module



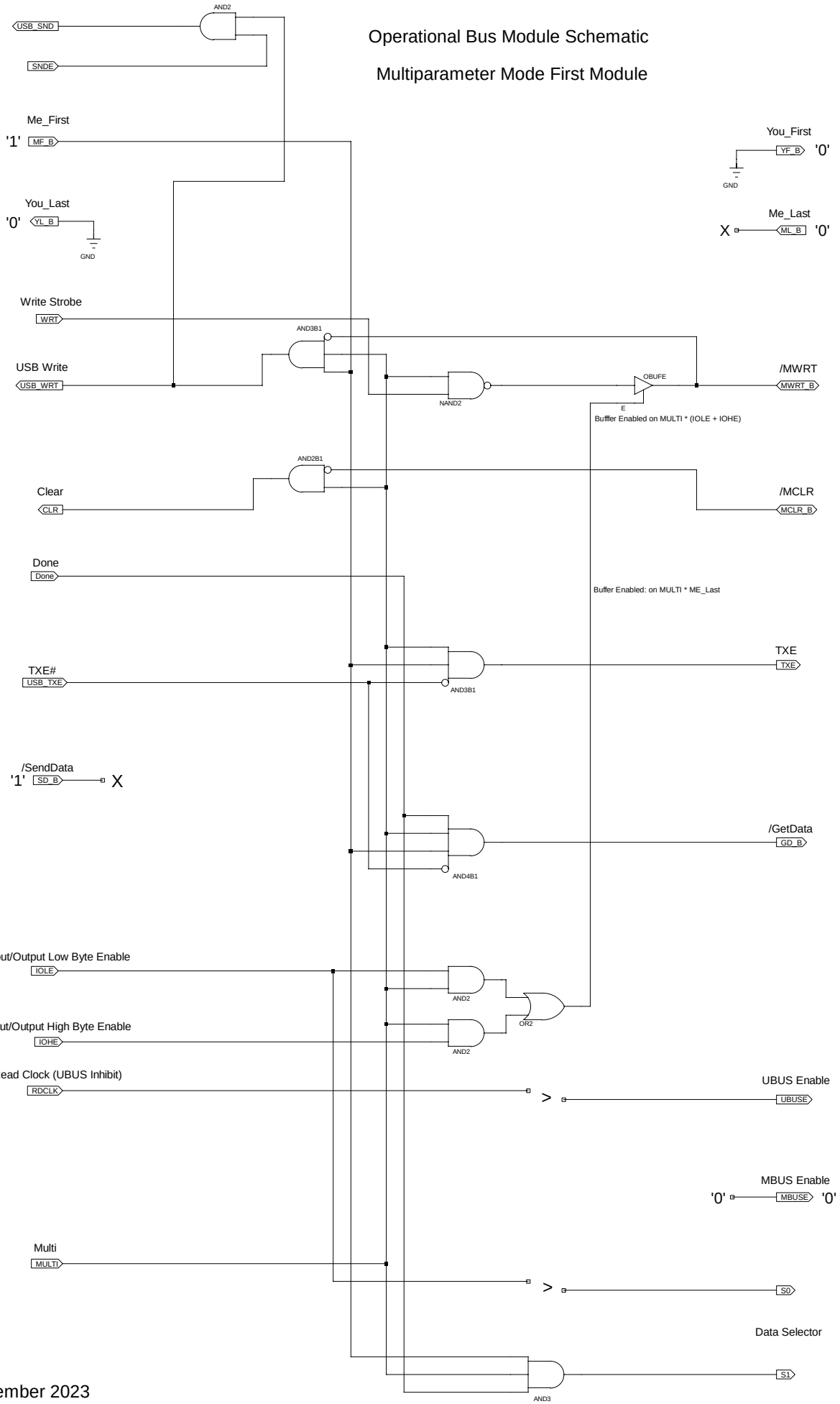
September 2023

Operational Bus Module Schematic

Not In Multiparameter Mode



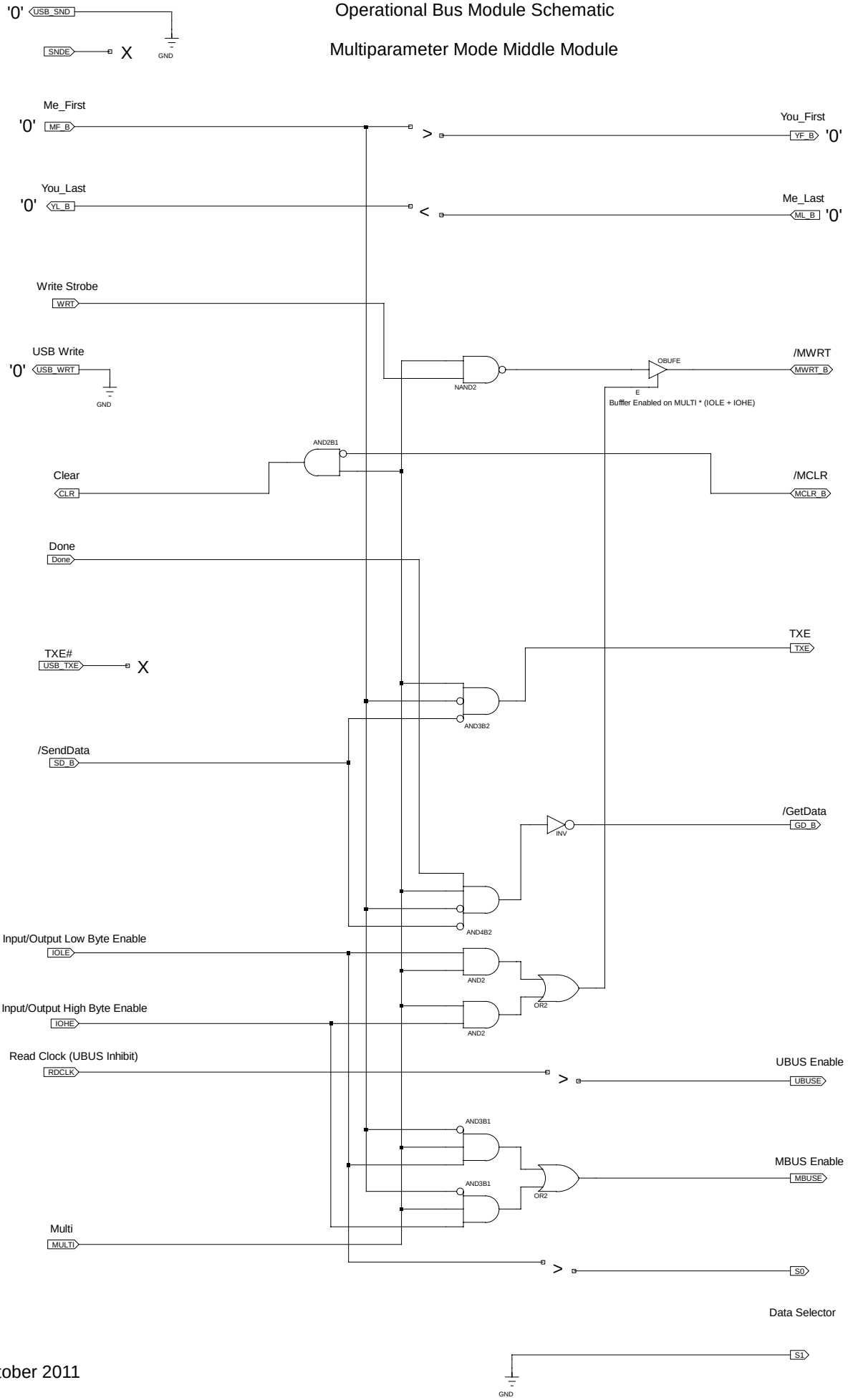
Multiple ADC/TMR Bus Control Module



September 2023

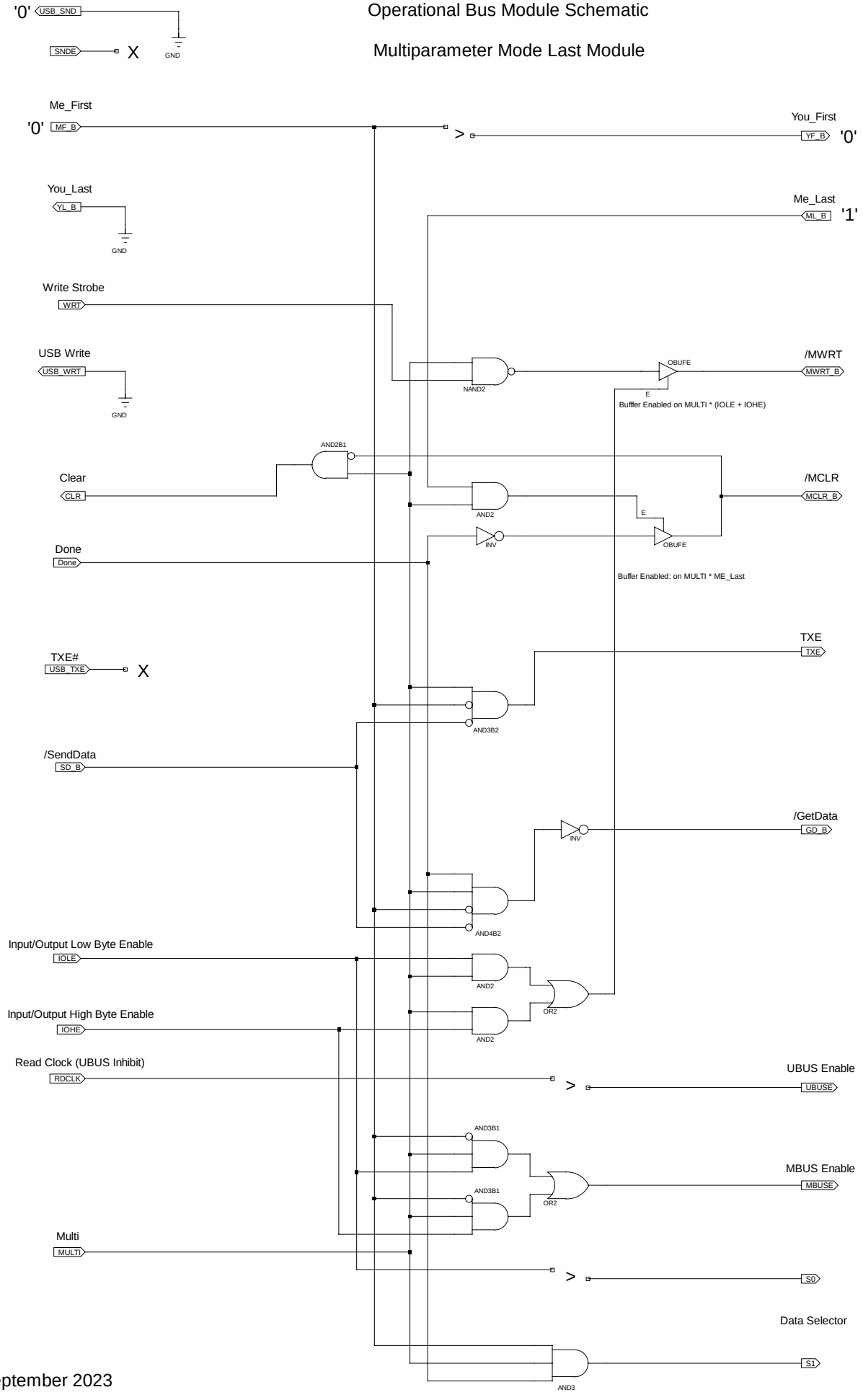
Operational Bus Module Schematic

Multiparameter Mode Middle Module



Operational Bus Module Schematic

Multiparameter Mode Last Module



```
cpldfit:  version O.40d                          Xilinx Inc.
                                Fitter Report
Design Name: USB_MCS_Timer_Multiple             Date:  9-28-2023, 11:07AM
Device Used: XC95108-15-PC84
Fitting Status: Successful

************************  Mapped Resource Summary  *************************

Macrocells     Product Terms    Function Block   Registers      Pins
Used/Tot       Used/Tot         Inps Used/Tot    Used/Tot       Used/Tot
103/108 ( 95%) 283 /540  ( 52%) 206/216 ( 95%)   59 /108 ( 55%) 55 /69  ( 80%)

** Function Block Resources **

Function    Mcells      FB Inps     Signals     Pterms      IO
Block       Used/Tot    Used/Tot    Used        Used/Tot    Used/Tot
FB1          14/18       35/36       35          38/90       6/12
FB2          18/18*      35/36       35          43/90       6/12
FB3          18/18*      31/36       31          42/90       7/12
FB4          17/18       36/36*      36          38/90       6/11
FB5          18/18*      36/36*      36          56/90       6/11
FB6          18/18*      33/36       33          66/90      10/11
             -----       -----                   -----       -----
            103/108     206/216                 283/540     41/69

* - Resource is exhausted

** Global Control Resources **

Signal 'WCLK' mapped onto global clock net GCK1.
Signal 'TCLK' mapped onto global clock net GCK2.
Signal 'RCLK' mapped onto global clock net GCK3.
Global output enable net(s) unused.
Global set/reset net(s) unused.

** Pin Resources **

Signal Type    Required     Mapped  |  Pin Type            Used    Total
------------------------------------|------------------------------------
Input         :   11          11    |  I/O              :    50      63
Output        :   23          23    |  GCK/IO           :     3       3
Bidirectional :   18          18    |  GTS/IO           :     1       2
GCK           :    3           3    |  GSR/IO           :     1       1
GTS           :    0           0    |
GSR           :    0           0    |
                 ----        ----
        Total     55          55

** Power Data **

There are 0 macrocells in high performance mode (MCHP).
There are 103 macrocells in low power mode (MCLP).
End of Mapped Resource Summary
```

********** Errors and Warnings **********

WARNING:Cpld - Unable to retrieve the path to the iSE Project Repository. Will use the default filename of 'USB_MCS_Timer_Multiple.ise'.
INFO:Cpld - Inferring BUFG constraint for signal 'RCLK' based upon the LOC constraint 'P12'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.
INFO:Cpld - Inferring BUFG constraint for signal 'TCLK' based upon the LOC constraint 'P10'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.
INFO:Cpld - Inferring BUFG constraint for signal 'WCLK' based upon the LOC constraint 'P9'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.

********** Summary of Mapped Logic **********

** 41 Outputs **

Signal Name	Total Pts	Total Inps	Loc	Pin No.	Pin Type	Pin Use	Pwr Mode	Slew Rate	Reg Init State
YF	1	2	FB1_2	1	I/O	O	LOW	SLOW	
GD_N	3	5	FB1_5	3	I/O	O	LOW	SLOW	
MWRT_N	2	3	FB1_6	4	I/O	I/O	LOW	SLOW	
MCLR_N	4	7	FB1_8	5	I/O	I/O	LOW	SLOW	SET
WCG	2	4	FB1_15	11	I/O	O	LOW	SLOW	
TCG	0	0	FB1_17	13	I/O	O	LOW	SLOW	
MBUS<2>	4	8	FB2_2	71	I/O	I/O	LOW	SLOW	
MBUS<1>	4	8	FB2_3	72	I/O	I/O	LOW	SLOW	
MBUS<0>	4	8	FB2_5	74	GSR/I/O	I/O	LOW	SLOW	
MD0	1	1	FB2_15	82	I/O	O	LOW	SLOW	
MD1	2	2	FB2_16	83	I/O	O	LOW	SLOW	
MD2	2	3	FB2_17	84	I/O	O	LOW	SLOW	
YL	1	2	FB3_2	14	I/O	O	LOW	SLOW	
WRT	2	4	FB3_11	21	I/O	O	LOW	SLOW	
UBUS<7>	2	2	FB3_12	23	I/O	I/O	LOW	SLOW	
UBUS<6>	2	2	FB3_14	24	I/O	I/O	LOW	SLOW	
UBUS<5>	2	2	FB3_15	25	I/O	I/O	LOW	SLOW	
UBUS<4>	4	6	FB3_16	26	I/O	I/O	LOW	SLOW	
UBUS<3>	4	6	FB3_17	31	I/O	I/O	LOW	SLOW	
XTMR<12>	3	16	FB4_2	57	I/O	O	LOW	SLOW	RESET
MBUS<7>	4	8	FB4_11	66	I/O	I/O	LOW	SLOW	
MBUS<6>	4	8	FB4_12	67	I/O	I/O	LOW	SLOW	
MBUS<5>	4	8	FB4_14	68	I/O	I/O	LOW	SLOW	
MBUS<4>	4	8	FB4_15	69	I/O	I/O	LOW	SLOW	
MBUS<3>	4	8	FB4_17	70	I/O	I/O	LOW	SLOW	
UBUS<2>	4	6	FB5_2	32	I/O	I/O	LOW	SLOW	
UBUS<1>	4	6	FB5_3	33	I/O	I/O	LOW	SLOW	
UBUS<0>	4	6	FB5_5	34	I/O	I/O	LOW	SLOW	
SND	2	5	FB5_6	35	I/O	O	LOW	SLOW	
XTMR<0>	3	4	FB5_15	43	I/O	O	LOW	SLOW	RESET
XTMR<1>	4	7	FB5_17	44	I/O	O	LOW	SLOW	RESET
XTMR<2>	3	6	FB6_2	45	I/O	O	LOW	SLOW	RESET
XTMR<3>	4	9	FB6_3	46	I/O	O	LOW	SLOW	RESET
XTMR<4>	4	10	FB6_5	47	I/O	O	LOW	SLOW	RESET
XTMR<5>	3	9	FB6_6	48	I/O	O	LOW	SLOW	RESET
XTMR<6>	4	5	FB6_9	51	I/O	O	LOW	SLOW	RESET
XTMR<7>	3	11	FB6_11	52	I/O	O	LOW	SLOW	RESET
XTMR<8>	3	12	FB6_12	53	I/O	O	LOW	SLOW	RESET
XTMR<9>	3	13	FB6_14	54	I/O	O	LOW	SLOW	RESET
XTMR<10>	4	5	FB6_15	55	I/O	O	LOW	SLOW	RESET

Signal Name	Total Pts	Total Inps	Loc	Pin No.	Pin Type	Pin Use	Pwr Mode	Slew Rate	Reg Init State
XTMR<11>	3	15	FB6_17	56	I/O	O	LOW	SLOW	RESET

** 62 Buried Nodes **

Signal Name	Total Pts	Total Inps	Loc	Pwr Mode	Reg Init State
XLXN_169	1	1	FB1_9	LOW	RESET
XLXN_157<3>	1	1	FB1_10	LOW	RESET
$OpTx$FX_DC$18	1	4	FB1_11	LOW	
XLXI_24/XLXI_89/XLXN_624	3	5	FB1_12	LOW	RESET
XLXI_24/XLXI_89/XLXN_621	3	5	FB1_13	LOW	RESET
XLXI_24/XLXI_89/XLXN_623	4	7	FB1_14	LOW	RESET
XLXI_24/XLXI_89/XLXN_622	4	6	FB1_16	LOW	RESET
XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2	9	16	FB1_18	LOW	
XLXN_157<2>	1	1	FB2_1	LOW	RESET
XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2	1	6	FB2_4	LOW	
XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF	1	3	FB2_6	LOW	
$OpTx$FX_DC$5	1	4	FB2_7	LOW	
$OpTx$FX_DC$25	1	2	FB2_8	LOW	
XLXI_24/XLXI_81/XLXN_370	2	4	FB2_9	LOW	RESET
$OpTx$FX_DC$27	2	4	FB2_10	LOW	
XLXI_24/XLXI_88/XLXI_109/Q3	3	7	FB2_11	LOW	RESET
XLXI_24/XLXI_88/XLXI_109/Q2	3	6	FB2_12	LOW	RESET
XLXI_24/XLXI_81/XLXN_386	3	5	FB2_13	LOW	RESET
XLXI_24/XLXI_88/XLXI_109/Q1	4	7	FB2_14	LOW	RESET
XLXI_24/XLXI_88/XLXI_109/Q0	4	6	FB2_18	LOW	RESET
XLXN_157<1>	1	1	FB3_1	LOW	RESET
XLXN_135/XLXN_135_D2	1	3	FB3_3	LOW	
XLXN_88	2	5	FB3_4	LOW	RESET
XLXI_28/XLXN_595	2	1	FB3_5	LOW	RESET
XLXI_28/XLXN_506	2	3	FB3_6	LOW	RESET
XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF	2	3	FB3_7	LOW	
XLXN_182/XLXN_182_D2	3	4	FB3_8	LOW	

XLXN_130	3	4	FB3_10	LOW	RESET
XLXI_21/XLXN_290	3	3	FB3_13	LOW	RESET
XLXI_21/XLXN_27	3	3	FB3_18	LOW	RESET
XLXN_157<0>	1	1	FB4_3	LOW	RESET
XLXN_149	1	1	FB4_4	LOW	RESET
XLXN_123	1	1	FB4_5	LOW	RESET
XLXI_24/XLXN_679	1	1	FB4_6	LOW	RESET
XLXI_24/XLXN_677	0	0	FB4_7	LOW	RESET
$OpTx$FX_DC$36	1	8	FB4_8	LOW	
$OpTx$FX_DC$34	1	12	FB4_9	LOW	
$OpTx$FX_DC$33	1	3	FB4_10	LOW	
XLXI_24/XLXN_540	2	3	FB4_13	LOW	RESET

Signal Name	Total Pts	Total Inps	Loc	Pwr Mode	Reg Init State
XLXN_171	3	3	FB4_16	LOW	RESET
XLXI_24/XLXN_545	3	4	FB4_18	LOW	RESET
XLXI_24/XLXN_678	1	1	FB5_1	LOW	RESET
XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2	1	7	FB5_4	LOW	
XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF	1	2	FB5_7	LOW	
XLXI_21/XLXN_360	2	2	FB5_8	LOW	RESET
XLXI_24/XLXI_89/XLXN_611	3	5	FB5_9	LOW	RESET
XLXI_21/XLXN_389	3	3	FB5_10	LOW	RESET
XLXI_24/XLXI_89/XLXN_630	4	6	FB5_11	LOW	RESET
XLXI_24/XLXI_89/XLXN_629	4	7	FB5_12	LOW	RESET
XLXI_24/XLXI_89/XLXN_620	4	10	FB5_13	LOW	RESET
XLXI_24/XLXI_89/XLXN_619	4	9	FB5_14	LOW	RESET
XLXI_24/XLXI_89/XLXN_618	4	8	FB5_16	LOW	RESET
XLXI_24/XLXI_88/XLXN_346	4	5	FB5_18	LOW	RESET
$OpTx$FX_DC$16	1	4	FB6_1	LOW	
XLXI_24/XLXI_81/XLXN_389	3	5	FB6_4	LOW	RESET
XLXI_24/XLXI_81/XLXN_384	3	5	FB6_7	LOW	RESET
XLXI_24/XLXI_81/XLXN_408	4	6	FB6_8	LOW	RESET
XLXI_24/XLXI_81/XLXN_392	4	7	FB6_10	LOW	RESET
XLXI_24/XLXI_81/XLXN_387	4	6	FB6_13	LOW	RESET
XLXI_24/XLXI_81/XLXN_371	4	7	FB6_16	LOW	RESET
XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2	9	13	FB6_18	LOW	

** 14 Inputs **

Signal Name	Loc	Pin No.	Pin Type	Pin Use
ML	FB1_3	2	I/O	I
SD_N	FB1_9	6	I/O	I
WCLK	FB1_12	9	GCK/I/O	GCK
TCLK	FB1_14	10	GCK/I/O	GCK
RCLK	FB1_16	12	GCK/I/O	GCK/I
COIN	FB2_9	77	GTS/I/O	I
XID<0>	FB2_11	79	I/O	I
XID<1>	FB2_12	80	I/O	I
XID<2>	FB2_14	81	I/O	I
MF	FB3_3	15	I/O	I
PD2	FB3_5	17	I/O	I
PD1	FB3_6	18	I/O	I
PD0	FB3_8	19	I/O	I
TXE_N	FB3_9	20	I/O	I

Legend:
Pin No. - ~ - User Assigned

********** Function Block Details **********

Legend:

Total Pt - Total product terms used by the macrocell signal

Imp Pt - Product terms imported from other macrocells

Exp Pt - Product terms exported to other macrocells in direction shown

Unused Pt - Unused local product terms remaining in macrocell

Loc - Location where logic was mapped in device

Pin Type/Use - I - Input; O - Output; (b) - Buried macrocell; GCK - Global Clock; GTS - Global Output Enable; GSR - Global Set/Reset

X(@) - Signal used as input (wire-AND input) to the macrocell logic. The number of Signals Used may exceed the number of FB Inputs Used due to wire-ANDing in the switch matrix.

Pin No. - ~ - User Assigned

```
********************************** FB1  **********************************
Number of function block inputs used/remaining:              35/1
Number of signals used by logic mapping into function block:  35
Signal              Total   Imp   Exp Unused  Loc     Pin   Pin     Pin
Name                Pt      Pt    Pt  Pt                #    Type    Use
(unused)              0       0     0   5     FB1_1         (b)
YF                    1       0     0   4     FB1_2   1     I/O     O
(unused)              0       0     0   5     FB1_3   2     I/O     I
(unused)              0       0     0   5     FB1_4         (b)
GD_N                  3       0     0   2     FB1_5   3     I/O     O
MWRT_N                2       0     0   3     FB1_6   4     I/O     I/O
(unused)              0       0     0   5     FB1_7         (b)
MCLR_N                4       0     0   1     FB1_8   5     I/O     I/O
XLXN_169              1       0     0   4     FB1_9   6     I/O     I
XLXN_157<3>           1       0     0   4     FB1_10        (b)     (b)
$OpTx$FX_DC$18        1       0     0   4     FB1_11  7     I/O     (b)
XLXI_24/XLXI_89/XLXN_624
                      3       0     0   2     FB1_12  9     GCK/I/O GCK
XLXI_24/XLXI_89/XLXN_621
                      3       0     0   2     FB1_13        (b)     (b)
XLXI_24/XLXI_89/XLXN_623
                      4       0     0   1     FB1_14  10    GCK/I/O GCK
WCG                   2       0     0   3     FB1_15  11    I/O     O
XLXI_24/XLXI_89/XLXN_622
                      4       0     0   1     FB1_16  12    GCK/I/O GCK/I
TCG                   0       0   \/4   1     FB1_17  13    I/O     O
XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2
                      9       4<-   0   0     FB1_18        (b)     (b)

Signals Used by Logic in Function Block
  1: $OpTx$FX_DC$18                                    13: XLXI_24/XLXI_89/XLXN_623             25: XLXN_130
  2: $OpTx$FX_DC$25                                    14: XLXI_24/XLXI_89/XLXN_624             26: XLXN_135/XLXN_
135_D2
  3: $OpTx$FX_DC$27                                    15: XLXI_24/XLXI_89/XLXN_629             27: UBUS<0>.PIN
  4: MCLR_N                                            16: XLXI_24/XLXI_89/XLXN_630             28: UBUS<7>.PIN
  5: XLXI_21/XLXN_360                                  17: XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 29: XLXN_157<0>
  6: XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2 18: XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 30: XLXN_157<1>
  7: XLXI_24/XLXI_89/XLXN_611                          19: XLXI_24/XLXN_679                     31: XLXN_157<2>
  8: XLXI_24/XLXI_89/XLXN_618                          20: XLXI_28/XLXN_595                     32: XLXN_157<3>
  9: XLXI_24/XLXI_89/XLXN_619                          21: ML                                   33: XLXN_169
 10: XLXI_24/XLXI_89/XLXN_620                          22: MF                                   34: XLXN_182/XLXN_
182_D2
 11: XLXI_24/XLXI_89/XLXN_621                          23: SD_N                                 35: XLXN_88
 12: XLXI_24/XLXI_89/XLXN_622                          24: XLXN_123

Signal                        1         2         3         4 Signals FB
Name                0----+----0----+----0----+----0----+----0 Used    Inputs
YF                   .....................X.X.............. 2       2
GD_N                 ...X..................XX.X.......X...... 5       5
MWRT_N               .X.....................X..........X..... 3       3
MCLR_N               ..XXX..............XX..XX.............. 7       7
XLXN_169             ............................X............ 1       1
XLXN_157<3>          .............................X........... 1       1
$OpTx$FX_DC$18       .....X....XXX.......................... 4       4
XLXI_24/XLXI_89/XLXN_624
                     X............X...XX.............X....... 5       5
XLXI_24/XLXI_89/XLXN_621
                     .....X....X......XX.............X....... 5       5
XLXI_24/XLXI_89/XLXN_623
                     .....X....XXX....XX.............X....... 7       7
WCG                  ..XXX............................X...... 4       4
XLXI_24/XLXI_89/XLXN_622
                     .....X....XX.....XX.............X....... 6       6
TCG                  ....................................... 0       0
XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2
                     ......XXXXXXXXXX...........XXXXX....... 16      16
                    0----+----1----+----2----+----3----+----4
                              0         0         0         0
```

```
********************************* FB2  *********************************
Number of function block inputs used/remaining:              35/1
Number of signals used by logic mapping into function block:  35
Signal              Total   Imp   Exp Unused  Loc     Pin   Pin     Pin
Name                Pt      Pt    Pt  Pt                #    Type    Use
XLXN_157<2>           1       0     0   4     FB2_1         (b)     (b)
MBUS<2>               4       0     0   1     FB2_2   71    I/O     I/O
MBUS<1>               4       0     0   1     FB2_3   72    I/O     I/O
XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2
                      1       0     0   4     FB2_4         (b)     (b)
MBUS<0>               4       0     0   1     FB2_5   74    GSR/I/O I/O
XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF
                      1       0     0   4     FB2_6   75    I/O     (b)
$OpTx$FX_DC$5         1       0     0   4     FB2_7         (b)     (b)
$OpTx$FX_DC$25        1       0     0   4     FB2_8   76    GTS/I/O (b)
XLXI_24/XLXI_81/XLXN_370
                      2       0     0   3     FB2_9   77    GTS/I/O I
$OpTx$FX_DC$27        2       0     0   3     FB2_10        (b)     (b)
XLXI_24/XLXI_88/XLXI_109/Q3
                      3       0     0   2     FB2_11  79    I/O     I
XLXI_24/XLXI_88/XLXI_109/Q2
                      3       0     0   2     FB2_12  80    I/O     I
XLXI_24/XLXI_81/XLXN_386
                      3       0     0   2     FB2_13        (b)     (b)
XLXI_24/XLXI_88/XLXI_109/Q1
                      4       0     0   1     FB2_14  81    I/O     I
MD0                   1       0     0   4     FB2_15  82    I/O     O
MD1                   2       0     0   3     FB2_16  83    I/O     O
MD2                   2       0     0   3     FB2_17  84    I/O     O
XLXI_24/XLXI_88/XLXI_109/Q0
                      4       0     0   1     FB2_18        (b)     (b)

Signals Used by Logic in Function Block
  1: $OpTx$FX_DC$25               13: XLXI_24/XLXI_88/XLXI_109/Q2           25: XLXN_130
  2: PD0                          14: XLXI_24/XLXI_88/XLXI_109/Q3           26: XLXN_131
  3: PD1                          15: XLXI_24/XLXI_88/XLXN_346              27: XLXN_135/XLXN_135_D2
  4: PD2                          16: XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2  28: UBUS<6>.PIN
  5: XLXI_21/XLXN_290             17: XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2  29: XLXN_169
  6: XLXI_21/XLXN_389             18: XLXI_24/XLXN_679                      30: XTMR<0>
  7: XLXI_24/XLXI_81/XLXN_370     19: MBUS<0>.PIN                           31: XTMR<10>
  8: XLXI_24/XLXI_81/XLXN_371     20: MBUS<1>.PIN                           32: XTMR<1>
  9: XLXI_24/XLXI_81/XLXN_386     21: MBUS<2>.PIN                           33: XTMR<2>
 10: XLXI_24/XLXI_81/XLXN_408     22: MCLR_N.PIN                            34: XTMR<8>
 11: XLXI_24/XLXI_88/XLXI_109/Q0  23: MF                                    35: XTMR<9>
 12: XLXI_24/XLXI_88/XLXI_109/Q1  24: XLXN_123

Signal                        1         2         3         4 Signals FB
Name                0----+----0----+----0----+----0----+----0 Used    Inputs
XLXN_157<2>          ..........................X............ 1       1
MBUS<2>              X...................X.XX.XX...X.X....... 8       8
MBUS<1>              X...................X..XX.XX....X..X..... 8       8
XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2
                     ..........XXXXXX....................... 6       6
MBUS<0>              X.................X...XX.XX..X...X...... 8       8
XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF
                     ......................X.X....X........... 3       3
$OpTx$FX_DC$5        ......XXXX............................. 4       4
$OpTx$FX_DC$25       ........................XX.............. 2       2
XLXI_24/XLXI_81/XLXN_370
                     ......X........X.X..........X........... 4       4
$OpTx$FX_DC$27       ....XX.................X....X........... 4       4
XLXI_24/XLXI_88/XLXI_109/Q3
                     ..........XXX.XX.X..........X........... 7       7
XLXI_24/XLXI_88/XLXI_109/Q2
                     ..........XX..XX.X..........X........... 6       6
XLXI_24/XLXI_81/XLXN_386
                     ......X.X......X.X..........X........... 5       5
XLXI_24/XLXI_88/XLXI_109/Q1
                     ..........XX..XXXX..........X........... 7       7
MD0                  .X...................................... 1       1
MD1                  .XX..................................... 2       2
MD2                  .XXX.................................... 3       3
XLXI_24/XLXI_88/XLXI_109/Q0
                     ..........X...XXXX..........X........... 6       6
                    0----+----1----+----2----+----3----+----4
                              0         0         0         0
```

********** FB3 **********

Number of function block inputs used/remaining: 31/5
Number of signals used by logic mapping into function block: 31

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
XLXN_157<1>	1	0	0	4	FB3_1		(b)	(b)
YL	1	0	0	4	FB3_2	14	I/O	O
XLXN_135/XLXN_135_D2	1	0	0	4	FB3_3	15	I/O	I
XLXN_88	2	0	0	3	FB3_4		(b)	(b)
XLXI_28/XLXN_595	2	0	0	3	FB3_5	17	I/O	I
XLXI_28/XLXN_506	2	0	0	3	FB3_6	18	I/O	I
XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF	2	0	0	3	FB3_7		(b)	(b)
XLXN_182/XLXN_182_D2	3	0	0	2	FB3_8	19	I/O	I
XLXN_131	3	0	0	2	FB3_9	20	I/O	I
XLXN_130	3	0	0	2	FB3_10		(b)	(b)
WRT	2	0	0	3	FB3_11	21	I/O	O
UBUS<7>	2	0	0	3	FB3_12	23	I/O	I/O
XLXI_21/XLXN_290	3	0	0	2	FB3_13		(b)	(b)
UBUS<6>	2	0	0	3	FB3_14	24	I/O	I/O
UBUS<5>	2	0	0	3	FB3_15	25	I/O	I/O
UBUS<4>	4	0	0	1	FB3_16	26	I/O	I/O
UBUS<3>	4	0	0	1	FB3_17	31	I/O	I/O
XLXI_21/XLXN_27	3	0	0	2	FB3_18		(b)	(b)

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$27
2: MBUS<5>
3: MBUS<6>
4: MBUS<7>
5: MCLR_N
6: WCG
7: XLXI_21/XLXN_27
8: XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF
9: COIN
10: XLXI_21/XLXN_360
11: XLXI_28/XLXN_506
12: XLXI_28/XLXN_595
13: MBUS<3>.PIN
14: MBUS<4>.PIN
15: MWRT_N.PIN
16: MCLR_N.PIN
17: ML
18: TXE_N
19: MF
20: SD_N
21: XLXN_123
22: XLXN_130
23: XLXN_131
24: XLXN_135/XLXN_135_D2
25: UBUS<5>.PIN
26: RCLK
27: XLXN_88
28: XTMR<11>
29: XTMR<12>
30: XTMR<3>
31: XTMR<4>

Signal Name	0----+----0----+----0----+----0----+----0	Signals Used	FB Inputs
XLXN_157<1>	.....X.....	1	1
YL	.....X...X.....	2	2
XLXN_135/XLXN_135_D2	....X.....X.X.....	3	3
XLXN_88	....XX....XX.....X.....	5	5
XLXI_28/XLXN_595	.....X.....	1	1
XLXI_28/XLXN_506	.....X....X.....X.....	3	3
XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF	....X.....X....X.....	3	3
XLXN_182/XLXN_182_D2	.....XXXX.....	4	4
XLXN_131	X...X....X.X.....XX.....	6	6
XLXN_130	X........X.X.....X.....	4	4
WRT	.....X...X.X.....X.....	4	4
UBUS<7>	...X.....X.....	2	2
XLXI_21/XLXN_290	......XXX.....	3	3
UBUS<6>	..X.....X.....	2	2
UBUS<5>	.X.....X.....	2	2
UBUS<4>	.....X........XX.X..X.X.....	6	6
UBUS<3>	.....X.....XX.X.X.X.....	6	6
XLXI_21/XLXN_27	.......XX.....X.....	3	3
	0----+----1----+----2----+----3----+----4		
	0 0 0 0		

********** FB4 **********

Number of function block inputs used/remaining: 36/0
Number of signals used by logic mapping into function block: 36

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
(unused)	0	0	0	5	FB4_1		(b)	
XTMR<12>	3	0	0	2	FB4_2	57	I/O	O
XLXN_157<0>	1	0	0	4	FB4_3	58	I/O	(b)
XLXN_149	1	0	0	4	FB4_4		(b)	(b)
XLXN_123	1	0	0	4	FB4_5	61	I/O	(b)
XLXI_24/XLXN_679	1	0	0	4	FB4_6	62	I/O	(b)
XLXI_24/XLXN_677	0	0	0	5	FB4_7		(b)	(b)
$OpTx$FX_DC$36	1	0	0	4	FB4_8	63	I/O	(b)
$OpTx$FX_DC$34	1	0	0	4	FB4_9	65	I/O	(b)
$OpTx$FX_DC$33	1	0	0	4	FB4_10		(b)	(b)
MBUS<7>	4	0	0	1	FB4_11	66	I/O	I/O
MBUS<6>	4	0	0	1	FB4_12	67	I/O	I/O
XLXI_24/XLXN_540	2	0	0	3	FB4_13		(b)	(b)
MBUS<5>	4	0	0	1	FB4_14	68	I/O	I/O
MBUS<4>	4	0	0	1	FB4_15	69	I/O	I/O
XLXN_171	3	0	0	2	FB4_16		(b)	(b)
MBUS<3>	4	0	0	1	FB4_17	70	I/O	I/O
XLXI_24/XLXN_545	3	0	0	2	FB4_18		(b)	(b)

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$25	13: MBUS<6>.PIN	25: XTMR<10>
2: XID<0>	14: MBUS<7>.PIN	26: XTMR<11>
3: XID<1>	15: MF	27: XTMR<12>
4: XID<2>	16: XLXN_123	28: XTMR<1>
5: XLXI_24/XLXN_540	17: XLXN_131	29: XTMR<2>
6: XLXI_24/XLXN_545	18: XLXN_135/XLXN_135_D2	30: XTMR<3>
7: XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2	19: UBUS<1>.PIN	31: XTMR<4>
8: XLXI_24/XLXN_678	20: UBUS<2>.PIN	32: XTMR<5>
9: XLXI_24/XLXN_679	21: UBUS<4>.PIN	33: XTMR<6>
10: MBUS<3>.PIN	22: XLXN_169	34: XTMR<7>
11: MBUS<4>.PIN	23: XLXN_171	35: XTMR<8>
12: MBUS<5>.PIN	24: XTMR<0>	36: XTMR<9>

Signal Name	1 0---+---0	2 0---+---0	3 0---+---0	4 0---+---0	Signals Used	FB Inputs
XTMR<12>	....X...X.	....XXXXX.	XXXXXXXXX.	...	16	16
XLXN_157<0>	.....	.....X..	.....	...	1	1
XLXN_149	.....	.....X..	.....	...	1	1
XLXN_123	.....	.....X..	.....	...	1	1
XLXI_24/XLXN_679	.....X..	.....	.....	...	1	1
XLXI_24/XLXN_677	.....	.....	.....	...	0	0
$OpTx$FX_DC$36	....X...	.....XX.	..XXXXX.	.....	8	8
$OpTx$FX_DC$34	....X...	.....XX.	..XXXXXXXX	....	12	12
$OpTx$FX_DC$33	....X...	.....XX.	.....	...	3	3
MBUS<7>	X..X....	.XXXXX..	.....	X.....	8	8
MBUS<6>	X.X.....	X.XXXX..	.....	X.....	8	8
XLXI_24/XLXN_540	X....X..	X.....	.....	...	3	3
MBUS<5>	XX.....	X..XXXX.	.....	X.....	8	8
MBUS<4>	X.....	X...XXXX	.....	X...X...	8	8
XLXN_171	....X...	X.....	.....	...	3	3
MBUS<3>	X.....	X....XXX	X.....	X...X...	8	8
XLXI_24/XLXN_545	....XXX.	X.....	.....	...	4	4

0---+---1---+---2---+---3---+---4

0 0 0 0

```
********************************* FB5  *********************************
Number of function block inputs used/remaining:              36/0
Number of signals used by logic mapping into function block:  36
Signal              Total   Imp   Exp Unused  Loc     Pin   Pin     Pin
Name                Pt      Pt    Pt  Pt                #    Type    Use
XLXI_24/XLXN_678      1       0     0   4     FB5_1         (b)     (b)
UBUS<2>               4       0     0   1     FB5_2   32    I/O     I/O
UBUS<1>               4       0     0   1     FB5_3   33    I/O     I/O
XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2
                      1       0     0   4     FB5_4         (b)     (b)
UBUS<0>               4       0     0   1     FB5_5   34    I/O     I/O
SND                   2       0     0   3     FB5_6   35    I/O     O
XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF
                      1       0     0   4     FB5_7         (b)     (b)
XLXI_21/XLXN_360      2       0     0   3     FB5_8   36    I/O     (b)
XLXI_24/XLXI_89/XLXN_611
                      3       0     0   2     FB5_9   37    I/O     (b)
XLXI_21/XLXN_389      3       0     0   2     FB5_10        (b)     (b)
XLXI_24/XLXI_89/XLXN_630
                      4       0     0   1     FB5_11  39    I/O     (b)
XLXI_24/XLXI_89/XLXN_629
                      4       0     0   1     FB5_12  40    I/O     (b)
XLXI_24/XLXI_89/XLXN_620
                      4       0     0   1     FB5_13        (b)     (b)
XLXI_24/XLXI_89/XLXN_619
                      4       0     0   1     FB5_14  41    I/O     (b)
XTMR<0>               3       0     0   2     FB5_15  43    I/O     O
XLXI_24/XLXI_89/XLXN_618
                      4       0     0   1     FB5_16        (b)     (b)
XTMR<1>               4       0     0   1     FB5_17  44    I/O     O
XLXI_24/XLXI_88/XLXN_346
                      4       0     0   1     FB5_18        (b)     (b)

Signals Used by Logic in Function Block
  1: $OpTx$FX_DC$33                          13: XLXI_24/XLXN_540                       25: UBUS<3>.PIN
  2: XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF  14: XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2  26: XLXN_149
  3: XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF  15: XLXI_24/XLXN_677                       27: RCLK
  4: XLXI_24/XLXI_88/XLXN_346                16: XLXI_24/XLXN_679                       28: XLXN_169
  5: XLXI_24/XLXI_89/XLXN_611                17: MBUS<0>.PIN                            29: XLXN_171
  6: XLXI_24/XLXI_89/XLXN_618                18: MBUS<1>.PIN                            30: XLXN_88
  7: XLXI_24/XLXI_89/XLXN_619                19: MBUS<2>.PIN                            31: XTMR<0>
  8: XLXI_24/XLXI_89/XLXN_620                20: MWRT_N.PIN                             32: XTMR<10>
  9: XLXI_24/XLXI_89/XLXN_629                21: MF                                     33: XTMR<1>
 10: XLXI_24/XLXI_89/XLXN_630                22: XLXN_123                               34: XTMR<2>
 11: XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2    23: XLXN_131                               35: XTMR<8>
 12: XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2    24: XLXN_135/XLXN_135_D2                   36: XTMR<9>

Signal                        1         2         3         4 Signals FB
Name                0----+----0----+----0----+----0----+----0 Used    Inputs
XLXI_24/XLXN_678     ..............X..........................  1       1
UBUS<2>              ..................X...XX..X....X.X......  6       6
UBUS<1>              ..................X....XX..X.....X..X....  6       6
XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2
                     ....XXXXXX.X...........................  7       7
UBUS<0>              ................X.....XX..X...X...X.....  6       6
SND                  ...................XXX...X...X..........  5       5
XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF
                     .X........................X............  2       2
XLXI_21/XLXN_360     .X......................X..............  2       2
XLXI_24/XLXI_89/XLXN_611
                     ....X......X.X.X...........X............  5       5
XLXI_21/XLXN_389     ..X........................XX...........  3       3
XLXI_24/XLXI_89/XLXN_630
                     ....X....X.X.X.X...........X............  6       6
XLXI_24/XLXI_89/XLXN_629
                     ....X...XX.X.X.X...........X............  7       7
XLXI_24/XLXI_89/XLXN_620
                     ....XXXXXX.X.X.X...........X............ 10      10
XLXI_24/XLXI_89/XLXN_619
                     ....XXX.XX.X.X.X...........X............  9       9
XTMR<0>              ............X..X...........XX...........  4       4
XLXI_24/XLXI_89/XLXN_618
                     ....XX..XX.X.X.X...........X............  8       8
XTMR<1>              X...........X..X...........XX.X.X.......  7       7
XLXI_24/XLXI_88/XLXN_346
                     ...X......XX...X...........X............  5       5
                    0----+----1----+----2----+----3----+----4
                              0         0         0         0
```

```
********************************* FB6  *********************************
Number of function block inputs used/remaining:              33/3
Number of signals used by logic mapping into function block:  33
Signal              Total   Imp   Exp Unused  Loc     Pin   Pin     Pin
Name                Pt      Pt    Pt  Pt                #    Type    Use
$OpTx$FX_DC$16        1       0   /\2   2     FB6_1         (b)     (b)
XTMR<2>               3       0     0   2     FB6_2   45    I/O     O
XTMR<3>               4       0     0   1     FB6_3   46    I/O     O
XLXI_24/XLXI_81/XLXN_389
                      3       0     0   2     FB6_4         (b)     (b)
XTMR<4>               4       0     0   1     FB6_5   47    I/O     O
XTMR<5>               3       0     0   2     FB6_6   48    I/O     O
XLXI_24/XLXI_81/XLXN_384
                      3       0     0   2     FB6_7         (b)     (b)
XLXI_24/XLXI_81/XLXN_408
                      4       0     0   1     FB6_8   50    I/O     (b)
XTMR<6>               4       0     0   1     FB6_9   51    I/O     O
XLXI_24/XLXI_81/XLXN_392
                      4       0     0   1     FB6_10        (b)     (b)
XTMR<7>               3       0     0   2     FB6_11  52    I/O     O
XTMR<8>               3       0     0   2     FB6_12  53    I/O     O
XLXI_24/XLXI_81/XLXN_387
                      4       0     0   1     FB6_13        (b)     (b)
XTMR<9>               3       0     0   2     FB6_14  54    I/O     O
XTMR<10>              4       0     0   1     FB6_15  55    I/O     O
XLXI_24/XLXI_81/XLXN_371
                      4       0     0   1     FB6_16        (b)     (b)
XTMR<11>              3       0   \/2   0     FB6_17  56    I/O     O
XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2
                      9       4<-   0   0     FB6_18        (b)     (b)

Signals Used by Logic in Function Block
  1: $OpTx$FX_DC$16            12: XLXI_24/XLXI_81/XLXN_392             23: XTMR<0>
  2: $OpTx$FX_DC$33            13: XLXI_24/XLXI_81/XLXN_408             24: XTMR<10>
  3: $OpTx$FX_DC$34            14: XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 25: XTMR<1>
  4: $OpTx$FX_DC$36            15: XLXI_24/XLXN_540                     26: XTMR<2>
  5: $OpTx$FX_DC$5             16: XLXI_24/XLXN_679                     27: XTMR<3>
  6: XLXI_24/XLXI_81/XLXN_370  17: XLXN_157<0>                          28: XTMR<4>
  7: XLXI_24/XLXI_81/XLXN_371  18: XLXN_157<1>                          29: XTMR<5>
  8: XLXI_24/XLXI_81/XLXN_384  19: XLXN_157<2>                          30: XTMR<6>
  9: XLXI_24/XLXI_81/XLXN_386  20: XLXN_157<3>                          31: XTMR<7>
 10: XLXI_24/XLXI_81/XLXN_387  21: XLXN_169                             32: XTMR<8>
 11: XLXI_24/XLXI_81/XLXN_389  22: XLXN_171                             33: XTMR<9>

Signal                        1         2         3         4 Signals FB
Name                0----+----0----+----0----+----0----+----0 Used    Inputs
$OpTx$FX_DC$16       ....X..X.X.X.............................. 4       4
XTMR<2>              ..............XX....XXX.X................ 6       6
XTMR<3>              .X............XX....XXX.XXX.............. 9       9
XLXI_24/XLXI_81/XLXN_389
                     X.........X..X.X....X.................... 5       5
XTMR<4>              .X............XX....XXX.XXXX............ 10      10
XTMR<5>              ..............XX....XXX.XXXX............ 9       9
XLXI_24/XLXI_81/XLXN_384
                     ....X..X.....X.X....X.................... 5       5
XLXI_24/XLXI_81/XLXN_408
                     .....X..X...XX.X....X.................... 6       6
XTMR<6>              ...X...........X....X.......XX.......... 5       5
XLXI_24/XLXI_81/XLXN_392
                     ....X..X.X.X.X.X....X.................... 7       7
XTMR<7>              ..............XX....XXX.XXXXXX.......... 11      11
XTMR<8>              ..............XX....XXX.XXXXXXX......... 12      12
XLXI_24/XLXI_81/XLXN_387
                     ....X..X.X...X.X....X.................... 6       6
XTMR<9>              ..............XX....XXX.XXXXXXXX........ 13      13
XTMR<10>             ..X............X....X..X........X....... 5       5
XLXI_24/XLXI_81/XLXN_371
                     .....XX.X...XX.X....X.................... 7       7
XTMR<11>             ..............XX....XXXXXXXXXXXXX....... 15      15
XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2
                     .....XXXXXXXX...XXXXX.................... 13      13
                    0----+----1----+----2----+----3----+----4
                              0         0         0         0
```

```
*****************************  Equations  ******************************

********** Mapped Logic **********


$OpTx$FX_DC$16 <= (XLXI_24/XLXI_81/XLXN_384 AND
        XLXI_24/XLXI_81/XLXN_387 AND XLXI_24/XLXI_81/XLXN_392 AND $OpTx$FX_DC$5);


$OpTx$FX_DC$18 <= (XLXI_24/XLXI_89/XLXN_621 AND
        XLXI_24/XLXI_89/XLXN_622 AND XLXI_24/XLXI_89/XLXN_623 AND
        XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2);


$OpTx$FX_DC$25 <= (NOT XLXN_131 AND NOT XLXN_130);


$OpTx$FX_DC$27 <= ((XLXI_21/XLXN_290 AND XLXN_169 AND XLXN_123)
        OR (XLXI_21/XLXN_389 AND XLXN_169 AND NOT XLXN_123));


$OpTx$FX_DC$33 <= (XTMR(0) AND XLXN_171 AND XLXI_24/XLXN_540);


$OpTx$FX_DC$34 <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(9) AND XTMR(3) AND XTMR(7) AND XTMR(0) AND XTMR(4) AND
        XTMR(8) AND XLXN_171 AND XLXI_24/XLXN_540);


$OpTx$FX_DC$36 <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(3) AND
        XTMR(0) AND XTMR(4) AND XLXN_171 AND XLXI_24/XLXN_540);


$OpTx$FX_DC$5 <= (XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_386 AND XLXI_24/XLXI_81/XLXN_408 AND
        XLXI_24/XLXI_81/XLXN_371);


GD_N <= ((MCLR_N AND XLXN_123)
        OR (SD_N AND NOT XLXN_135/XLXN_135_D2)
        OR (XLXN_135/XLXN_135_D2 AND NOT XLXN_182/XLXN_182_D2));


MBUS_I(0) <= NOT (((NOT XTMR(0) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(8) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(0).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(0) <= MBUS_I(0) when MBUS_OE(0) = '1' else 'Z';
MBUS_OE(0) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(1) <= NOT (((NOT XTMR(1) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(9) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(1).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(1) <= MBUS_I(1) when MBUS_OE(1) = '1' else 'Z';
MBUS_OE(1) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(2) <= NOT (((NOT XTMR(2) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(10) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(2).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(2) <= MBUS_I(2) when MBUS_OE(2) = '1' else 'Z';
MBUS_OE(2) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(3) <= NOT (((NOT XTMR(3) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(11) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(3).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(3) <= MBUS_I(3) when MBUS_OE(3) = '1' else 'Z';
MBUS_OE(3) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(4) <= NOT (((NOT XTMR(4) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(12) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(4).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(4) <= MBUS_I(4) when MBUS_OE(4) = '1' else 'Z';
MBUS_OE(4) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(5) <= NOT (((NOT XTMR(5) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT XID(0) AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(5).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(5) <= MBUS_I(5) when MBUS_OE(5) = '1' else 'Z';
```

```
MBUS_I(6) <= NOT (((NOT XTMR(6) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT XID(1) AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(6).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(6) <= MBUS_I(6) when MBUS_OE(6) = '1' else 'Z';
MBUS_OE(6) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);


MBUS_I(7) <= NOT (((NOT XTMR(7) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT XID(2) AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(7).PIN AND XLXN_135/XLXN_135_D2)));
MBUS(7) <= MBUS_I(7) when MBUS_OE(7) = '1' else 'Z';
MBUS_OE(7) <= (NOT MF AND XLXN_123 AND NOT $OpTx$FX_DC$25);

FDCPE_MCLR_N: FDCPE port map (MCLR_N_I,MCLR_N,XLXI_28/XLXN_595,'0',MCLR_N_PRE);
MCLR_N <= (MCLR_N AND NOT XLXN_130);
MCLR_N_PRE <= (NOT XLXI_21/XLXN_360 AND NOT $OpTx$FX_DC$27);
MCLR_N <= MCLR_N_I when MCLR_N_OE = '1' else 'Z';
MCLR_N_OE <= (XLXN_123 AND ML);


MD0 <= NOT PD0;


MD1 <= PD0
         XOR
MD1 <= PD1;


MD2 <= PD2
         XOR
MD2 <= (PD1 AND PD0);


MWRT_N_I <= NOT ((XLXN_88 AND XLXN_123));
MWRT_N <= MWRT_N_I when MWRT_N_OE = '1' else 'Z';
MWRT_N_OE <= (XLXN_123 AND NOT $OpTx$FX_DC$25);


SND <= ((XLXN_88 AND NOT XLXN_123 AND XLXN_149)
        OR (MF AND NOT MWRT_N.PIN AND XLXN_123 AND XLXN_149));


TCG <= '1';


UBUS_I(0) <= NOT (((NOT XTMR(0) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(8) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(0).PIN AND XLXN_135/XLXN_135_D2)));
UBUS(0) <= UBUS_I(0) when UBUS_OE(0) = '1' else 'Z';
UBUS_OE(0) <= RCLK;


UBUS_I(1) <= NOT (((NOT XTMR(1) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(9) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(1).PIN AND XLXN_135/XLXN_135_D2)));
UBUS(1) <= UBUS_I(1) when UBUS_OE(1) = '1' else 'Z';
UBUS_OE(1) <= RCLK;


UBUS_I(2) <= NOT (((NOT XTMR(2) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(10) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(2).PIN AND XLXN_135/XLXN_135_D2)));
UBUS(2) <= UBUS_I(2) when UBUS_OE(2) = '1' else 'Z';
UBUS_OE(2) <= RCLK;


UBUS_I(3) <= NOT (((NOT XTMR(3) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(11) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(3).PIN AND XLXN_135/XLXN_135_D2)));
UBUS(3) <= UBUS_I(3) when UBUS_OE(3) = '1' else 'Z';
UBUS_OE(3) <= RCLK;


UBUS_I(4) <= NOT (((NOT XTMR(4) AND XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XTMR(12) AND NOT XLXN_131 AND NOT XLXN_135/XLXN_135_D2)
        OR (NOT XLXN_131 AND NOT MBUS(4).PIN AND XLXN_135/XLXN_135_D2)));
UBUS(4) <= UBUS_I(4) when UBUS_OE(4) = '1' else 'Z';
UBUS_OE(4) <= RCLK;
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UBUS_I(5) <= MBUS(5);
UBUS(5) <= UBUS_I(5) when UBUS_OE(5) = '1' else 'Z';
UBUS_OE(5) <= RCLK;


UBUS_I(6) <= MBUS(6);
UBUS(6) <= UBUS_I(6) when UBUS_OE(6) = '1' else 'Z';
UBUS_OE(6) <= RCLK;


UBUS_I(7) <= MBUS(7);
UBUS(7) <= UBUS_I(7) when UBUS_OE(7) = '1' else 'Z';
UBUS_OE(7) <= RCLK;


WCG <= NOT (((MCLR_N AND XLXI_21/XLXN_360 AND XLXN_182/XLXN_182_D2)
        OR (MCLR_N AND $OpTx$FX_DC$27 AND XLXN_182/XLXN_182_D2)));


WRT <= ((XLXN_88 AND NOT XLXN_123)
        OR (MF AND NOT MWRT_N.PIN AND XLXN_123));

FDCPE_XLXI_21/XLXN_27: FDCPE port map (XLXI_21/XLXN_27,XLXN_123,COIN,NOT XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF,'0');


XLXI_21/XLXN_27/XLXI_21/XLXN_27_RSTF <= (XLXN_169 AND XLXN_123 AND MCLR_N.PIN);

FDCPE_XLXI_21/XLXN_290: FDCPE port map (XLXI_21/XLXN_290,XLXI_21/XLXN_27,NOT COIN,NOT XLXI_21/XLXN_27/XLXI_21/XLXN_27_R
STF,'0');

FDCPE_XLXI_21/XLXN_360: FDCPE port map (XLXI_21/XLXN_360,UBUS(3).PIN,RCLK,XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF,'0');


XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF <= ((NOT MCLR_N AND NOT XLXN_123)
        OR (XLXN_123 AND NOT MCLR_N.PIN));

FDCPE_XLXI_21/XLXN_389: FDCPE port map (XLXI_21/XLXN_389,XLXN_169,XLXN_171,NOT XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF,'
0');


XLXI_21/XLXN_389/XLXI_21/XLXN_389_RSTF <= (XLXN_169 AND NOT XLXI_21/XLXN_360/XLXI_21/XLXN_360_RSTF);

FDCPE_XLXI_24/XLXI_81/XLXN_370: FDCPE port map (XLXI_24/XLXI_81/XLXN_370,XLXI_24/XLXI_81/XLXN_370_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_370_D <= (XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_370 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2);

FTCPE_XLXI_24/XLXI_81/XLXN_371: FTCPE port map (XLXI_24/XLXI_81/XLXN_371,XLXI_24/XLXI_81/XLXN_371_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_371_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_81/XLXN_371)
        OR (XLXI_24/XLXI_81/XLXN_371 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_386 AND XLXI_24/XLXI_81/XLXN_408 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2));

FDCPE_XLXI_24/XLXI_81/XLXN_384: FDCPE port map (XLXI_24/XLXI_81/XLXN_384,XLXI_24/XLXI_81/XLXN_384_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_384_D <= ((XLXN_169 AND XLXI_24/XLXI_81/XLXN_384 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND NOT $OpTx$FX_DC$5)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_384 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND $OpTx$FX_DC$5));

FDCPE_XLXI_24/XLXI_81/XLXN_386: FDCPE port map (XLXI_24/XLXI_81/XLXN_386,XLXI_24/XLXI_81/XLXN_386_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_386_D <= ((XLXN_169 AND XLXI_24/XLXI_81/XLXN_370 AND
        NOT XLXI_24/XLXI_81/XLXN_386 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_386 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2));

FDCPE_XLXI_24/XLXI_81/XLXN_387: FDCPE port map (XLXI_24/XLXI_81/XLXN_387,XLXI_24/XLXI_81/XLXN_387_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_387_D <= ((XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_384 AND
        XLXI_24/XLXI_81/XLXN_387 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_387 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND NOT $OpTx$FX_DC$5)
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_384 AND
        NOT XLXI_24/XLXI_81/XLXN_387 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND
        $OpTx$FX_DC$5));

FDCPE_XLXI_24/XLXI_81/XLXN_389: FDCPE port map (XLXI_24/XLXI_81/XLXN_389,XLXI_24/XLXI_81/XLXN_389_D,XLXI_24/XLXN_679,'0
','0');
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XLXI_24/XLXI_81/XLXN_389_D <= ((XLXN_169 AND XLXI_24/XLXI_81/XLXN_389 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND NOT $OpTx$FX_DC$16)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_389 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND $OpTx$FX_DC$16));

FTCPE_XLXI_24/XLXI_81/XLXN_392: FTCPE port map (XLXI_24/XLXI_81/XLXN_392,XLXI_24/XLXI_81/XLXN_392_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_392_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_81/XLXN_392)
        OR (XLXI_24/XLXI_81/XLXN_392 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_384 AND
        XLXI_24/XLXI_81/XLXN_387 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND
        $OpTx$FX_DC$5));

FDCPE_XLXI_24/XLXI_81/XLXN_408: FDCPE port map (XLXI_24/XLXI_81/XLXN_408,XLXI_24/XLXI_81/XLXN_408_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_81/XLXN_408_D <= ((XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_408 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_81/XLXN_386 AND
        XLXI_24/XLXI_81/XLXN_408 AND NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_386 AND NOT XLXI_24/XLXI_81/XLXN_408 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2));

FTCPE_XLXI_24/XLXI_88/XLXI_109/Q0: FTCPE port map (XLXI_24/XLXI_88/XLXI_109/Q0,XLXI_24/XLXI_88/XLXI_109/Q0_T,XLXI_24/XL
XN_679,NOT XLXN_169,'0');
XLXI_24/XLXI_88/XLXI_109/Q0_T <= ((NOT XLXI_24/XLXI_88/XLXI_109/Q0 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXI_24/XLXI_88/XLXN_346 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND NOT XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2));

FTCPE_XLXI_24/XLXI_88/XLXI_109/Q1: FTCPE port map (XLXI_24/XLXI_88/XLXI_109/Q1,XLXI_24/XLXI_88/XLXI_109/Q1_T,XLXI_24/XL
XN_679,NOT XLXN_169,'0');
XLXI_24/XLXI_88/XLXI_109/Q1_T <= ((NOT XLXI_24/XLXI_88/XLXI_109/Q1 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXI_24/XLXI_88/XLXI_109/Q0 AND
        XLXI_24/XLXI_88/XLXN_346 AND XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND
        NOT XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2));

FTCPE_XLXI_24/XLXI_88/XLXI_109/Q2: FTCPE port map (XLXI_24/XLXI_88/XLXI_109/Q2,XLXI_24/XLXI_88/XLXI_109/Q2_T,XLXI_24/XL
XN_679,NOT XLXN_169,'0');
XLXI_24/XLXI_88/XLXI_109/Q2_T <= (XLXI_24/XLXI_88/XLXI_109/Q0 AND
        XLXI_24/XLXI_88/XLXI_109/Q1 AND XLXI_24/XLXI_88/XLXN_346 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2);

FTCPE_XLXI_24/XLXI_88/XLXI_109/Q3: FTCPE port map (XLXI_24/XLXI_88/XLXI_109/Q3,XLXI_24/XLXI_88/XLXI_109/Q3_T,XLXI_24/XL
XN_679,NOT XLXN_169,'0');
XLXI_24/XLXI_88/XLXI_109/Q3_T <= (XLXI_24/XLXI_88/XLXI_109/Q0 AND
        XLXI_24/XLXI_88/XLXI_109/Q1 AND XLXI_24/XLXI_88/XLXI_109/Q2 AND
        XLXI_24/XLXI_88/XLXN_346 AND XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2);

FDCPE_XLXI_24/XLXI_88/XLXN_346: FDCPE port map (XLXI_24/XLXI_88/XLXN_346,XLXI_24/XLXI_88/XLXN_346_D,XLXI_24/XLXN_679,NO
T XLXN_169,'0');
XLXI_24/XLXI_88/XLXN_346_D <= ((NOT XLXI_24/XLXI_88/XLXN_346 AND
        NOT XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2)
        OR (XLXI_24/XLXI_88/XLXN_346 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 AND NOT XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2));


XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2 <= (XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_629 AND XLXI_24/XLXI_89/XLXN_618 AND
        XLXI_24/XLXI_89/XLXN_619 AND XLXI_24/XLXI_89/XLXN_620 AND
        XLXI_24/XLXI_89/XLXN_630 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2);

FDCPE_XLXI_24/XLXI_89/XLXN_611: FDCPE port map (XLXI_24/XLXI_89/XLXN_611,XLXI_24/XLXI_89/XLXN_611_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_611_D <= ((XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        NOT XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));

FTCPE_XLXI_24/XLXI_89/XLXN_618: FTCPE port map (XLXI_24/XLXI_89/XLXN_618,XLXI_24/XLXI_89/XLXN_618_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_618_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_89/XLXN_618)
        OR (XLXI_24/XLXI_89/XLXN_618 AND
        XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_629 AND XLXI_24/XLXI_89/XLXN_630 AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));
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FTCPE_XLXI_24/XLXI_89/XLXN_619: FTCPE port map (XLXI_24/XLXI_89/XLXN_619,XLXI_24/XLXI_89/XLXN_619_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_619_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_89/XLXN_619)
        OR (XLXI_24/XLXI_89/XLXN_619 AND
        XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_629 AND XLXI_24/XLXI_89/XLXN_618 AND
        XLXI_24/XLXI_89/XLXN_630 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));

FTCPE_XLXI_24/XLXI_89/XLXN_620: FTCPE port map (XLXI_24/XLXI_89/XLXN_620,XLXI_24/XLXI_89/XLXN_620_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_620_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_89/XLXN_620)
        OR (XLXI_24/XLXI_89/XLXN_620 AND
        XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_629 AND XLXI_24/XLXI_89/XLXN_618 AND
        XLXI_24/XLXI_89/XLXN_619 AND XLXI_24/XLXI_89/XLXN_630 AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));

FDCPE_XLXI_24/XLXI_89/XLXN_621: FDCPE port map (XLXI_24/XLXI_89/XLXN_621,XLXI_24/XLXI_89/XLXN_621_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_621_D <= ((XLXN_169 AND XLXI_24/XLXI_89/XLXN_621 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND
        NOT XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_89/XLXN_621 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND
        XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2));

FDCPE_XLXI_24/XLXI_89/XLXN_622: FDCPE port map (XLXI_24/XLXI_89/XLXN_622,XLXI_24/XLXI_89/XLXN_622_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_622_D <= ((XLXN_169 AND NOT XLXI_24/XLXI_89/XLXN_621 AND
        XLXI_24/XLXI_89/XLXN_622 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_622 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND
        NOT XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_621 AND
        NOT XLXI_24/XLXI_89/XLXN_622 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND
        XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2));

FTCPE_XLXI_24/XLXI_89/XLXN_623: FTCPE port map (XLXI_24/XLXI_89/XLXN_623,XLXI_24/XLXI_89/XLXN_623_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_623_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_89/XLXN_623)
        OR (XLXI_24/XLXI_89/XLXN_623 AND
        XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_621 AND
        XLXI_24/XLXI_89/XLXN_622 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND
        XLXI_24/XLXI_89/XLXN_542/XLXI_24/XLXI_89/XLXN_542_D2));

FDCPE_XLXI_24/XLXI_89/XLXN_624: FDCPE port map (XLXI_24/XLXI_89/XLXN_624,XLXI_24/XLXI_89/XLXN_624_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_624_D <= ((XLXN_169 AND XLXI_24/XLXI_89/XLXN_624 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND NOT $OpTx$FX_DC$18)
        OR (XLXN_169 AND NOT XLXI_24/XLXI_89/XLXN_624 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 AND $OpTx$FX_DC$18));

FTCPE_XLXI_24/XLXI_89/XLXN_629: FTCPE port map (XLXI_24/XLXI_89/XLXN_629,XLXI_24/XLXI_89/XLXN_629_T,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_629_T <= ((NOT XLXN_169 AND XLXI_24/XLXI_89/XLXN_629)
        OR (XLXI_24/XLXI_89/XLXN_629 AND
        XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_630 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));

FDCPE_XLXI_24/XLXI_89/XLXN_630: FDCPE port map (XLXI_24/XLXI_89/XLXN_630,XLXI_24/XLXI_89/XLXN_630_D,XLXI_24/XLXN_679,'0
','0');
XLXI_24/XLXI_89/XLXN_630_D <= ((XLXN_169 AND NOT XLXI_24/XLXI_89/XLXN_611 AND
        XLXI_24/XLXI_89/XLXN_630 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_630 AND
        NOT XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2)
        OR (XLXN_169 AND XLXI_24/XLXI_89/XLXN_611 AND
        NOT XLXI_24/XLXI_89/XLXN_630 AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2));


XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2 <= ((XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_370 AND XLXN_157(1) AND XLXI_24/XLXI_81/XLXN_386 AND
        XLXI_24/XLXI_81/XLXN_387 AND XLXI_24/XLXI_81/XLXN_392 AND XLXN_157(2))
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_370 AND XLXN_157(1) AND XLXI_24/XLXI_81/XLXN_386 AND
        XLXI_24/XLXI_81/XLXN_392 AND XLXI_24/XLXI_81/XLXN_408 AND XLXN_157(2) AND
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        XLXI_24/XLXI_81/XLXN_389 AND NOT XLXN_157(3))
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_370 AND NOT XLXN_157(1) AND XLXI_24/XLXI_81/XLXN_384 AND
        XLXI_24/XLXI_81/XLXN_387 AND NOT XLXN_157(3))
        OR (XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_370 AND NOT XLXN_157(1) AND XLXI_24/XLXI_81/XLXN_384 AND
        XLXI_24/XLXI_81/XLXN_386 AND NOT XLXN_157(3))
        OR (XLXN_169 AND NOT XLXN_157(0) AND NOT XLXN_157(1) AND
        NOT XLXN_157(2) AND NOT XLXN_157(3))
        OR (XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_408 AND NOT XLXN_157(2) AND NOT XLXN_157(3))
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_370 AND
        NOT XLXN_157(1) AND NOT XLXN_157(2) AND NOT XLXN_157(3))
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_81/XLXN_370 AND NOT XLXN_157(2) AND XLXI_24/XLXI_81/XLXN_371 AND
        NOT XLXN_157(3))
        OR (XLXN_169 AND XLXI_24/XLXI_81/XLXN_370 AND
        XLXI_24/XLXI_81/XLXN_386 AND XLXI_24/XLXI_81/XLXN_387 AND
        XLXI_24/XLXI_81/XLXN_392 AND XLXN_157(3)));


XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2 <= (XLXI_24/XLXI_88/XLXI_109/Q0 AND
        XLXI_24/XLXI_88/XLXI_109/Q1 AND XLXI_24/XLXI_88/XLXI_109/Q2 AND
        XLXI_24/XLXI_88/XLXI_109/Q3 AND XLXI_24/XLXI_88/XLXN_346 AND
        XLXI_24/XLXN_516/XLXI_24/XLXN_516_D2);

FDCPE_XLXI_24/XLXN_540: FDCPE port map (XLXI_24/XLXN_540,XLXI_24/XLXN_540_D,XLXI_24/XLXN_679,'0','0');
XLXI_24/XLXN_540_D <= (XLXI_24/XLXN_545 AND $OpTx$FX_DC$25);

FDCPE_XLXI_24/XLXN_545: FDCPE port map (XLXI_24/XLXN_545,XLXI_24/XLXN_545_D,XLXI_24/XLXN_679,XLXI_24/XLXN_540,'0');
XLXI_24/XLXN_545_D <= (NOT XLXI_24/XLXN_545 AND
        NOT XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2);


XLXI_24/XLXN_574/XLXI_24/XLXN_574_D2 <= ((XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXI_24/XLXI_89/XLXN_621 AND NOT XLXN_157(1) AND
        XLXI_24/XLXI_89/XLXN_620 AND XLXI_24/XLXI_89/XLXN_630 AND XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXI_24/XLXI_89/XLXN_629 AND
        XLXI_24/XLXI_89/XLXN_621 AND NOT XLXN_157(1) AND XLXI_24/XLXI_89/XLXN_622 AND
        XLXI_24/XLXI_89/XLXN_630 AND XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXI_24/XLXI_89/XLXN_621 AND
        XLXI_24/XLXI_89/XLXN_622 AND XLXI_24/XLXI_89/XLXN_619 AND
        XLXI_24/XLXI_89/XLXN_620 AND XLXI_24/XLXI_89/XLXN_630 AND
        XLXI_24/XLXI_89/XLXN_623 AND XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXI_24/XLXI_89/XLXN_629 AND
        XLXI_24/XLXI_89/XLXN_621 AND XLXI_24/XLXI_89/XLXN_622 AND
        XLXI_24/XLXI_89/XLXN_620 AND XLXI_24/XLXI_89/XLXN_630 AND
        XLXI_24/XLXI_89/XLXN_623 AND XLXN_157(2) AND XLXI_24/XLXI_89/XLXN_624 AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND NOT XLXN_157(3) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_629 AND NOT XLXN_157(1) AND NOT XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND NOT XLXN_157(1) AND XLXI_24/XLXI_89/XLXN_618 AND
        NOT XLXN_157(2) AND XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXN_157(1) AND XLXI_24/XLXI_89/XLXN_619 AND
        XLXI_24/XLXI_89/XLXN_620 AND NOT XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2)
        OR (XLXN_169 AND NOT XLXN_157(0) AND
        XLXI_24/XLXI_89/XLXN_611 AND XLXN_157(1) AND XLXI_24/XLXI_89/XLXN_619 AND
        XLXI_24/XLXI_89/XLXN_630 AND NOT XLXN_157(2) AND
        XLXI_24/XLXN_517/XLXI_24/XLXN_517_D2));

FTCPE_XLXI_24/XLXN_677: FTCPE port map (XLXI_24/XLXN_677,'1',TCLK,'0','0');

FTCPE_XLXI_24/XLXN_678: FTCPE port map (XLXI_24/XLXN_678,'1',XLXI_24/XLXN_677,'0','0');

FTCPE_XLXI_24/XLXN_679: FTCPE port map (XLXI_24/XLXN_679,'1',XLXI_24/XLXN_678,'0','0');

FDCPE_XLXI_28/XLXN_506: FDCPE port map (XLXI_28/XLXN_506,XLXI_28/XLXN_506_D,WCLK,WCG,'0');
XLXI_28/XLXN_506_D <= (NOT XLXN_88 AND NOT XLXI_28/XLXN_506);

FDCPE_XLXI_28/XLXN_595: FDCPE port map (XLXI_28/XLXN_595,NOT WCG,WCLK,WCG,'0');
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FDCPE_XLXN_123: FDCPE port map (XLXN_123,UBUS(2).PIN,RCLK,'0','0');

FDCPE_XLXN_130: FDCPE port map (XLXN_130,XLXN_131,XLXI_28/XLXN_595,XLXN_130_CLR,'0');
XLXN_130_CLR <= (NOT XLXI_21/XLXN_360 AND NOT $OpTx$FX_DC$27);

FDCPE_XLXN_131: FDCPE port map (XLXN_131,XLXN_131_D,XLXI_28/XLXN_595,XLXN_131_CLR,'0');
XLXN_131_D <= (MCLR_N AND NOT XLXN_131 AND NOT XLXN_130);
XLXN_131_CLR <= (NOT XLXI_21/XLXN_360 AND NOT $OpTx$FX_DC$27);


XLXN_135/XLXN_135_D2 <= (NOT MCLR_N AND MF AND XLXN_123);

FDCPE_XLXN_149: FDCPE port map (XLXN_149,UBUS(1).PIN,RCLK,'0','0');

FDCPE_XLXN_1570: FDCPE port map (XLXN_157(0),UBUS(4).PIN,RCLK,'0','0');

FDCPE_XLXN_1571: FDCPE port map (XLXN_157(1),UBUS(5).PIN,RCLK,'0','0');

FDCPE_XLXN_1572: FDCPE port map (XLXN_157(2),UBUS(6).PIN,RCLK,'0','0');

FDCPE_XLXN_1573: FDCPE port map (XLXN_157(3),UBUS(7).PIN,RCLK,'0','0');

FDCPE_XLXN_169: FDCPE port map (XLXN_169,UBUS(0).PIN,RCLK,'0','0');

FTCPE_XLXN_171: FTCPE port map (XLXN_171,XLXI_24/XLXN_540,XLXI_24/XLXN_679,NOT XLXN_169,'0');


XLXN_182/XLXN_182_D2 <= ((MF AND NOT TXE_N)
        OR (NOT TXE_N AND NOT XLXN_123)
        OR (NOT MF AND NOT SD_N AND XLXN_123));

FDCPE_XLXN_88: FDCPE port map (XLXN_88,XLXN_88_D,WCLK,WCG,'0');
XLXN_88_D <= (MCLR_N AND NOT XLXN_88 AND NOT XLXI_28/XLXN_506 AND
        XLXI_28/XLXN_595);

FTCPE_XTMR0: FTCPE port map (XTMR(0),XTMR_T(0),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(0) <= (XLXN_171 AND XLXI_24/XLXN_540);

FDCPE_XTMR1: FDCPE port map (XTMR(1),XTMR_D(1),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_D(1) <= ((NOT XTMR(1) AND NOT $OpTx$FX_DC$33)
        OR (XTMR(1) AND XTMR(0) AND XLXN_171 AND XLXI_24/XLXN_540));

FTCPE_XTMR2: FTCPE port map (XTMR(2),XTMR_T(2),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(2) <= (XTMR(1) AND XTMR(0) AND XLXN_171 AND XLXI_24/XLXN_540);

FTCPE_XTMR3: FTCPE port map (XTMR(3),XTMR_T(3),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(3) <= ((XTMR(1) AND XTMR(2) AND NOT XTMR(3) AND $OpTx$FX_DC$33)
        OR (XTMR(1) AND XTMR(2) AND XTMR(3) AND XTMR(0) AND
        XLXN_171 AND XLXI_24/XLXN_540));

FTCPE_XTMR4: FTCPE port map (XTMR(4),XTMR_T(4),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(4) <= ((XTMR(1) AND XTMR(2) AND XTMR(3) AND NOT XTMR(4) AND
        $OpTx$FX_DC$33)
        OR (XTMR(1) AND XTMR(2) AND XTMR(3) AND XTMR(0) AND
        XTMR(4) AND XLXN_171 AND XLXI_24/XLXN_540));

FTCPE_XTMR5: FTCPE port map (XTMR(5),XTMR_T(5),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(5) <= (XTMR(1) AND XTMR(2) AND XTMR(3) AND XTMR(0) AND
        XTMR(4) AND XLXN_171 AND XLXI_24/XLXN_540);

FDCPE_XTMR6: FDCPE port map (XTMR(6),XTMR_D(6),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_D(6) <= ((NOT XTMR(6) AND NOT $OpTx$FX_DC$36)
        OR (XTMR(5) AND XTMR(6) AND $OpTx$FX_DC$36));

FTCPE_XTMR7: FTCPE port map (XTMR(7),XTMR_T(7),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(7) <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(3) AND XTMR(0) AND XTMR(4) AND XLXN_171 AND XLXI_24/XLXN_540);

FTCPE_XTMR8: FTCPE port map (XTMR(8),XTMR_T(8),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(8) <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(3) AND XTMR(7) AND XTMR(0) AND XTMR(4) AND XLXN_171 AND
        XLXI_24/XLXN_540);

FTCPE_XTMR9: FTCPE port map (XTMR(9),XTMR_T(9),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(9) <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(3) AND XTMR(7) AND XTMR(0) AND XTMR(4) AND XTMR(8) AND
        XLXN_171 AND XLXI_24/XLXN_540);

FDCPE_XTMR10: FDCPE port map (XTMR(10),XTMR_D(10),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_D(10) <= ((NOT XTMR(10) AND NOT $OpTx$FX_DC$34)
        OR (XTMR(9) AND XTMR(10) AND $OpTx$FX_DC$34));
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FTCPE_XTMR11: FTCPE port map (XTMR(11),XTMR_T(11),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(11) <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(9) AND XTMR(10) AND XTMR(3) AND XTMR(7) AND XTMR(0) AND
        XTMR(4) AND XTMR(8) AND XLXN_171 AND XLXI_24/XLXN_540);

FTCPE_XTMR12: FTCPE port map (XTMR(12),XTMR_T(12),XLXI_24/XLXN_679,NOT XLXN_169,'0');
XTMR_T(12) <= (XTMR(1) AND XTMR(5) AND XTMR(2) AND XTMR(6) AND
        XTMR(9) AND XTMR(10) AND XTMR(3) AND XTMR(7) AND XTMR(0) AND
        XTMR(11) AND XTMR(4) AND XTMR(8) AND XLXN_171 AND XLXI_24/XLXN_540);

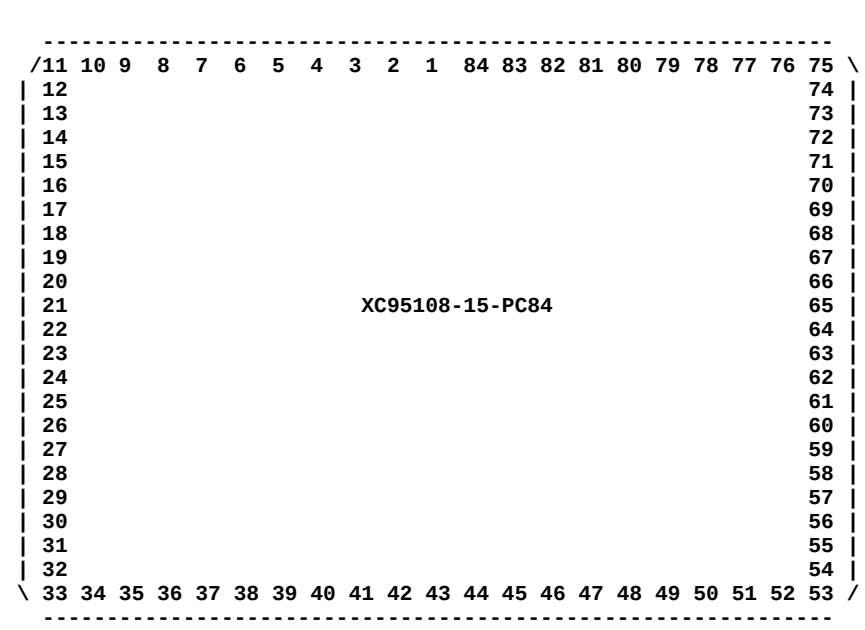

YF <= (MF AND NOT XLXN_123);


YL <= (NOT XLXN_123 AND ML);

Register Legend:
 FDCPE (Q,D,C,CLR,PRE);
 FTCPE (Q,D,C,CLR,PRE);
 LDCP  (Q,D,G,CLR,PRE);
```

********** Device Pin Out **********

Device : XC95108-15-PC84



Pin No.	Signal Name	Pin No.	Signal Name
1	YF	43	XTMR<0>
2	ML	44	XTMR<1>
3	GD_N	45	XTMR<2>
4	MWRT_N	46	XTMR<3>
5	MCLR_N	47	XTMR<4>
6	SD_N	48	XTMR<5>
7	PGND	49	GND
8	GND	50	PGND
9	WCLK	51	XTMR<6>
10	TCLK	52	XTMR<7>
11	WCG	53	XTMR<8>
12	RCLK	54	XTMR<9>
13	TCG	55	XTMR<10>
14	YL	56	XTMR<11>
15	MF	57	XTMR<12>
16	GND	58	PGND
17	PD2	59	TDO
18	PD1	60	GND
19	PD0	61	PGND
20	TXE_N	62	PGND
21	WRT	63	PGND
22	VCC	64	VCC
23	UBUS<7>	65	PGND
24	UBUS<6>	66	MBUS<7>
25	UBUS<5>	67	MBUS<6>
26	UBUS<4>	68	MBUS<5>
27	GND	69	MBUS<4>
28	TDI	70	MBUS<3>
29	TMS	71	MBUS<2>
30	TCK	72	MBUS<1>
31	UBUS<3>	73	VCC
32	UBUS<2>	74	MBUS<0>
33	UBUS<1>	75	PGND
34	UBUS<0>	76	PGND
35	SND	77	COIN
36	PGND	78	VCC
37	PGND	79	XID<0>
38	VCC	80	XID<1>
39	PGND	81	XID<2>
40	PGND	82	MD0
41	PGND	83	MD1
42	GND	84	MD2

Legend : NC = Not Connected, unbonded pin
PGND = Unused I/O configured as additional Ground pin
TIE = Unused I/O floating -- must tie to VCC, GND or other signal
VCC = Dedicated Power Pin

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        TDI  = Test Data In, JTAG pin
        TDO  = Test Data Out, JTAG pin
        TCK  = Test Clock, JTAG pin
        TMS  = Test Mode Select, JTAG pin
 PROHIBITED  = User reserved pin
```

********** Compiler Options **********

Following is a list of all global compiler options used by the fitter run.

Device(s) Specified	: xc95108-15-PC84
Optimization Method	: DENSITY
Multi-Level Logic Optimization	: ON
Ignore Timing Specifications	: OFF
Default Register Power Up Value	: LOW
Keep User Location Constraints	: ON
What-You-See-Is-What-You-Get	: OFF
Exhaustive Fitting	: OFF
Keep Unused Inputs	: OFF
Slew Rate	: SLOW
Power Mode	: LOW
Ground on Unused IOs	: ON
Global Clock Optimization	: ON
Global Set/Reset Optimization	: ON
Global Ouput Enable Optimization	: ON
FASTConnect/UIM optimzation	: ON
Local Feedback	: OFF
Pin Feedback	: OFF
Input Limit	: 36
Pterm Limit	: 90