Multiparameter IO Module

ADC

Revisions & Operation

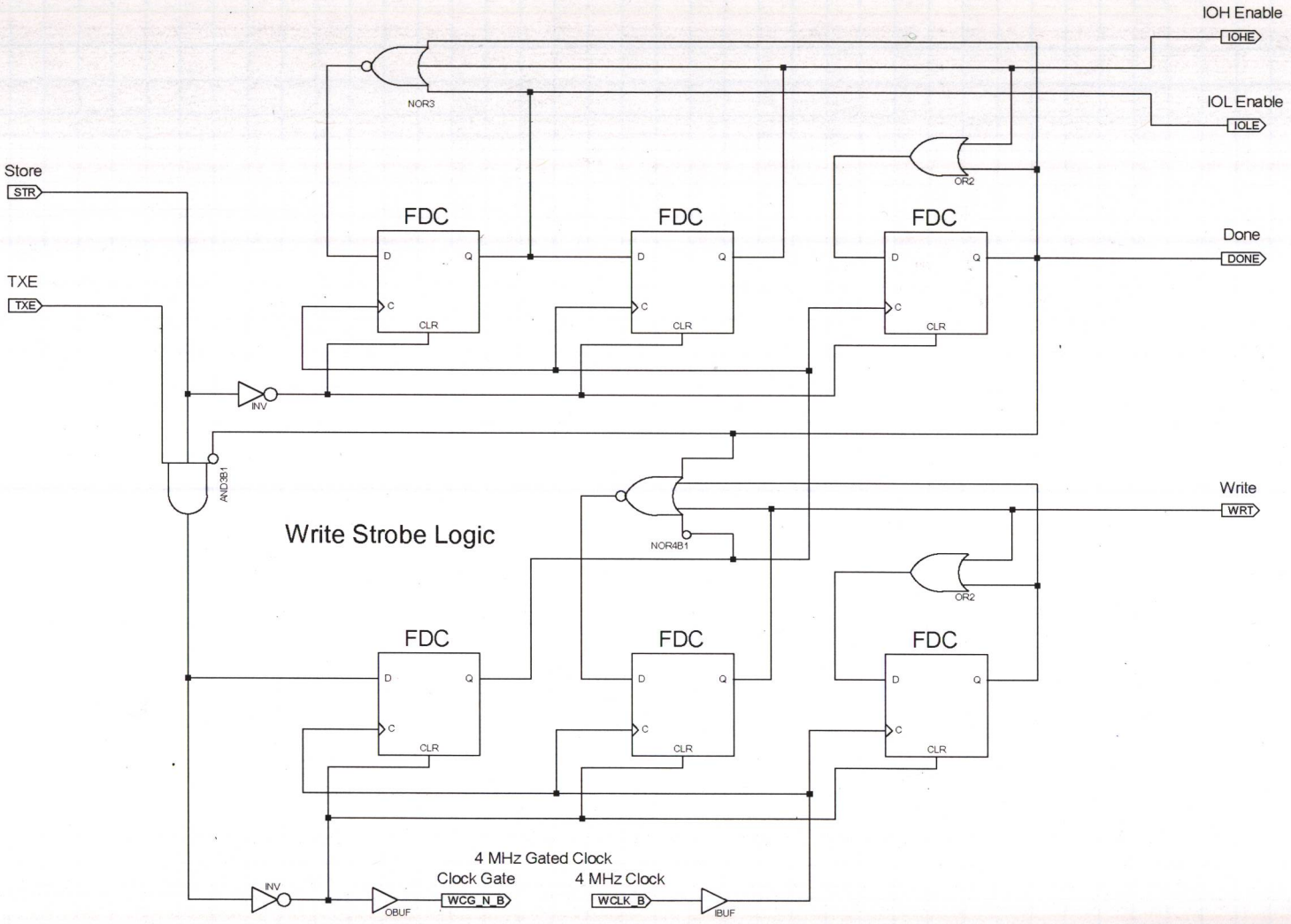
After extensive timing testing it was determined that the 10 MHz readout clock was too fast for reliable readout timing. Component C10 (270pf for a 10 MHz clock) has been changed to 680pf (4 MHz clock).

Additional Logic changes have been implemented for the ReadOut and Bus modules. These are described in detail in the following pages

AGB
30 Sept. 2023

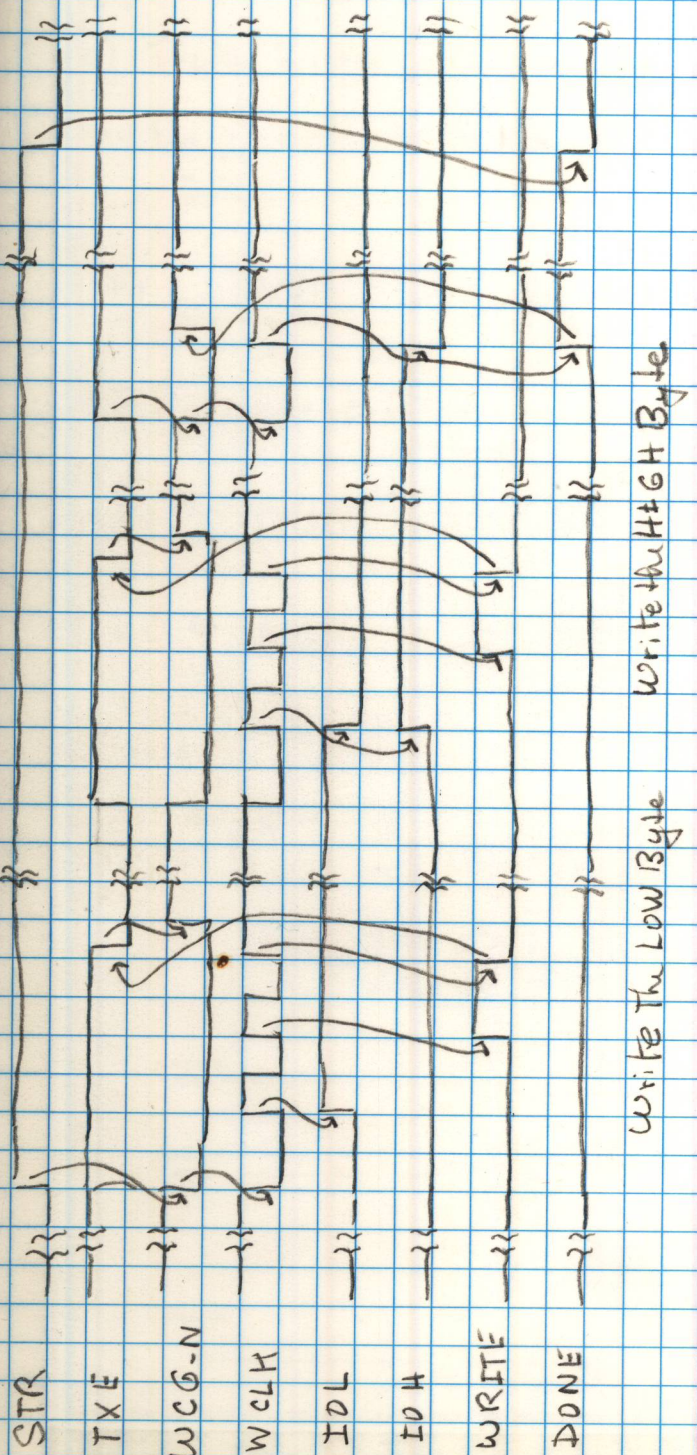
ReadOut Module

Readout Sequencer



September 2023

Read out Sequence Details



The combination of the STR and TXE becoming active triggers the transfer of two bytes to the USB controller.

The sequencer waits in the DONE state until the STR signal negates which initializes the sequencer for the Next Transfer.

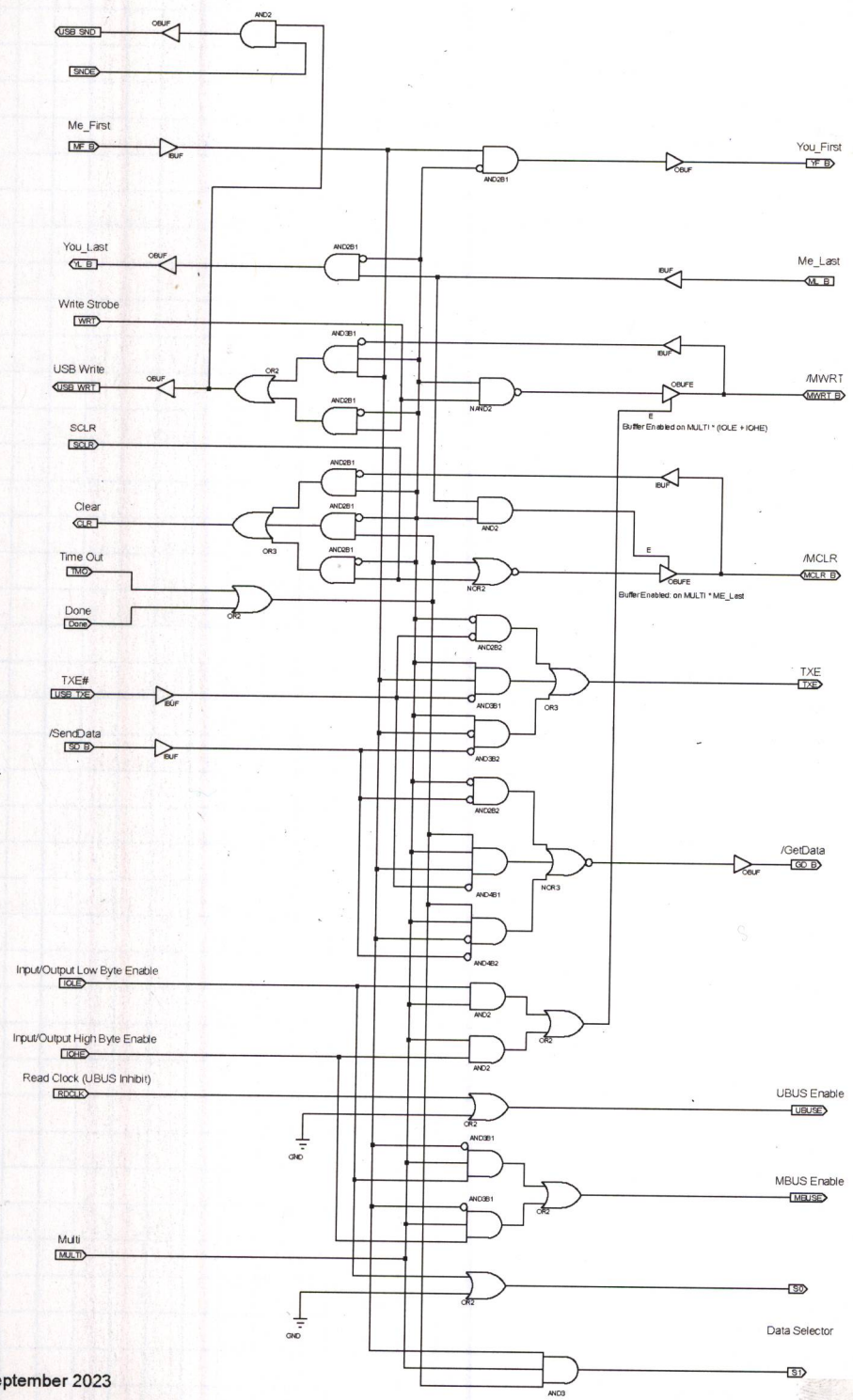
Typical Transfer Rate

~3.5 µs for 2 Bytes

ARB

30 Sept 2023

Multiple ADC Bus Module Control



September 2023

The updated BUS Module

The BUS module controls the transfer of Data from modules in single and multiparameter modes. These modes are:

1) NON Multiparameter Mode

2) First Module of a Multiparameter Chain

3) Middle Module of a Multiparameter Chain

4) Last Module of a Multiparameter Chain

and

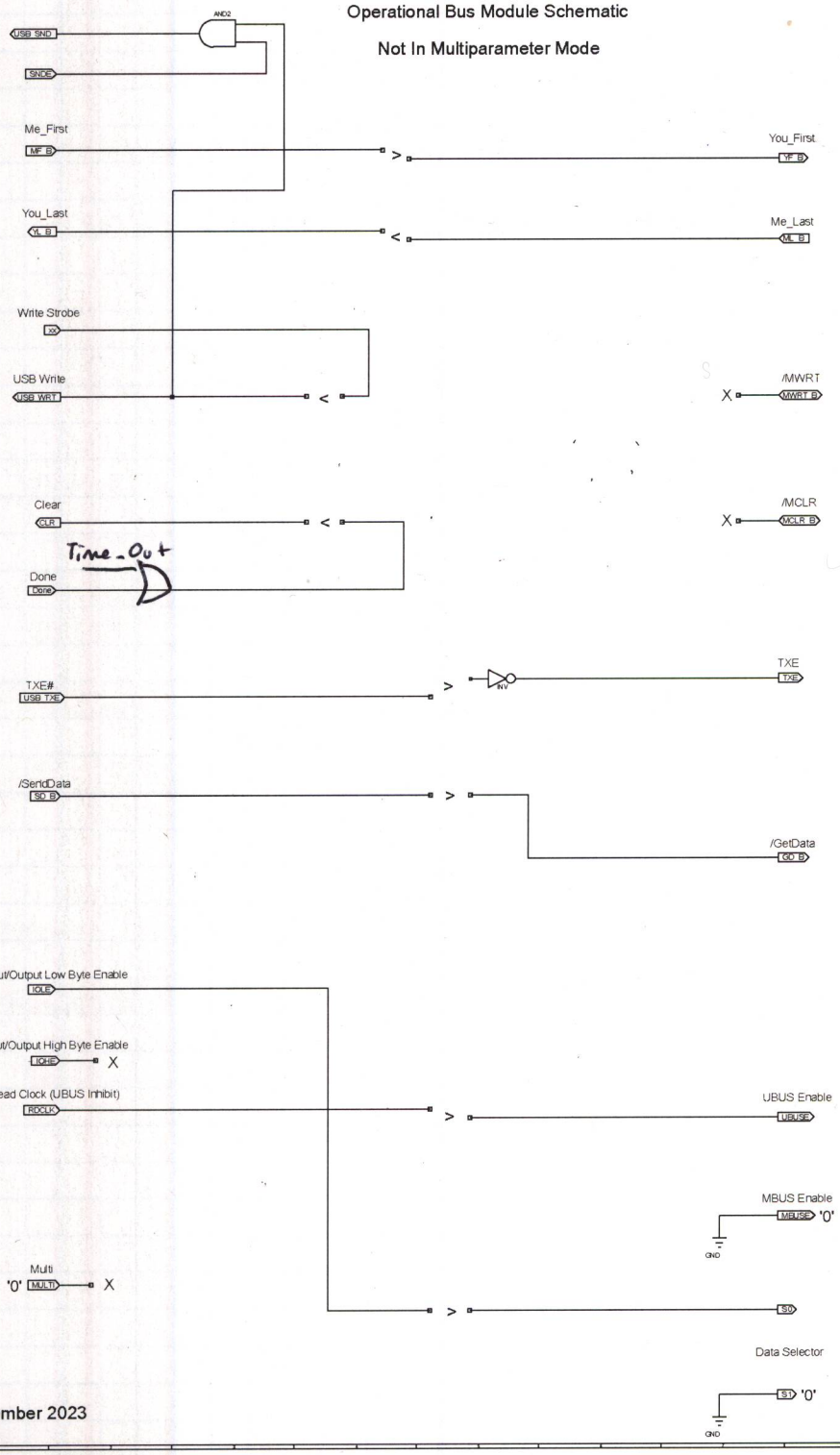
5) First and Last Module of a Multiparameter Chain
   ie the only Module in Multiparameter Mode
   (allows coincidence operation)

ARB
30 Sept. 2023

Multiple ADC/TMR Bus Control Module

Operational Bus Module Schematic

Not In Multiparameter Mode



September 2023

NOT in multi-parameter mode

This is a simplified diagram of the signal flow in the BUS module when not in the multiparameter mode

The multimode control signals are set as pass-through signals:

Me_First → You-First

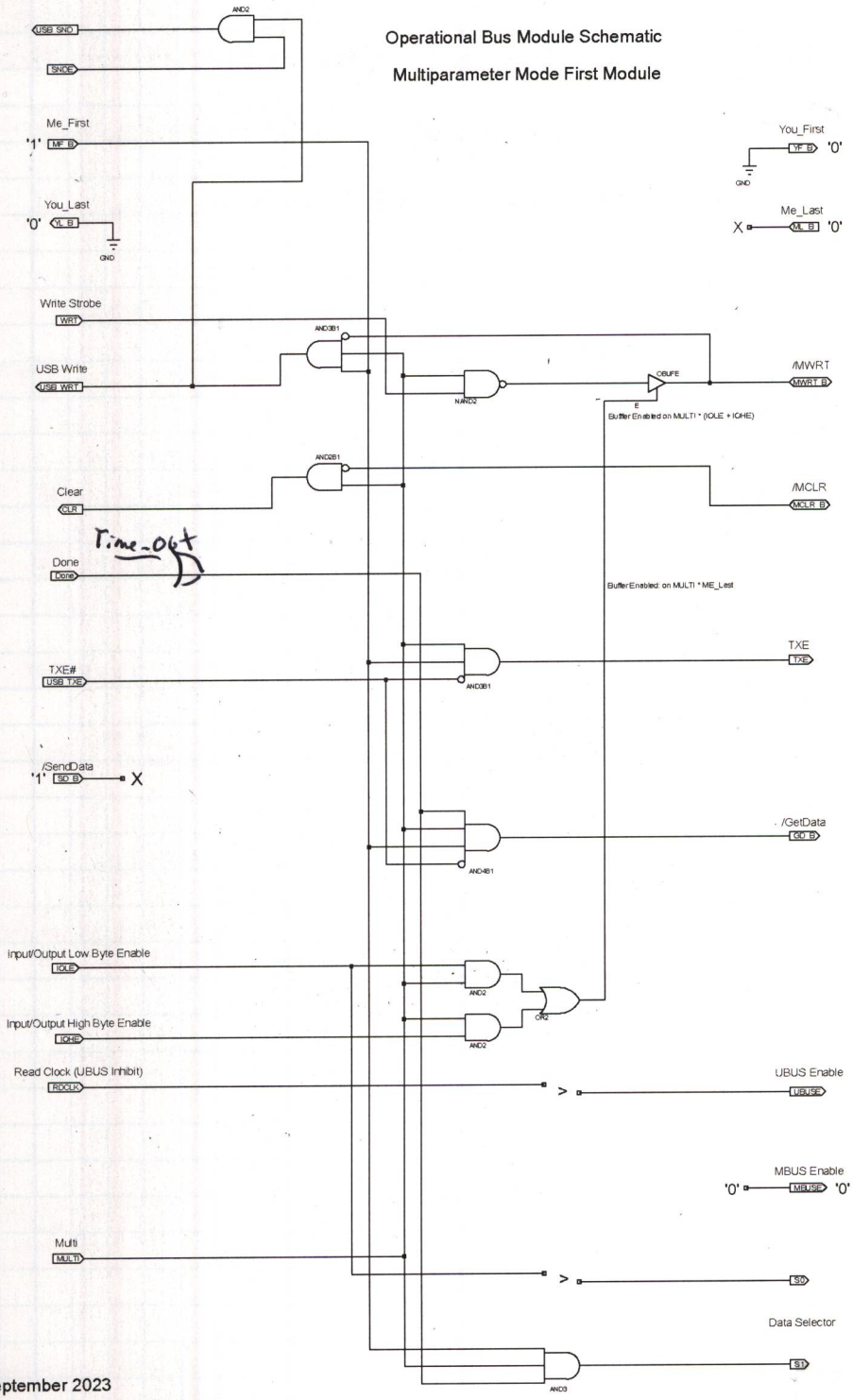
You-Last ← Me_Last

This allows single mode modules to be placed between multiparameter mode modules.

All other relavant signals are internally controlled independantly of multimode operation.

ARB
30 Sept. 2023

Multiple ADC/TMR Bus Control Module



September 2023

First Module in a Multiparameter Chain

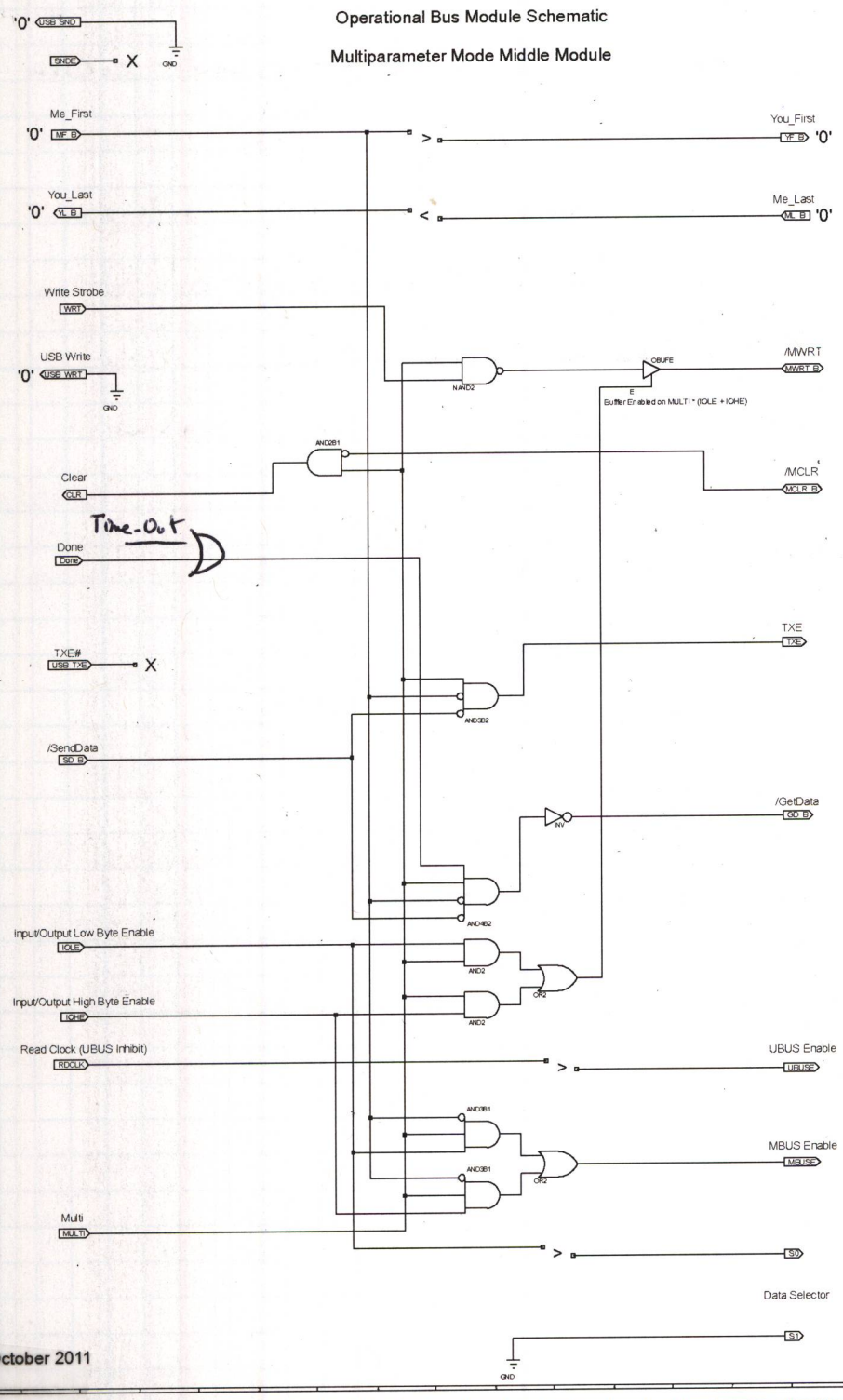
The first module in a multiparameter chain is the module having the lowest ID number and is in multiparameter mode. The first module performs all data transfers for the multiparameter chain modules.

The first module has the Me. First signal at the '1' level. This signal configures the BUS Module to perform all data transfers, internal and external, for the multiparameter chain:

First Module		Next Module (BUS)	
USB Write/MCLR	←	MWRT_B	or WRT
CLR	←	MCLR_B	(from Last Module)
TXEH → TXE	→	GD_B	(at DONE)
multi enable		BUS Data to USB	(at DONE)

ARB
30 Sept. 2023

Multiple ADC/TMR Bus Control Module



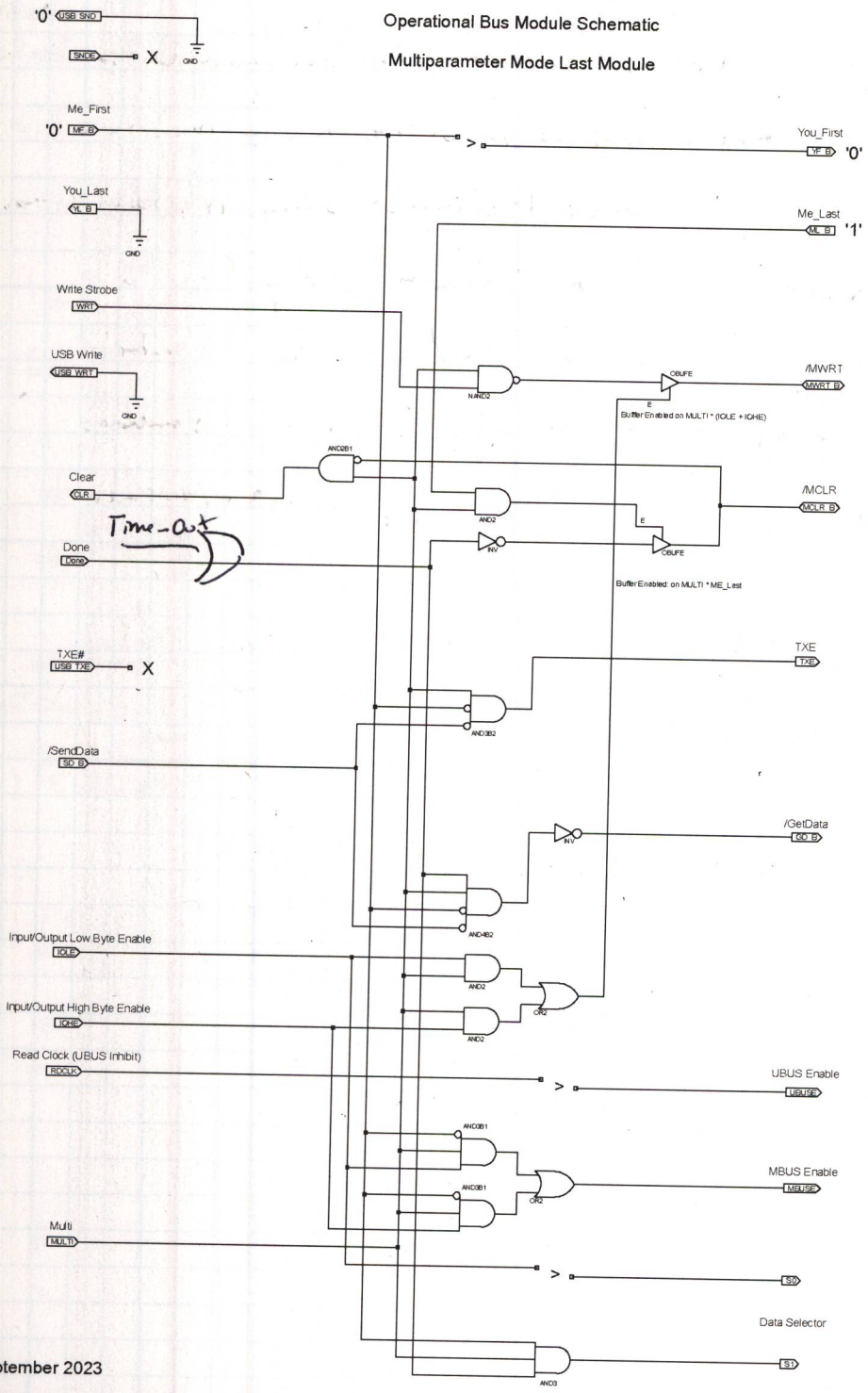
Middle Modules in a Multiparameter Chain

A middle module is not a first or Last module within a multiparameter module chain.
Data transfer is initiated by the assertion of the SD_B (/Send Data) signal which produces the pseudo TXE signal. Transfer proceeds when the TXE and STR signal within this module becom active.
The BUS signals:

Previous Module	Middle Module	Next Module
SD_B (/Send Data) →	GD_B (/Get Data) → TXE	→ GD_B (/Get Data) (at DONE)
←	CLR	← MCLR_B (/MCLR)
←	MWRT_B (/MWRT) (from IOL & IOH) & WRT	

ABB
30 Sept 2023

Multiple ADC/TMR Bus Control Module



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The Last Module in a Multiparameter Chain

The Last multiparameter module in a chain controls the completion of the final modules' data transfer and terminates the multiparameter transaction. The receipt of the SD-B signal (/Send Data) generates the pseudo TXE signal. When the TXE and modules STR signal become active the data transfer begins. At the completion of the data transfer the DONE signal generates the MCLR-B signal (/MCLR) which then clears all the modules in the multiparameter chain. This readys the chain for another event.

ARB
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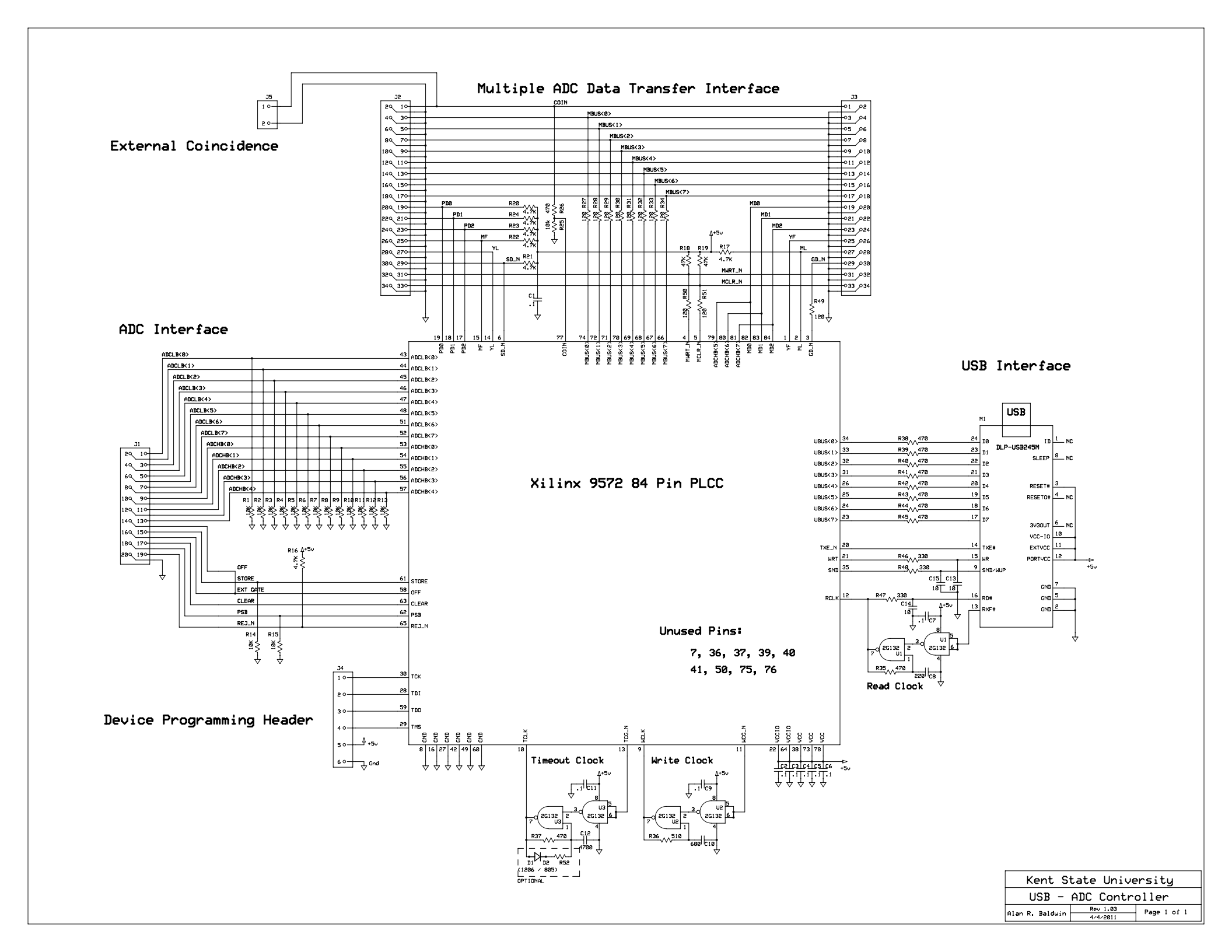
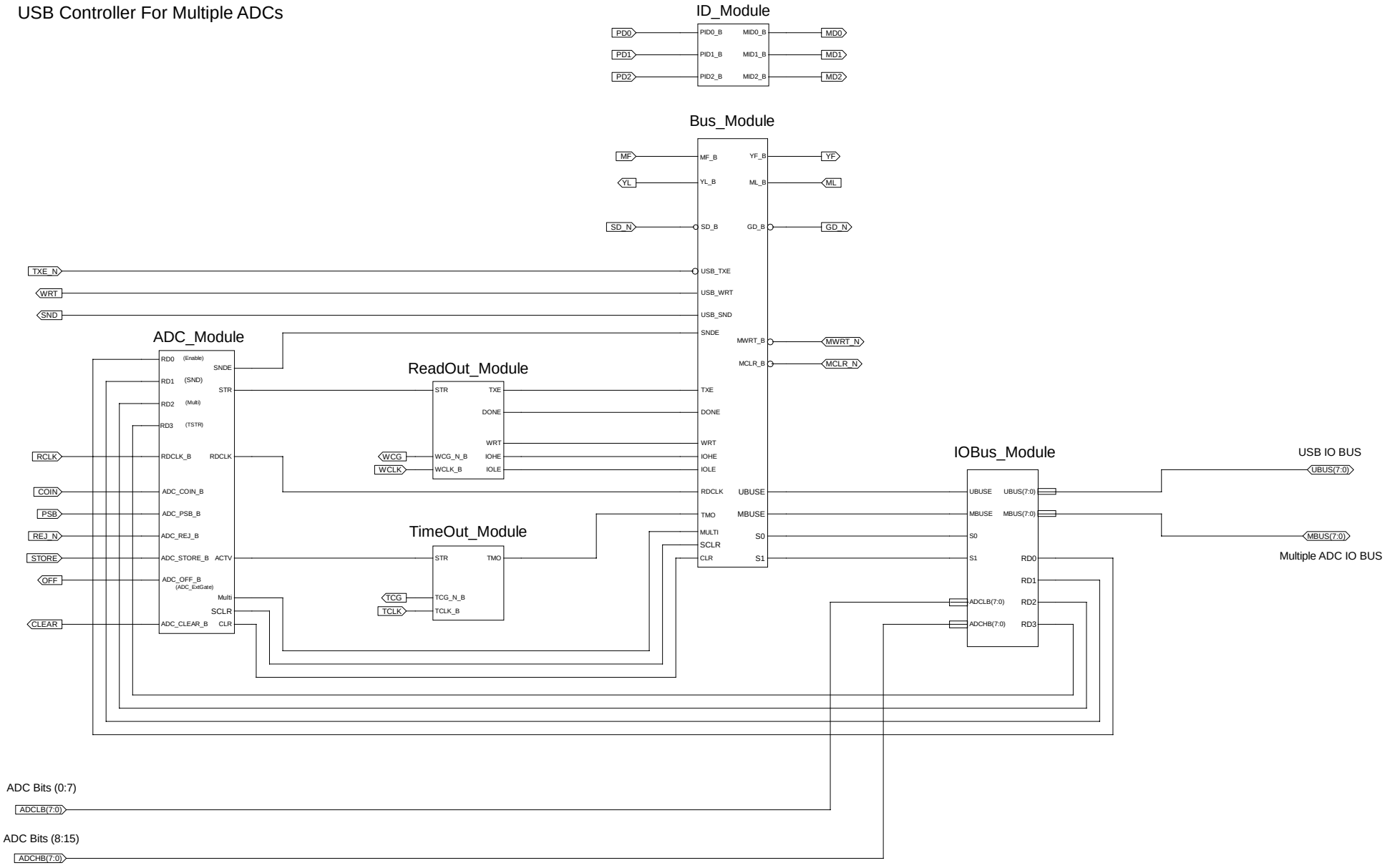
When a module is enabled as a multiparamter module and is the only such module it operates as the first and last module simultaneously.

This mode is useful if acquisition uses the COIN signal to enable the processing of ADC signals with specific requirements.

30 Sept 2023
ABS

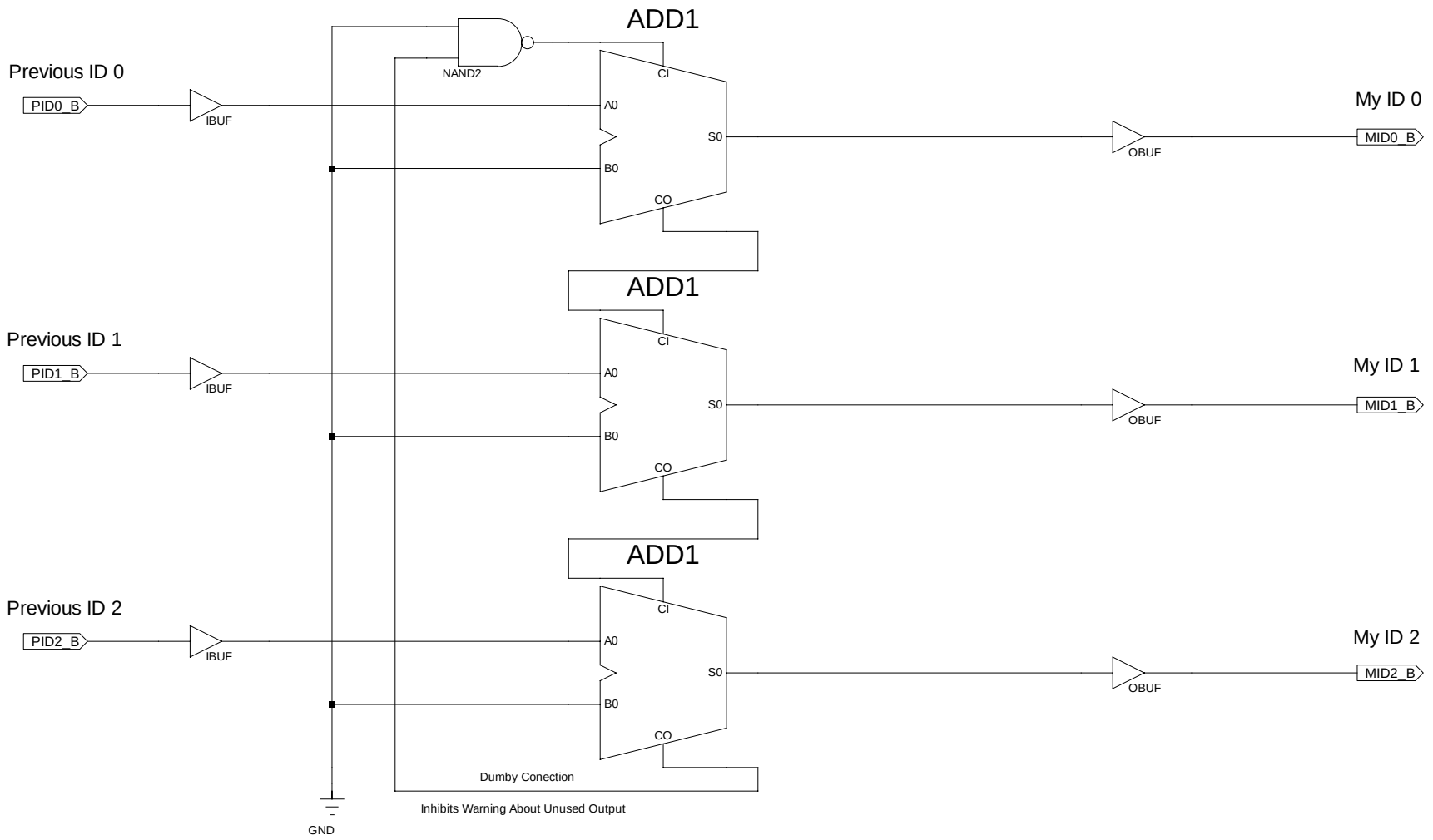

Multiple ADC Data Transfer Interface
External Coincidence
ADC Interface
USB Interface
Xilinx 9572 84 Pin PLCC
Unused Pins:
7, 36, 37, 39, 40
41, 50, 75, 76
Device Programming Header
Timeout Clock
Write Clock
Read Clock
USB
DLP-USB245M
OPTIONAL
Kent State University
USB - ADC Controller
Alan R. Baldwin
Rev 1.03
4/4/2011
Page 1 of 1

USB Controller For Multiple ADCs



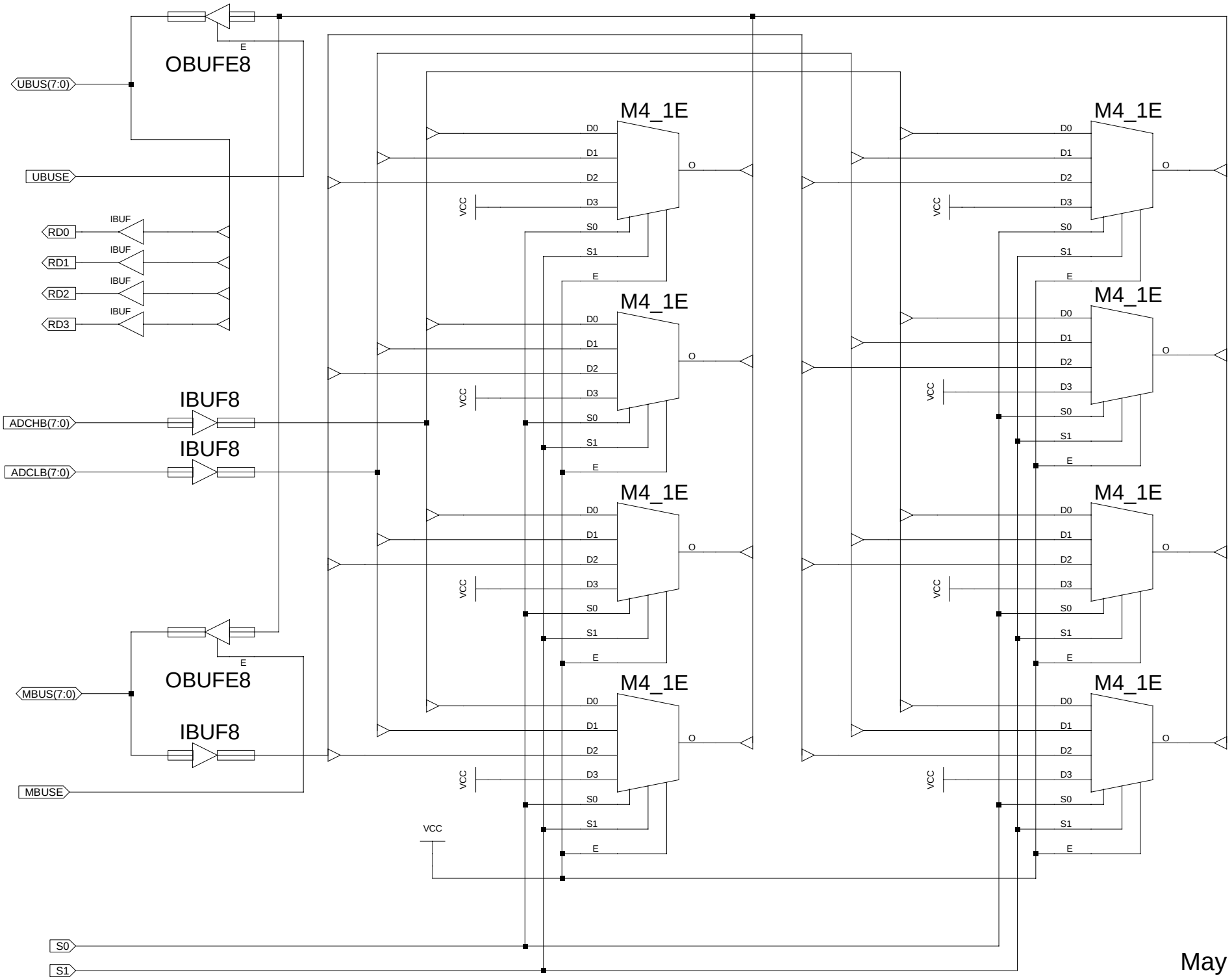
May 2011

Interface ID Module



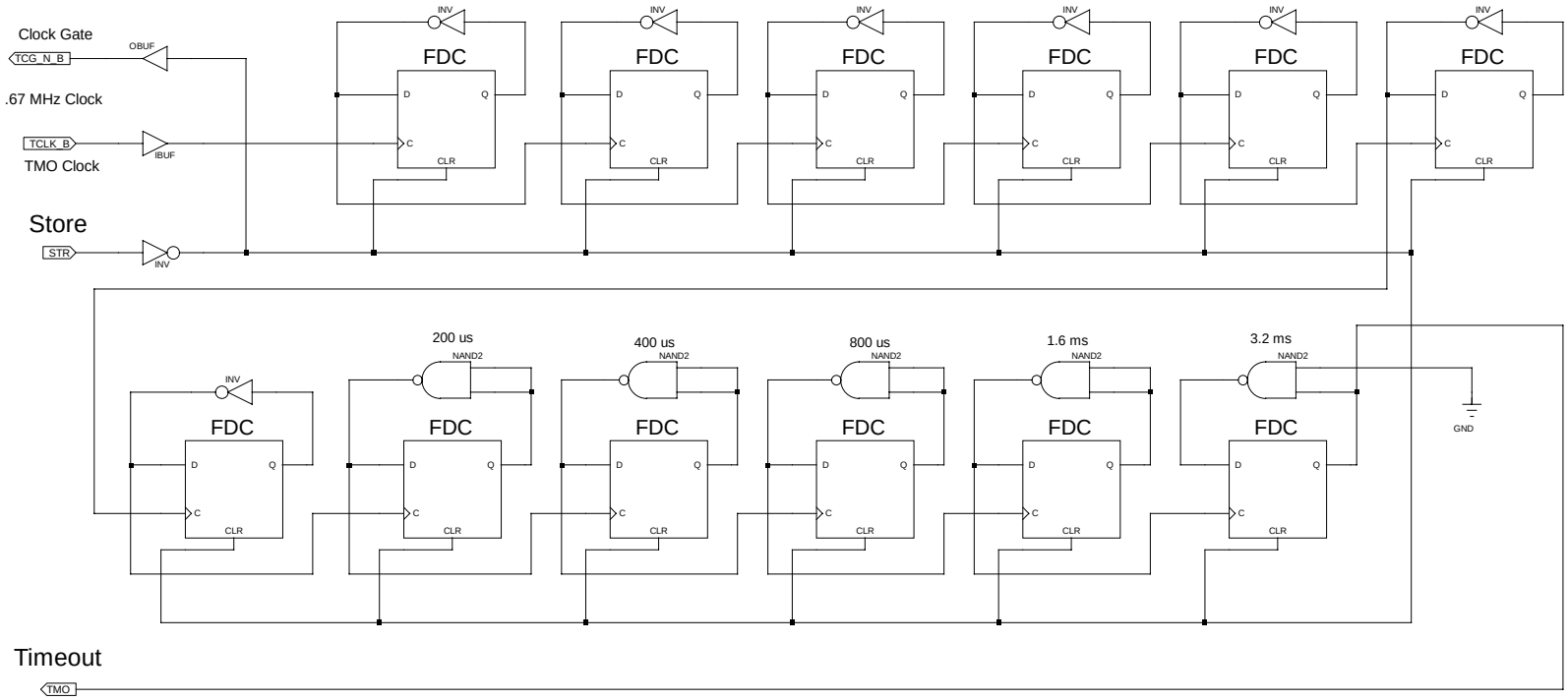
May 2011

IO Bus Module



May 2011

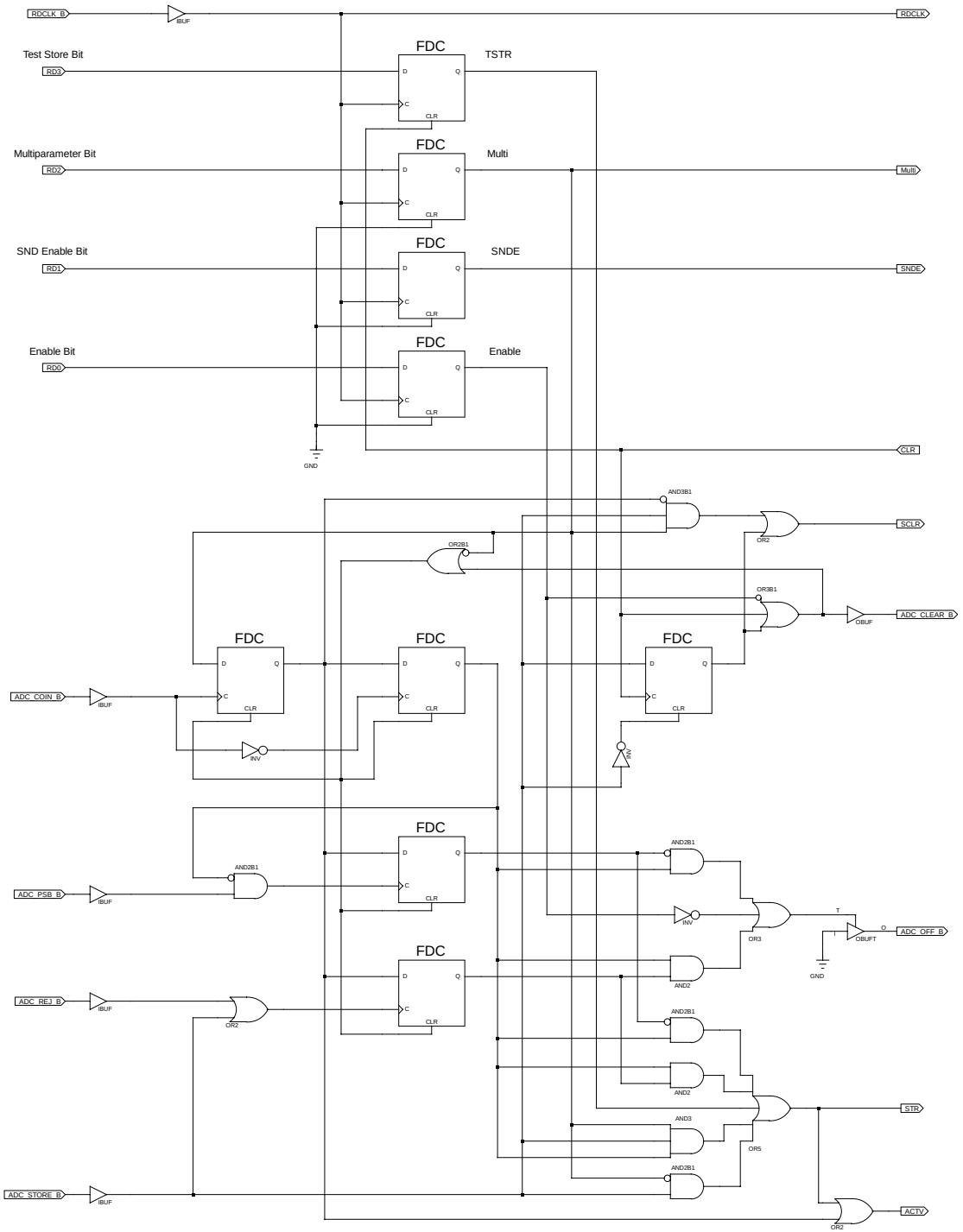
Timeout Module



USB ADC Control Logic Element
September 2011

Symbol: TIMEOUT_MODULE

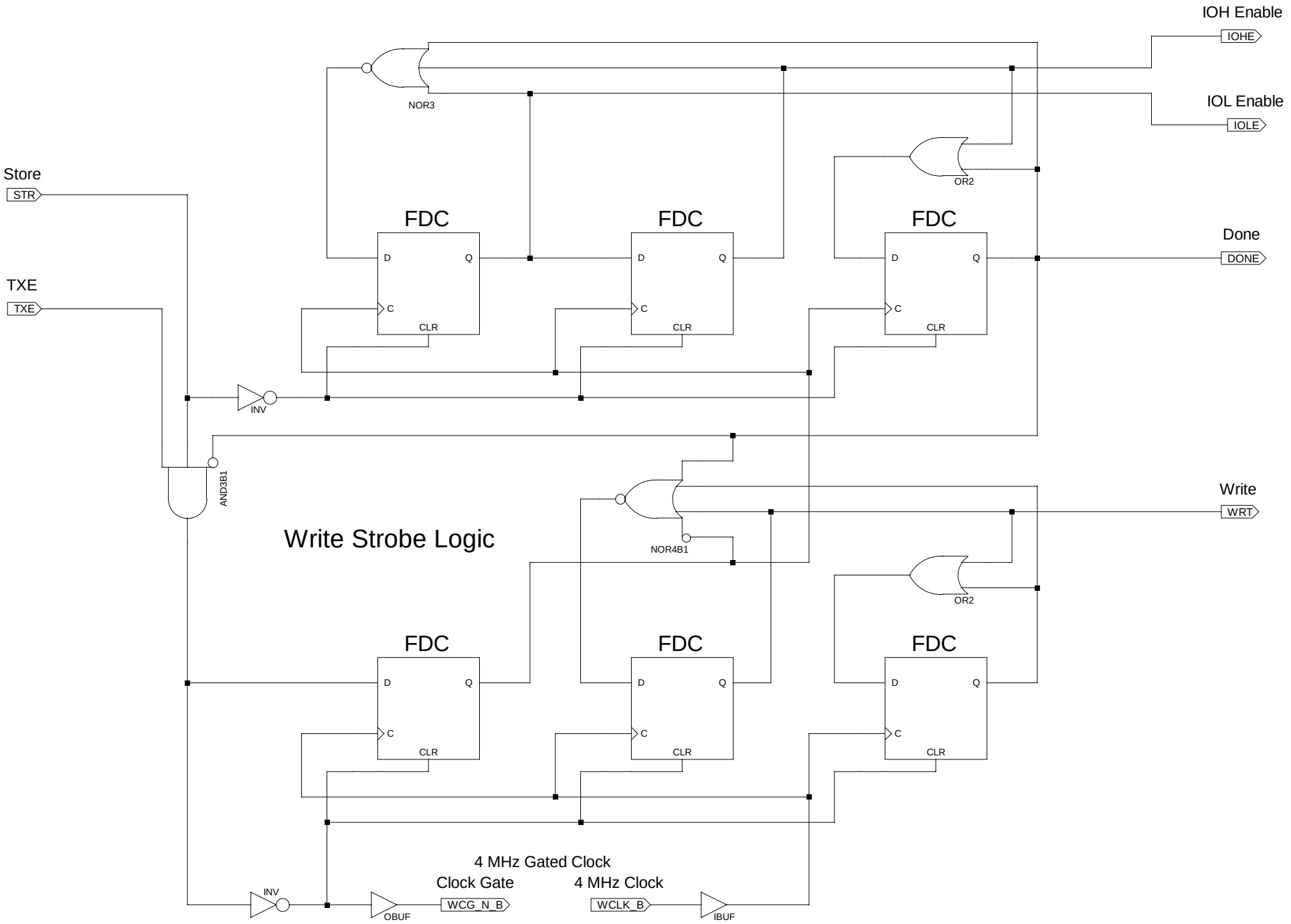
ADC Module



May 2011

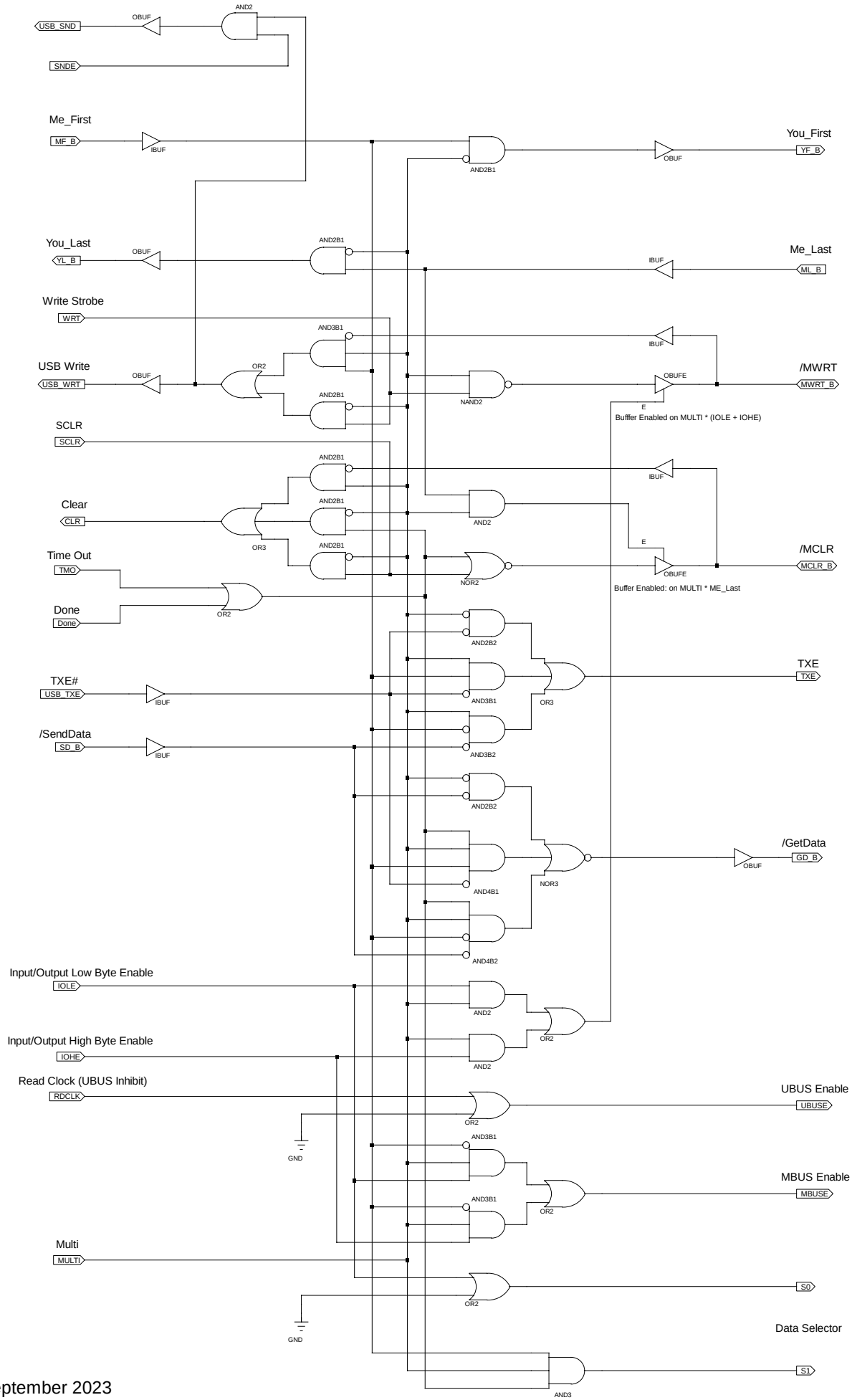
ReadOut Module

Readout Sequencer



September 2023

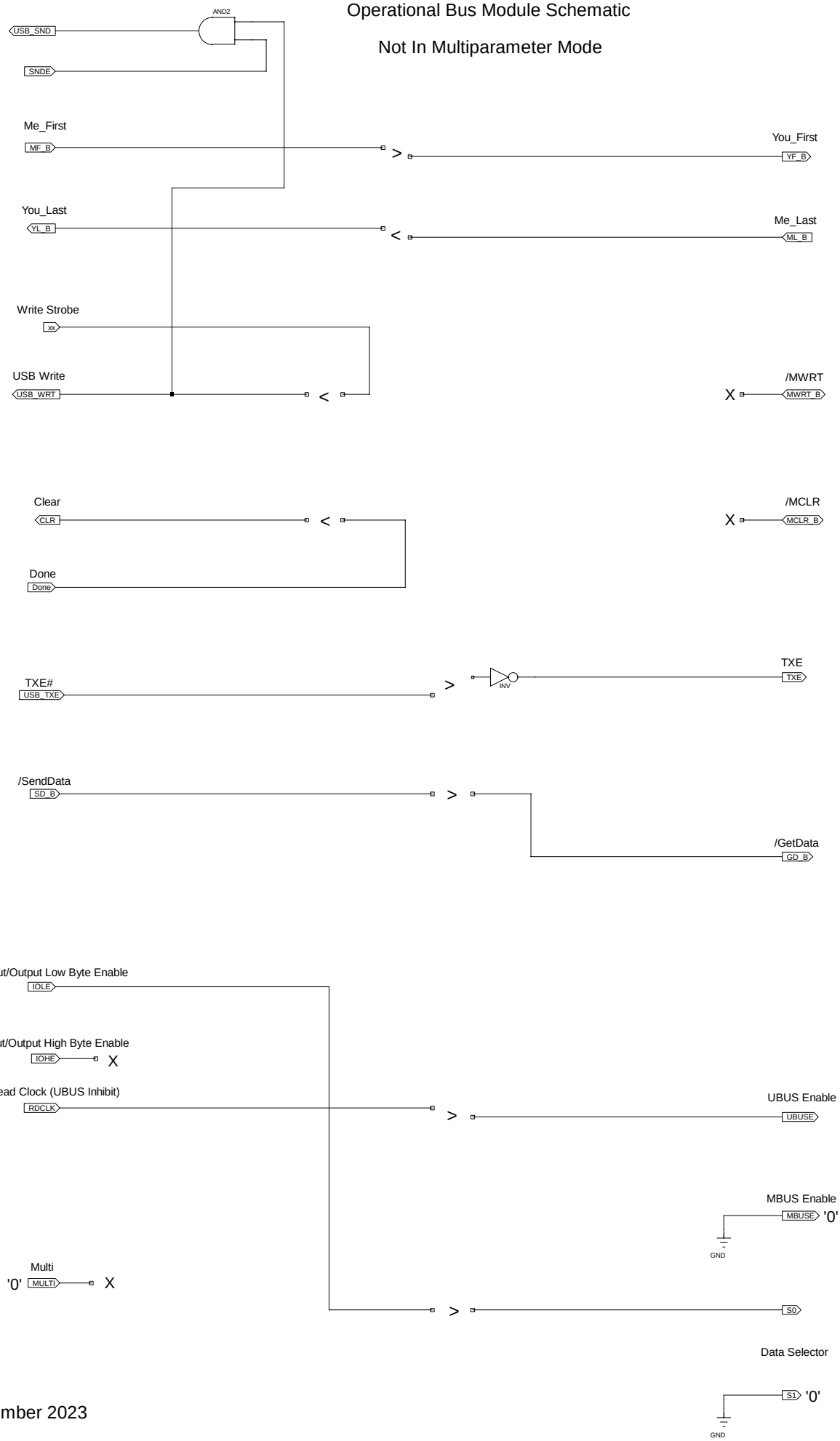
Multiple ADC Bus Module Control



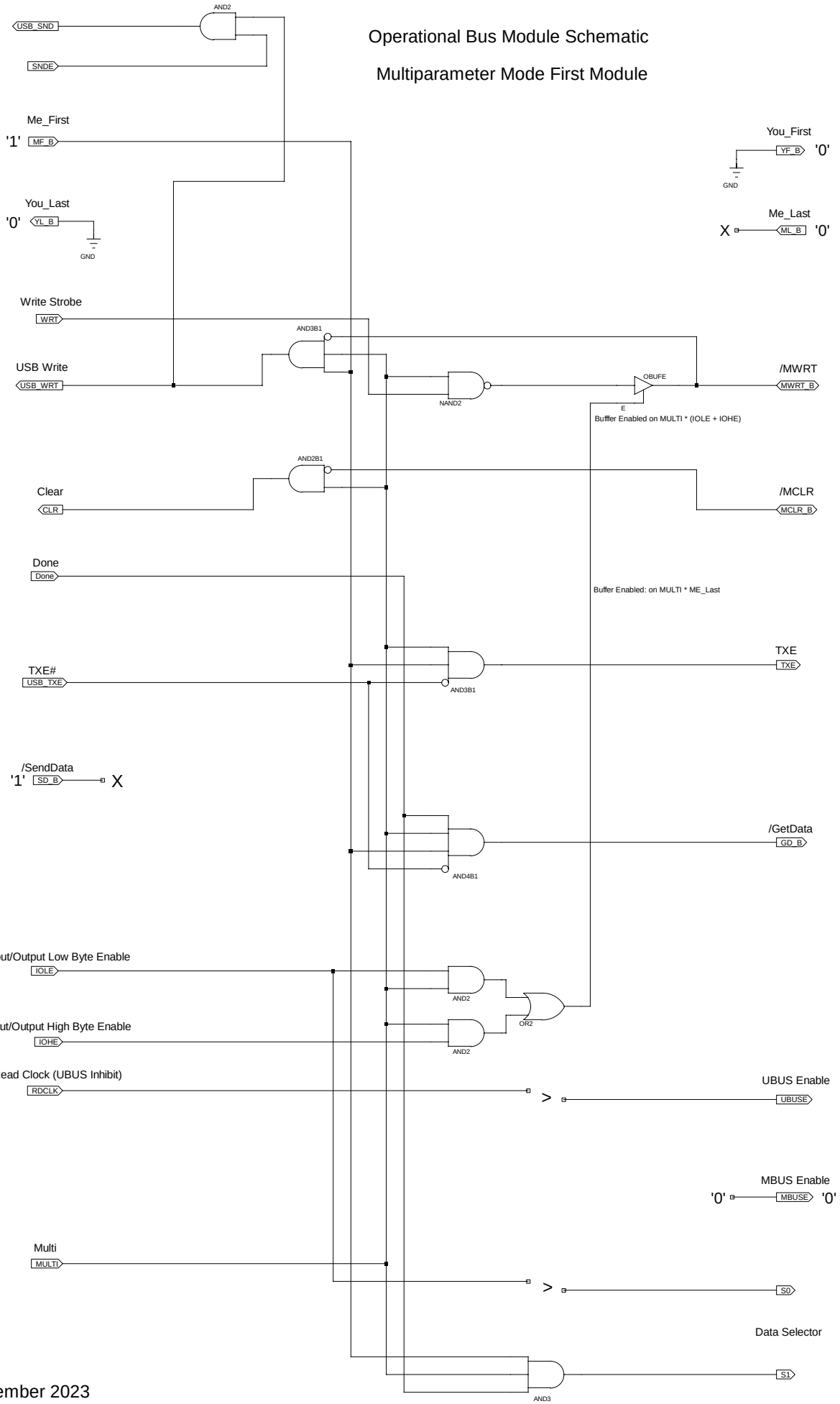
September 2023

Operational Bus Module Schematic

Not In Multiparameter Mode



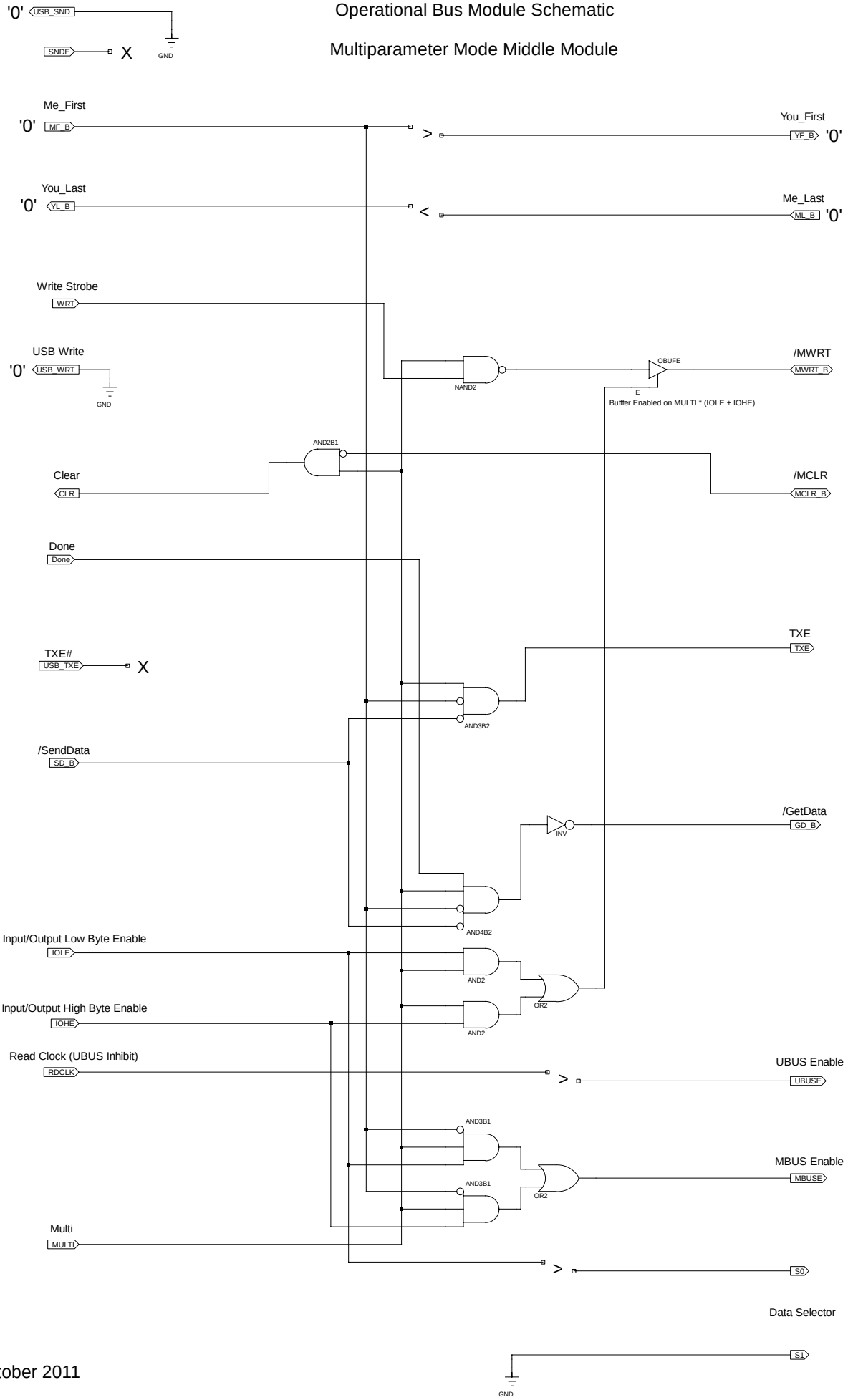
Multiple ADC/TMR Bus Control Module



September 2023

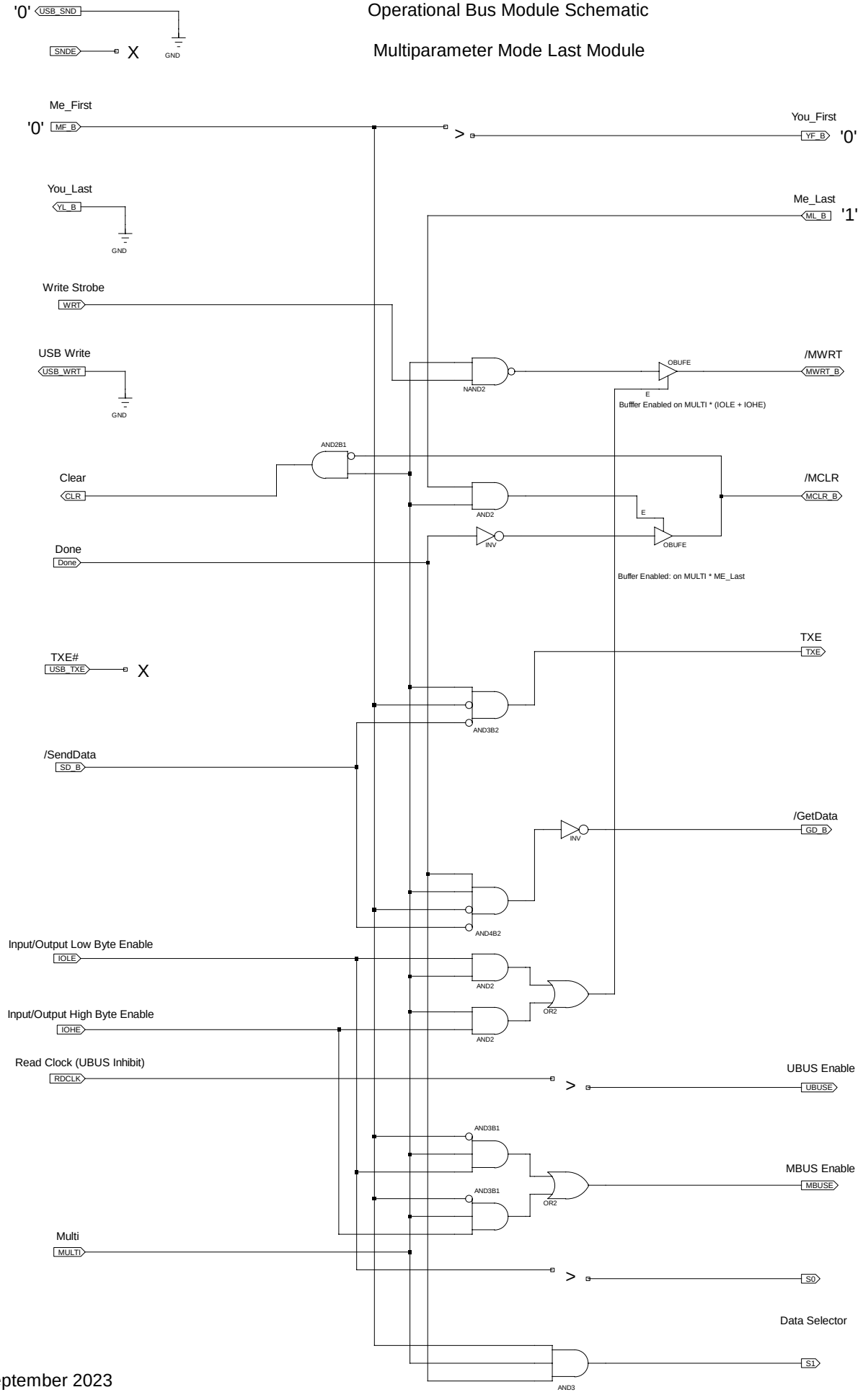
Operational Bus Module Schematic

Multiparameter Mode Middle Module



Operational Bus Module Schematic

Multiparameter Mode Last Module



```
cpldfit:  version O.40d                          Xilinx Inc.
                                Fitter Report
Design Name: USB_ADC_Controller_Multiple         Date:  9-28-2023, 12:35PM
Device Used: XC9572-15-PC84
Fitting Status: Successful

************************  Mapped Resource Summary  *************************

Macrocells     Product Terms    Function Block   Registers      Pins
Used/Tot       Used/Tot         Inps Used/Tot    Used/Tot       Used/Tot
64 /72  ( 89%) 151 /360  ( 42%) 117/144 ( 81%)   27 /72  ( 37%) 60 /69  ( 87%)

** Function Block Resources **

Function    Mcells      FB Inps     Signals     Pterms      IO
Block       Used/Tot    Used/Tot    Used        Used/Tot    Used/Tot
FB1          17/18       26/36       26          43/90       9/18
FB2          13/18       32/36       32          35/90      11/17
FB3          16/18       33/36       33          41/90       8/17
FB4          18/18*      26/36       26          32/90       2/17
             -----       -----                   -----       -----
             64/72      117/144                 151/360     30/69

* - Resource is exhausted

** Global Control Resources **

Signal 'WCLK' mapped onto global clock net GCK1.
Signal 'TCLK' mapped onto global clock net GCK2.
Signal 'RCLK' mapped onto global clock net GCK3.
Global output enable net(s) unused.
Global set/reset net(s) unused.

** Pin Resources **

Signal Type    Required     Mapped  |  Pin Type            Used    Total
------------------------------------|------------------------------------
Input         :   27          27    |  I/O             :    55      63
Output        :   16          16    |  GCK/IO          :     3       3
Bidirectional :   14          14    |  GTS/IO          :     1       2
GCK           :    3           3    |  GSR/IO          :     1       1
GTS           :    0           0    |
GSR           :    0           0    |
                 ----        ----
        Total     60          60

** Power Data **

There are 64 macrocells in high performance mode (MCHP).
There are 0 macrocells in low power mode (MCLP).
End of Mapped Resource Summary
```

********** Errors and Warnings **********

WARNING:Cpld - Unable to retrieve the path to the iSE Project Repository. Will use the default filename of 'USB_ADC_Controller_Multiple.ise'.
INFO:Cpld - Inferring BUFG constraint for signal 'XLXI_3/WCLK' based upon the LOC constraint 'P9'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.
INFO:Cpld - Inferring BUFG constraint for signal 'XLXI_4/TCLK' based upon the LOC constraint 'P10'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.
INFO:Cpld - Inferring BUFG constraint for signal 'XLXI_15/RCLK' based upon the LOC constraint 'P12'. It is recommended that you declare this BUFG explicitedly in your design. Note that for certain device families the output of a BUFG constraint can not drive a gated clock, and the BUFG constraint will be ignored.

********** Summary of Mapped Logic **********

** 30 Outputs **

Signal Name	Total Pts	Total Inps	Loc	Pin No.	Pin Type	Pin Use	Pwr Mode	Slew Rate	Reg Init State
MWRT_N	2	3	FB1_1	4	I/O	I/O	STD	SLOW	
YF	1	2	FB1_2	1	I/O	O	STD	SLOW	
GD_N	4	6	FB1_6	3	I/O	O	STD	SLOW	
WCG	5	7	FB1_7	11	I/O	O	STD	SLOW	
MCLR_N	4	7	FB1_8	5	I/O	I/O	STD	SLOW	
TCG	1	3	FB1_10	13	I/O	O	STD	SLOW	
YL	1	2	FB1_15	14	I/O	O	STD	SLOW	
UBUS<7>	4	6	FB1_16	23	I/O	O	STD	SLOW	
UBUS<6>	2	2	FB1_18	24	I/O	O	STD	SLOW	
CLEAR	1	3	FB2_1	63	I/O	O	STD	SLOW	
MBUS<4>	4	7	FB2_2	69	I/O	I/O	STD	SLOW	
MBUS<6>	4	7	FB2_3	67	I/O	I/O	STD	SLOW	
MBUS<5>	4	7	FB2_4	68	I/O	I/O	STD	SLOW	
MBUS<3>	4	7	FB2_5	70	I/O	I/O	STD	SLOW	
MBUS<2>	2	3	FB2_6	71	I/O	I/O	STD	SLOW	
MBUS<1>	4	7	FB2_8	72	I/O	I/O	STD	SLOW	
MBUS<0>	4	7	FB2_9	74	GSR/I/O	I/O	STD	SLOW	
MD1	2	2	FB2_15	83	I/O	O	STD	SLOW	
MD0	1	1	FB2_16	82	I/O	O	STD	SLOW	
MD2	2	3	FB2_17	84	I/O	O	STD	SLOW	
UBUS<5>	2	2	FB3_1	25	I/O	O	STD	SLOW	
UBUS<3>	2	2	FB3_3	31	I/O	I/O	STD	SLOW	
UBUS<2>	4	6	FB3_4	32	I/O	I/O	STD	SLOW	
UBUS<0>	4	6	FB3_6	34	I/O	I/O	STD	SLOW	
SND	2	5	FB3_7	35	I/O	O	STD	SLOW	
WRT	2	4	FB3_8	21	I/O	O	STD	SLOW	
UBUS<4>	2	2	FB3_9	26	I/O	O	STD	SLOW	
UBUS<1>	4	6	FB3_11	33	I/O	I/O	STD	SLOW	
OFF	1	2	FB4_12	58	I/O	O	STD	SLOW	
MBUS<7>	2	3	FB4_17	66	I/O	I/O	STD	SLOW	

** 34 Buried Nodes **

Signal Name	Total Pts	Total Inps	Loc	Pwr Mode	Reg Init State
XLXN_88	2	5	FB1_4	STD	RESET
XLXI_3/XLXN_595	2	1	FB1_5	STD	RESET
XLXI_3/XLXN_506	2	3	FB1_9	STD	RESET
XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF	2	5	FB1_11	STD	
$OpTx$FX_DC$3	2	4	FB1_12	STD	
XLXN_92	3	5	FB1_13	STD	RESET
XLXN_131	3	6	FB1_14	STD	RESET
XLXN_130	3	4	FB1_17	STD	RESET
XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF	1	4	FB2_14	STD	
XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST	2	3	FB2_18	STD	
XLXN_149	1	1	FB3_10	STD	RESET
XLXI_4/XLXN_275	2	4	FB3_12	STD	RESET
XLXI_4/XLXN_143	2	4	FB3_13	STD	RESET
$OpTx$FX_DC$5	2	4	FB3_14	STD	
XLXI_15/XLXN_49	3	4	FB3_15	STD	RESET
XLXI_15/XLXN_42	3	3	FB3_16	STD	RESET
XLXI_15/XLXN_286	3	3	FB3_17	STD	RESET
XLXI_15/XLXN_27	3	3	FB3_18	STD	RESET
XLXN_123	1	1	FB4_1	STD	RESET
XLXI_4/XLXN_79	1	3	FB4_2	STD	RESET
XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF	1	2	FB4_3	STD	
XLXI_15/XLXN_239	1	1	FB4_4	STD	RESET
XLXN_96	2	4	FB4_5	STD	RESET
XLXI_4/XLXN_85	2	4	FB4_6	STD	RESET
XLXI_4/XLXN_78	2	4	FB4_7	STD	RESET
XLXI_4/XLXN_35	2	4	FB4_8	STD	RESET
XLXI_4/XLXN_299	2	4	FB4_9	STD	RESET
XLXI_4/XLXN_298	2	4	FB4_10	STD	RESET
XLXI_4/XLXN_296	2	4	FB4_11	STD	RESET
XLXI_4/XLXN_295	2	4	FB4_13	STD	RESET
XLXI_4/XLXN_277	2	4	FB4_14	STD	RESET
XLXI_15/XLXN_213	2	2	FB4_15	STD	RESET
$OpTx$FX_DC$4	2	3	FB4_16	STD	
XLXI_15/XLXN_248	3	2	FB4_18	STD	RESET

** 30 Inputs **

Signal Name	Loc	Pin No.	Pin Type	Pin Use
SD_N	FB1_3	6	I/O	I
ML	FB1_5	2	I/O	I

TCLK	FB1_11	10	GCK/I/O	GCK
PD1	FB1_12	18	I/O	I
TXE_N	FB1_13	20	I/O	I
RCLK	FB1_14	12	GCK/I/O	GCK/I
MF	FB1_17	15	I/O	I
COIN	FB2_11	77	GTS/I/O	I
ADCHB<5>	FB2_12	79	I/O	I
ADCHB<6>	FB2_13	80	I/O	I
ADCHB<7>	FB2_14	81	I/O	I
PD2	FB3_2	17	I/O	I
PD0	FB3_5	19	I/O	I
ADCLB<0>	FB3_13	43	I/O	I
ADCLB<2>	FB3_16	45	I/O	I
ADCLB<3>	FB4_1	46	I/O	I
ADCLB<1>	FB4_2	44	I/O	I
ADCLB<6>	FB4_3	51	I/O	I
ADCLB<7>	FB4_4	52	I/O	I
ADCLB<4>	FB4_5	47	I/O	I
ADCHB<1>	FB4_6	54	I/O	I
ADCHB<2>	FB4_7	55	I/O	I
ADCLB<5>	FB4_8	48	I/O	I
ADCHB<4>	FB4_10	57	I/O	I
ADCHB<0>	FB4_11	53	I/O	I
STORE	FB4_13	61	I/O	I
ADCHB<3>	FB4_14	56	I/O	I
REJ_N	FB4_15	65	I/O	I
PSB	FB4_16	62	I/O	I

Legend:
Pin No. - ~ - User Assigned

```
************************  Function Block Details  ************************
Legend:
Total Pt     - Total product terms used by the macrocell signal
Imp Pt       - Product terms imported from other macrocells
Exp Pt       - Product terms exported to other macrocells
               in direction shown
Unused Pt    - Unused local product terms remaining in macrocell
Loc          - Location where logic was mapped in device
Pin Type/Use - I  - Input             GCK - Global Clock
               O  - Output            GTS - Global Output Enable
              (b) - Buried macrocell  GSR - Global Set/Reset
X(@)         - Signal used as input (wire-AND input) to the macrocell logic.
               The number of Signals Used may exceed the number of FB Inputs
               Used due to wire-ANDing in the switch matrix.
Pin No.      - ~  - User Assigned
```

********** FB1 **********

Number of function block inputs used/remaining: 26/10
Number of signals used by logic mapping into function block: 26

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
MWRT_N	2	0	0	3	FB1_1	4	I/O	I/O
YF	1	0	0	4	FB1_2	1	I/O	O
(unused)	0	0	0	5	FB1_3	6	I/O	I
XLXN_88	2	0	0	3	FB1_4	7	I/O	(b)
XLXI_3/XLXN_595	2	0	0	3	FB1_5	2	I/O	I
GD_N	4	0	0	1	FB1_6	3	I/O	O
WCG	5	0	0	0	FB1_7	11	I/O	O
MCLR_N	4	0	0	1	FB1_8	5	I/O	I/O
XLXI_3/XLXN_506	2	0	0	3	FB1_9	9	GCK/I/O	GCK
TCG	1	0	0	4	FB1_10	13	I/O	O
XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF	2	0	0	3	FB1_11	10	GCK/I/O	GCK
$OpTx$FX_DC$3	2	0	0	3	FB1_12	18	I/O	I
XLXN_92	3	0	0	2	FB1_13	20	I/O	I
XLXN_131	3	0	0	2	FB1_14	12	GCK/I/O	GCK/I
YL	1	0	0	4	FB1_15	14	I/O	O
UBUS<7>	4	0	0	1	FB1_16	23	I/O	O
XLXN_130	3	0	0	2	FB1_17	15	I/O	I
UBUS<6>	2	0	0	3	FB1_18	24	I/O	O

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$3.LFBK	10: MBUS<7>.PIN	19: SD_N
2: $OpTx$FX_DC$5	11: XLXI_3/XLXN_506.LFBK	20: XLXN_123
3: MBUS<6>	12: XLXI_3/XLXN_595.LFBK	21: XLXN_130.LFBK
4: XLXI_15/XLXN_213	13: XLXI_3/XLXN_623.LFBK	22: XLXN_131.LFBK
5: XLXI_15/XLXN_248	14: MCLR_N.PIN	23: RCLK
6: STORE	15: ML	24: XLXN_88.LFBK
7: XLXI_15/XLXN_27	16: XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST	25: XLXN_92.LFBK
8: ADCHB<7>	17: TXE_N	26: XLXN_96
9: ADCLB<7>	18: MF	

Signal Name	1 0---+---0---+---0---+---0---+---0	Signals Used	FB Inputs
MWRT_N	...............X...X...X.....	3	3
YF	.................X.X.....	2	2
XLXN_88	..........XXX..........XX.....	5	5
XLXI_3/XLXN_595	............X.....	1	1
GD_N	................XXXX....XX.....	6	6
WCG	.X.X............XXXX....X.....	7	7
MCLR_N	....XXX.......X....X....XX.....	7	7
XLXI_3/XLXN_506	..........X.X..........X.....	3	3
TCG	.X.X..X.....	3	3
XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF	....X........X.....X....XX.....	5	5
$OpTx$FX_DC$3	.................X.X....XX.....	4	4
XLXN_92	.X.X.......X........X...X.....	5	5
XLXN_131	.X.X.......X........XX..X.....	6	6
YL	..............X....X.....	2	2
UBUS<7>	X......XXX...........XX.....	6	6
XLXN_130	.X.X.......X.........X.....	4	4
UBUS<6>	..X...................X.....	2	2
	0---+---1---+---2---+---3---+---4		
	0 0 0 0		

********** FB2 **********

Number of function block inputs used/remaining: 32/4
Number of signals used by logic mapping into function block: 32

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
CLEAR	1	0	0	4	FB2_1	63	I/O	O
MBUS<4>	4	0	0	1	FB2_2	69	I/O	I/O
MBUS<6>	4	0	0	1	FB2_3	67	I/O	I/O
MBUS<5>	4	0	0	1	FB2_4	68	I/O	I/O
MBUS<3>	4	0	0	1	FB2_5	70	I/O	I/O
MBUS<2>	2	0	0	3	FB2_6	71	I/O	I/O
(unused)	0	0	0	5	FB2_7	76	GTS/I/O	
MBUS<1>	4	0	0	1	FB2_8	72	I/O	I/O
MBUS<0>	4	0	0	1	FB2_9	74	GSR/I/O	I/O
(unused)	0	0	0	5	FB2_10	75	I/O	
(unused)	0	0	0	5	FB2_11	77	GTS/I/O	I
(unused)	0	0	0	5	FB2_12	79	I/O	I
(unused)	0	0	0	5	FB2_13	80	I/O	I
XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF	1	0	0	4	FB2_14	81	I/O	I
MD1	2	0	0	3	FB2_15	83	I/O	O
MD0	1	0	0	4	FB2_16	82	I/O	O
MD2	2	0	0	3	FB2_17	84	I/O	O
XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST	2	0	0	3	FB2_18		(b)	(b)

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$3	12: ADCHB<4>	23: MBUS<3>.PIN
2: UBUS<2>	13: ADCHB<5>	24: MBUS<4>.PIN
3: XLXI_15/XLXN_239	14: ADCHB<6>	25: MBUS<5>.PIN
4: XLXI_15/XLXN_248	15: ADCLB<0>	26: MBUS<6>.PIN
5: XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF	16: ADCLB<1>	27: MCLR_N.PIN
6: PD0	17: ADCLB<3>	28: XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK
7: PD1	18: ADCLB<4>	29: MF
8: PD2	19: ADCLB<5>	30: XLXN_123
9: ADCHB<0>	20: ADCLB<6>	31: XLXN_130
10: ADCHB<1>	21: MBUS<0>.PIN	32: XLXN_131
11: ADCHB<3>	22: MBUS<1>.PIN	

Signal Name	1 0----+----0	2 ----+----0	3 ----+----0	4 ----+----0	Signals Used	FB Inputs
CLEAR	..XXX				3	3
MBUS<4>	X.....X	X	X	...XX..X	7	7
MBUS<6>	X.....X	X	X	.XX..X	7	7
MBUS<5>	X.....X	X	X	..XX..X	7	7
MBUS<3>	X.....X	X	X	....XX..X	7	7
MBUS<2>	.X.....			XX	3	3
MBUS<1>	X.....X	X	X	.....XX..X	7	7
MBUS<0>	X.....X	X	X	......XX..X	7	7
XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF	..XX			..X.....	4	4
MD1	XX				2	2
MD0	X				1	1
MD2	XXX				3	3
XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST				XXX.....	3	3

0----+----1----+----2----+----3----+----4

0 0 0 0

********** FB3 **********

Number of function block inputs used/remaining: 33/3
Number of signals used by logic mapping into function block: 33

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
UBUS<5>	2	0	0	3	FB3_1	25	I/O	O
(unused)	0	0	0	5	FB3_2	17	I/O	I
UBUS<3>	2	0	0	3	FB3_3	31	I/O	I/O
UBUS<2>	4	0	0	1	FB3_4	32	I/O	I/O
(unused)	0	0	0	5	FB3_5	19	I/O	I
UBUS<0>	4	0	0	1	FB3_6	34	I/O	I/O
SND	2	0	0	3	FB3_7	35	I/O	O
WRT	2	0	0	3	FB3_8	21	I/O	O
UBUS<4>	2	0	0	3	FB3_9	26	I/O	O
XLXN_149	1	0	0	4	FB3_10	40	I/O	(b)
UBUS<1>	4	0	0	1	FB3_11	33	I/O	I/O
XLXI_4/XLXN_275	2	0	0	3	FB3_12	41	I/O	(b)
XLXI_4/XLXN_143	2	0	0	3	FB3_13	43	I/O	I
$OpTx$FX_DC$5	2	0	0	3	FB3_14	36	I/O	(b)
XLXI_15/XLXN_49	3	0	0	2	FB3_15	37	I/O	(b)
XLXI_15/XLXN_42	3	0	0	2	FB3_16	45	I/O	I
XLXI_15/XLXN_286	3	0	0	2	FB3_17	39	I/O	(b)
XLXI_15/XLXN_27	3	0	0	2	FB3_18		(b)	(b)

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$3	12: COIN	23: MBUS<2>.PIN
2: $OpTx$FX_DC$4	13: XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF	24: XLXI_4/XLXN_143.LFBK
3: $OpTx$FX_DC$5.LFBK	14: XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF	25: XLXI_4/XLXN_35
4: MBUS<3>	15: ADCHB<0>	26: MWRT_N.PIN
5: MBUS<4>	16: ADCHB<1>	27: MF
6: MBUS<5>	17: ADCHB<2>	28: XLXN_123
7: XLXI_15/XLXN_213	18: ADCLB<0>	29: XLXN_131
8: STORE	19: ADCLB<1>	30: UBUS<1>.PIN
9: XLXI_15/XLXN_27.LFBK	20: ADCLB<2>	31: XLXN_149.LFBK
10: PSB	21: MBUS<0>.PIN	32: RCLK
11: XLXI_15/XLXN_286.LFBK	22: MBUS<1>.PIN	33: XLXN_88

Signal Name	1 0----+----0----+----0----+----0----+----0	Signals Used	FB Inputs
UBUS<5>	.....X.....X.....	2	2
UBUS<3>	...X.....X.....	2	2
UBUS<2>	X.....X..X..X.....X..X.....	6	6
UBUS<0>	X.....X..X..X.....X..X.....	6	6
SND	.....XXX..X.X.....	5	5
WRT	.....XXX....X.....	4	4
UBUS<4>	....X.....X.....	2	2
XLXN_149	.....X.....	1	1
UBUS<1>	X.....X..X..X.....X..X.....	6	6
XLXI_4/XLXN_275	..X...X.X.....X.....	4	4
XLXI_4/XLXN_143	..X...X.X.....X.....	4	4
$OpTx$FX_DC$5	.X.....X..X.....X.....	4	4
XLXI_15/XLXN_49	.....XXX..X.....	4	4
XLXI_15/XLXN_42	.....X...XX.....	3	3
XLXI_15/XLXN_286	.....X..X.X.....	3	3
XLXI_15/XLXN_27	.....X.X.....X.....	3	3
	0----+----1----+----2----+----3----+----4		
	0 0 0 0		

********** FB4 **********

Number of function block inputs used/remaining: 26/10
Number of signals used by logic mapping into function block: 26

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pin #	Pin Type	Pin Use
XLXN_123	1	0	0	4	FB4_1	46	I/O	I
XLXI_4/XLXN_79	1	0	0	4	FB4_2	44	I/O	I
XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF	1	0	0	4	FB4_3	51	I/O	I
XLXI_15/XLXN_239	1	0	0	4	FB4_4	52	I/O	I
XLXN_96	2	0	0	3	FB4_5	47	I/O	I
XLXI_4/XLXN_85	2	0	0	3	FB4_6	54	I/O	I
XLXI_4/XLXN_78	2	0	0	3	FB4_7	55	I/O	I
XLXI_4/XLXN_35	2	0	0	3	FB4_8	48	I/O	I
XLXI_4/XLXN_299	2	0	0	3	FB4_9	50	I/O	(b)
XLXI_4/XLXN_298	2	0	0	3	FB4_10	57	I/O	I
XLXI_4/XLXN_296	2	0	0	3	FB4_11	53	I/O	I
OFF	1	0	0	4	FB4_12	58	I/O	O
XLXI_4/XLXN_295	2	0	0	3	FB4_13	61	I/O	I
XLXI_4/XLXN_277	2	0	0	3	FB4_14	56	I/O	I
XLXI_15/XLXN_213	2	0	0	3	FB4_15	65	I/O	I
$OpTx$FX_DC$4	2	0	0	3	FB4_16	62	I/O	I
MBUS<7>	2	0	0	3	FB4_17	66	I/O	I/O
XLXI_15/XLXN_248	3	0	0	2	FB4_18		(b)	(b)

Signals Used by Logic in Function Block

1: $OpTx$FX_DC$4.LFBK
2: $OpTx$FX_DC$5
3: UBUS<7>
4: XLXI_15/XLXN_213.LFBK
5: XLXI_15/XLXN_239.LFBK
6: XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF
7: STORE
8: XLXI_15/XLXN_27
9: REJ_N
10: XLXI_15/XLXN_286
11: XLXI_15/XLXN_42
12: XLXI_15/XLXN_49
13: XLXI_4/XLXN_275
14: XLXI_4/XLXN_277.LFBK
15: XLXI_4/XLXN_295.LFBK
16: XLXI_4/XLXN_296.LFBK
17: XLXI_4/XLXN_298.LFBK
18: XLXI_4/XLXN_299.LFBK
19: XLXI_4/XLXN_78.LFBK
20: XLXI_4/XLXN_79.LFBK
21: XLXI_4/XLXN_85.LFBK
22: XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST
23: MF
24: UBUS<2>.PIN
25: UBUS<0>.PIN
26: UBUS<3>.PIN

Signal Name	0----+----1----+----2----+----3----+----4	Signals Used	FB Inputs
XLXN_123	.....X.....	1	1
XLXI_4/XLXN_79	.X.X...X.....	3	3
XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF	......X.X.....	2	2
XLXI_15/XLXN_239	.....X.....	1	1
XLXN_96	.X.X...X.....X.....	4	4
XLXI_4/XLXN_85	.X.X...X.....X.....	4	4
XLXI_4/XLXN_78	.X.X...X.....X.....	4	4
XLXI_4/XLXN_35	.X.X...X.....X.....	4	4
XLXI_4/XLXN_299	.X.X...X.....X.....	4	4
XLXI_4/XLXN_298	.X.X...X.....X.....	4	4
XLXI_4/XLXN_296	.X.X...X.....X.....	4	4
OFF	X...X.....	2	2
XLXI_4/XLXN_295	.X.X...X.....X.....	4	4
XLXI_4/XLXN_277	.X.X...X.....X.....	4	4
XLXI_15/XLXN_213	.....X.....X.....	2	2
$OpTx$FX_DC$4	.....XXX.....	3	3
MBUS<7>	..X.....XX.....	3	3
XLXI_15/XLXN_248	.....XX.....	2	2
	0----+----1----+----2----+----3----+----4		

```
*****************************  Equations  *****************************

********** Mapped Logic **********


$OpTx$FX_DC$3 <= ((MF AND XLXN_123 AND XLXN_96)
        OR (MF AND XLXN_123 AND XLXN_92.LFBK));


$OpTx$FX_DC$4 <= ((NOT XLXI_15/XLXN_286)
        OR (NOT XLXI_15/XLXN_42 AND XLXI_15/XLXN_49));


$OpTx$FX_DC$5 <= ((NOT STORE AND $OpTx$FX_DC$4)
        OR (XLXN_123 AND NOT XLXI_15/XLXN_286.LFBK));


CLEAR <= NOT ((NOT XLXI_15/XLXN_248 AND XLXI_15/XLXN_239 AND
        XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF));


GD_N <= ((NOT MF AND SD_N)
        OR (SD_N AND NOT XLXN_123)
        OR (MF AND TXE_N AND XLXN_123)
        OR (XLXN_123 AND NOT XLXN_96 AND NOT XLXN_92.LFBK));


MBUS_I(0) <= NOT (((XLXN_131 AND NOT ADCLB(0) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(0) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(0).PIN AND $OpTx$FX_DC$3)));
MBUS(0) <= MBUS_I(0) when MBUS_OE(0) = '1' else 'Z';
MBUS_OE(0) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(1) <= NOT (((XLXN_131 AND NOT ADCLB(1) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(1) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(1).PIN AND $OpTx$FX_DC$3)));
MBUS(1) <= MBUS_I(1) when MBUS_OE(1) = '1' else 'Z';
MBUS_OE(1) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(2) <= UBUS(2);
MBUS(2) <= MBUS_I(2) when MBUS_OE(2) = '1' else 'Z';
MBUS_OE(2) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(3) <= NOT (((XLXN_131 AND NOT ADCLB(3) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(3) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(3).PIN AND $OpTx$FX_DC$3)));
MBUS(3) <= MBUS_I(3) when MBUS_OE(3) = '1' else 'Z';
MBUS_OE(3) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(4) <= NOT (((XLXN_131 AND NOT ADCLB(4) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(4) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(4).PIN AND $OpTx$FX_DC$3)));
MBUS(4) <= MBUS_I(4) when MBUS_OE(4) = '1' else 'Z';
MBUS_OE(4) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(5) <= NOT (((XLXN_131 AND NOT ADCLB(5) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(5) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(5).PIN AND $OpTx$FX_DC$3)));
MBUS(5) <= MBUS_I(5) when MBUS_OE(5) = '1' else 'Z';
MBUS_OE(5) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(6) <= NOT (((XLXN_131 AND NOT ADCLB(6) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(6) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(6).PIN AND $OpTx$FX_DC$3)));
MBUS(6) <= MBUS_I(6) when MBUS_OE(6) = '1' else 'Z';
MBUS_OE(6) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST.LFBK);


MBUS_I(7) <= UBUS(7);
MBUS(7) <= MBUS_I(7) when MBUS_OE(7) = '1' else 'Z';
MBUS_OE(7) <= (NOT MF AND XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST);


MCLR_N_I <= ((XLXI_15/XLXN_27 AND NOT XLXI_15/XLXN_248 AND NOT XLXN_96 AND
        NOT XLXN_92.LFBK)
        OR (NOT STORE AND NOT XLXI_15/XLXN_248 AND NOT XLXN_96 AND
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        OR (NOT XLXN_123 AND NOT XLXI_15/XLXN_248 AND NOT XLXN_96 AND
        NOT XLXN_92.LFBK));
MCLR_N <= MCLR_N_I when MCLR_N_OE = '1' else 'Z';
MCLR_N_OE <= (XLXN_123 AND ML);


MD0 <= NOT PD0;


MD1 <= PD0
         XOR
MD1 <= PD1;


MD2 <= PD2
         XOR
MD2 <= (PD1 AND PD0);


MWRT_N_I <= NOT ((XLXN_123 AND XLXN_88.LFBK));
MWRT_N <= MWRT_N_I when MWRT_N_OE = '1' else 'Z';
MWRT_N_OE <= XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST;


OFF_I <= '0';
OFF <= OFF_I when OFF_OE = '1' else 'Z';
OFF_OE <= (XLXI_15/XLXN_239.LFBK AND $OpTx$FX_DC$4.LFBK);


SND <= ((XLXN_88 AND NOT XLXN_123 AND XLXN_149.LFBK)
        OR (MF AND NOT MWRT_N.PIN AND XLXN_123 AND XLXN_149.LFBK));


TCG <= (NOT XLXI_15/XLXN_27 AND NOT XLXI_15/XLXN_213 AND
        $OpTx$FX_DC$5);


UBUS_I(0) <= NOT (((XLXN_131 AND NOT ADCLB(0) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(0) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(0).PIN AND $OpTx$FX_DC$3)));
UBUS(0) <= UBUS_I(0) when UBUS_OE(0) = '1' else 'Z';
UBUS_OE(0) <= RCLK;


UBUS_I(1) <= NOT (((XLXN_131 AND NOT ADCLB(1) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(1) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(1).PIN AND $OpTx$FX_DC$3)));
UBUS(1) <= UBUS_I(1) when UBUS_OE(1) = '1' else 'Z';
UBUS_OE(1) <= RCLK;


UBUS_I(2) <= NOT (((XLXN_131 AND NOT ADCLB(2) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT ADCHB(2) AND NOT $OpTx$FX_DC$3)
        OR (NOT XLXN_131 AND NOT MBUS(2).PIN AND $OpTx$FX_DC$3)));
UBUS(2) <= UBUS_I(2) when UBUS_OE(2) = '1' else 'Z';
UBUS_OE(2) <= RCLK;


UBUS_I(3) <= MBUS(3);
UBUS(3) <= UBUS_I(3) when UBUS_OE(3) = '1' else 'Z';
UBUS_OE(3) <= RCLK;


UBUS_I(4) <= MBUS(4);
UBUS(4) <= UBUS_I(4) when UBUS_OE(4) = '1' else 'Z';
UBUS_OE(4) <= RCLK;


UBUS_I(5) <= MBUS(5);
UBUS(5) <= UBUS_I(5) when UBUS_OE(5) = '1' else 'Z';
UBUS_OE(5) <= RCLK;


UBUS_I(6) <= MBUS(6);
UBUS(6) <= UBUS_I(6) when UBUS_OE(6) = '1' else 'Z';
UBUS_OE(6) <= RCLK;


UBUS_I(7) <= NOT (((NOT ADCHB(7) AND NOT XLXN_131.LFBK AND NOT $OpTx$FX_DC$3.LFBK)
        OR (NOT ADCLB(7) AND XLXN_131.LFBK AND NOT $OpTx$FX_DC$3.LFBK)
        OR (NOT MBUS(7).PIN AND NOT XLXN_131.LFBK AND $OpTx$FX_DC$3.LFBK)));
UBUS(7) <= UBUS_I(7) when UBUS_OE(7) = '1' else 'Z';
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UBUS_OE(7) <= RCLK;


WCG <= ((XLXN_92.LFBK)
        OR (MF AND TXE_N)
        OR (TXE_N AND NOT XLXN_123)
        OR (NOT XLXI_15/XLXN_213 AND $OpTx$FX_DC$5)
        OR (NOT MF AND SD_N AND XLXN_123));


WRT <= ((XLXN_88 AND NOT XLXN_123)
        OR (MF AND NOT MWRT_N.PIN AND XLXN_123));

FDCPE_XLXI_15/XLXN_213: FDCPE port map (XLXI_15/XLXN_213,UBUS(3).PIN,RCLK,NOT XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF,'0
');

FDCPE_XLXI_15/XLXN_239: FDCPE port map (XLXI_15/XLXN_239,UBUS(0).PIN,RCLK,'0','0');

FDCPE_XLXI_15/XLXN_248: FDCPE port map (XLXI_15/XLXN_248,STORE,NOT XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF,NOT STORE,'0'
);


XLXI_15/XLXN_248/XLXI_15/XLXN_248_CLKF <= ((XLXN_123 AND MCLR_N.PIN)
        OR (NOT XLXN_123 AND NOT XLXI_15/XLXN_248 AND NOT XLXN_96 AND
        NOT XLXN_92.LFBK));

FDCPE_XLXI_15/XLXN_27: FDCPE port map (XLXI_15/XLXN_27,XLXN_123,COIN,NOT XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF,'0');

FDCPE_XLXI_15/XLXN_286: FDCPE port map (XLXI_15/XLXN_286,XLXI_15/XLXN_27.LFBK,NOT COIN,NOT XLXI_15/XLXN_42/XLXI_15/XLXN
_42_RSTF,'0');

FDCPE_XLXI_15/XLXN_42: FDCPE port map (XLXI_15/XLXN_42,XLXI_15/XLXN_27.LFBK,NOT XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF,NO
T XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF,'0');


XLXI_15/XLXN_42/XLXI_15/XLXN_42_CLKF <= (NOT STORE AND NOT REJ_N);


XLXI_15/XLXN_42/XLXI_15/XLXN_42_RSTF <= (XLXN_123 AND NOT XLXI_15/XLXN_248 AND XLXI_15/XLXN_239 AND
        MCLR_N.PIN);

FDCPE_XLXI_15/XLXN_49: FDCPE port map (XLXI_15/XLXN_49,XLXI_15/XLXN_27.LFBK,XLXI_15/XLXN_49_C,NOT XLXI_15/XLXN_42/XLXI_
15/XLXN_42_RSTF,'0');
XLXI_15/XLXN_49_C <= (PSB AND NOT XLXI_15/XLXN_286.LFBK);

FDCPE_XLXI_3/XLXN_506: FDCPE port map (XLXI_3/XLXN_506,XLXI_3/XLXN_506_D,WCLK,XLXI_3/XLXN_623.LFBK,'0');
XLXI_3/XLXN_506_D <= (NOT XLXN_88.LFBK AND NOT XLXI_3/XLXN_506.LFBK);

FDCPE_XLXI_3/XLXN_595: FDCPE port map (XLXI_3/XLXN_595,NOT XLXI_3/XLXN_623.LFBK,WCLK,XLXI_3/XLXN_623.LFBK,'0');

FTCPE_XLXI_4/XLXN_143: FTCPE port map (XLXI_4/XLXN_143,'1',NOT XLXI_4/XLXN_35,XLXI_4/XLXN_143_CLR,'0');
XLXI_4/XLXN_143_CLR <= (NOT XLXI_15/XLXN_213 AND NOT XLXI_15/XLXN_27.LFBK AND
        $OpTx$FX_DC$5.LFBK);

FTCPE_XLXI_4/XLXN_275: FTCPE port map (XLXI_4/XLXN_275,'1',NOT XLXI_4/XLXN_143.LFBK,XLXI_4/XLXN_275_CLR,'0');
XLXI_4/XLXN_275_CLR <= (NOT XLXI_15/XLXN_213 AND NOT XLXI_15/XLXN_27.LFBK AND
        $OpTx$FX_DC$5.LFBK);

FTCPE_XLXI_4/XLXN_277: FTCPE port map (XLXI_4/XLXN_277,'1',NOT XLXI_4/XLXN_275,XLXI_4/XLXN_277_CLR,'0');
XLXI_4/XLXN_277_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_295: FTCPE port map (XLXI_4/XLXN_295,'1',NOT XLXI_4/XLXN_85.LFBK,XLXI_4/XLXN_295_CLR,'0');
XLXI_4/XLXN_295_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_296: FTCPE port map (XLXI_4/XLXN_296,'1',NOT XLXI_4/XLXN_295.LFBK,XLXI_4/XLXN_296_CLR,'0');
XLXI_4/XLXN_296_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_298: FTCPE port map (XLXI_4/XLXN_298,'1',NOT XLXI_4/XLXN_299.LFBK,XLXI_4/XLXN_298_CLR,'0');
XLXI_4/XLXN_298_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_299: FTCPE port map (XLXI_4/XLXN_299,'1',NOT XLXI_4/XLXN_296.LFBK,XLXI_4/XLXN_299_CLR,'0');
XLXI_4/XLXN_299_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_35: FTCPE port map (XLXI_4/XLXN_35,'1',NOT XLXI_4/XLXN_78.LFBK,XLXI_4/XLXN_35_CLR,'0');
XLXI_4/XLXN_35_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);
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FTCPE_XLXI_4/XLXN_78: FTCPE port map (XLXI_4/XLXN_78,'1',NOT XLXI_4/XLXN_79.LFBK,XLXI_4/XLXN_78_CLR,'0');
XLXI_4/XLXN_78_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_79: FTCPE port map (XLXI_4/XLXN_79,'1',TCLK,XLXI_4/XLXN_79_CLR,'0');
XLXI_4/XLXN_79_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);

FTCPE_XLXI_4/XLXN_85: FTCPE port map (XLXI_4/XLXN_85,'1',NOT XLXI_4/XLXN_277.LFBK,XLXI_4/XLXN_85_CLR,'0');
XLXI_4/XLXN_85_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);


XLXI_6/XLXN_334/XLXI_6/XLXN_334_TRST <= ((XLXN_131 AND XLXN_123)
        OR (XLXN_130 AND XLXN_123));

FDCPE_XLXN_123: FDCPE port map (XLXN_123,UBUS(2).PIN,RCLK,'0','0');

FDCPE_XLXN_130: FDCPE port map (XLXN_130,XLXN_131.LFBK,XLXI_3/XLXN_595.LFBK,XLXN_130_CLR,'0');
XLXN_130_CLR <= (NOT XLXI_15/XLXN_213 AND $OpTx$FX_DC$5);

FDCPE_XLXN_131: FDCPE port map (XLXN_131,XLXN_131_D,XLXI_3/XLXN_595.LFBK,XLXN_131_CLR,'0');
XLXN_131_D <= (NOT XLXN_92.LFBK AND NOT XLXN_131.LFBK AND NOT XLXN_130.LFBK);
XLXN_131_CLR <= (NOT XLXI_15/XLXN_213 AND $OpTx$FX_DC$5);

FDCPE_XLXN_149: FDCPE port map (XLXN_149,UBUS(1).PIN,RCLK,'0','0');

FDCPE_XLXN_88: FDCPE port map (XLXN_88,XLXN_88_D,WCLK,XLXI_3/XLXN_623.LFBK,'0');
XLXN_88_D <= (NOT XLXN_92.LFBK AND NOT XLXN_88.LFBK AND
        XLXI_3/XLXN_595.LFBK AND NOT XLXI_3/XLXN_506.LFBK);

FDCPE_XLXN_92: FDCPE port map (XLXN_92,XLXN_92_D,XLXI_3/XLXN_595.LFBK,XLXN_92_CLR,'0');
XLXN_92_D <= (NOT XLXN_92.LFBK AND NOT XLXN_130.LFBK);
XLXN_92_CLR <= (NOT XLXI_15/XLXN_213 AND $OpTx$FX_DC$5);

FDCPE_XLXN_96: FDCPE port map (XLXN_96,'1',NOT XLXI_4/XLXN_298.LFBK,XLXN_96_CLR,'0');
XLXN_96_CLR <= (NOT XLXI_15/XLXN_27 AND $OpTx$FX_DC$5 AND
        NOT XLXI_15/XLXN_213.LFBK);


YF <= (MF AND NOT XLXN_123);


YL <= (NOT XLXN_123 AND ML);

Register Legend:
 FDCPE (Q,D,C,CLR,PRE);
 FTCPE (Q,D,C,CLR,PRE);
 LDCP  (Q,D,G,CLR,PRE);
```
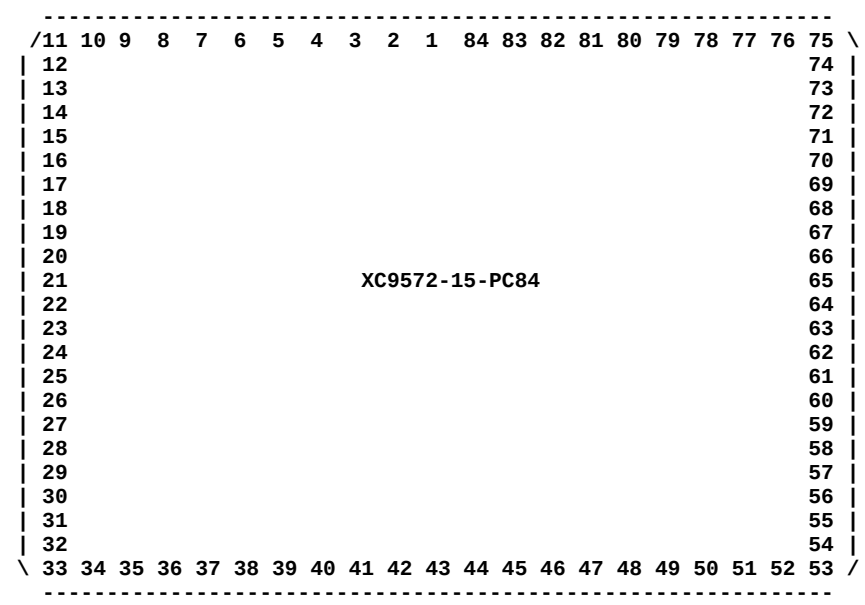

********** Device Pin Out **********

Device : XC9572-15-PC84



Pin No.	Signal Name	Pin No.	Signal Name
1	YF	43	ADCLB<0>
2	ML	44	ADCLB<1>
3	GD_N	45	ADCLB<2>
4	MWRT_N	46	ADCLB<3>
5	MCLR_N	47	ADCLB<4>
6	SD_N	48	ADCLB<5>
7	PGND	49	GND
8	GND	50	PGND
9	WCLK	51	ADCLB<6>
10	TCLK	52	ADCLB<7>
11	WCG	53	ADCHB<0>
12	RCLK	54	ADCHB<1>
13	TCG	55	ADCHB<2>
14	YL	56	ADCHB<3>
15	MF	57	ADCHB<4>
16	GND	58	OFF
17	PD2	59	TDO
18	PD1	60	GND
19	PD0	61	STORE
20	TXE_N	62	PSB
21	WRT	63	CLEAR
22	VCC	64	VCC
23	UBUS<7>	65	REJ_N
24	UBUS<6>	66	MBUS<7>
25	UBUS<5>	67	MBUS<6>
26	UBUS<4>	68	MBUS<5>
27	GND	69	MBUS<4>
28	TDI	70	MBUS<3>
29	TMS	71	MBUS<2>
30	TCK	72	MBUS<1>
31	UBUS<3>	73	VCC
32	UBUS<2>	74	MBUS<0>
33	UBUS<1>	75	PGND
34	UBUS<0>	76	PGND
35	SND	77	COIN
36	PGND	78	VCC
37	PGND	79	ADCHB<5>
38	VCC	80	ADCHB<6>
39	PGND	81	ADCHB<7>
40	PGND	82	MD0
41	PGND	83	MD1
42	GND	84	MD2

Legend : NC = Not Connected, unbonded pin
PGND = Unused I/O configured as additional Ground pin
TIE = Unused I/O floating -- must tie to VCC, GND or other signal
VCC = Dedicated Power Pin

```
        TDI  = Test Data In, JTAG pin
        TDO  = Test Data Out, JTAG pin
        TCK  = Test Clock, JTAG pin
        TMS  = Test Mode Select, JTAG pin
 PROHIBITED  = User reserved pin
```

********** Compiler Options **********

Following is a list of all global compiler options used by the fitter run.

Device(s) Specified	: xc9572-15-PC84
Optimization Method	: DENSITY
Multi-Level Logic Optimization	: ON
Ignore Timing Specifications	: OFF
Default Register Power Up Value	: LOW
Keep User Location Constraints	: ON
What-You-See-Is-What-You-Get	: OFF
Exhaustive Fitting	: OFF
Keep Unused Inputs	: OFF
Slew Rate	: SLOW
Power Mode	: STD
Ground on Unused IOs	: ON
Global Clock Optimization	: ON
Global Set/Reset Optimization	: ON
Global Ouput Enable Optimization	: ON
FASTConnect/UIM optimzation	: ON
Local Feedback	: ON
Pin Feedback	: ON
Input Limit	: 36
Pterm Limit	: 25