Tracor Northern

OPERATOR/TECHNICAL MANUAL
FOR

TN-1211A	TN-1241
TN-1212A	TN-1242
TN-1213A	TN-1243

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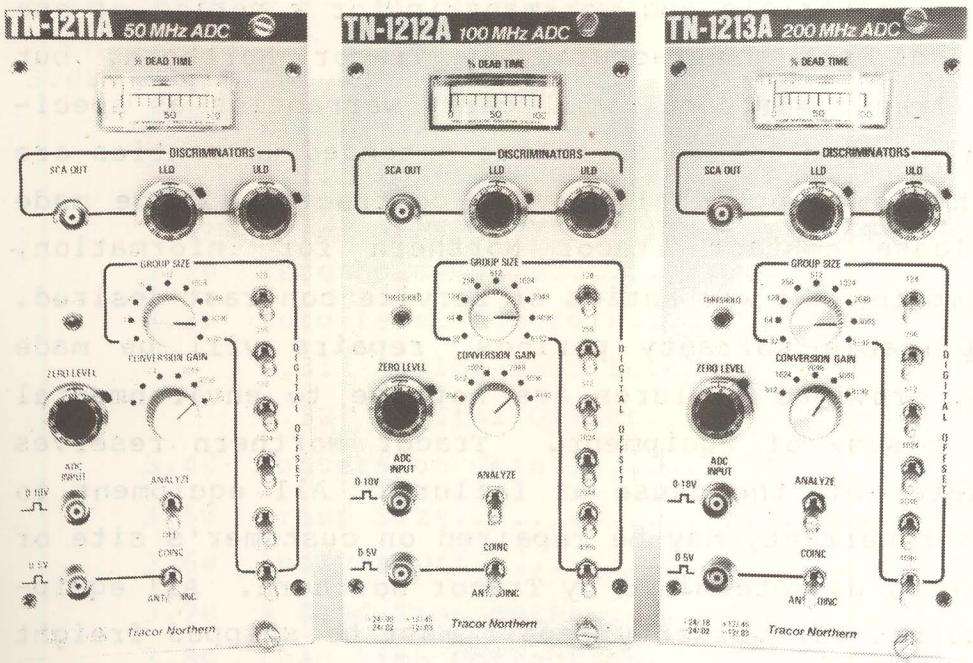
TN-1211A	TN-1241
TN-1212A	TN-1242
TN-1213A	TN-1243

TRACOR NORTHERN, INC.

Analog To Digital Converters

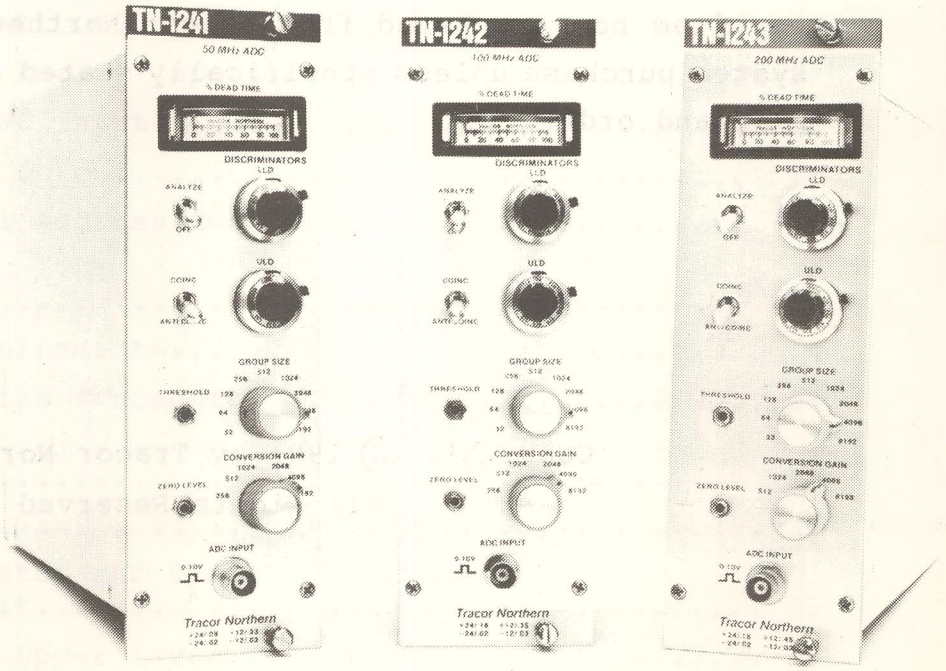
Operator/Technical Manual



TN-1211A

TN-1212A

TN-1213A



TN-1241

TN-1242

TN-1243

Tracor Northern

2551 West Beltline Highway / Middleton, Wisconsin 53562 / (608) 831-6511 / TWX-910-280-2521
Tracor Europa B.V. / Schiphol Airport Amsterdam / Building 106, The Netherlands / Telephone (020) 41 1865 / Telex 13695

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1.ØØ INTRODUCTION

This manual covers the following Analog-to-Digital Converters (ADCs): TN-1211A, TN-1212A, TN-1213A, TN-1241, TN-1242, and TN-1243. All six models are essentially identical from an operator's standpoint. Internally, the units use the same analog circuitry; only the integrated circuit types used in the converter logic are different. Logic input/output signals are identical to those of our previous modular ADCs, and these new models are interchangeable with older units by making a simple connector change.

As with previous Tracor Northern ADCs, the familiar Wilkinson conversion technique is employed. This method consists of charging a capacitor to the peak amplitude of an input pulse. At the conclusion of the charging process the capacitor is discharged linearly to zero. During the linear discharge a periodic pulse train (clock) is scaled into a binary scaler. The final binary address is directly proportional to the peak amplitude of the analog pulse since the scaling time is directly proportional to peak amplitude. The TN-1211A and TN-1241 use a 5Ø MHz clock for address encoding, the TN-1212A and TN-1242 use 1ØØ MHz, and the TN-1213A and TN-1243 use 2ØØ MHz. All scalers are of 13-bit capacity (8192 channels). The TN-1211A, TN-1212A, and TN-1213A include front panel selectable digital offset.

Extensive use of the latest linear integrated circuits (ICs designated in this text by U#) is made in these designs for improved linearity and stability. In the TN-1211A and TN-1241, Schottky-Clamped TTL is used for the high speed logic circuits. The TN-1212A, TN-1213A, TN-1242, and TN-1243 utilize Temperature-Compensated emitter-coupled logic (ECL) ICs in the high speed logic circuits. All six ADCs use new low power Schottky-Clamped TTL and CMOS where practicable for reduced power consumption. These ADCs also feature an adjustment-free logic scheme for the conversion process which provides reliable, stable performance without the need for special circuit precautions or component selection.

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2.ØØ GENERAL SYSTEM DESCRIPTION

The essentials of a data acquisition system using one of these ADCs are shown in Figure 1. Incident radiation at the detector is converted to an electrical signal pulse which is amplified and shaped before connecting to the ADC for conversion. The ADC accepts the analog signal and converts it into a binary address which is proportional to the peak amplitude of the input signal. At the end of the conversion the address is transferred to a memory unit or to a computer which has been suitably interfaced. At the end of transfer the ADC is reset and allowed to perform another conversion.

In addition to the basic function of converting an analog input into a binary address, the ADC performs several logic functions which greatly simplify its adaptation to any memory system. Memory systems and computers are available in a variety of sizes. Unless steps are taken to ensure ADC-to-Memory size compatibility, storage of erroneous data (i.e., address overflows) will result. Several logic functions are included in the ADCs to preclude storage of erroneous data due to address overflow, underflow, partial pulses, etc. Because these logic functions ensure system-size compatibility, only two logic signals are required to connect the ADC to any memory system. Of course, these two are in addition to the parallel connection of address data.

Figure 2 shows a timing diagram of the major signals involved in the conversion-data transfer-reset sequence. Signal STORE is generated approximately Ø.7 usec after conversion is complete. During this delay several tests are performed on the address: overflow, underflow (when using zero offset), and channel Ø (reserved for live-time storage). STORE is generated only if the address passes the acceptance tests performed, and then remains with the address data until a CLEAR is sent to the ADC from the memory unit. CLEAR is normally generated at the end of data transfer to the memory's input register, but there is no restriction on timing. Multiplexing of ADCs or other time-sharing operation of the computer/memory may preclude immediate response to a STORE signal. The address and STORE will remain until the memory is available to transfer data and generate the requisite CLEAR to reset the ADC.

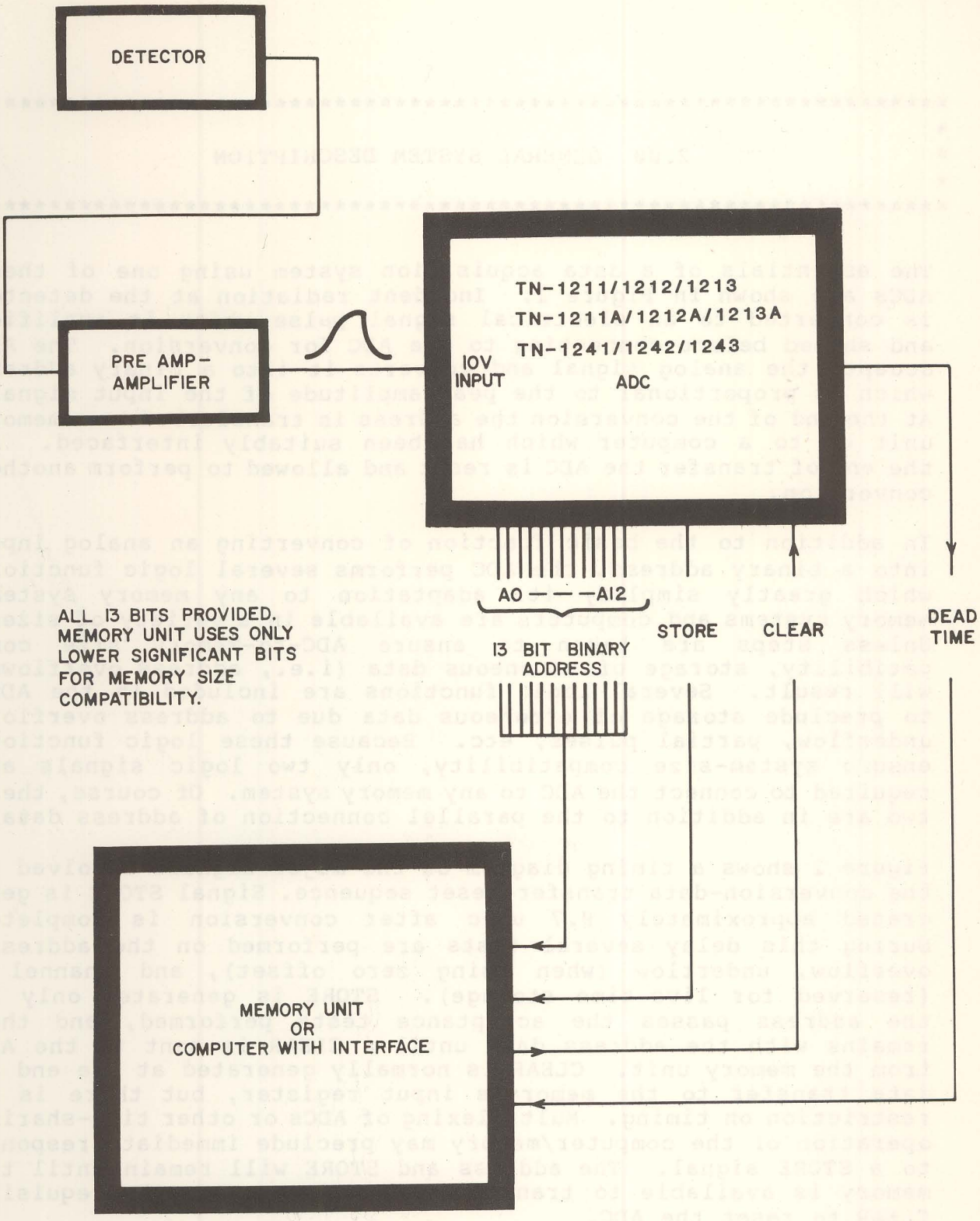
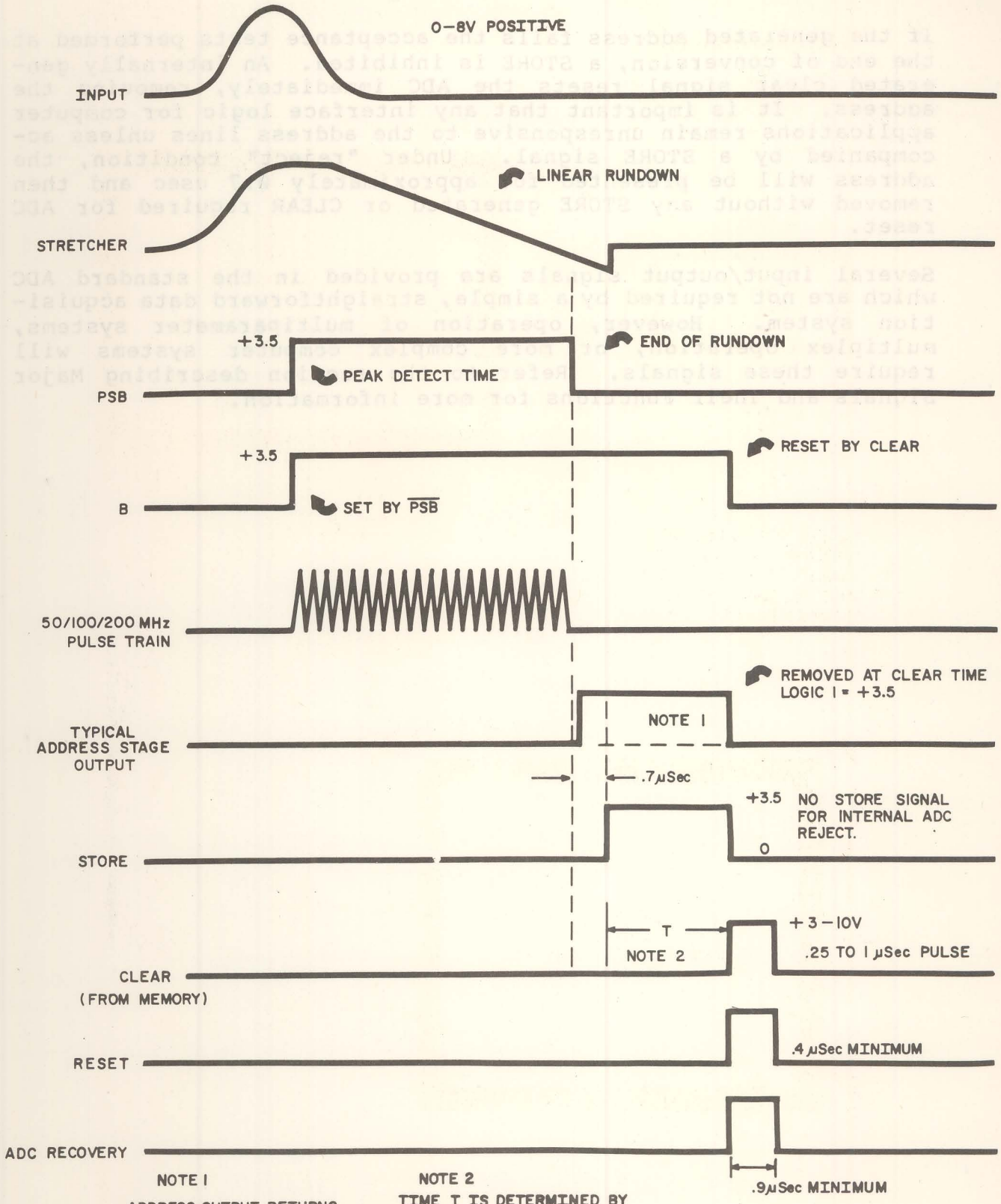


FIG. 1
BLOCK DIAGRAM OF SIMPLIFIED SYSTEM



NOTE 1

ADDRESS OUTPUT RETURNS TO 0V IN .7μSec UNDER INTERNAL REJECT CONDITIONS.

NOTE 2

TIME T IS DETERMINED BY MEMORY UNIT OR COMPUTER. ADDRESS AND STORE REMAIN UNTIL CLEAR IS RECEIVED BY ADC.

FIG. 2
ADC TIMING

If the generated address fails the acceptance tests performed at the end of conversion, a STORE is inhibited. An internally generated clear signal resets the ADC immediately, removing the address. It is important that any interface logic for computer applications remain unresponsive to the address lines unless accompanied by a STORE signal. Under "reject" condition, the address will be presented for approximately Ø.7 usec and then removed without any STORE generated or CLEAR required for ADC reset.

Several input/output signals are provided in the standard ADC which are not required by a simple, straightforward data acquisition system. However, operation of multiparameter systems, multiplex operation, or more complex computer systems will require these signals. Refer to the section describing Major Signals and Their Functions for more information.

3.00 OPERATING CONTROLS AND SPECIFICATIONS

3.10 DISCRIMINATORS

3.11 Lower Level (LLD)

Function: Sets lower limit on signals to be converted by the ADC. For a given signal, system dead time begins with the rise of the signal above LLD.

Range: 0-100% of the full-scale 0 to 8 volt conversion as set by the CONVERSION GAIN switch.

Control: 10-turn Helipot.

Stability: Maximum 100 ppm/^{o}C or 24 hours at constant temperature; typically 50 ppm.

3.12 Upper Level (ULD)

Function: Sets upper limit on signals to be converted by ADC. Dead time for signals above the upper limit is equal to signal time above the LLD to the end of signal above THRESHOLD.

Range: 5 to 125% of full-scale 8 V conversion.

Control: 10-turn Helipot.

Stability: Max. 100 ppm/^{o}C or 24 hours, typically 50 ppm.

3.20 THRESHOLD

Function: Discriminates the incoming signals from low level noise present in the system. This control determines the threshold level of input pulses to be analyzed by the ADC.

Range: -0.5 to +10% of full-scale, 8 volt conversion.

Control: 20-turn screwdriver-adjustable potentiometer.

3.30 ZERO LEVEL CONTROLS

3.31 Analog ZERO Level

Function: Adjusts the level of the analog input which corresponds to channel zero (extrapolated).

Range: -0.5 to 10% on 10-turn Helipot for the TN-1211A/1212A/1213A and a 20-turn trimpot on the TN-1241/1242/1243. Range refers to extrapolated zero intercept of a plot of channel number versus analog input amplitude.

Stability: 100 ppm/°C max, 20 ppm/°C typical; 100 ppm/24 hours at constant temperature; referred to full-scale analog input.

3.32 DIGITAL OFFSET (TN-1211A/1212A/1213A only)

Function: Digitally subtracts selected offset from converted address. Selection of DIGITAL OFFSET shifts the zero channel of storage memory to correspond to a desired ADC channel. Counts detected in ADC channels lower than the selected offset value are not stored in memory. The OFFSET switches are used in combination with the CONVERSION GAIN and GROUP SIZE selectors to analyze a segment of the full scale analog input range at a higher level of resolution.

Range: (0), 128, 256, ..., 4096 channels. Any additive combination of settings can be selected.

ADC Dead Time: Independent of digital offset for a given analog input.

Remarks: Underflow conversions (addresses less than 0 after offset subtraction) are rejected within the ADC; no STORE is generated and ADC is internally reset.

3.40 CONVERSION GAIN SWITCH

Function: Sets the number of channels corresponding to full scale analog input of 8 V. Switch selects magnitude of current effecting linear rundown of stretcher capacitor.

Positions: 256, 512, 1024, 2048, 4096, 8192 channels per 8 V input on TN-1211A, TN-1212A, TN-1241, and TN-1242. 512, 1024, 2048, 4096, 8192 channels per 8 V input on TN-1213A and TN-1243.

Stability: 100 ppm/°C max., 50 ppm/°C typical; 100 ppm/24 hours at constant temperature, referred to full scale analog input.

3.50 GROUP SIZE SWITCH

Function: Digitally sets upper limit on channel number to be stored in the memory unit. Addresses greater than the selected GROUP SIZE are automatically rejected within the ADC, and no STORE command is issued.

Range: 32 to 8192 channels in binary increments.

Remarks: Reject occurs when group size overflow is sensed after conversion. When digital offset is used, the group size begins with the effective "zero" channel; overflows are then sensed for channels beyond the selected group size + digital offset value.

3.60 ANALYZE/OFF SWITCH

ANALYZE Position: Normal operating position.

OFF Position: ADC is in DC reset condition.

Remarks: SCA output is present with the ANALYZE/OFF toggle switch in either position.

3.70 % DEAD TIME METER

Function: This meter indicates the percentage of time that the ADC is "busy" during data acquisition.

Dead time per event (Fixed + Variable) is as follows:

Fixed: 2.6 usec per conversion.

Variable: (0.005N + bp + tr) usec for TN-1213A
(0.010 + bp + tr) usec for TN-1212A
(0.020N + bp + tr) usec for TN-1211A

where N = converted ADC address
bp = input pulse rise time from LLD peak amplitude
tr = transfer time from ADC to memory.

The rise time of any signal above LLD will contribute to system dead time. If a signal falls below the LLD setting, it will not be converted by the ADC. Dead time for a pulse converted ends after address transfer to memory and the input has dropped below threshold. Note, the DEAD TIME meter also indicates input over threshold.

3.8Ø DEAD TIME CORRECTION (TN-1241/1242/1243 only)

Function: Switch in conjunction with an INput and OUTput BNC connector allows INTernal or EXTernal summation (logical OR) for total system DEAD TIME.

3.9Ø COUPLING (TN-1211A/1212A/1213A only)

Function: Switch provides direct, DC, connection or AC with baseline restorer to the ADC input. PASSIVE position provides AC coupling into a Robinson BLR (BaseLine Restorer). The ACTIVE position provides AC coupling into an operational amplifier with diode feedback. The DIRECT position provides DC coupling to the ADC.

4.00 CONNECTORS

4.10 FRONT PANEL

4.11 ADC Analog Input

Range: 0-10 V. Full scale with respect to the conversion gain is 8 V. The additional 25% overrange can be utilized by offsetting the ZERO LEVEL intercept and/or DIGITAL OFFSET by 25%.

Polarity: Positive unipolar.

Rise Time: 0.1 to 10 usec.

Fall Time: 0.1 to 10 usec; up to 5 usec is permissible but the linearity of the lower 5% of the range will be degraded.

Input Impedance: 1K ohm, DC connected to ground.

Coupling: Direct.

Remarks: This connector is also on the rear panel.

4.12 COINC or GATE Input

Positive 3 to 5 V signal performs coincidence function depending on position of COINC position switch.

Input Impedance: 3.3 K ohm, DC connected.

Timing Requirements: Refer to subsection 6.80.

Remarks: On the TN-1241/1242/1243, this connector is on the rear panel.

4.13 SCA OUTPUT

Function: Provides a logic pulse output (3.5 to 5 V, 0.5 usec) for each valid event at Peak Detect. The SCA OUTPUT is gated off by ADC BUSY, so only analyzed events will generate an output. The SCA OUTPUT is bracketed by the LLD and ULD discriminators such that a logic pulse is delivered for any event occurring within the LLD and ULD "window."

BNC Connector, output impedance = 50 ohms.

Remarks: The SCA output is present with the ANALYZER/OFF toggle switch in either position. On the TN-1241/1242/1243 ADCs, this SCA output is on the rear panel.

4.20 REAR PANEL ADDRESS CONNECTOR

Size: 37 pin "Rack and Panel" female connector.

Signals: Address, STORE, CLEAR, DT, plus several control input/output signals. Refer to subsection 8.20 for specific pin assignments and signal definitions.

Levels: Logic one = +3 V; Logic zero = 0 V.

The ADCs can also be ordered with a stabilizer connector. Refer to subsection 8.20 for pin assignments and signal definitions. Fixed Dead Time then becomes 3.0 usec.

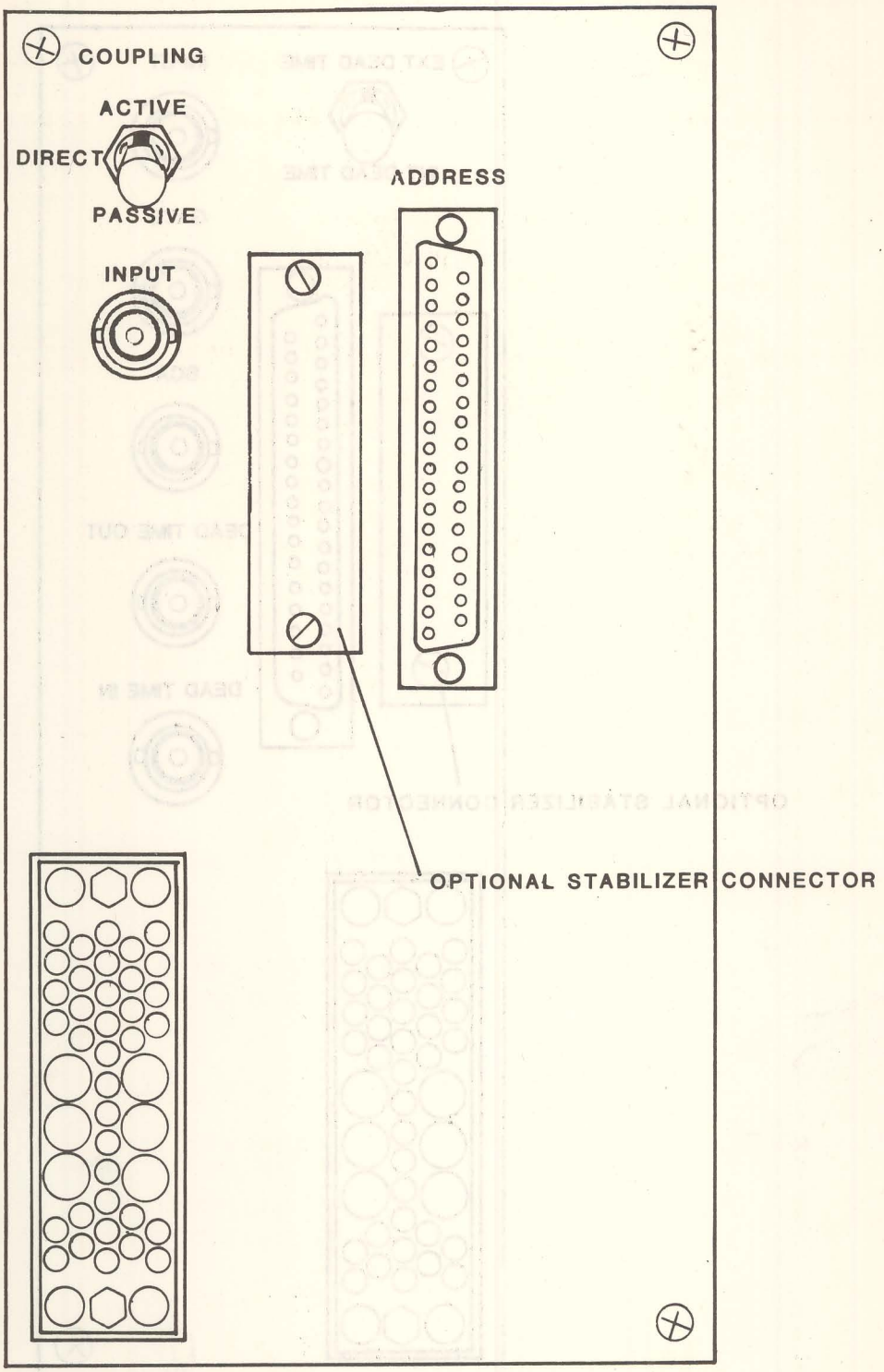


FIG. 3 TN-1211A/1212A/1213A REAR PANEL

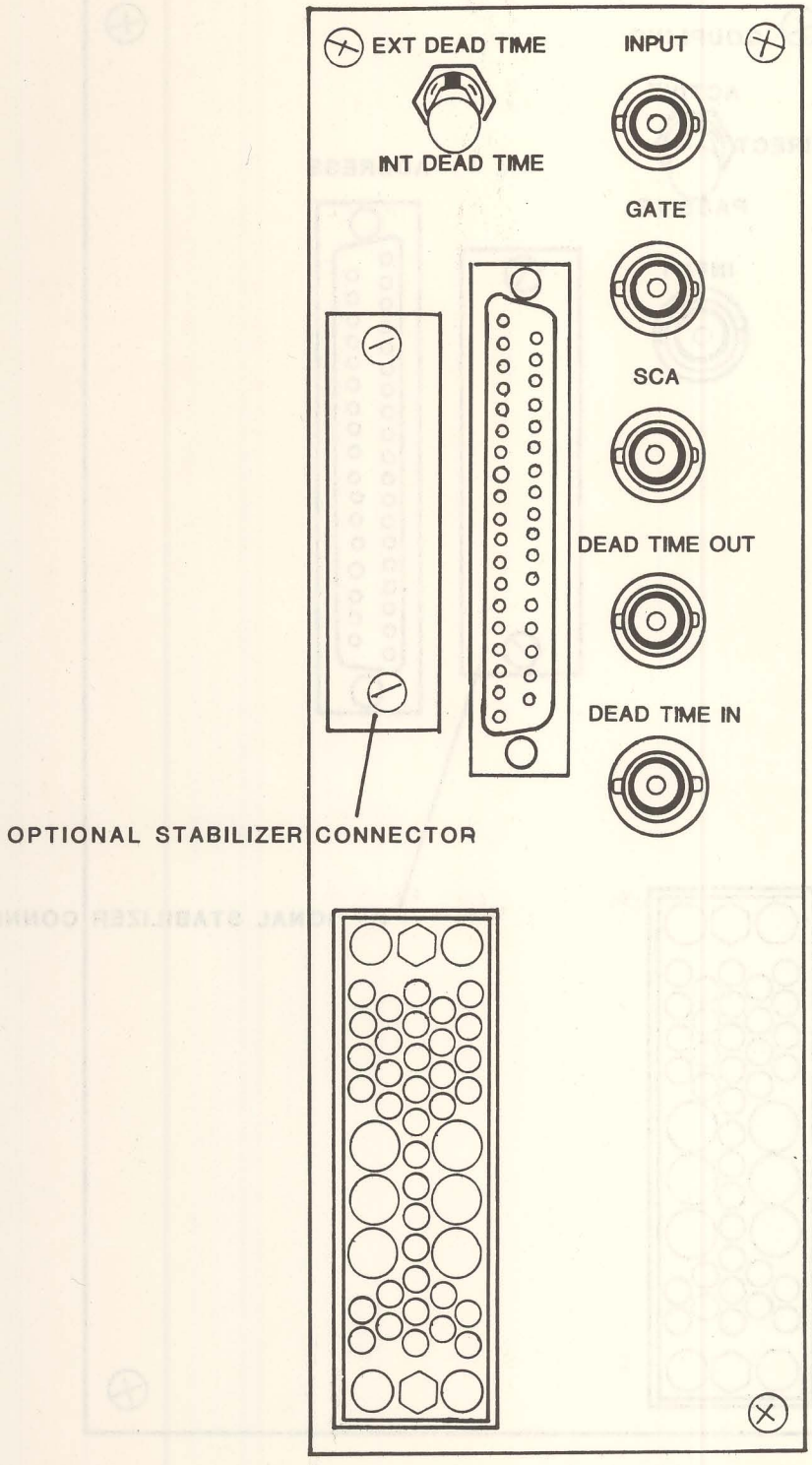


FIG. 4 TN-1241/42/43 REAR PANEL

5.00 INSTALLATION

5.10 POWER REQUIREMENTS

ADCs	+24 V	-24 V	+12 V	-12 V
TN-1213A:	200 mA	40 mA	450 mA	30 mA
TN-1212A:	110 mA	40 mA	450 mA	30 mA
TN-1211A:	70 mA	40 mA	370 mA	30 mA
TN-1243:	180 mA	20 mA	450 mA	30 mA
TN-1242	180 mA	20 mA	350 mA	30 mA
TN-1241	90 mA	20 mA	330 mA	30 mA

5.20 PROCEDURE

To install any of the ADCs, simply insert them in a standard NIM supply providing the proper power requirements (shown above).

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6.00 OPERATION

6.10 GENERAL

This section covers operation of the ADC in the pulse height analysis mode. The discussion here will pertain to the ADC connected to a Tracor Northern memory unit but the front-panel adjustments of the ADC are essentially the same when operating with a computer for data storage.

6.20 INITIAL SETUP AND OPERATION WITH THE MEMORY UNIT

Listed below are the switch positions and signal requirements which will ensure proper operation of the ADC and the memory unit after initial connection. It is assumed that the memory unit has been adjusted for the pulse height analysis mode of operation. If there is any question about proper switch positions for this mode, refer to the respective manual. This set-up procedure is for simple, straightforward pulse height analysis and does not utilize the full capabilities of the system. Subsections which follow cover the controls individually so that maximum acquisition efficiency can be achieved under more complex modes of operation.

To set up and operate the ADC:

a) Turn off the power on all units.

b) Connect the ADC to the memory unit using the appropriate cable.

c) Connect the signal source to the BNC input labeled ADC INPUT. Signal must be positive unipolar in the range of 0 to 10 V. (On the TN-1211A/1212A/1213A select the appropriate COUPLING.)

d) Set COINC/ANTI COINC switch to ANTI COINC.

e) Set ULD full clockwise (10.00 position).

f) Set LLD one-quarter turn from its full counterclockwise position (25 setting on small Helipot dial).

g) Set ZERO level at 50 small dial divisions.

h) Set CONVERSION GAIN to the switch position which corresponds to the memory size employed.

i) Set the GROUP SIZE switch to the same position as the CONVERSION GAIN switch.

j) Place all DIGITAL OFFSET switches off (down), if they are present.

k) Now energize the memory unit and the power supply in the NIM bin.

l) Place the ANALYZE/OFF switch on the ADC to the ANALYZE position.

m) Control the system with the START MEASURE and STOP pushbuttons on the memory unit or with the equivalent controls on the particular memory unit or computer employed.

The above procedure sets up the ADC for analysis of the entire range from LLD to full scale. The ZERO level is set close to 0,0 intercept (0.000 V in channel zero), and the Lower Level Discriminator is set slightly above maximum sensitivity. The THRESHOLD control is also set for approximate maximum sensitivity. If the % DEAD TIME meter reads 100% or if the DEAD TIME seems excessive for the input source count rate, the ADC may require some adjustment of the LLD or THRESHOLD controls. If so, refer to subsection 6.40 for the correct THRESHOLD adjustment procedure. Either the ADC ANALYZE OFF switch or the memory START MEASURE and STOP pushbuttons can be used to control analysis. The controls on the memory unit are preferred, however, because they also control operation of the clock/live timer in the memory unit. Accurate live time can be realized only when the memory unit pushbuttons are used to control analysis.

6.30 LOWER AND UPPER LEVEL DISCRIMINATORS

The lower and upper level discriminators are connected directly to the ADC input and are used to bracket the range of analog signals to be converted by the ADC. Internally, both discriminators are directly coupled to the ADC input. The range of the lower level discriminator extends below 0 volts, so that the full CCW position of the lower level discriminator Helipot will cause the discriminator to be triggered 100% of the time as indicated by 100% deflection on the dead time meter with no input signal. This is an improper operating LLD setting for the ADC, but the LLD was designed to accommodate small DC offsets of the input signal baseline when external restorers and DC input connec-

tion are used. The lower level discriminator is set for maximum sensitivity at the point where the dead time meter steeply drops from 100% to zero with no input signal. Operation at maximum sensitivity should be avoided, however, because any small drift in the system may cause the lower level discriminator to trigger 100% of the time. The maximum sensitivity point should be found experimentally and then the Helipot should be adjusted to approximately 5 small dial divisions above this point.

The upper level discriminator inhibits conversion of any signal above the upper level threshold. ADC dead time can be reduced considerably by adjusting the upper level threshold to be just above the maximum signal of interest. At low count rates this adjustment is not important but at high count rates considerable system dead time can be eliminated by proper setting of this control.

The upper and lower level discriminators should be adjusted to bracket the desired analysis region when using digital zero offset on the TN-1211A/1212A/1213A ADCs. With the discriminator set to convert the entire full scale spectrum, considerable dead time is used in converting signals which are later rejected by underflow and overflow tests performed after conversion. After the desired resolution and analysis region have been selected with the DIGITAL OFFSET, CONVERSION GAIN and GROUP SIZE controls, the upper and lower level thresholds should be adjusted to fall just outside the region of interest which has been bracketed digitally. Operation in this manner provides double selection of the analysis region or interest. The discriminators provide analog selection and reduce ADC dead time while the GROUP SIZE/DIGITAL OFFSET controls provide for logic functions which precisely select the region to be stored in the memory unit.

6.40 THRESHOLD

The function of the THRESHOLD control is to discriminate the incoming signals from the low-level noise present in the system. The THRESHOLD control is set at Tracor Northern and does not generally require further adjustment. However, since the INPUT is direct-connected, as are all internal analog circuits, it is possible for the signal source driving the ADC to disrupt proper operation. All adjustments made during checkout at the factory are made with a signal source whose baseline reference is 0.000 V. Most spectroscopy amplifiers/baseline restorers have a front panel DC offset or zero adjustment control. Adjusting this control for 0 ± 10 mV at the amplifier output will ensure proper ADC operation with no adjustment of THRESHOLD necessary. If this amplifier adjustment cannot be made, the following adjustment procedure will ensure proper THRESHOLD adjustment. Note that if the factory THRESHOLD

setting is changed, it should be rechecked if another signal source or amplifier is used or if the amplifier DC offset is changed.

To adjust the THRESHOLD setting:

a) Set up the ADC for normal PHA acquisition.

b) Connect the amplifier output to the ADC INPUT.

c) Turn the LLD one full turn clockwise from its counter-clockwise limit.

d) Remove the signal source so that amplifier output is essentially noise only.

e) Activate the system to ANALYZE or ACQUIRE DATA.

f) Turn THRESHOLD full counterclockwise or until the % DEAD TIME meter reads 1ØØ%.

g) Adjust THRESHOLD clockwise until a steep decrease in % dead time is observed; the % DEAD TIME meter should read virtually Ø% dead time.

h) Turn THRESHOLD one more turn clockwise.

i) Acquire data with a typical source at expected count rate and amplifier adjustments. Inspect the DEAD TIME meter and if dead time seems excessive for the count rate, turn THRESHOLD clockwise until ± 1/2 turn has little effect on % dead time. If more than one turn is required, check the amplifier pole-zero adjustment by using an oscilloscope and the amplifier manufacturer's instructions. Proper pole-zero adjustment is essential for proper ADC operation and dead time correction.

6.5Ø ZERO LEVEL ADJUSTMENT

Zero level is defined as that analog input level which corresponds to channel zero (extrapolated) in the stored analysis. By using the front panel ZERO LEVEL control, any analog input from zero through approximately Ø.4 volt can be adjusted to correspond to channel zero in the memory unit. The ZERO LEVEL control is analogous to the bias level on a biased amplifier; signals below the zero level are not converted by the ADC just as signals below this bias level are not amplified. As the ZERO LEVEL control is turned clockwise the channel number for a given energy is reduced. This has the effect of shifting the entire spectrum to lower channels when viewed from channel zero through 1Ø% of full scale. From the standpoint of the spectrum stored in the memory unit there is no difference

in the results obtained using the analog ZERO LEVEL control and the DIGITAL OFFSET switches. The main difference in the two, however, is that the analog zero level control does reduce the amount of dead time required for a given conversion. The digital offset switches operate on the address after conversion. That is, for a given energy, the conversion time is independent of the digital offset switch positions. By using analog offset, however, the dead time for a given conversion is reduced as the Zero Level intercept is increased. From a dead time standpoint only, analog adjustment would be preferred over digital offset of zero level. However, because the adjustment range of the analog ZERO LEVEL control is restricted to only Ø-1Ø% of the full scale input range, the DIGITAL OFFSET controls are usually preferred to selecting the zero level of the stored spectrum. The DIGITAL OFFSET controls, where they're available, are also more convenient in that they provide a simple means of shifting the spectrum by a binary fraction of the full scale conversion gain. Digital offset, conversion gain and memory group sizes are all in binary increments. The speed of the ADC is such that conversion times are low when digital offset is employed. For medium count rates the increased dead time is not significant, especially if the lower and upper level discriminators are adjusted properly to bracket the desired analysis region.

The ZERO LEVEL Helipot control is set to Ø.5Ø dial divisions at Tracor Northern for extrapolated true zero (Ø.ØØØ V in channel zero). Adjustment of the ZERO level control might be necessary if an external amplifier which has its DC level set greater than ± 5Ø mV is connected to the ADC INPUT, or when precise zero intercept calibration is required.

To adjust the ZERO LEVEL setting:

a) Acquire a PHA spectrum containing two known reference peaks (for example, Cs^{137}, which produces photopeaks at 32 KeV and 662 KeV). For precision, the reference peaks selected should be as widely separated as possible. In this example, do not use digital offset.

b) Calculate the KeV/channel by dividing the energy difference of the two reference peaks by the number of channels separating the two peaks. Suppose, for example, that the Cs^{137} 32 KeV peak centroid is in channel 58 and that the 662 KeV peak centroid is in channel 1Ø1Ø. The difference in energy is 662 - 32 = 63Ø KeV, and the number of channels separating the peaks is 1Ø1Ø - 58 = 952; the energy-per-channel is thus 63Ø/952 = Ø.66 KeV/channel.

c) Calculate the channel number that a particular reference peak centroid should be in to yield Ø KeV in channel zero. This is obtained by dividing the reference peak energy by the energy-per-channel. In our example, 32 KeV - Ø.66 KeV/channel = channel 48.

d) Locate the desired channel (48 in our example) by using the CURSOR, BUG, or equivalent function on your memory/display unit. Acquire a spectrum and adjust the ZERO LEVEL control until the reference peak centroid falls in the correct channel. It is helpful to repeatedly CLEAR DATA while adjusting the ZERO LEVEL control.

Note that changing the amplifier GAIN control effects a change in peak separation (KeV/channel), while changing the Z control effects a uniform shift of the spectrum (energy peaks move with a fixed separation). A plot of energy vs. channel number would follow the equation for a straight line; that is,

$$y = mx + b$$

where y = energy, m = energy/channel (slope), x = channel number, and b = energy (y) intercept. Changing the amplifier GAIN control changes the value of m, while changing the ZERO LEVEL control changes the value of b. In steps c) and d) above we have set b equal to zero.

While the analog zero level control performs the same function as the bias level on a biased amplifier, the disadvantages associated with biased amplifiers are not found in the ADC. It is normal for a biased amplifier to bias off the lower portion of the input signal with a resultant change in pulse shape for signals above the bias level. These ADCs, however, employ a different design technique whereby the signal as seen by the pulse stretcher is independent of the ZERO LEVEL control setting. The significant advantages of this technique are that the ADC linearity is independent of zero level adjustment, and also the ADC stability is not dependent on zero level setting. The next section (7.ØØ) on System and Circuit Design provides details on how this is accomplished.

6.6Ø CONVERSION GAIN

Front panel switch positions on the CONVERSION GAIN switch indicate the address generated for nominal 8 volt analog input signal. This switch then effectively adjusts the resolution of the ADC since the number of discrete channels that the full scale Ø to 8 V analog input range will be sorted into is a function of the setting of this switch. Internally this switch adjusts the magnitude of the rundown current which effects linear discharge of the stretcher

capacitor. If the entire energy range from zero to full scale is to be analyzed, the CONVERSION GAIN switch is set to the number which corresponds to the memory size employed. The ADC may be operated at higher resolution settings than this but only by viewing a smaller portion of the entire spectrum. For example, if a 1Ø24 channel memory is the size in use, then in order to view the entire voltage range from zero to 8 volts the conversion gain must be operated in the 1Ø24 position. The conversion gain may be operated at a setting of 8192, however, if only one-eighth of the spectrum is to be stored. The CONVERSION GAIN switch is adjusted first for the resolution desired; then DIGITAL OFFSET is used to shift the analysis region of interest into the memory size employed (e.g., memory channels Ø through 1Ø23). CONVERSION GAIN is thus selected to correspond to the spectral resolution desired and the size of the data storage memory employed.

6.7Ø GROUP SIZE SWITCH

The GROUP SIZE switch is essentially a digital upper level discriminator adjustment which sets the maximum address that will be transferred to the memory unit. This is accomplished by testing each conversion for an address greater than the number selected on the front panel GROUP SIZE switch. Addresses above the number selected cause STORE to be inhibited and the ADC to be reset internally. The overflow tests are performed after conversion so that digital offset is subtracted before the tests are performed. This means that the group size as selected refers to the number of channels above the effective zero channel. Conversions below channel zero are also rejected when underflow is sensed in the ADC.

In normal single parameter analysis, the GROUP SIZE switch is set to the position which corresponds to the memory size employed. If the memory unit or computer is being used at something less than full memory (quarters, halves), the switch position should correspond to the size of the memory group being used. Switch positions corresponding to very small group sizes, 32 and 64 channels for example, are provided for two parameter analysis in a 32 x 32 or 64 x 64 configuration of two ADCs. Where only 32 or 64 channels along one axis are being used, digital offset will most probably be employed. The DIGITAL OFFSET and GROUP SIZE switches provide for selecting a 32 or 64 channel region of interest with the ADC operating at much higher resolution (CONVERSION GAIN).

6.8Ø COINCIDENCE/ANTI-COINCIDENCE OPERATION

A front panel BNC is provided on the ADC for acceptance of a Ø to 5 V signal for coincidence or anti-coincidence operation of the ADC. A toggle switch next to the BNC controls the operating mode. Connection is direct so that this input may be used as an auxiliary start-stop control of the ADC using a logic signal. Circuitry is such that this input can also be used for time coincidence operation of the ADC.

6.81 Coincidence Operation

With the toggle switch in the COINC position, a linear gate in the stretcher input is held closed, such that the ADC cannot accept any unaccompanied analog input for conversion. Only those analog input signals accompanied by a positive 3.5 to 5 volt pulse will be accepted by the ADC for conversion. All other logic functions, both analog and digital in nature, will still apply to the subsequent conversion. The lower and upper level discriminators, zero level controls, digital offset, and group size functions operate in normal fashion so that acceptance of a signal by the ADC does not necessarily mean it will be transferred to memory. Timing requirements for the application of the 3.5 to 5 volt coincidence signal are fairly straightforward and non-critical. Pulse rise time for the coincidence input should be somewhere in the range between 25 and 25Ø nanoseconds. The coincidence pulse must arrive at the input no later than Ø.5 microsecond before the analog input signal reaches its peak amplitude. There is no delay line in the ADC so that an external delay line may be necessary to allow time for the external coincidence circuitry to make its decision. Application of the coincidence input opens the ADC linear gate and the signal passes through the open gate and connects to the stretcher circuitry. When the signal reaches peak amplitude, the peak detector is triggered. At peak detect time the linear gate is closed even if the coincidence input remains.

The duration of the coincidence input must be long enough to hold the linear gate open until it is closed by the ADC at peak detect time. The suggested pulse duration is one-quarter microsecond greater than baseline-to-peak time of the analog input signal.

During the conversion process the ADC BUSY signal keeps the linear gate closed and additional coincidence inputs have no effect on the conversion process. Once the ADC is reset, either by internal reject of a conversion or at the time a CLEAR signal is received from the memory unit, the coincidence input is again operative.

6.82 Anti-Coincidence Operation

Pulse requirements for anti-coincidence operation of the ADC are less stringent than for the coincidence mode. To inhibit an analog input, the anti-coincidence input must switch from Ø to 3.5-5 volts before a peak detect time and must hold for approximately 4ØØ nanoseconds thereafter. Pulse durations longer than the 4ØØ nanosecond minimum, or pulses applied before peak detect time, have no effect on operation. Pulses of approximately two microsecond duration applied at the same time the analog signal is applied are suggested when analyzing one to two microsecond input pulses. The dead time for an analog input which is inhibited is equal to the analog input time beginning at LLD to the end of threshold. The COINC input can be used as an auxiliary analyze-stop control for the ADC. The anti-coincidence input signal is not included in ADC dead time however, so that accurate live time operation cannot be realized if this mode of operation is used to control analysis.

6.83 Analyzing DC or Slowly Varying AC Signals

DC or slow AC signals can be analyzed by the ADC by sampling at its input. The COINC/ANTI COINC switch should be set to the COINC position corresponding to the coincidence pulse. A positive 3.5 to 5 volt pulse source is required at the COINC input to strobe the ADC input. The pulse duration should be a minimum of one microsecond and a maximum of 4 microseconds. Operation is as follows. With the COINC/ANTI COINC switch in the COINC position, the linear gate is held closed. The DC applied at the ADC input is connected to the linear gate but is blocked. Application of a 4 volt, one microsecond pulse at the coincidence input opens the linear gate for one microsecond. This effectively generates a one microsecond pulse at the linear gate with a peak amplitude equal to the DC input. The ADC converts the one microsecond pulse in identical fashion to normal pulse inputs. All front panel controls are operative in this mode.

For analysis of slow AC signals, the ADC front panel controls are set up the same as for DC signals. The ADC operated in this mode will convert only the positive portion of the AC input. Internal circuitry clips the negative portion of any input and coincidence pulses applied at this time will not produce conversions. If analysis of the entire signal is required, the AC signal must be superimposed on a DC reference such that the input to the ADC is always positive with respect to ground. As with DC inputs, all front panel controls remain operative so that the discriminators, zero level, conversion gain, and digital offset controls can be used to bracket a region of interest. Once the ADC has accepted an input for analysis, the busy signal holds the linear gate closed until the ADC is ready to accept another pulse. Application of additional coincident pulses will not affect the conversion of the accepted input.

6.90 BASELINE RESTORERS, COUPLING (TN-1211A/1212A/1213A only)

A choice of either DIRECT COUPLING, ACTIVE or PASSIVE baseline restoration is provided in the ADC. If the ADC is to be operated with external baseline restoration, the COUPLING should be switched to DC and both internal restorers will be switched out. The DIRECT position is also used when the ADC is converting DC or slow AC signals. The choice of baseline restorers under normal operating conditions is left to the user with the following guidelines. For bipolar pulses the passive restorer must be used. For unipolar input pulses at low count rates the passive restorer will yield a somewhat higher resolution than the active. In general, because the passive restorer will accept bipolar inputs, proper pole-zero, or delay line clipping adjustments are not so critical as for the active restorer. The disadvantages of the passive restorer are as follows: First, the recovery to true baseline for a well-adjusted unipolar input is considerably longer than with the active baseline restorer. In fact, recovery to the true baseline for a passive BLR may be faster with a slight overshoot on the trailing edge of the pulse. Second, the input impedance at the ADC input is a function of signal level. This is characteristic of passive restorers and is due to the non-linear diode turn-off. In these ADCs the impedance change introduces a small zero level shift and differential non-linearity in about the lower 3% of the analog input range. In many applications this small non-linearity is offset by the improved resolution afforded by baseline restoration. The degree of non-linearity is a function of both pulse shape and pulse duration. The coupling capacitor, C5, as installed at the factory is a compromise between best lin-

earity on the low end and fastest recovery. The recovery time of the restorer can be improved by reducing the capacitor from its normal Ø.Ø22 microfarad down to Ø.ØØ5 or even Ø.ØØ1 microfarad. Reducing the capacitor size, however, will make the low end non-linearity and zero level shift more pronounced. In fact, the non-linearity may extend into the lower 5% of the range. For a given pulse shape the non-linearity will remain constant and repeatable so that differential linearity checks could be performed and subsequent correction factors applied to the analyses.

The ACTIVE baseline restorer employs an operational amplifier with diode-connected feedback at the ADC input. The impedance to positive signals is very high while the impedance to negative signals is very low due to the operational amplifier. Because of the high impedance to positive inputs there is very little charge gained on the coupling capacitor during the normal pulse input. When the signal returns to zero the charge gained is quickly discharged through the low impedance at the operational amplifier input. The impedance ratio is such that the charge gained on the positive input is lost within three microseconds after the input pulse returns to baseline. While the active restorer provides for very rapid discharge of the capacitor and return of the ADC input to zero, it has some disadvantages when operating with normal nuclear pulse amplifier outputs. First, the input signal must very accurately return to zero because any excursion below the baseline will cause the capacitor to gain an erroneous charge very quickly. Second, amplifier noise is not unipolar in nature, that is, while the pulse out of the amplifier may be unipolar, the noise makes excursions both positive and negative with respect to the baseline. The baseline restorer will keep the coupling capacitor charged to the average negative excursion made by system noise. The net effect is that the baseline itself is determined by noise, and in the final analysis the resolution of the system may be poorer than if the passive baseline restorer were used. Under high count rate conditions the active baseline restorer will definitely improve the resolution over what will be achieved with a passive restorer. At some count rate there is a crossover between the loss of resolution due to amplifier noise. In general, the active baseline restorer should be used only with amplifiers equipped with pole zero cancellation so that the output pulse returns to the baseline very closely. The characteristics of the active restorer are such that it does not introduce the non-linearity associated with the passive restorer in the lower 3 to 5% of the input range. After careful adjustment of the amplifier, the best operating position of the restorer switch should be determined experimentally. At low count rates there is no question but that the passive restorer will be preferred over the active. At medium count rates with carefully adjusted amplifier there may be some advantage to the active

restorer. At high count rates the active restorer will definitely prove superior to the passive in high resolution systems, after careful pole zero cancellation adjustments.

7.00 SYSTEM AND CIRCUIT DESIGN

7.10 GENERAL

This section provides detailed coverage of the ADC logic circuits, signal timing, and circuit design. Block diagrams and timing diagrams are provided to facilitate explanation of the basic operation. Transistor and integrated circuit numbers are used on the block diagram to simplify cross referencing of logic blocks to the circuits. A section just prior to the schematics contains general notes which explain the symbols used on our schematics and block diagrams. Spending a few minutes studying this section will greatly simplify understanding the various signal sources and loads throughout the unit. The circuitry contained on the ADC board is shown on one schematic. A second schematic shows all front panel controls and switches. Finally, a list of major signals and their functions is included to cover the signals which may be omitted in the text. This list explains the function of all major signals found in the TN-1211A/1212A/1213A and in the TN-1241/1242/1243.

In the discussion of the system and circuit design which follows, no attempt is made to discuss the block diagram and schematics separately. Rather, the block diagram and systems are discussed in detail and reference is made to individual circuits only where their complexity warrants further discussion. The system is separated into two sections to simplify explanation. The first section will deal with the basic component parts of the ADC. The second section will deal primarily with logic functions which occur after the conversion process and involve the store and reset circuitry of the ADC.

7.20 THE BASIC ADC CIRCUITRY

7.21 ADC Input Circuits

Refer to the block diagrams of Figures 5 and 6 and the respective board schematic for the circuits covered in this section. Figure 7 is a timing diagram of the analog and logic signals for the basic ADC.

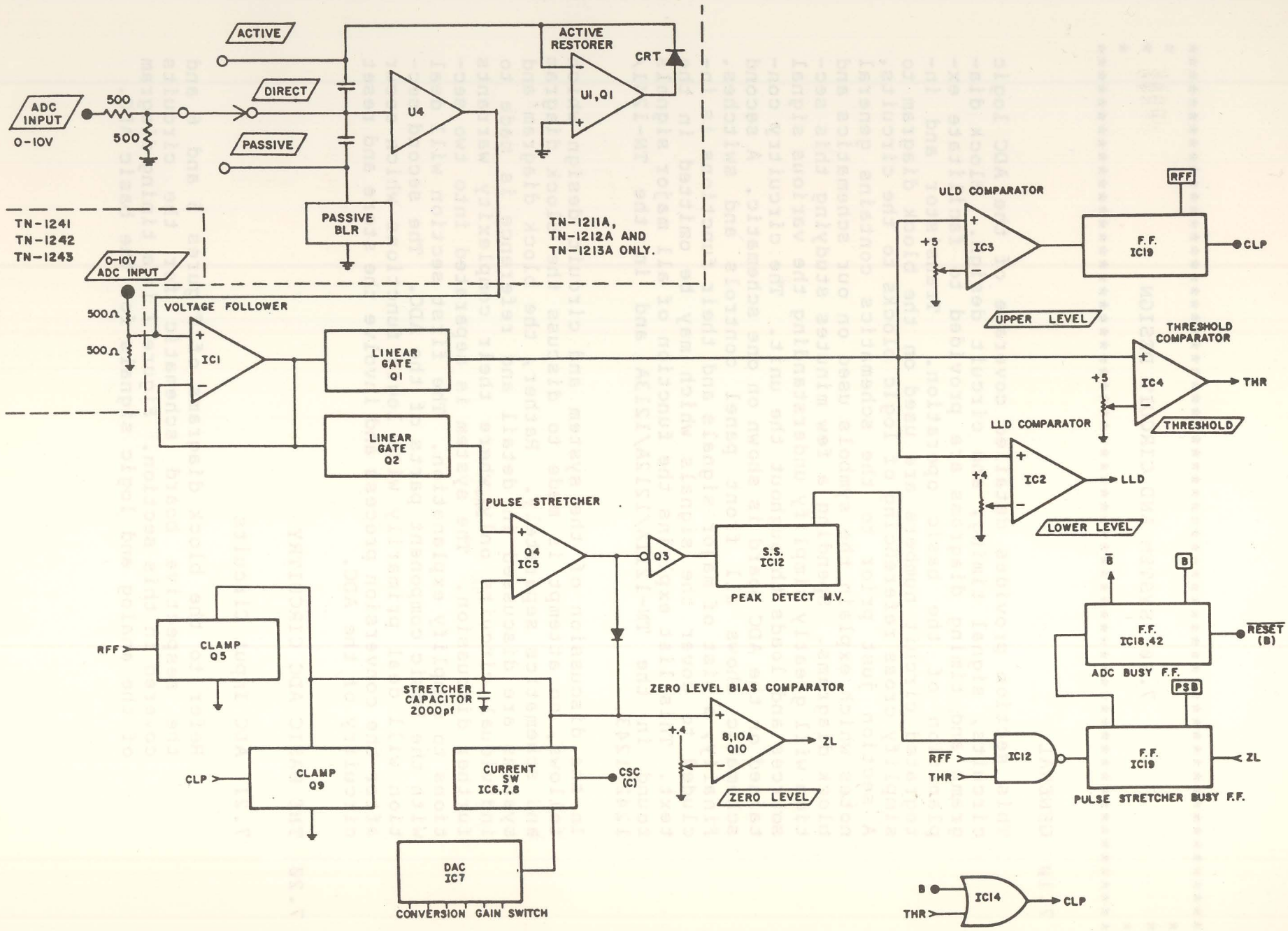
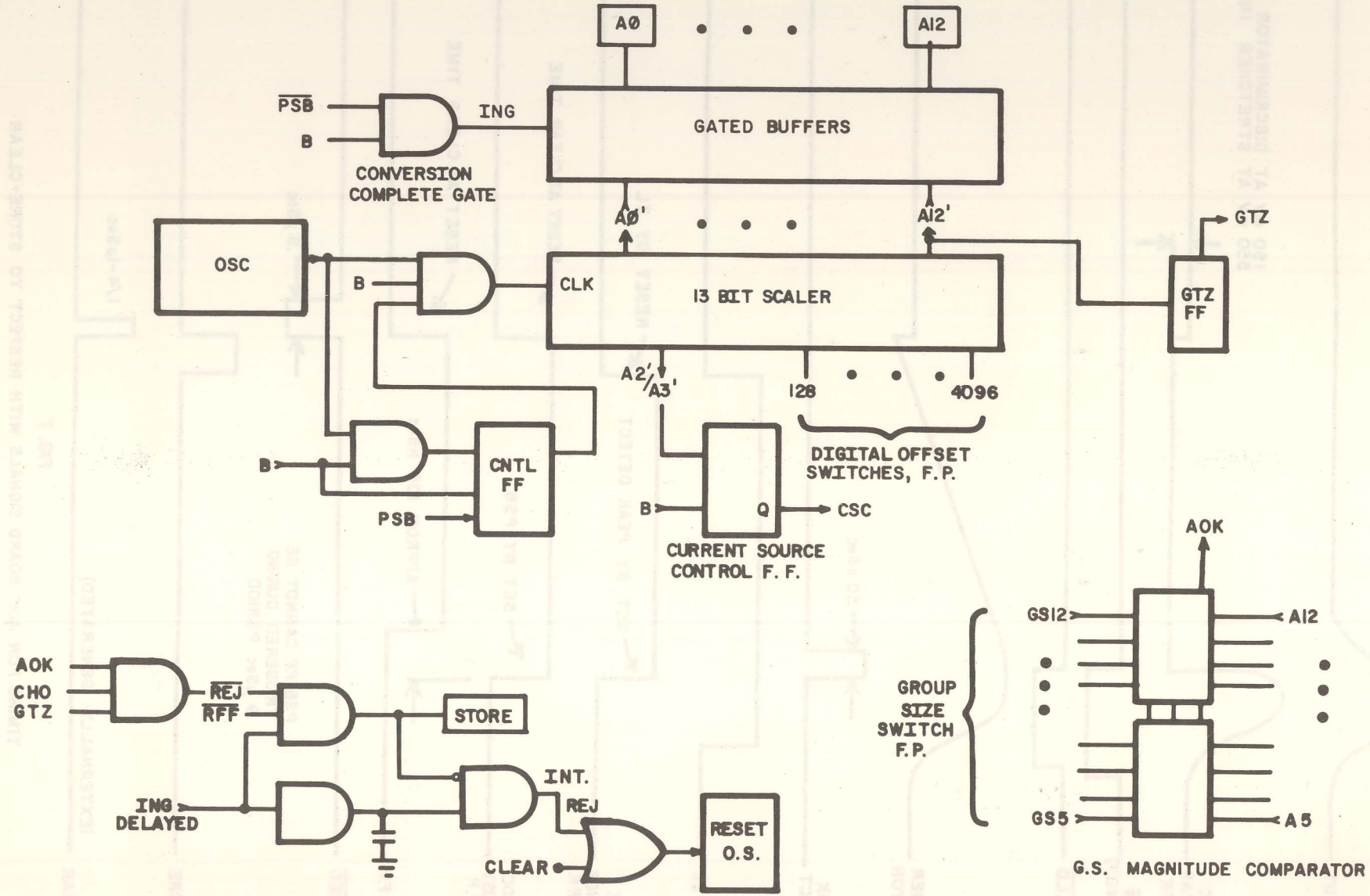


FIG. 5

BLOCK DIAGRAM OF BOARD ANALOG CIRCUITS



BLOCK DIAGRAM OF DIGITAL CIRCUITS

FIG. 6

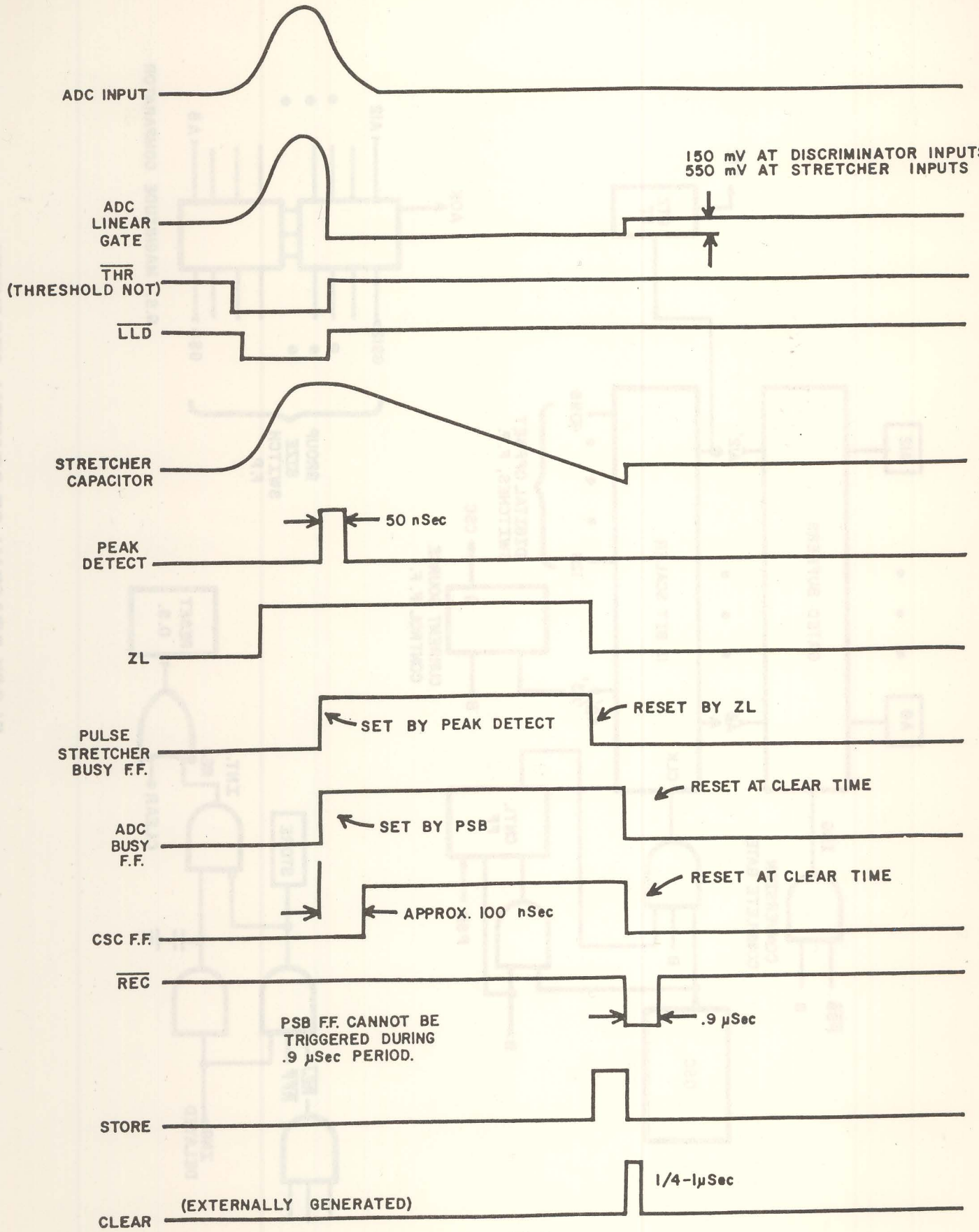


FIG. 7

TIMING FOR ADC BOARD SIGNALS WITH RESPECT TO STORE-CLEAR

The signal connected to the ADC INPUT BNC is attenuated by a factor of 2 by 2 metal film precision resistors at the amplifier input. This means that all the analog circuitry in the ADC operates on a Ø to 5 volt signal rather than the Ø to 1Ø volt input. The resistor values may be changed by the user if he desires some input range other than Ø to 1Ø volts. If the resistors are changed to give different attentuation ratios, the Thevenin source impedance should be at or below 5ØØ ohms.

On the TN-1211A/1212A/1213A the function of the attenuating resistors connects to an analog switch, U3, on the Baseline Restorer board where baseline restored or DIRECT coupling is selected. The rear panel COUPLING switch along U2 control U3 to select PASSIVE BLR, DIRECT or ACTIVE BLR COUPLING. For example, when $\overline{\text{PAS}}$ is GNDed U3 pin 16 is at a logic 1. The corresponding section of U3 is on and the passive BLR (BaseLine Restorer) is enabled. The passive baseline restorer is composed of two back-to-back diodes, CR4 and 5, with one referenced to ground. A potentiometer adjustment is provided to adjust diode drops to be exactly equal such that with the baseline restorer connected the ADC reference is at ground. The active bseline restorer is composed of an operational amplifier, U1 and Transistor 1. Again, a potentiometer adjustment is provided to adjust the baseline reference to be ground. The active baseline restorer operates in the following manner. Pin number 9 of U1 is the input of a darlington differential transistor pair, and is the inverting input of an operational amplifier whose feedback loop is closed by the diode between the collector of transistor 1 and U1 pin 9. In the quiescent state, the only current through the diode is the base current into pin 9, approximately 1/2 microamp. Positive input signals are inverted by the restorer and the collector of transistor 1 swings negative, turning off the diode which closed the feedback loop. For positive inputs the amplifier operates essentially open loop and the input impedance at pin 9 is very high because of the darlington connected input transistors. When the input signal returns to zero and tries to swing negative, the amplifier amplifies this negative excursion and the positive output at Q1 collector causes the diode to conduct and clamp pin Ø at ground. The coupling capacitor at the ADC input discharges very rapidly through the diode. The impedance ratios and time constants are such that the capacitor is discharged in approximately 3 microseconds. The output is buffered by U4, an LM-31Ø on the BLR board on all three ADCs (TN-1211A/1212A/1213A).

A LM-310 operational amplifier forms the input circuitry to the ADC. This IC type is a gain-of-one voltage follower by design. The output of this stage connects to both the stretcher/peak-detector circuitry and to the threshold and the lower and upper level discriminators. Each signal path is equipped with a linear gate, Q1 for the discriminators, and Q2 for the ADC's stretcher.

7.22 Stretcher/Peak Detector Circuitry

Another operational amplifier composed of transistor 4 and U5 form the pulse stretcher for the ADC. The amplifier is operated as a gain-of-one voltage follower with the circuit modified to perform pulse stretching. The incoming positive pulse is applied to pin 9 of U5. The amplifier loop is closed by means of a diode from the collector of Q4 to the inverting input of the amplifier at pin 3 of U5. The stretcher capacitors are also connected at pin 3. As the input signal goes positive, the diode conducts and pin 3 follows the input signal up to peak amplitude. As the signal passes through peak amplitude, pin 3 remains at peak voltage due to the stretcher capacitors. The loop now opens because of the polarity reversal at the diode closing the loop. The collector of Q4 swings negative with respect to ground and turns on transistor 3, which amplifies the negative signal. The amplified signal at the collector of 3 is used to trigger the peak-detect monostable found in U12. The output at pin 8 of U12 serves as a Peak-Detect strobe. The strobe is ANDed with LLD and $\overline{\text{RFF}}$ in U12. The output pulse at pin 8 (PD) is present for signals above the lower level discriminator threshold, provided that the Reject Flip-Flop is not set. The Peak-Detect strobe signal (PD) at U12 pin 8 connects to a NAND gate, U17 pin 12, where ADC conversions are controlled by mode signal $\overline{\text{OFF}}$ at pin 2 of U16. Signal $\overline{\text{OFF}}$ is at zero when the front panel ANALYZE-OFF switch is in the OFF position so that no ADC conversions are triggered by logic circuitry which follows this gate.

Pin 11 of U17 switches negative for approximately 50 nanoseconds and sets the Pulse Stretcher Busy flip-flop U19, on the trailing edge of the pulse. Signals $\overline{\text{PSB}}$ and PSB, the outputs of the flip-flop, are used to trigger logic circuits which effect a conversion. To prevent the start of conversion, Reject Flip-Flop (RFF) must be set before the Peak-Detect clocks the PSB flip-flop. At this time it is important to understand the relationship of the Peak-Detect strobe with respect to the pulse stretcher, and the function of the Pulse Stretcher Busy flip-flop. A peak detect

strobe pulse represents the first logic signal derived from the analog input. The remaining logic circuitry can be treated with logic description rather than with detailed circuit description.

Several other circuits are connected to the stretcher capacitors and these circuits will be discussed later.

7.23 Discriminators

Lower Level Discriminator

The output signal from the input voltage follower connects to the lower level discriminator through a series resistor. Transistor 1 acts as a linear gate at the discriminator inputs. The quiescent condition of the inear gate is with 1 turned off such that an analog input is applied to the lower and upper level discriminators and to the threshold discriminator. U2 operates as a comparator with the positive analog signal at pin 3 compared with a positive reference at pin 2. The reference level is set by the front panel Lower Level Discriminator Helipot. Signals above the LLD bias level generate a negative output which is coupled to the peak detect circuit at U12 and coupled into the Dead Time signal DT at U13.

Signal LLD is mainly used to allow triggering of the peak detect monostable. Analog input signals below the lower level discriminator threshold are not gated off, but are allowed to drive the stretcher/peak detector circuit. Pin 1Ø of U12 goes negative for approximately 5Ø nanoseconds when the peak amplitude of the input signal is detected. Unless signal LLD is positive ($\overline{\text{LLD}}$ at U12 pin 11 is low) at this time signal PD remains at a logic Ø and no further ADC logic signals are triggered.

Upper Level Discriminator

A second comparator, U3, is used as the Upper Level discriminator (ULD). The ULD's reference voltage is again determined by the front panel Helipot setting and ranges from approximately Ø.2 volts to +5 volts. Signals above the discriminator threshold generate a negative-going output to pin 9 of U13. The output of U13 pin 8 is inverted by U16 which in turn sets the Reject flip-flop in U19. The outputs of the flip-flop, signals RFF and $\overline{\text{RFF}}$ perform the following functions. Signal RFF is resistor-coupled to the base of transistors 2 and 5. Transistor 5 acts as a second shunt across the stretcher capacitors. When

signal RFF goes positive, Q5 saturates and the stretcher capacitor has effectively 220 ohms placed across it. This causes the stretcher capacitor to discharge on the trailing edge of the input signal, and in fact, the capacitor voltage follows the input signal down to the baseline. The Reject flip-flop is reset when the input signal drops below the Threshold discriminator's bias level and CLP switches negative. With the flip-flop reset, Q5 is turned off, removing the very low impedance shunt from the stretcher capacitor. However, at the same time Q9 is turned back on by the recovery of signal $\overline{\text{CLP}}$. The higher resistance shunt path provided by Q9 will then return and hold the stretcher capacitor at its quiescent level.

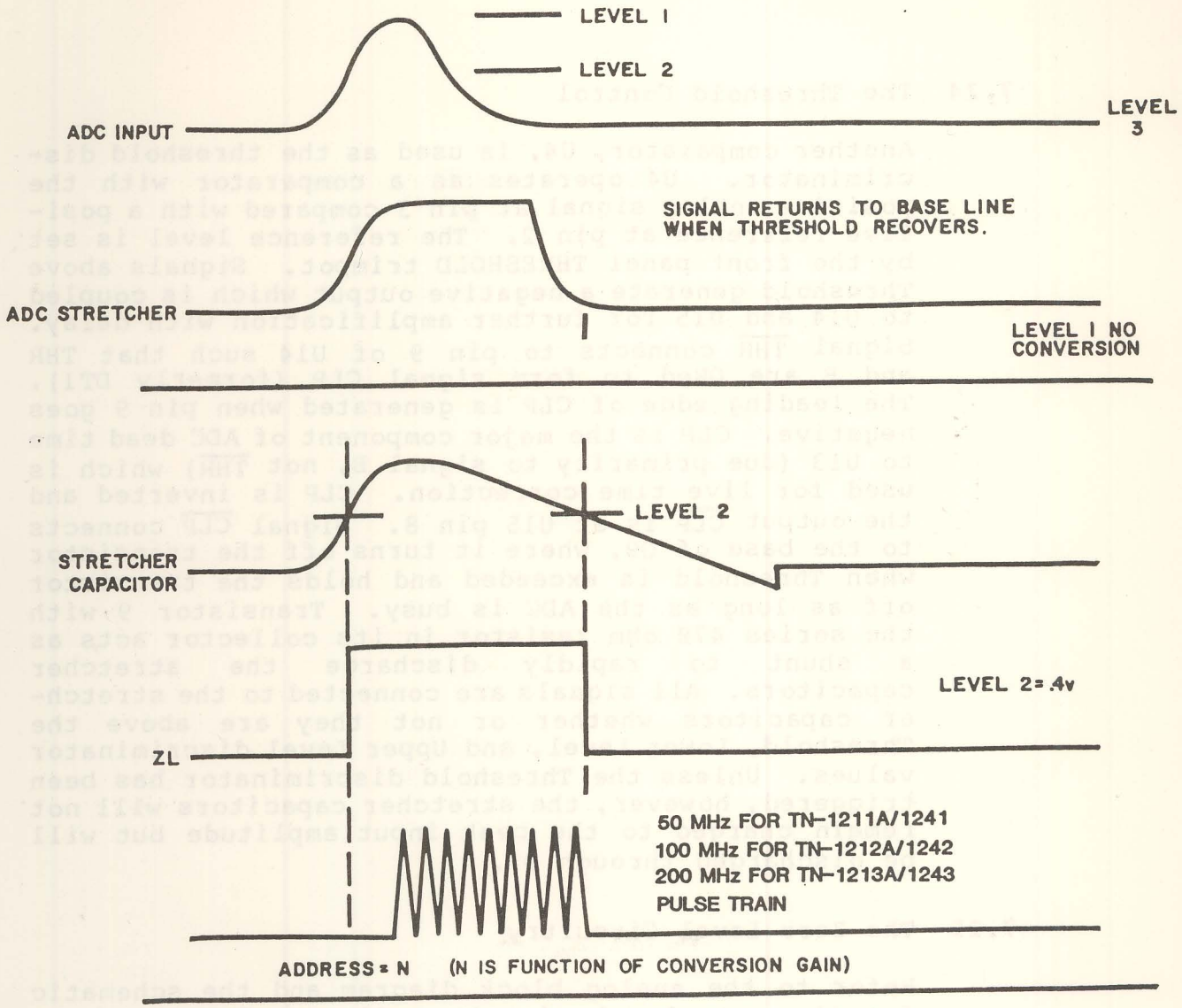
The Reject flip-flop connects to two more circuits. First, signal $\overline{\text{RFF}}$ connects to pin 2 of U19 where it prevents the PSB flip-flop from setting for reject conditions. This inhibits the start of an ADC conversion. Signal $\overline{\text{RFF}}$ also connects to the STORE-REJECT logic circuitry (U18) and acts as a logic backup in the event the PSB flip-flop does get triggered by a partial pulse. In this case, the following sequence of events occurs. The PSB flip-flop will set the ADC Busy flip-flop. Signal CLP is composed of THR + B and the Reject flip-flop is reset by CLP. If for some reason the Busy flip-flop is set, the Reject flip-flop will not be reset when Threshold recovers. Instead, the normal reject circuitry of the STORE REJECT logic will be activated. As soon as a "reject" is sensed, the internal reset circuitry will reset the Busy flip-flop. At the same time a STORE command is inhibited. Under normal operating conditions this sequence does not occur. Under high count rate/pulse pile-up conditions the normal ADC logic sequence may be upset, however. The sequence of events involving $\overline{\text{RFF}}$ and the ADC Busy flip-flop then take over to reset the ADC and inhibit storage of an erroneous conversion. Note that under normal operating conditions the dead time added to the system by a signal which triggers the upper level discriminator is equal to the time the threshold discriminator is triggered. Signal CLP, which is a component of the ADC dead time, will be positive only for the duration the threshold discriminator is triggered.

7.24 The Threshold Control

Another comparator, U4, is used as the threshold discriminator. U4 operates as a comparator with the positive analog signal at pin 3 compared with a positive reference at pin 2. The reference level is set by the front panel THRESHOLD trimpot. Signals above Threshold generate a negative output which is coupled to U14 and U15 for further amplification with delay. Signal $\overline{\text{THR}}$ connects to pin 9 of U14 such that THR and B are ORed to form signal CLP (formerly DT1). The leading edge of CLP is generated when pin 9 goes negative. CLP is the major component of ADC dead time to U13 (due primarily to signal B, not $\overline{\text{THR}}$) which is used for live time correction. CLP is inverted and the output $\overline{\text{CLP}}$ is at U15 pin 8. Signal $\overline{\text{CLP}}$ connects to the base of Q9, where it turns off the transistor when Threshold is exceeded and holds the transistor off as long as the ADC is busy. Transistor 9 with the series 47Ø ohm resistor in its collector acts as a shunt to rapidly discharge the stretcher capacitors. All signals are connected to the stretcher capacitors whether or not they are above the Threshold, Lower Level, and Upper Level discriminator values. Unless the Threshold discriminator has been triggered, however, the stretcher capacitors will not remain charged to the peak input amplitude but will be discharged through Q9.

7.25 The Zero Level Circuitry

Refer to the analog block diagram and the schematic for the zero level circuitry discussed here. Two comparators, U8 and U1ØA are used as the zero level discriminator. One input to the first comparator, U8, connects to the stretcher capacitors. The level for comparison at U8 is derived from the front panel ZERO LEVEL control and connects to pin 3. The voltage at the input, pin 3, ranges from about Ø.1 to +1 volt, depending on the front panel pot adjustment and the selected Conversion Gain. The output of the first comparator connects to Q1Ø. The output on the emitter of Q1Ø is a logic function that has a finite transition time determined by the 47 pf capacitor and 12K4 resistor. The emitter of Q1Ø connects to one input of the second comparator, U1ØA. The other input of U1ØA pin 3 has an adjustable DC level. The output of the comparator, U1ØA, is a logic function having additional adjustable delay from the output of the first comparator. Signal ZL at the output of U1ØA connects to only one point, that is pin 1 of U19, the PSB flip-flop. Signal ZL acts as a DC reset for the flip-flop when ZL is at zero. When the signal at the ADC stretcher exceeds the zero level bias or


LEVEL 1
LEVEL 2
LEVEL 3
ADC INPUT
SIGNAL RETURNS TO BASE LINE WHEN THRESHOLD RECOVERS.
ADC STRETCHER
LEVEL 1 NO CONVERSION

LEVEL 2
STRETCHER CAPACITOR
LEVEL 2=.4v
ZL
50 MHz FOR TN-1211A/1241
100 MHz FOR TN-1212A/1242
200 MHz FOR TN-1213A/1243
PULSE TRAIN
ADDRESS = N (N IS FUNCTION OF CONVERSION GAIN)

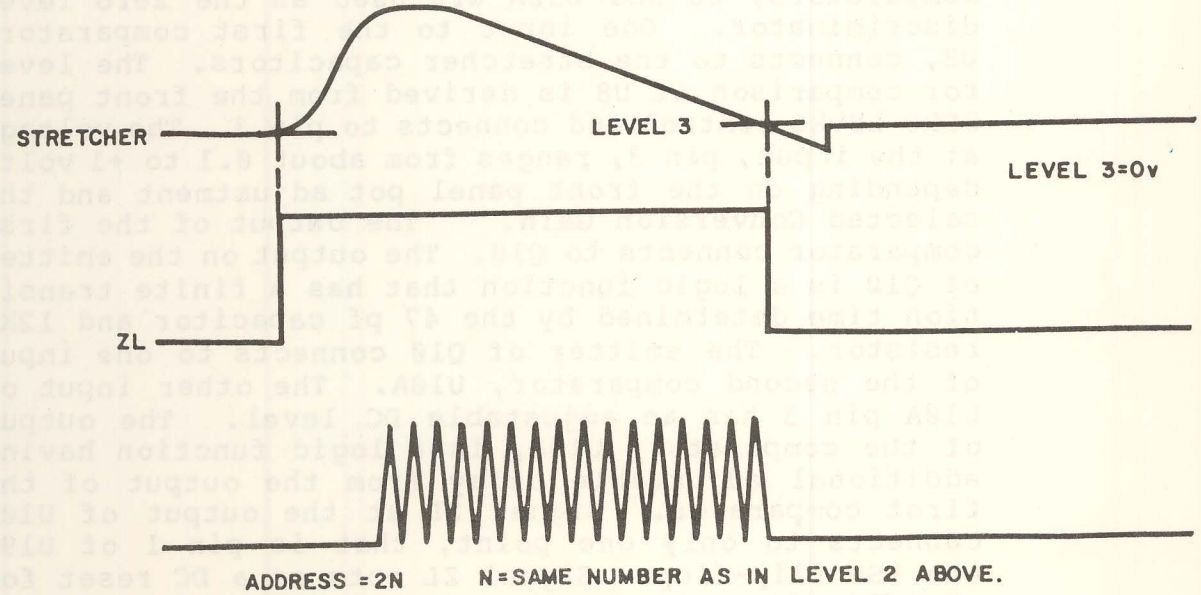

LEVEL 3
STRETCHER
LEVEL 3=0v
ZL
ADDRESS = 2N N=SAME NUMBER AS IN LEVEL 2 ABOVE.

FIG. 8

reference signal, ZL goes positive. This removes the DC reset on the PSB flip-flop and normally occurs somewhere on the leading edge of the input signal. When the input signal reaches peak amplitude, the peak detect monostable triggers, in turn setting the PSB flip-flop. In the event that ZL is not in the one state at peak detect time (signals below the zero level bias), the peak detect monostable will not set the PSB flip-flop due to its DC reset. Therefore, the leading edge of signal ZL acts as a logic function whereby no conversions will be started unless ZL is positive at peak detect time. For input signals above the zero level bias, linear rundown from Address Ø will begin approximately Ø.9 microsecond after PSB is triggered. At some instant in the linear rundown, the voltage at the stretcher capacitor will pass through the zero level bias on its way toward the baseline. At this time signal ZL returns to the zero state and resets the PSB flip-flop. The trailing edge of PSB is used to close the gate which terminates the scaling of the 5Ø/1ØØ/2ØØ MHz clock into the address scaler. Thus, the zero level discriminator performs a dual function. First, only signals above zero level bias are permitted to allow triggering of the PSB flip-flop, and second, the final encoded address is a function of the time that ZL returns to the zero state. This in turn is a function of the zero level bias. Figure 6 shows an input signal of 4 V with three different zero level bias settings. The first setting corresponds to a bias greater than the input signal. ZL is not generated and no conversion of the input results. The second condition is with the zero level bias set for approximately half signal amplitude. Note the pulse train duration and the address of the converted signal. The third condition shows the zero level bias set approximately for zero; that is, such that the slope intercept is at zero-zero. Again, note the number of address advance pulses and the final address generated. It can be seen from these diagrams that in all cases the pulse shape as seen by the pulse stretcher is the same. The final encoded address, however, is a function of the zero level bias. Operation of the zero level circuitry in this manner provides all the advantages of biased amplifier operation without the disadvantages normally associated with them. The signal as connected to the ADC stretcher and other analog circuitry in the ADC is the same for any zero level bias. ADC stability and linearity are essentially independent of zero bias setting.

7.26 Rundown Current and Conversion Gain

Circuitry for this section is all contained on the board schematic. Approximately Ø.1 microsecond after PSB is generated, a constant current is applied to the stretcher capacitor to provide linear discharge of the capacitor. The rundown current is selected by the front panel CONVERSION GAIN switch. This switch, through U6, selects a digital code to the DAC, Digital to Analog Converter, U7. The digital code sets the current output from the DAC which becomes the discharge current. Additionally, the output current of U7 pin 4 is a linear function of the reference voltage through the resistors to pins 14 and 15. This reference voltage, nominally 1Ø volts, is derived from the +6.8 V reference supply through two inverting operational amplifiers, U9 and U1Ø.

Rundown begins when signal CSC goes to the one state. This turns Q6 off, in turn "pinching off" Field Effect Transistor (FET) 7. Because Q7 is no longer "sinking" the current output from pin 4 of U7, the voltage at pin 4 swings negative until FET 8 turns on. Linear rundown begins when FET 8 turns on. The rundown current remains switched on until the address as converted is either stored or rejected within the ADC. Later sections deal with a more detailed description of the timing of the ADC logic signals. At this time it is important to know only that signal CSC goes to the one state after PSB flip-flop is set. Signal CSC returns to the zero state when the ADC is reset, either internally under reject conditions or at the time a clear signal is received from the memory section.

7.27 5Ø MHz (TN-1211A/1241), 1ØØ MHz (TN-1212A/1242), and 2ØØ MHz (TN-1213A/1243) Oscillators

The oscillators are designed specifically for the respective ADC types and circuitry. Refer to the appropriate board schematic for the following discussion.

The 5Ø MHz oscillator is an inverter of U35 in the TN-1211A and TN-1241. This IC type is a Schottky diode-clamped version of the standard 74ØØ quadruple two-input NAND gate. The diode clamp provides near class A operation of the inverting gates which increases the switching speed considerably. One gate with inputs on pins 1 and 2 has a parallel resonant circuit connected to a bypassed 33Ø ohm resistor which connects to the gate output, pin 3. The resistor provides a stable operating point for the oscilla-

tor circuit. A 50 MHz third overtone crystal connects directly from pin 3 to pins 1 and 2 on U35. The resonant circuit provides high impedance to 50 MHz only, causing oscillation only on the third overtone. The remaining gates in U35 gate the 50 MHz and also buffer the oscillator from the scaler.

For the TN-1212A/TN-1242's 100 MHz oscillator, transistor 32 is the active device. The crystal connects to the base of the transistor and the 1K resistor at the base keeps the transistor biased in the active region. The 100 MHz crystal is a fifth overtone type with oscillation at the proper overtone selected by the resonant circuit at the collector. The oscillator's output is AC coupled into one input of a two input ECL NOR gate, U36. The DC bias at this input is determined by a second inverting gate of U36 which has its output pin 2 tied back to its inputs, pins 4 and 5. The remaining gates in U36 buffer and gate the 100 MHz to the scaler.

In the TN-1213A and TN-1243 the 200 MHz oscillator is similar to that in the TN-1212A and TN-1242. Transistor 32 is again the active device with a parallel resonant circuit at its collector. A 200 MHz, ninth overtone crystal is its frequency determining element, with the parallel LC tank circuit tuned to the correct overtone.

The oscillator's output is AC coupled to one input of a two input ECL NOR gate, U39 pin 10 similar to the 100 MHz oscillator. The DC bias at this input is, however, determined by a voltage divider formed by the 221 and 750 ohm resistors. The remaining gates in U39 buffer and gate the 200 MHz to the scaler.

7.28 Address Scaler

The address scalers in the TN-1211A, TN-1241, TN-1212A, TN-1242, TN-1213A, and TN-1243 are almost identical. However, the first two stages of the TN-1212A and TN-1242 are Fairchild ECL types and the first three stages of the TN-1213A and TN-1243 are Motorola and Fairchild ECL types while the TN-1211A and TN-1241 use TTL exclusively. The address scalers are 13 bits in length plus a 14th bit described later.

In the TN-1211A and TN-1241, U36 and U37 are Schottky diode-clamped TTL for 50 MHz and 25 MHz scaling. The first 2 address scaler stages are then U37. The remaining 12 stages are low-powered Schottky TTL types.

In the TN-1212A and TN-1242, U35 and U37 are Fairchild temperature-compensated ECL types for 100 MHz and 50 MHz scaling. The first 2 address scaler stages are then U35. Transistors 20 through 26 translate the ECL levels for readout and/or further scaling in the 12 following TTL scaler stages.

In the TN-1213A and TN-1243, U35 and U41 are Motorola MECL III for 200 MHz scaling and U34 and U38 are Fairchild temperature-compensated ECL for 100 and 50 MHz scaling. U35 and U34 are now the first 3 address scaler stages. Transistors 20 through 29 translate the ECL levels to TTL levels for readout and/or further scaling in the 11 following TTL scaler stages.

Beyond the first two address stages (three for the TN-1213A and TN-1243), the circuitry for the ADCs is essentially the same. The discussion which follows applies to either unit with any differences noted in the discussion.

The address scaler is composed of 2 or 3 flip-flops described above followed by 12 or 11 flip-flops respectively of LS (Low Power Schottky) TTL from the 7400 family. Note that the output of the third address scaler stage in U27 connects as a carry to two flip-flops. One flip-flop of the two is address scaler stage A3 (A4 in the TN-1213A and TN-1243). The other flip-flop, U21, is used as the Current Source Control (CSC) flip-flop. This flip-flop is set when the "carry" from pin 5 of the third stage switches positive, the fourth stage in the TN-1213A and TN-1243. Remember that signal CSC begins linear rundown. Following sections will discuss the timing of the logic signals in more detail. Note that this flip-flop is DC reset by signal B when the Busy flip-flop is reset at CLEAR time.

There are 13 IC gates in U26, 28, 31, and 38 (TN-1211A/1212A/1241/1242) or 26, 28, 36, and 36A (TN-1213A/1243) which act as gated buffers for the address scaler outputs. Two signals connect to the inputs of the gated-buffer stages. One signal is the output of the scaler flip-flop, the other is signal ING. ING is a logic "0" at all times except immediately after rundown. Signal ING is generated at pins 4 and 10 of U41 (TN-1211A/1241/1212A/1242) and U40 (TN-1213A/1243) and is equal to B $\overline{PSB}$. The thirteen buffers are held off by ING until the end of conversion. With ING a a logic "1", the outputs of the IC scaler stages determine whether their respective buffers are at logic zero or one. Thus, the encoded address as contained in the IC scaler is presented to the memory when the control of the

buffers is switched from ING to the scaler at the end of conversion. Address output lines AØ through A12 remain at zero volts (TTL logic Ø) until the address is presented.

7.29 Conversion Logic Timing

Previous sections discussed individual circuits and logic blocks without any attempt to tie them all together in the system design. This section will cover the sequence of events from the arrival of the analog input through the end of conversion. Refer to Figure 9 which shows the timing of the major signals which will be discussed here. Figures 5 and 6 may also be valuable at this time. To simplify discussion, the ADC is assumed to be operated in the following manner. The upper and lower level discriminators are set for conversion of the entire range from zero to full scale. The ZERO LEVEL control is set for approximate Ø,Ø intercept. The CONVERSION GAIN switch is set to the memory size. However, for this discussion, CONVERSION GAIN is not at 256 in the TN-1212A or TN-1242 nor at 512 in the TN-1213A or TN-1243. The ADC is operated in a normal fashion; this precludes coincidence operation. No Digital Offset is used, and the ADC is analyzing normal pulses rather than DC or slow AC signals.

The incoming positive signal connects first to the gain-of-one voltage follower. The output of the voltage follower connects to the pulse stretcher, to the lower and upper level discriminators, and to the threshold discriminator. As the signal starts positive, the threshold discriminator triggers which removes the clamp across the stretcher capacitor. Then the Lower Level Discriminator triggers, in turn removing the inhibit on the peak detect monostable. The positive signal across the stretcher capacitor is coupled to the zero level discriminator and it triggers, generating positive signal ZL. With ZL in the one state, the PSB flip-flop can now be triggered when peak detection occurs. The signal continues positive and all the proper logic levels have been established, awaiting peak detection to start the conversion. When the pulse reaches maximum amplitude, the charging current to the stretcher capacitor drops to zero. Shortly thereafter the input signal starts down and peak detection occurs. A 5Ø nanosecond Peak Detect strobe is generated and this triggers the PSB flip-flop, setting it to the one state. Signal $\overline{PSB}$ goes positive and $\overline{PSB}$ goes to Ø V. PSB sets the ADC Busy This prevents the clamp on the stretcher capacitor from being turned back on until the flip-flop is reset. Signal $\overline{B}$ also generates

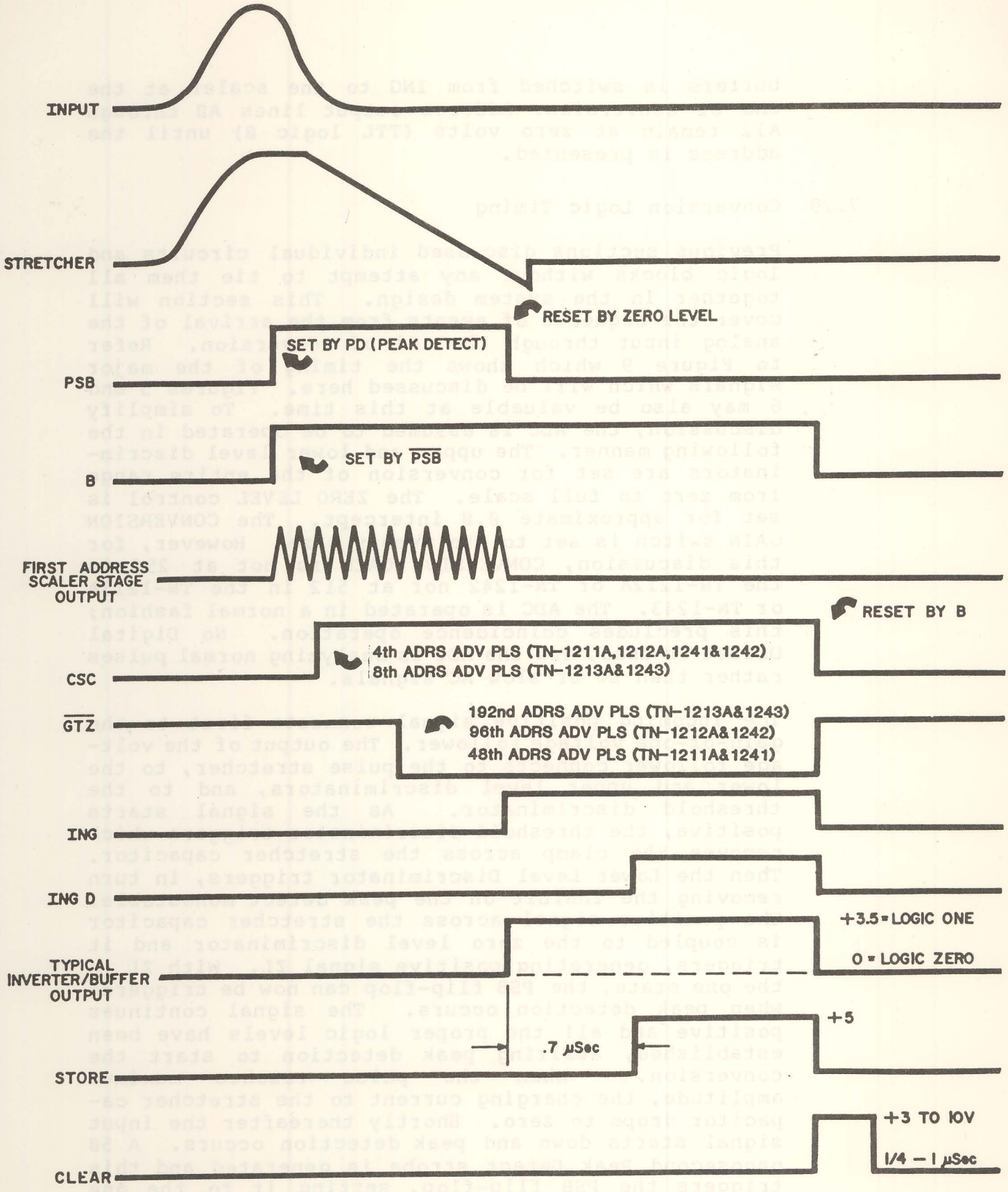


FIG. 9
ADC MAJOR SIGNAL TIMING

signal LGS which closes the linear gates for the stretcher and discriminators. This holds the discriminators and the stretcher capacitors inoperative until this conversion-STORE sequence is complete. Signal B is differentiated and the resultant pulse sets the clock synchronizing flip-flop, U36 for the TN-1211A and TN-1241, U37 for the TN-1212A and TN-1242, and U38 and 41 for the TN-1213A and TN-1243. The output of this flip-flop switches to the 1 state and the clock signal is now connected to the input of the first address stage and it begins to scale. Four clock pulses later the carry output of A2', U27, the third address scaler stage, switches positive. This sets the CSC flip-flop. On the TN-1213A and TN-1243, however, eight clock pulses are required to set the CSC flip-flop from A3' of U27. Signal CSC turns on the rundown current. With no digital offset, address stages A4, A6 through A12, (A5, A7 through A12 for the TN-1212A and TN-1242; A6 through A12 for the TN-1213A/1243) will be in the "set" state and stages AØ through A3 and A5 (AØ through A4 and A6 for the TN-1212A/1242; AØ through A5 and A7C for the TN-1213A/1243) will be "reset" when scaling begins. After 47 clock pulses (95 for the TN-1212A/1242 and 191 for the TN-1213A/1243) all address stages will be in the one state. One pulse later all address stages switch to the zero state. At this time a carry pulse from the last address stage A12 sets the GTZ flip-flop and signal $\overline{\text{GTZ}}$ switches to zero. The address scaler at this time is in channel Ø. It is important to recognize that the address scaler has been reset to the equivalent of -48 (-96 in TN-1212A/1242, or -192 in TN-1213A/1243); that is, it takes 48 pulses from the 5Ø MHz clock (96 from the 1ØØ Mhz clock, 192 from the 2ØØ MHz clock) to place the address scaler in channel Ø. The scaler requires Ø.96 microsecond to arrive at channel Ø due to this built-in digital offset. The design of the analog circuitry is such that with the ZERO LEVEL control set for Ø,Ø, there are exactly 48 channels (96 for TN-1212A/1242, and 192 for TN-1213A/1243) of equivalent pedestal built into the analog circuitry. With a 256 channel Conversion Gain in the TN-1212A and TN-1242, the prescale time is reduced from Ø.96 microsecond to Ø.72 microsecond. Similarly for the TN-1213A and TN-1243, with 512 channel Conversion Gain, the prescale time is reduced from Ø.96 to Ø.8 microseconds. Correspondingly, the analog Zero Level reference voltage is changed for each Conversion Gain setting. Even with no front panel Digital Offset, the address transferred to the memory unit differs from the number of address-advance pulses by a fixed quantity of 48 for the TN-1211A and TN-1241, 96 for the TN-1212A and TN-1242, 192 for the TN-1213A and

TN-1243. The offset serves two purposes. First, the turn-on of the rundown current is synchronized to the clock by scaling four address-advance pulses in the TN-1211A, TN-1241, TN-1212A and TN-1242 (8 in the TN-1213A and TN-1243) before setting the CSC flip-flop. No attempt is made to synchronize opening of the address scaler gate with the clock. The triggering uncertainty in the first stage has no effect on the ADC synchronization. For good channel profile it is essential that start of rundown current be well synchronized to the clock. This is accomplished by scaling in four or eight pulses from the clock before signal CSC is generated. The first three address stages actually perform the synchronization. By the time the scaler has scaled four clock pulses, the transitions are well synchronized to the clock.

The second function of the offset is in providing the ADC with settling time. At peak detect time several circuits are triggered and several logic transitions occur. The Ø.96 usec period before reaching address zero allows the analog circuitry and the zero level discriminator to settle to quiescent state before an acceptable address is converted.

At this time the sequence of events which began the conversion process has been covered. The address scaler has been advanced to channel Ø by scaling through the built-in offset. The encoding process now continues until the voltage at the stretcher capacitor reaches the ZERO level bias. With a small delay from the ZERO LEVEL threshold, signal ZL returns to a zero and resets the PSB flip-flop. Signal PSB's transition to zero starts clock pulses to scale in the clock synchronizing flip-flop, U36 in the TN-1211A and TN-1241, U37 in the TN-1212A and TN-1242, and U38 and 41 in the TN-1213A and TN-1243. The output of the flip-flop switches positive in synchronization to the clock and gates off the clock to the address scaler (switches negative in the TN-1211A and TN-1241).

Now that the address has been generated, it is presented to the memory unit and to the "acceptance test" logic circuitry. This is accomplished in the following way. Signal ING switches to one when PSB returns to logic "Ø" and the buffers are allowed to switch to the states determined by their respective scaler stages. This presents the address to both the memory and the acceptance test logic circuitry.

Address acceptance is determined at U33, a three input NAND gate. AOK, GTZ, and $\overline{\text{CHO}}$ are the inputs to this circuit. A logic "Ø" on any of these causes the output at pin 12 to go high. This output is inverted by another gate in U33 for signal $\overline{\text{REJ}}$ (reject not) low. So address reject will occur for AOK invalid, for address overflow, for CHO (address in channel zero), and for GTZ invalid (address underflow which may occur when using digital offset).

Conversion complete signal ING is again inverted at U15 pin 12. The output (pin 13 of U15) connects through a 2K2 resistor to the CHO gate and tests the address for channel zero (reserved for live/clock time storage) at ING time. If the address scaler stops in channel zero, the base and thus the collector of Q31, signal $\overline{\text{CHO}}$, switches to zero signifying a "reject" condition.

The conversion complete signal also connects through a two input NAND gate of U42, allowing external control of the store sequence. The NAND gate's output connects to the input of a pulse delay circuit comprised of one-half of U37 or 4Ø, a 74LS221, and one gate of U4Ø or 41. The approximate Ø.7 usec width of the pulse at the 74LS221's output determines the delay in this circuit. The circuit's output is a conversion complete delayed signal, INGD. This delay allows for the address scaler propagation delay and allows time for all address tests and reject signal set up for invalid addresses.

The delayed conversion complete signal, INGD, ties to pin 12 of U18, and, if all acceptance tests are passed the other inputs to this gate, $\overline{\text{REJ}}$, $\overline{\text{RFF}}$, and EXT $\overline{\text{REJ}}$, will be positive. Pin 8 of U18 switches to zero and is inverted to generate STORE at pin 8 of U16.

When pin 8 of U18 switches to zero, the NAND gate in U17 is disabled at pin 5. If any reject is generated by the address (overflow, underflow, or channel zero, for example), pin 8 of U18 will not go to zero when "conversion complete" is applied to pin 12 of U18. Now both inputs to U17 at pins 4 and 5 will be positive and the reset monostable, the cross coupled gate of U4Ø or 41 and 42, will be triggered. This resets the ADC with no STORE generated. Note, that if STORE is generated, pin 5 of U17 will be at zero and the only way the ADC can be reset is by a CLEAR signal applied at the base of Q17.

This completes the basic conversion process. The address as presented will either be transferred to the memory or rejected by the acceptance test circuitry. This is covered in the next section.

7.30 ACCEPTANCE, TEST, STORE, AND RESET CIRCUITS

7.31 General

This section deals with the sequence of events which immediately follow the end of the conversion. This includes the address acceptance tests followed by a STORE or internal reset of the ADC. Refer to the schematic or separate block diagram, Figure 6. The schematics take the form of a detailed block diagram and will be used for this discussion.

7.32 STORE Command and ADC Reset

Signal STORE is the flag to the computer or memory device signifying that a conversion is complete and that the address passed all tests whose limits are set by the front panel controls. STORE and address remain at the ADC output until a CLEAR is received from the computer or memory unit. interface.

Refer to the appropriate board schematic and find where $\overline{\text{PSB}}$ connects to pin 5 of U42. The output of U42 at pin 6 is $\overline{\text{PSB}}$ B, the inverted conversion complete signal. This output is re-inverted by two gates in U40/41 and generates ING on pins 4 and 10. ING goes to logic "1" when conversion is complete and allows the address-scaler buffers to present the address to both the rear panel output connector and to the GROUP SIZE overflow circuitry.

Address overflow is tested, according to the selected GROUP SIZE value, when the address scaler buffers present an address to the "B" inputs of U23 and 25. U23 and 25, 4-bit magnitude comparators, are cascaded to compare the Address to the front panel selected GROUP SIZE of 32 (GS5) to 4096 (GS12) through the inverters of U22 and 24. If the converted address is less than the selected GROUP SIZE, then AOK (Address OK) is a logic "1". However, if the address exceeds the selected GROUP SIZE, then AOK is a logic "0". Note that when GROUP SIZE 8192 (GS13) is selected, AOK is always enabled through U25A. When the address scaler exceeds channel 8192, the GTZ (Greater Than Zero) flip-flop is set to a logic "0" ($\overline{\text{GTZ}}$ at 1). GTZ at 0 rejects the conversion.

Typical $\overline{\text{RESET}}$ pulse width is Ø.4 microseconds. If the width of CLEAR exceeds the Ø.4 microsecond time, $\overline{\text{RESET}}$ will remain as long as CLEAR is present. $\overline{\text{RESET}}$ also triggers the REC' (recovery monostable) which resets the B flip-flop and provides corresponding dead time correction. Reset is ORed with REC' for a corrected recovery signal in U39 (U43 in TN-1213A/1243) to preclude incorrect reset for a long CLEAR pulse.

7.33 Digital Offset Circuitry (TN-1211A/1212A/1213A only)

Refer to the schematics for the front panel and the board for the circuitry in this section. Note that address scaler stages A7 through A12, implemented in U3Ø and 32, can be preset from the front panel DIGITAL OFFSET switches. If no digital offset is selected, they are "set". The front panel toggle switch associated with each address stage controls the state of its respective stage when a reset pulse is generated at CLEAR time. For example, the 4Ø96 switch controls address stage A12 with signal DO12, and is loaded with a logic "Ø" when the switch is on (up). In similar fashion the state of stage A11 is determined by the front panel switch labeled 2Ø48, A1Ø by 1Ø24, A9 by 512, etc. When $\overline{\text{RESET}}$ goes low the 74LS197s (U3Ø and 32 as well as U27) are then parallel-loaded to the states existing on their parallel inputs, pins 4, 1Ø, 3, and 11. When $\overline{\text{RESET}}$ returns high, the 74LS197s no longer respond to the parallel inputs. The scaler stages are preset for the next conversion.

The manner in which digital offset is accomplished can be best explained by using two examples. The first will use no digital offset while the second will have 4Ø96 digital offset. Assume for the moment then that all digital offset switches are off (this is always the case for the TN-1241/1242/1243). When the address scaler is cleared, stages A7 through A12 will be set, that is, the true outputs will all be in the 1 state. Stages AØ through A6 are set as described in subsection 7.29 on Conversion Logic Timing for equivalent Ø.96 microsecond for the respective units. The GTZ (Greater Than Zero) flip-flop contained in U32 will also be reset and signal GTZ will be negative. Assume the address scaler gate is opened and that the scaler begins scaling clock pulses. Forty-seven address advance pulses later all stages AØ through A12 will be in the 1 state on the TN-1211A and TN-1241. For the TN-1212A and TN-1242, 95 address advance pulses put all stages in the 1 state. For the TN-1213A and TN-1243, 191 address advance pulses put all stages in the 1 state. One more address ad-

vance pulse will reset stage AØ which will propagate a carry to A1 and reset it. This in turn will propagate a carry to stage A2, resetting it. The process continues such that a carry is propagated through the thirteen stages of the address scaler. A carry is also propagated to the GTZ flip-flop at this time. Signal $\overline{GTZ}$ switches to zero and the address scaler is in channel zero. If the address scaler were to stop here, the Channel Zero reject gate would inhibit storage. If the address scaler continues to advance beyond channel zero and does not exceed group size, it will generate STORE. Under these conditions the address as presented differs from the number of clock pulses by 48 clock pulses for the TN-1211A/1241, 96 clock pulses for the TN-1212A/1242, and 192 clock pulses for the TN-1213A/1243.

Now let's switch in 4Ø96 channels of digital offset on the TN-1211A/1212A/1213A. With the front panel toggle switch "on," address stage A12 will always be cleared to the zero state so that 48, 96, or 192 (TN-1211A, TN-1212A, or TN-1213A) address advance pulses will put stages AØ through A11 in the zero state and a carry will propagate to stage A12 where it will be set. At this time no carry is propagated to the GTZ flip-flop. If conversion ceases at this time, the channel zero reject gate will not reject the conversion but signal GTZ will remain at logic "Ø" and keep signal $\overline{REJ}$ at ground, rejecting the conversion. Assume conversion continues for 4Ø95 additional address advance pulses. Now stages AØ through A12 will all be in the 1 state. Remember that this is the condition corresponding to 48, 96, or 192 address advance pulses with no digital offset. With one additional pulse, stages AØ through A12 will be switched to the zero state and a carry will propagate to the GTZ flip-flop removing the reject condition. However, at this time, the channel Ø reject gate will still reject this conversion. All conversions generating more than 48, 96, or 192 plus 4Ø96 address advance pulses will generate a memory cycle as long as they do not exceed the memory group size.

The ADC is designed with built-in digital offset. This offset is compensated for in the analog circuitry. It can be shown that the number of address advance pulses required to place the address scaler in channel Ø is equal to the digital offset switched in on the front panel plus the constant 48, 96, or 192 for the TN-1211A/1241, TN-1212A/1242, and TN-1213A/1243 respectively. Digital offset can be thought of in another way. The address scaler can be thought of as being initially reset to a negative number. Also, all negative-number conversions will

automatically be rejected by the logic circuitry. Thus, a digital offset of 4096 can be thought of as a minus 4096 condition of the address scaler. No memory cycle will occur until the scaler has been advanced through the negative number and this means a minimum of 4096 plus 48, 96, or 192 address advance pulses. Note that for a given analog input the amount of offset does not affect the conversion dead time. At high count rates and high resolution settings of the conversion gain switch it is sometimes wise to consider using analog offset with the ZERO LEVEL control for reduced dead time. With 50, 100, or 200 MHz digitizing rate, however, the analog control may be worthwhile only in extremely high count rate/resolution experiments.

7.34 Dead Time Signal and ADC Recovery Circuitry

Signal DT is positive any time the ADC is busy and not capable of accepting another input for conversion. Signal CLP, formerly DT1, is composed of THR + B. CLP connects to pin 9 of U15 with the output appearing at pin 8 as $\overline{\text{CLP}}$. CLP also connects to the reset not input of a flip-flop in U21. When an event comes along, normally the reset is removed first, then $\overline{\text{LLD}}$ which is connected to the set not input triggers and sets the flip-flop to assert dead time on U16 pin 8 and thus DT on U25A pin 11. After the event is transferred, CLP returns low and resets the DTQ flip-flop in U27. $\overline{\text{DTQ}}$ or $\overline{\text{REC}}$ then (normally) determines the end of DT. At the time the ADC is reset, either internally or externally, an ADC recovery one-shot, U40 (37 in the TN-1213A and TN-1243) is triggered. This monostable is provided to allow the 0.8 microsecond for the ADC to recover from the transients generated by the address transfer. Note, as described earlier in subsection 7.32, $\overline{\text{REC}}$' is ORed with $\overline{\text{RESET}}$ to ensure a recovery signal longer than the CLEAR signal. The ADC discriminators, stretcher, and logic circuits are enabled at reset time. However, any signal detected during the 0.8 microsecond period time must be included in ADC dead time for accurate live time operation. This is accomplished by connecting $\overline{\text{REC}}$ to pin 1 of U13. Thus, the total dead time signal for a conversion begins with triggering of the Lower Level (earlier units used Threshold) Discriminator and extends for 0.8 microsecond after the leading edge of the CLEAR and hence $\overline{\text{RESET}}$ pulse has been generated.

Intentionally Blank

8.00 MAJOR SIGNALS AND THEIR FUNCTIONS

8.10 GENERAL SIGNAL GLOSSARY

Signal	Function
A0 through A12	Rear panel 13-bit address output lines which connect to memory unit. Logic zero < 0.4 V, logic one = +2.5 to 3.5 V from TTL source.
ACN	Connects to COINC BNC in the ANTI COINC position of the mode switch. Positive signal inhibits conversion by preventing PSB flip-flop from being triggered. Input impedance is 3K3, DC connected. Refer to subsection 6.82 for details on Anti-Coincidence operation.
AOK	Address OK, positive logic signal generated for any address within the selected group size. Addresses not within the selected group size normally cause STORE to be inhibited and the ADC to reset internally.
B	Output of ADC busy flip-flop. Flip-flop is set by $\overline{PSB}$ and reset by $\overline{REC}$. This signal sets clock synchronizing flip-flop and is the major component of dead time signal. It also connects to STORE logic, and holds ADC linear gates closed while in the "one" state.
CG8	Control signal which connects to front panel CONVERSION GAIN switch. Signal is +5 V when a conversion gain of 256 is selected. Note that the TN-1213A and TN-1243 don't have 256 channel Conversion Gain as it begins at 512 (CG9).
CG9 through CG12	Same functions as CG8 for their respective switch positions and circuitry.
CLEAR	Rear panel input to the ADC to reset the ADC after data transfer. Requirements: Positive 3-10 V pulse, 1/4 to 1 usec duration. Input impedance: 2.2K DC connected.

CLP	Positive whenever THRESHOLD or B is positive. Major component of dead time signal. Used to control clamp across stretcher capacitor.
CNC	Connects to COINC BNC in the COINC position of the mode switch, and to +5 in the ANTI COINC position of the mode switch. Positive input opens linear gate to allow ADC conversion. Input impedance: 3.3K, DC connected. See subsection 6.81 on COINC operation for more details.
CSC	Current source control flip-flop output. Connects to rundown-current switch and starts linear rundown when switched to the one state. Flip-flop is set by carry from third stage of address scaler and reset by the ADC Busy flip-flop output, signal B (fourth stage in the TN-1213A and TN-1243).
DO7	Control signal which connects to front panel 128 DIGITAL OFFST switch. Signal is +5 V when "128" switch is up, and grounded when switch is down.
DO8 through DO12	Same function as DO7 for their respective switches and circuitry.
DT	Dead Time signal appearing on rear panel connector. Signal is +3.5 whenever the ADC is busy converting an input or whenever it is insensitive to an input. Typically used in the memory unit for dead time correction in the live timer (REC + DTQ + LLD).
DTM	Dead Time Meter drive signal (DT + THR). Connects to front panel % DEAD TIME meter.
EXT B	Buffered output of ADC Busy flip-flop available on ADC rear panel. Logic zero = Ø V, logic one = +3.5 V.
EXT CNTL	Rear panel EXTernal CoNTroL input provided to disable normal STORE-REJECT logic. Used by NS-641 Two Parameter Adapater or equivalent to disable ADC logic. External source must sink approximately 1.4 mA at Ø V.
EXT GATE	Input on rear panel provided to force channel zero on address output lines. Used by NS-641 Two Parameter Adapater or equivalent for storage of Singles and/or Live Time counts.

EXT REJ — Rear panel input provided to reject a conversion. Input requirements: +3.5 to +5 V pulse, 1/4 to 1 usec duration. Pulse must be applied after the analog input signal triggers THRESHOLD and before the end of conversion. Pulse sets Reject flip-flop which inhibits STORE and automatically causes ADC reset. Dead time after pulse application is approximately 2 usec for any analog input amplitude/conversion gain or time for signal above THRESHOLD, whichever is longer. This input can be used as a delayed anti-coincidence input. Maximum delay to ensure reject for any amplitude/ conversion gain is approximately 1.5 usec after the analog input reaches peak amplitude. If the pulse is applied sooner than Ø.1 usec before peak amplitude, the PSB and B flip-flops will not be set. The stretcher capacitors will be "crow-barred" and the dead time will essentially be signal time above threshold.

EXT $\overline{\text{REJ}}$ — Rear panel input provide to inhibit STORE and cause internal ADC reset. Input requirements: To inhibit STORE, this input must be at Ø V when PSB returns to Ø V and hold for at least 1 usec thereafter. External source must sink approximately 1.4 mA at Ø V. Used by NS-4Ø9 and NS-454 Digital Stabilizers.

GS5 — Control signal which connects to front panel GROUP SIZE switch. Signal is shorted to GSC when a group size of 32 is selected.

GS6 through GS13 — Same functions as GS5 for their respective switch positions and circuitry.

GSC — Group Size Common connected to the selected Group Size; normally Ø volts except for inverted logic applications, in which case it is +5 volts.

GTZ — Greater Than Zero flip-flop output, formerly Underflow flip-flop output. Signal is positive until address scaler has advanced through channel Ø. Provides automatic reject of conversions below channel Ø when using digital offset.

LGS	Linear Gate Source. LGS = B + $\overline{\text{CNC}}$. The linear gates for the ADC stretcher and discriminators are closed whenever LGS is in the one state.
OFF	Connects to front panel ANALYZE-OFF switch and rear panel CONNECTOR INPUT (pin 22). Ground in ANALYZE switch position, +5 V in the OFF position. Holds ADC in DC reset condition. Also used by Tracor Northern Memory Unit or Computer Interface Units and with Tracor Northern Two Parameter Adapter to hold timing scalers reset until analysis begins. External source must sink approximately 5 mA to Ø volts.
PSB	Pulse Stretcher Busy flip-flop output. Set by peak detect strobe and reset by ZL in the zero state. Triggers and/or controls several ADC logic functions at the start and end of conversion which are indicated by the leading and trailing edges of this signal respectively.
REC	Ø.9 usec output of the Recovery Single Shot. Inhibits start of conversion within Ø.9 usec after ADC is reset. Triggered on the leading edge of ADC CLEAR by internal RESET.
REJ	Reject signal which connects to STORE-REJECT logic. Signal is Ø V when conversion is below channel Ø (due to GTZ), or is at channel Ø (CHO gate), or is greater than the selected GROUP SIZE, so that STORE is inhibited and the ADC is automatically reset.
RFF	Buffered Output of Reject flip-flop which connects to rear panel. RFF is set by ULD + Ext REJ + ACN PSB and is reset by CLP when it returns to Ø V. Used by the NS-641 Two Parameter Adapter.
SCA	Front panel Single Channel Analyzer output. Pulse is Ø.5 usec, approximately 5 volts through 5Ø ohm output and is triggered by Peak Detect in accordance with Upper Level and Lower Level Discriminator settings.
SET B	Rear panel input provided to set analyzer Busy. Positive $\geq$ 3 volt signal, input impedance 3.3K DC. Sets Busy flip-flop. Busy flip-flop is reset as soon as this input is allowed to return to Ø because of the invalid address in the scaler.

STORE	Positive 2.5 to 5 V rear panel signal which indicates conversion complete and acceptable address for storage in the memory. STORE and address remain until a CLEAR is received by the ADC.
X PSB	Buffered output of Pulse Stretcher Busy flip-flop available on ADC rear panel. Logic zero < Ø.4 V, logic one = +3.5 V.
+5	Plus 5 volt internal supply.
+6.8	Plus "6.8" volt internal reference supply set to +7.Ø volts in the TN-1211A/1212A/1213A/1241/1242/1243.

8.2Ø REAR PANEL ADC I/O CONNECTOR DEFINTIONS

37 Socket "RACK and PANEL" Connector, M/W Cinch-Jones DC-37P

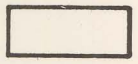
PIN	SIGNAL	
1	AØ	13 bit address output, LSB to MSB standard TTL source, logic "Ø" < Ø.4 V, logic "1" +2.5 to 3.5 V typical
2	A1	
3	A2	
4	A3	
5	A4	
6	A5	
7	A6	
8	A7	
9	A8	
1Ø	A9	
11	A1Ø	
12	A11	
13	A12	
14	DT	Dead time output. TTL logic 1 whenever the ADC is busy converting an input or insensitive to an input.
2Ø	STORE	Standard TTL output. Logic 1 indicates conversion complete and acceptable address ready for storage.
21	CLEAR	Input to ADC to reset ADC after address data transfer. Requires +3 to 1Ø V pulse of 1/4 to 1 usec duration. Input impedance 2.2K direct connected.
22	OFF	Ground in ANALYZE. OFF is +5 V and holds ADC reset. Also connects to front panel ANALYZE-OFF switch.
23	EXT B	Standard TTL output. Buffered output of ADC Busy flip-flop.
24	$\overline{\text{REJ}}$	Schottky low power TTL output. Negative pulse of approximately Ø.5 usec for invalid address conversions. Normally causes automatic reset in ADC.
25	EXT CONT	Normally high input to ADC. TTL logic "Ø" disables normal STORE-REJECT logic until input returns to logic "1".

26	EXT REJ	Input to reject a conversion. Requires +3.5 to 5 volt pulse of 1/4 microsecond minimum duration. Pulse must be applied after the analog signal triggers THRESHOLD and before the end of conversion.
27	EXT GATE	Input provided to force channel Ø on address output lines by applying +3.5 to 5 volt level.
28	SET B	Input provided to force Busy flip-flop to a set state with application of +3.5 to 5 volt signal.
29	X PSB	Standard TTL output. Positive logic buffered output of Pulse Stretcher Busy flip-flop.
3Ø	X RFF	Standard TTL output. Buffered output of Reject flip-flop.
32	EXT $\overline{\text{REJ}}$	Rear panel input inhibits STORE and causes internal ADC reset. To inhibit STORE, this input must be at Ø volts when PSB resets and hold for a minimum of 1 microsecond thereafter.
33	CLP	Low power Schottky output. Positive logic level whenever THRESHOLD or B is positive.
34 35 36	$\overline{\text{CSØ}}$ $\overline{\text{CS1}}$ $\overline{\text{CS2}}$	Conversion Gain switch contacts to GND. Encoding is as follows: Ø = 256 3 = 2Ø48 1 = 512 4 = 4Ø96 2 = 1Ø24 5 = 8192
37	GND	

Optional 25 Socket STABILIZER Connector, M/W Cinch-Jones DB-25P

PIN	SIGNAL	
1	AØ	
2	A1	
3	A2	
4	A3	
5	A4	13 bit address output
6	A5	LSB to MSB standard TTL source,
7	A6	logic "Ø" < Ø.4 V,
8	A7	logic "1" is +2.5 to 3.5 V typical.
9	A8	
1Ø	A9	
11	A1Ø	
12	A11	
13	A12	
14	EXT B	Standard TTL output. Buffered output of ADC. Busy flip-flop.
15	X PSB	Standard TTL output. Positive logic buffered output of Pulse Stretcher Busy flip-flop.
16	EXT REJ	TTL input inhibits STORE and causes internal ADC reset. To inhibit STORE this input must be at Ø volts when PSB resets (± Ø.2 usec) and hold for a minimum of 1 usec thereafter.
17	ZL STAB	Zero Level analog STABilize Input.
18	ZL Ref	Zero Level analog Reference output (Ø - 1 V).
19	GTZ	Greater Than Zero TTL output. This output sets up after PSB resets if conversion is greater than zero.
2Ø	-13.6S	Analog stabilized -13.6 V gain reference input.
21	-13.6	-13.6 "gain" reference output for stabilization.
25	GND	

9.ØØ SCHEMATICS

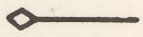


Designates signal source which connects to loads off this board and may also have loads on this board.

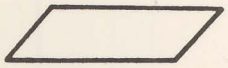
Designates signal from a source not on this board.

Designates source for a signal used only on this board.

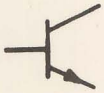
Designates load for signal used only on this board.



Designates a signal source and load at this point used only on this board.



Designates front and rear panel labeling.



All NPN transistors are 2N2369 or equivalent unless otherwise marked.

All PNP transistors are 2N4126 or equivalent unless otherwise marked.

All resistors are ¼ watt 5%, unless otherwise marked.

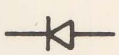
4K7

Resistor whose value is 4700 ohms.

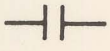
4M7

Resistor whose value is 4.7 megohm.

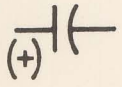
MF designates precision metal film ½ w ± 1% resistors, unless otherwise specified.



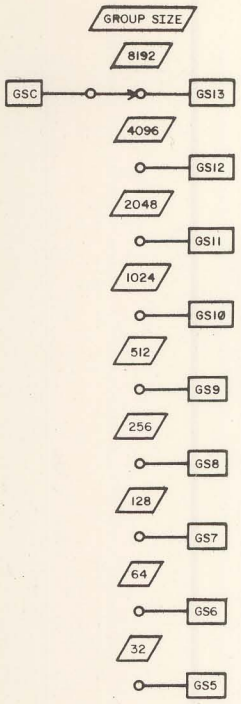
All diodes are Fairchild 1N4150 or equivalent unless otherwise specified.

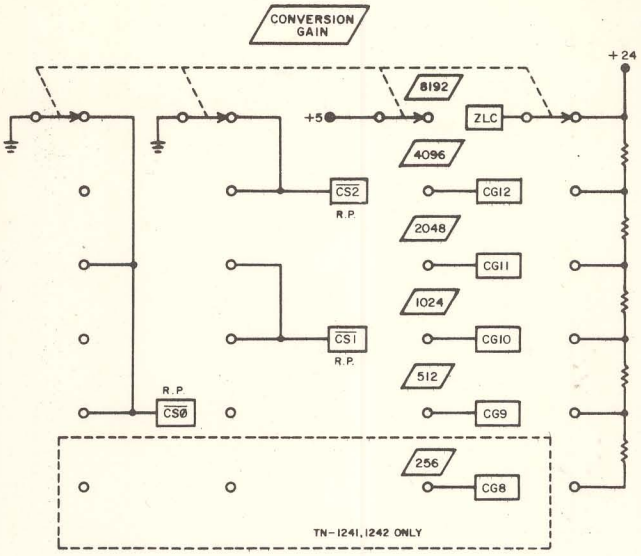


Capacitance values shown as whole numbers are in picofarads (1000 = 1000pf). Capacitance values expressed with decimal points are in microfarads (.05 = .05 microfarads). Polarized capacitors may be exceptions to these rules.

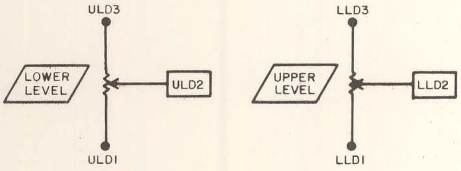


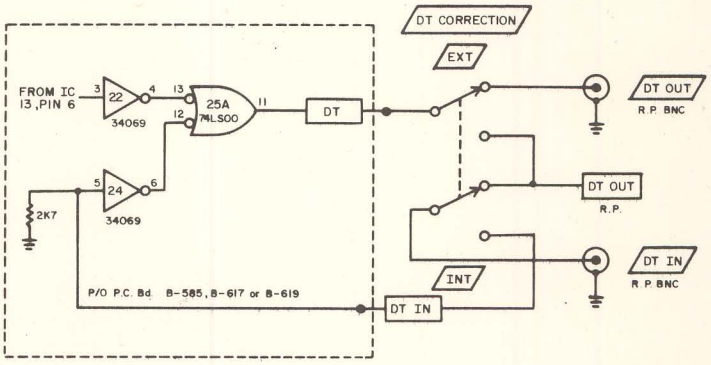
Polarized capacitors are as shown.

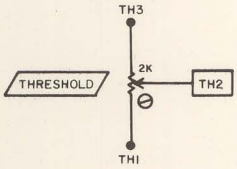


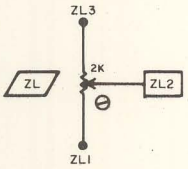


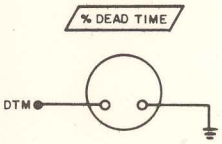
TN-1241	TN-1242	TN-1243
499	1K0	2K32
1K21	2K94	7K15
3K24	10K	48K7
10K	215K	215K
249K	NONE	NONE

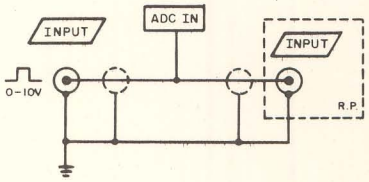


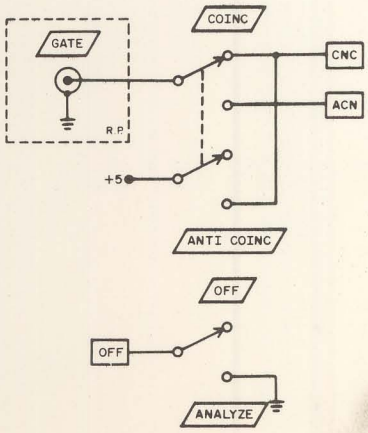


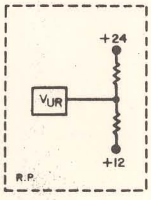




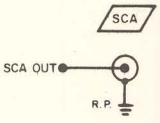






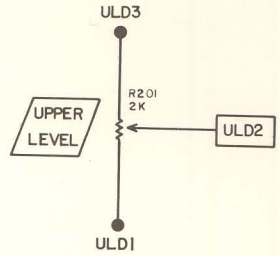


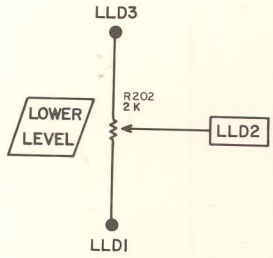
TN-1241	TN-1242	TN-1243
250,5W SERIES W/ 47,1W	100,5W	100,5W
10,5W SERIES W/ 2.7	10,5W SERIES W/ 2.7	10,5W

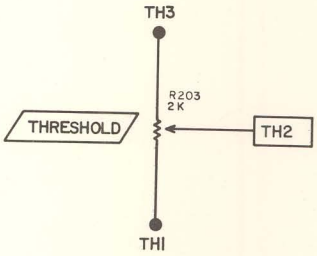


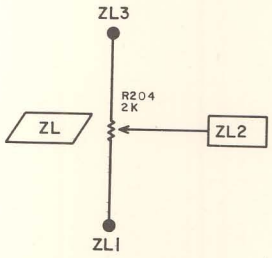
REVISION	DESCRIPTION		DATE
	TN-1241,1242,1243 ADC FRONT & REAR PANEL		TRACOR NORTHERN
DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
1/4/79	J.A.H.	G.R.B.	S-773

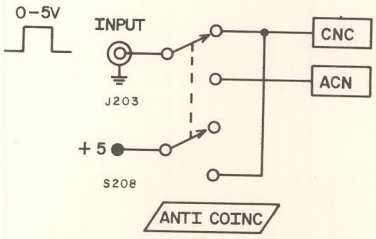
GSC

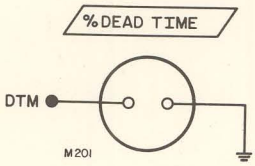

ULD3
R201
2K
UPPER
LEVEL
ULD2
ULD1

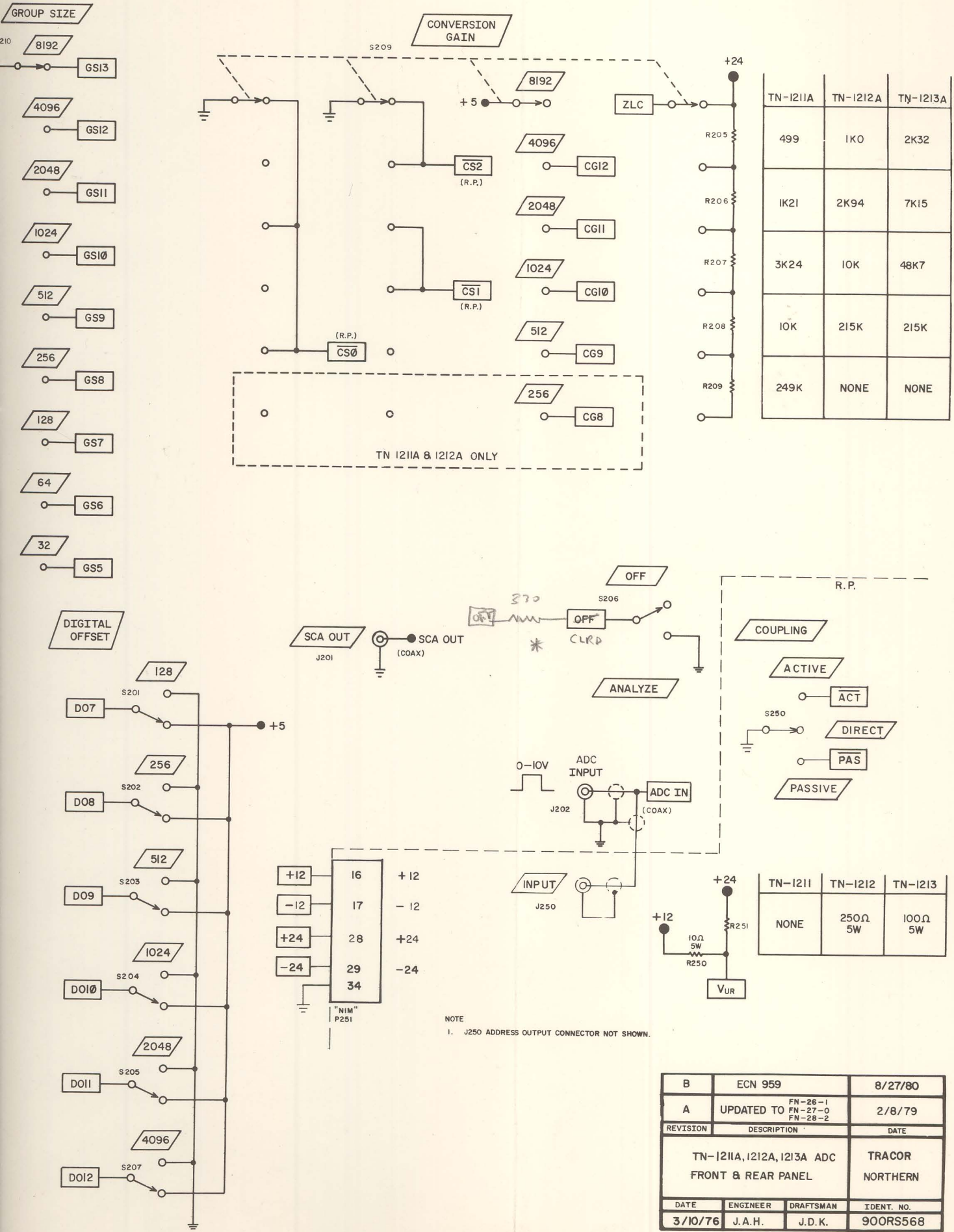

LLD3
R202
2K
LOWER
LEVEL
LLD2
LLD1


TH3
R203
2K
THRESHOLD
TH2
TH1


ZL3
R204
2K
ZL
ZL2
ZL1


0-5V
INPUT
J203
CNC
ACN
+5
S208
ANTI COINC


%DEAD TIME
DTM
M201



NOTE

1. J250 ADDRESS OUTPUT CONNECTOR NOT SHOWN.

REVISION	DESCRIPTION	DATE
B	ECN 959	8/27/80
A	UPDATED TO FN-26-1 FN-27-0 FN-28-2	2/8/79

TN-1211A, 1212A, 1213A ADC FRONT & REAR PANEL

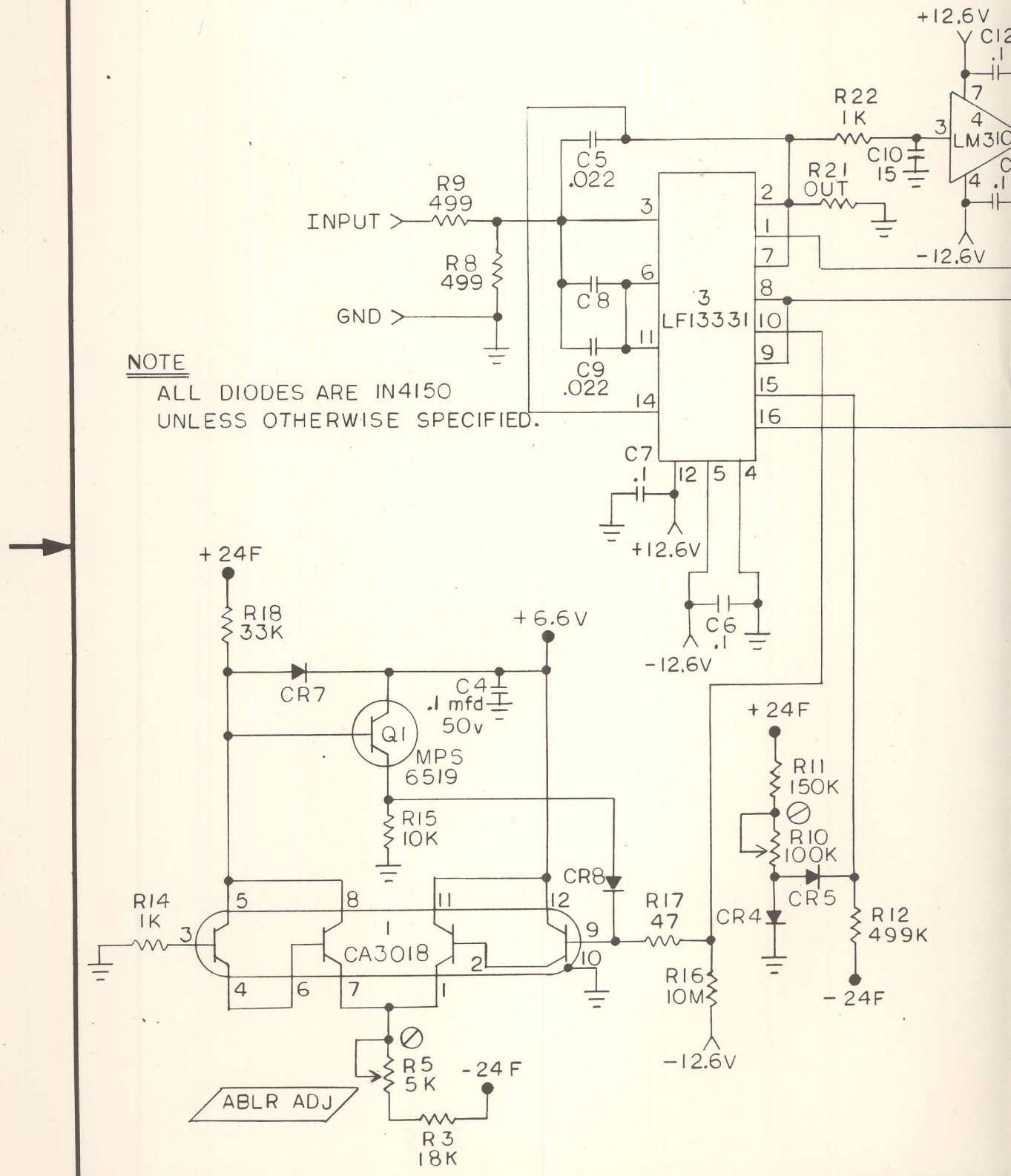
TRACOR NORTHERN

DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
3/10/76	J.A.H.	J.D.K.	900RS568

SHEET OF

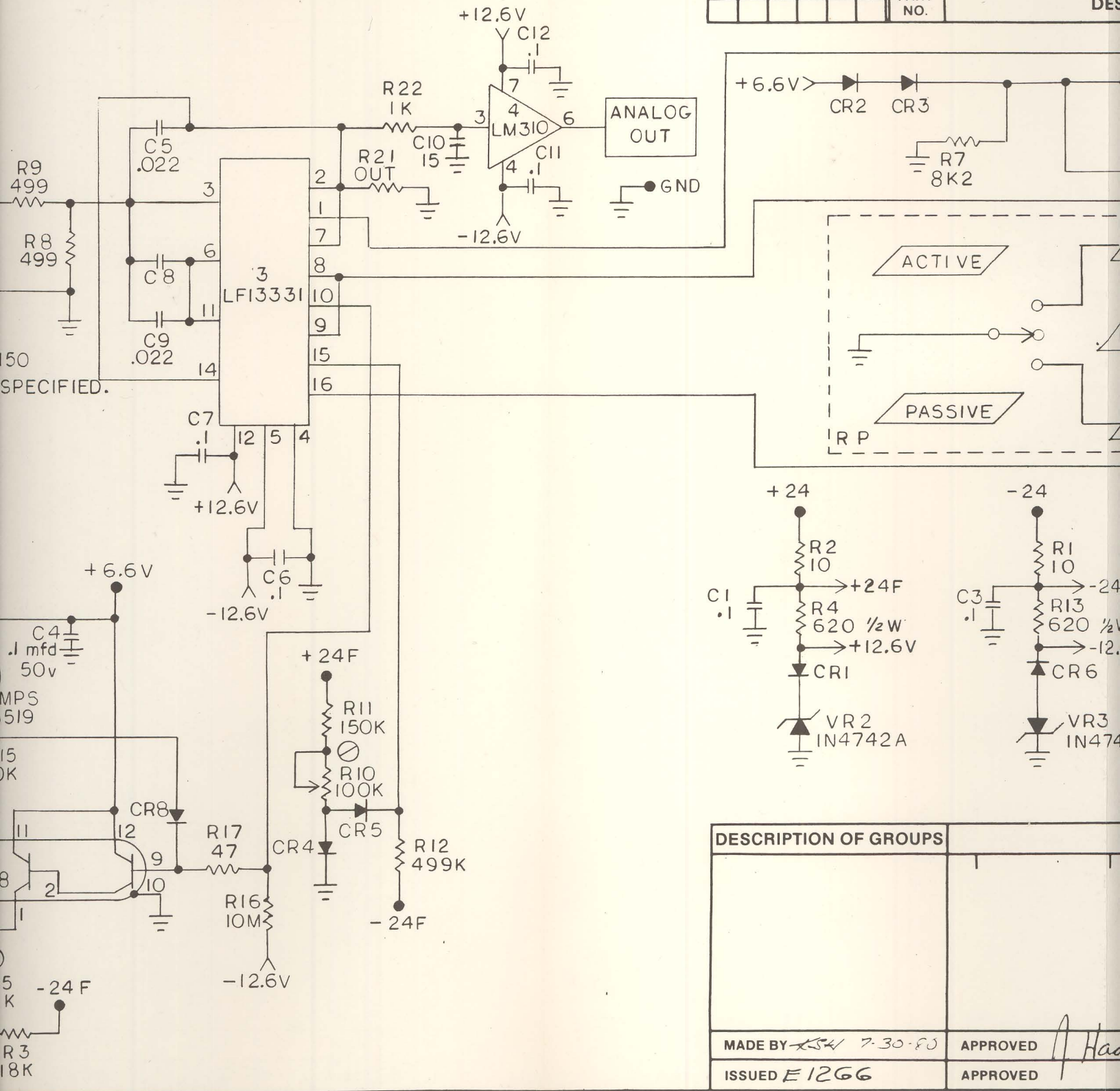
REVISIONS CONTINUED

UNLESS OTHERWISE SPECIFIED USE THE FO				
DIAMETERS	SURFACES	DECIMALS	FRACTIONS	ANGLES
	√			



FORM 800C2

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING						REV. NO.	TITLE
DIAMETERS	SURFACES	DECIMALS	FRACTIONS	ANGLES	BREAK SHARP EDGES AND CORNERS		ADC BASE
	√					SHEET OF	FIRST MADE FOR TN
						GROUP NO. AND QTY. / PART NO.	DES



DESCRIPTION OF GROUPS	
MADE BY KSH 7-30-80	APPROVED
ISSUED E1266	APPROVED

Tracor Northern 174B1034 SHEET 1 OF 1

LLOWING | REV. NO. | TITLE

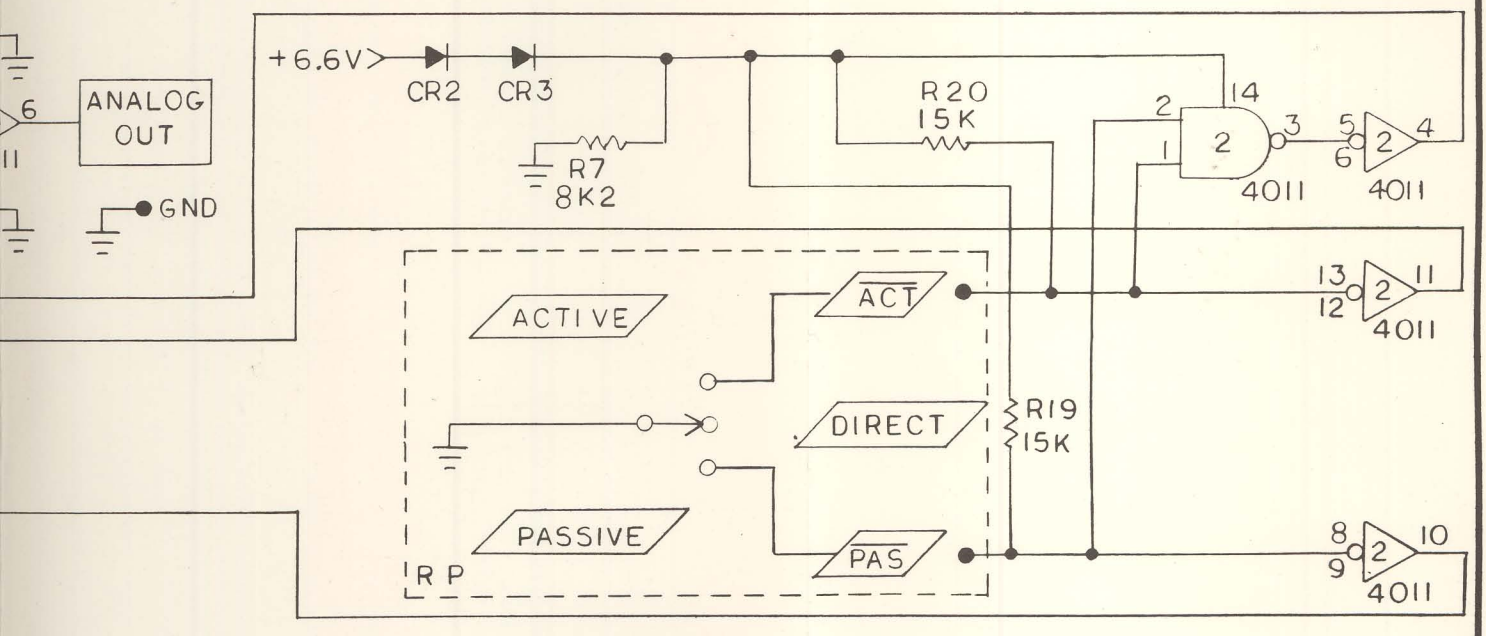
BREAK SHARP EDGES AND CORNERS

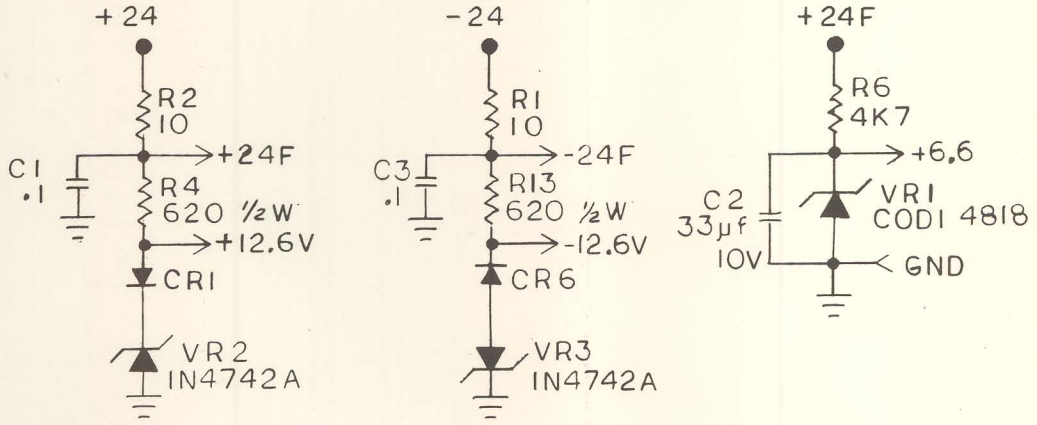
SHEET OF

ADC BASELINE RESTORER

FIRST MADE FOR TN 1211/1212/1213

GROUP NO. AND QTY.	PART NO.	DESCRIPTION	IDENT. NO.



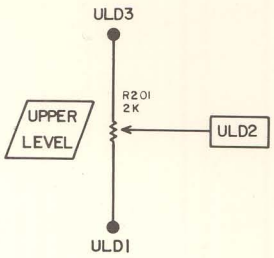


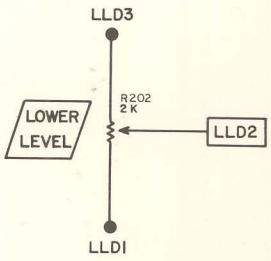
DESCRIPTION OF GROUPS	REVISIONS	PRINTS TO

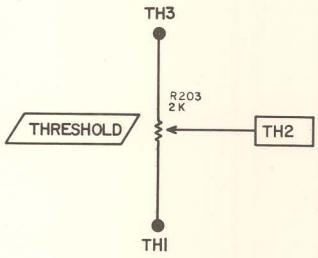
MADE BY KSH 7-30-80 | APPROVED A Haas 8/4/80 | 174B1034

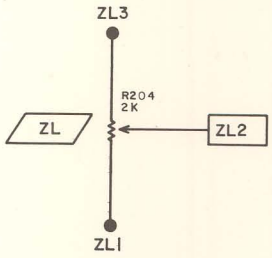
ISSUED E1266 | APPROVED | SHEET 1 OF 1

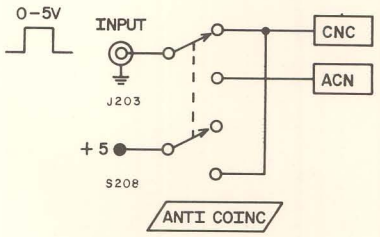
GSC

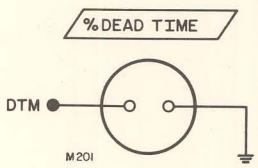

ULD3
R201
2K
UPPER
LEVEL
ULD2
ULD1

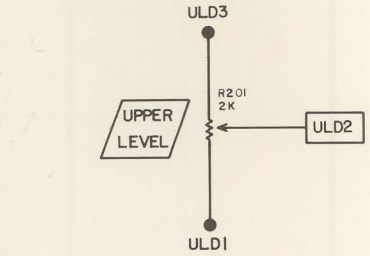

LLD3
R202
2K
LOWER
LEVEL
LLD2
LLD1

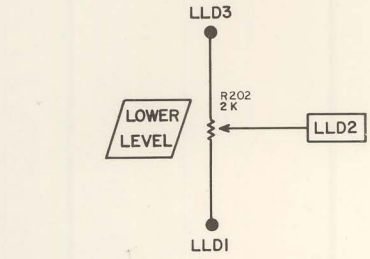

TH3
R203
2K
THRESHOLD
TH2
TH1

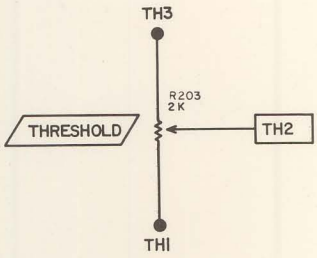

ZL3
R204
2K
ZL
ZL2
ZL1

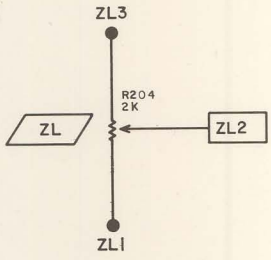

0-5V
INPUT
J203
CNC
ACN
+5
S208
ANTI COINC

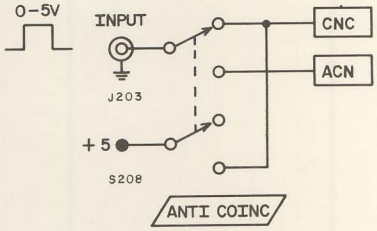

%DEAD TIME
DTM
M201

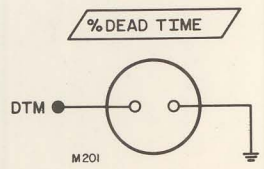


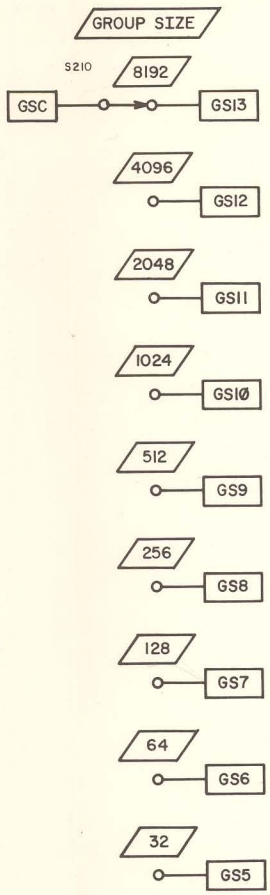


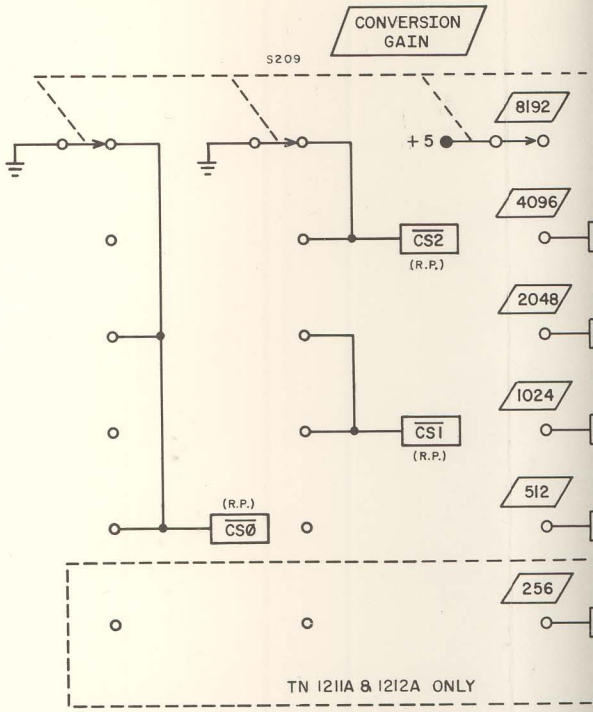


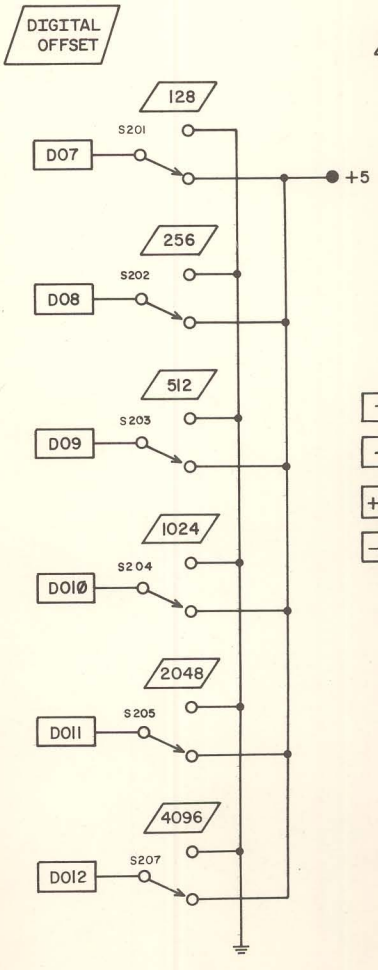


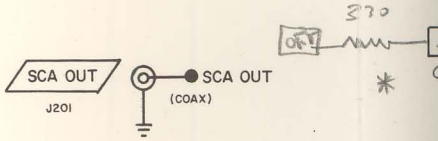


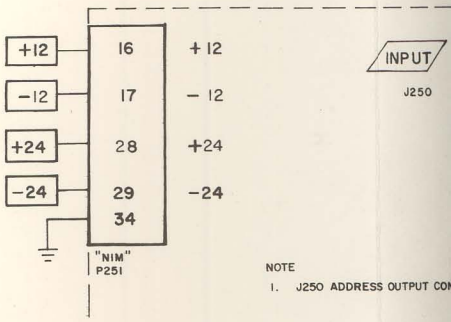




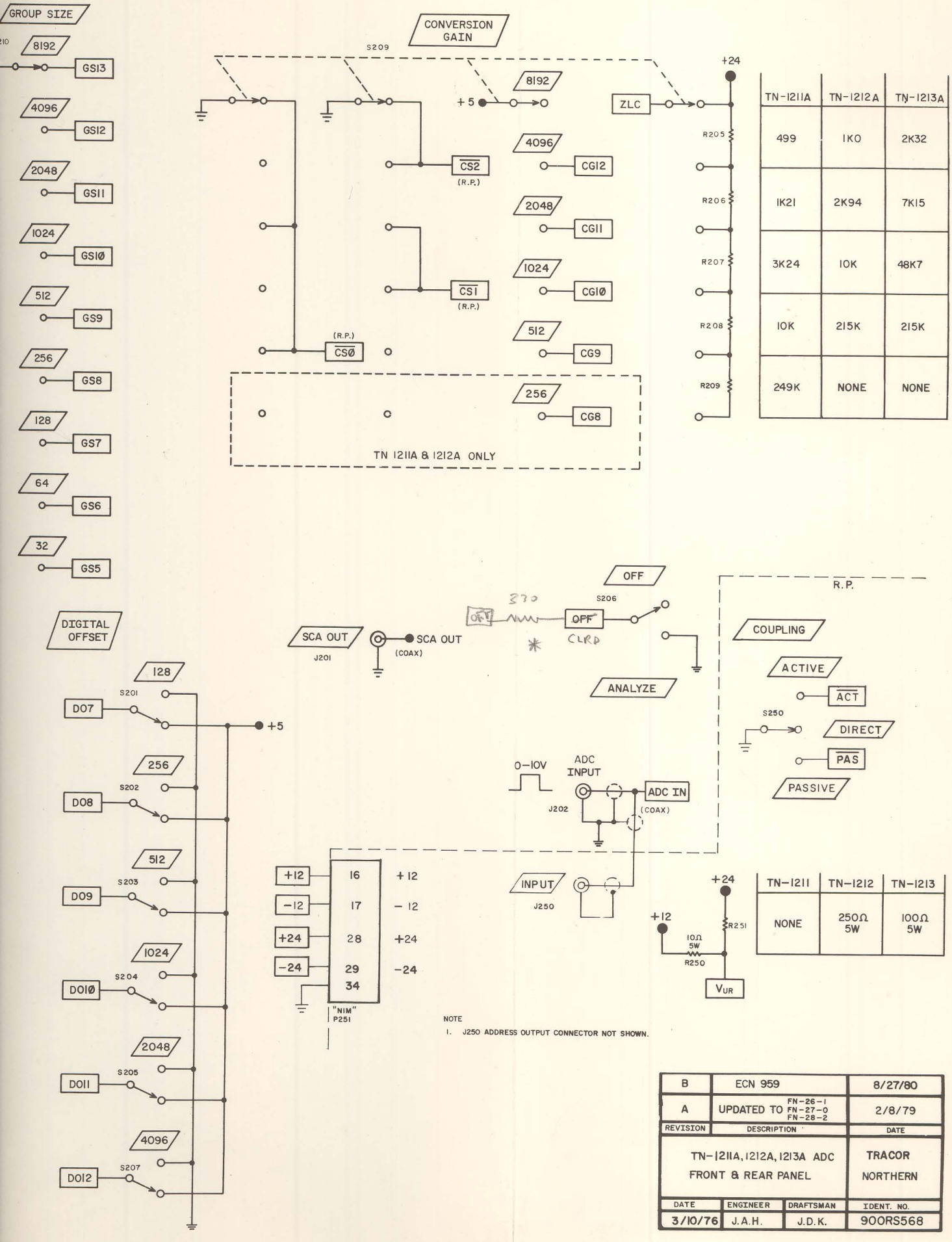








NOTE
1. J250 ADDRESS OUTPUT CON

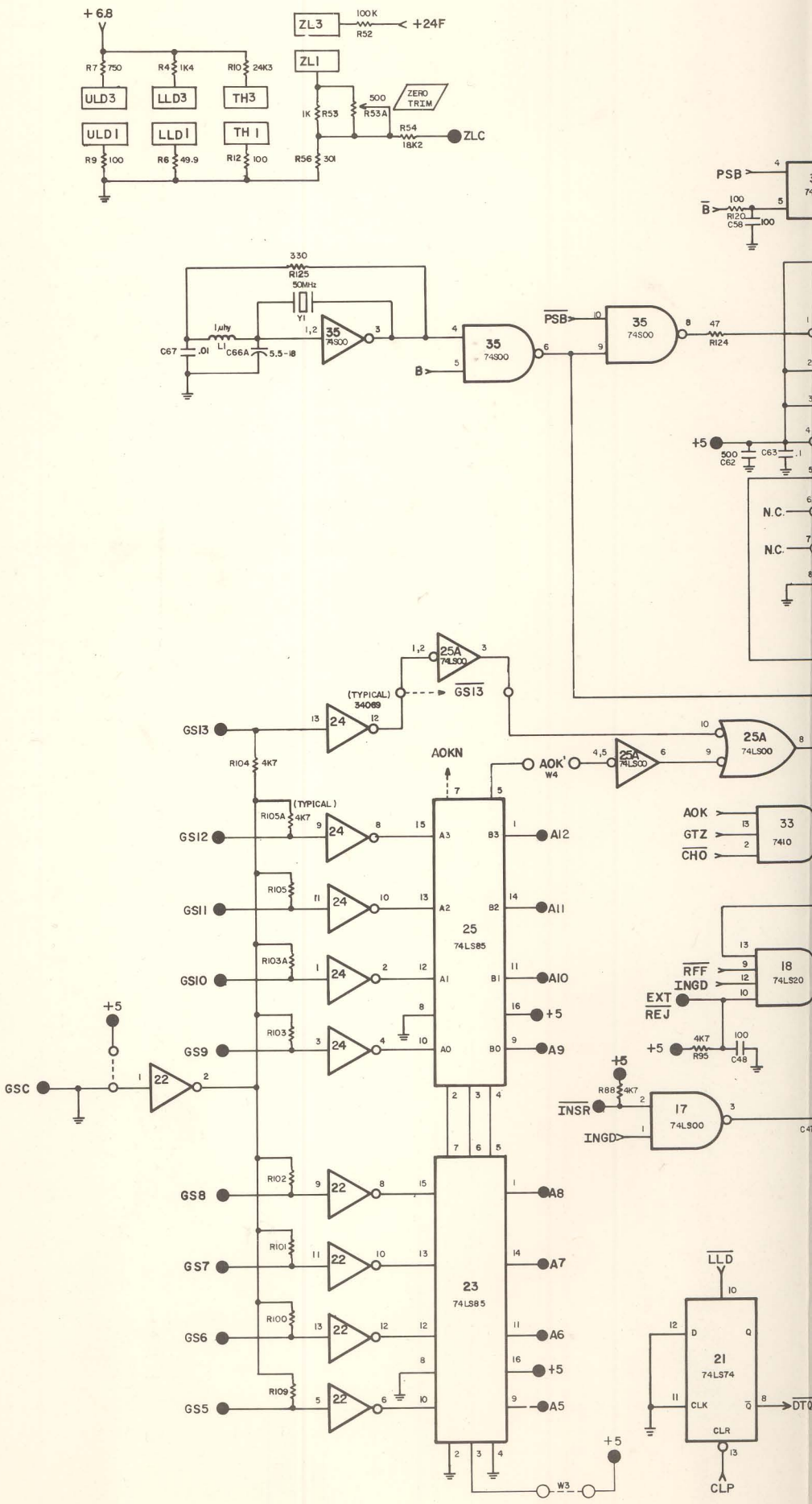


REVISION	DESCRIPTION	DATE
B	ECN 959	8/27/80
A	UPDATED TO FN-26-1 FN-27-0 FN-28-2	2/8/79

TN-1211A, 1212A, 1213A ADC FRONT & REAR PANEL

TRACOR NORTHERN

DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
3/10/76	J.A.H.	J.D.K.	900RS568


+6.8
R7 750
R4 1K4
R10 24K3
ULD3
LLD3
TH3
ULD1
LLD1
TH1
R9 100
R6 49.9
R12 100
R56 301
ZL3
100K
R52
+24F
ZL1
1K R53
500 R53A
ZERO TRIM
R54 18K2
ZLC
PSB
B
100 R120
C58 100
330 R125
50MHz Y1
1µhy L1
C67 .01
C66A 5.5-18
35 74S00
47 R124
+5
500 C62
C63 .1
N.C.
25A 74LS00
(TYPICAL) 34069
GS13
R104 4K7
AOKN
AOK' W4
(TYPICAL) R105A 4K7
GS12
GS11
GS10
GS9
GSC
R105
R103A
R103
25 74LS85
AI2
AI1
AI0
A9
A8
A7
A6
A5
AOK
GTZ
CHO
33 7410
RFF
INGD
EXT REJ
18 74LS20
4K7 R95
100 C48
R88 4K7
INSR
INGD
17 74LS00
R102
R101
R100
R109
GS8
GS7
GS6
GS5
23 74LS85
W3
LLD
21 74LS74
CLP
DTC

< +24F

ZERO TRIM

R54 18K2

ZLC

PSB

B

R120 100

C58 100

39 74LS00

35 74S00

R124 47

R123 100

36 74S112 (TYPICAL)

CK, IK, IJ, PR, Q, $\overline{Q}$, GND, Vcc, CLR, 2CLR, 2CK, 2K, 2J, 2PR, 2Q

N.C.

+5

C63 .1

C62 500

DT IN

R111 2K7

24 4069

25A 74LS00

DT

+24F

R13 18K2

22 4069

LLD

OFF

DTQ

REC

13 74LS20

MPS2222

10K R73A

DTM

CR13

CR12

C38 3.3µf 15V

6K8 R73

CR16

15K R113

CLP

CR19

C59

RESET

R122 47

37 74S112

C61

C60 500

R113A 47

AI'

AO'

C

B

A

REVISION

GS13

AOKN

AOK'

W4

AOK

25 74LS85

A3, B3, A2, B2, A1, B1, A0, B0

AI2, AI1, AI0, A9

23 74LS85

A8, A7, A6, A5

AOK

GTZ

CHO

33 7410

OPTION

REJ

RFF

INGD

EXT REJ

18 74LS20

16 7404

STORE

R95 4K7

C48 100

INSR

R88 4K7

17 74LS00

C47 100

INGD

INSR

SW

multi

swipe

CLRD

CLEAR

CR20

R85 3K3

R86 2K2

R87 56K

15 74LS04

17

-24F

CLR

41 7402

42 74LS00

OFF

RESET

C70 390

R133 2K2

R134 2K2

DO7

DO8

DO9

DO10

DO11

DO12

R126 4K7, TYPICAL)

R110

R127

R129

R128

R130

C53 .1

C53A 33µf/1

C54

21 74LS74

LLD

DTQ

CLP

CSC

A2'

B

20 74LS00

40 74LS221

REC'

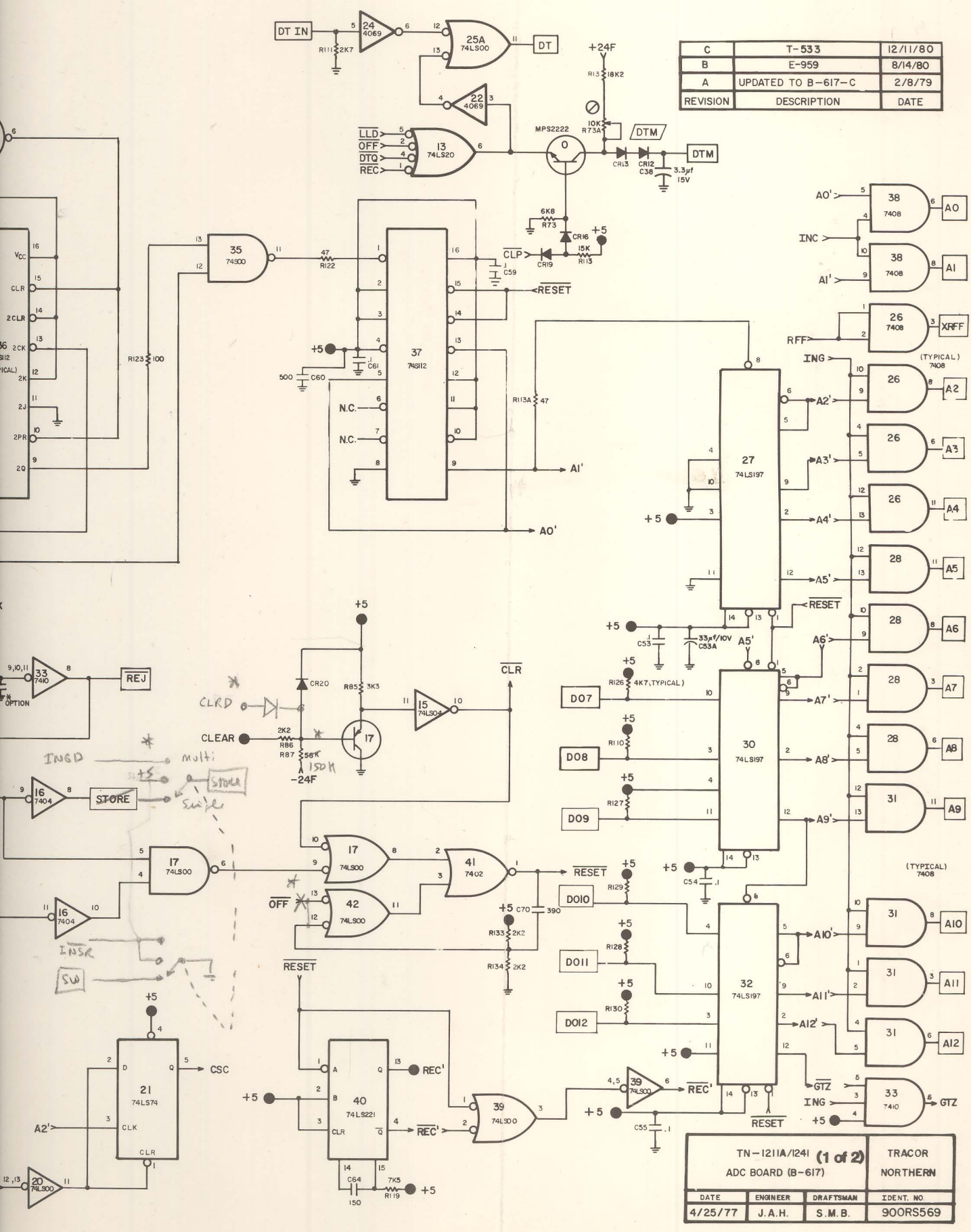
C64 150

R119 7K5

C55 .1

W3

4/25



REVISION	DESCRIPTION	DATE
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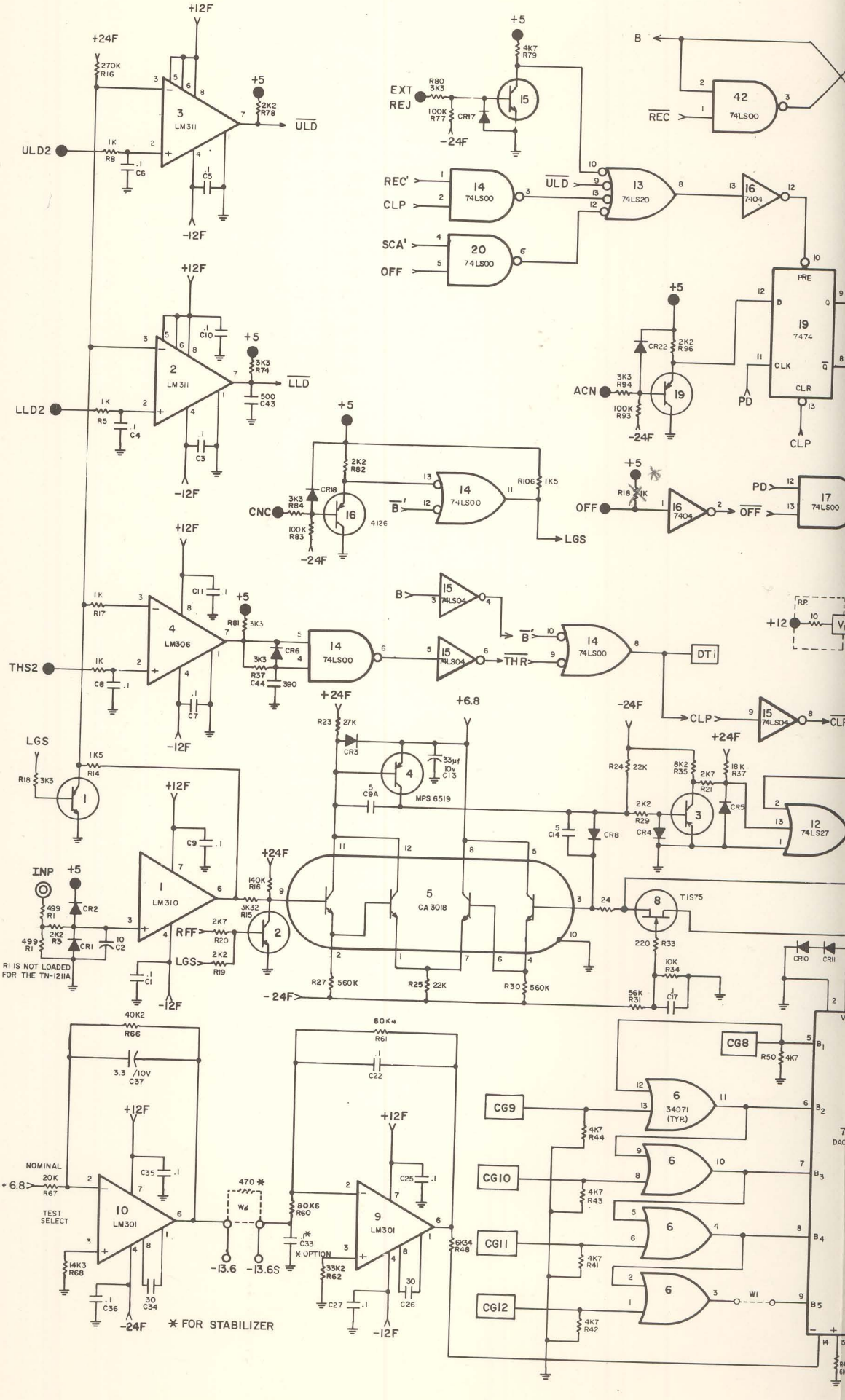
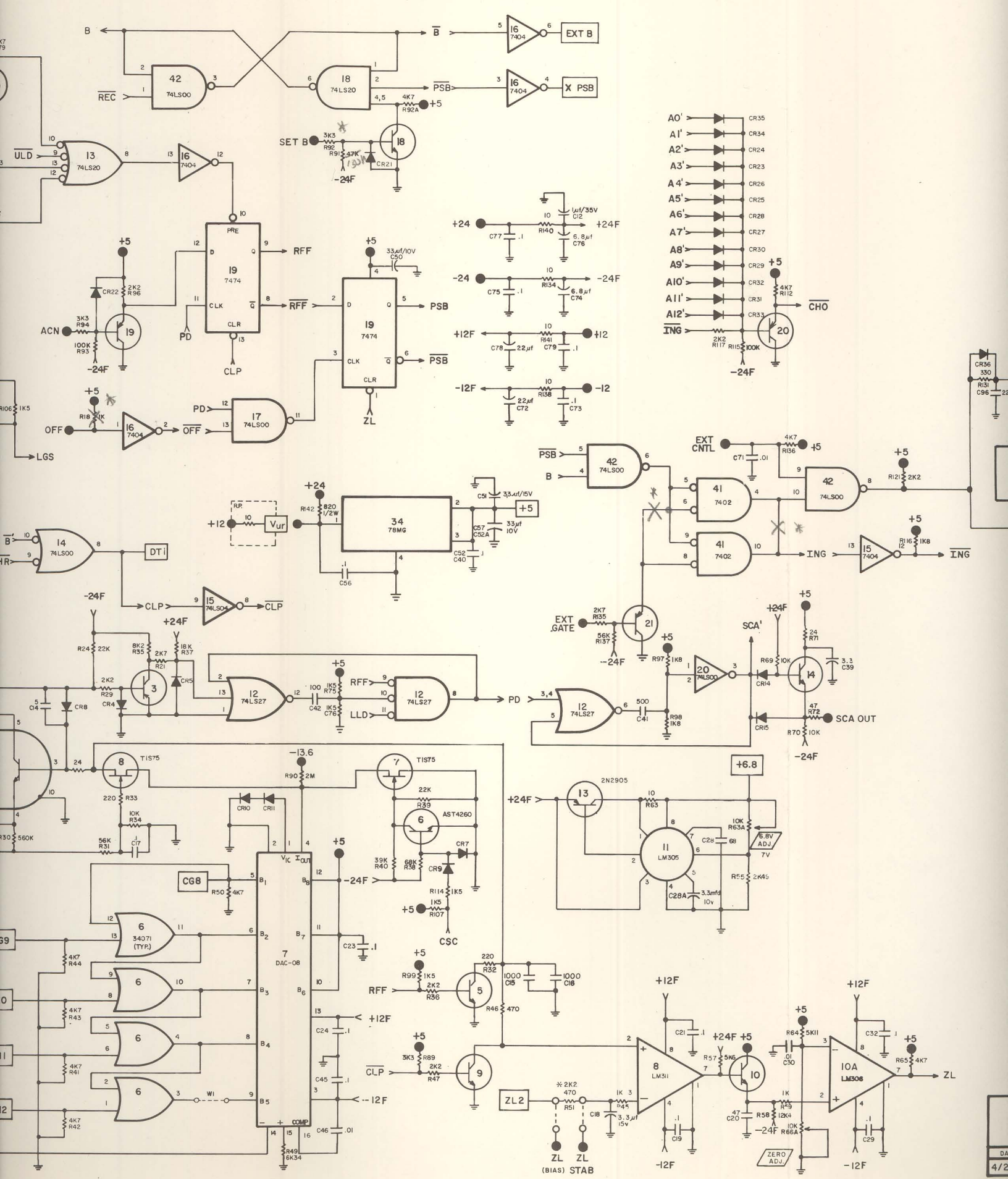
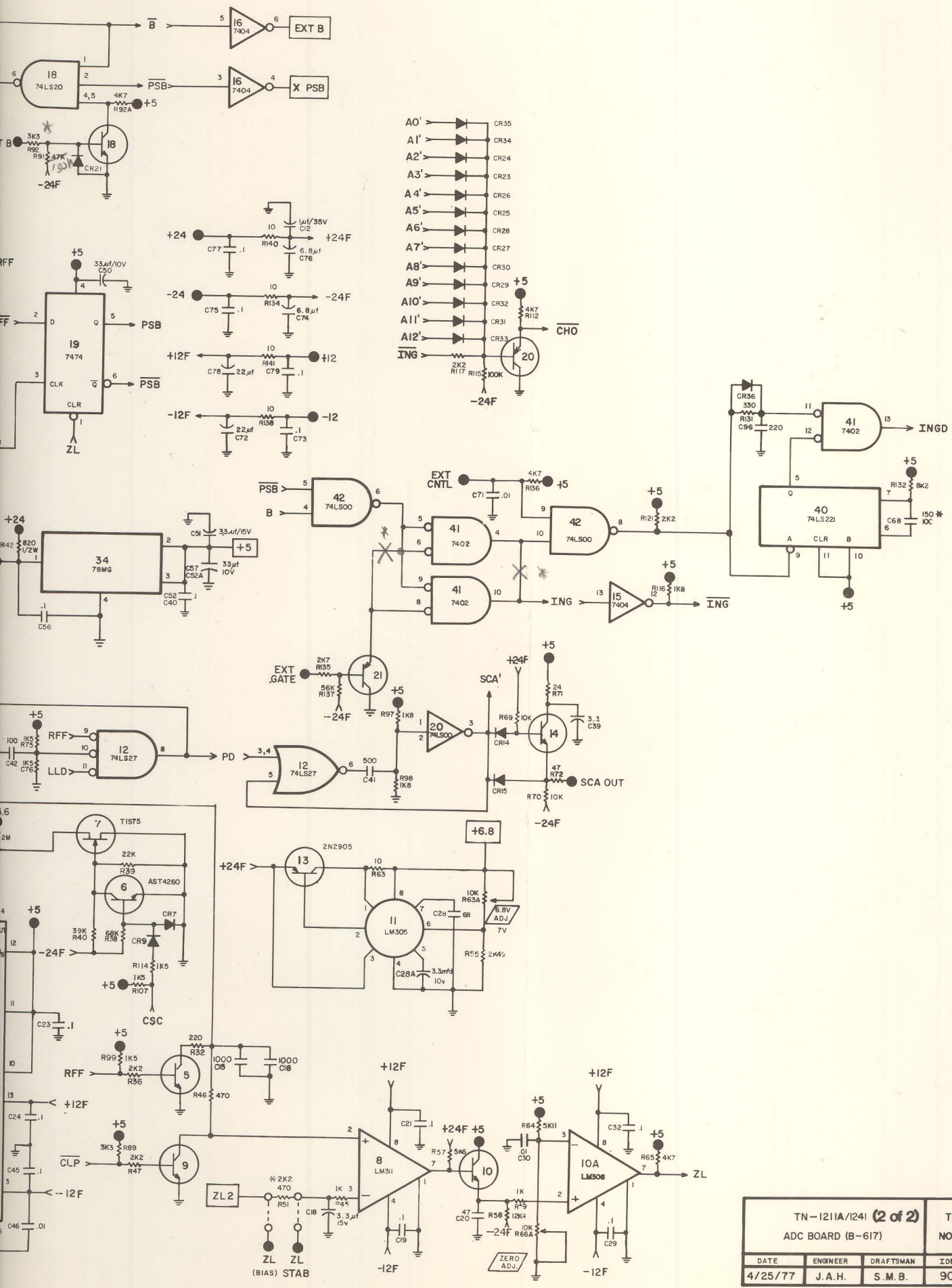
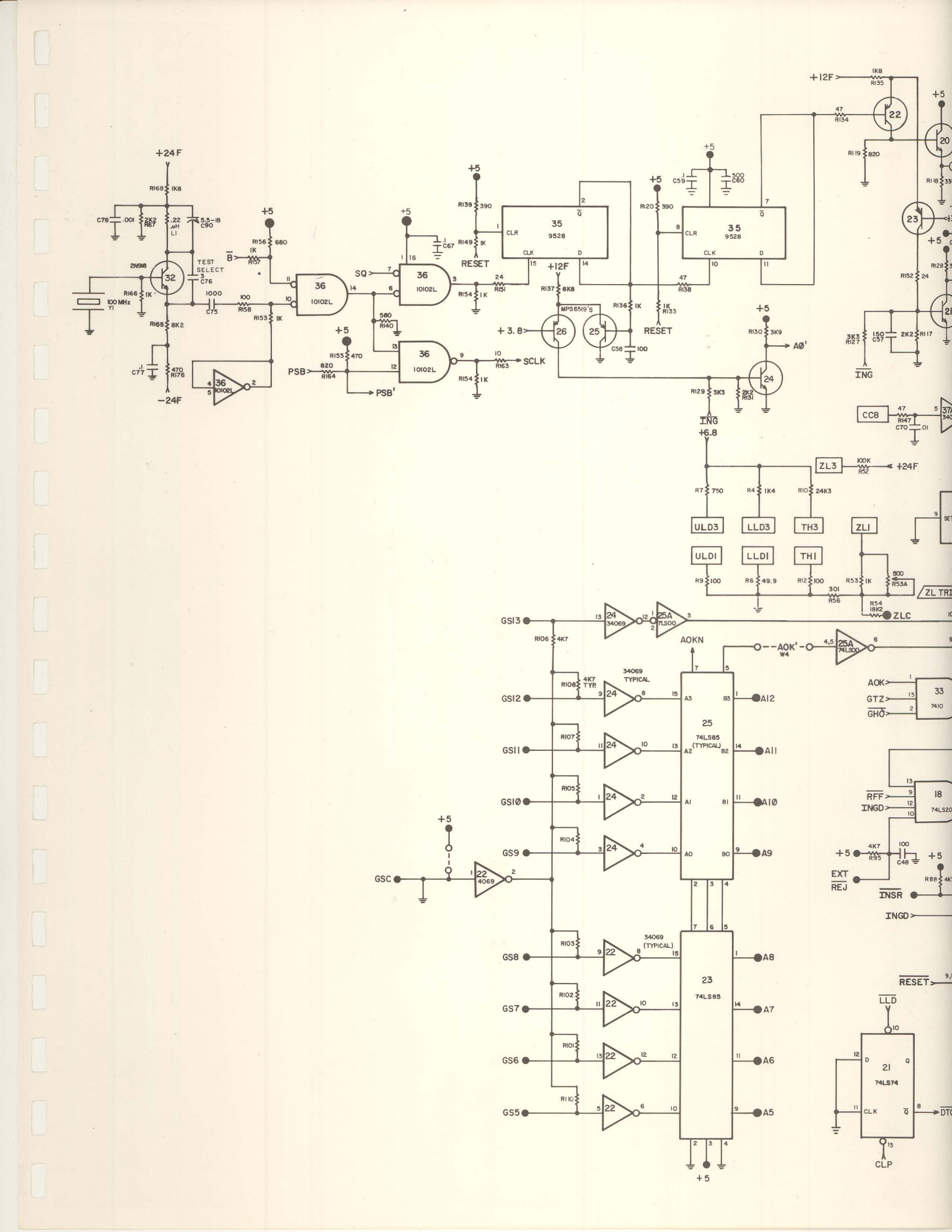
B	E-959	8/14/80
A	UPDATED TO B-617-C	2/8/79

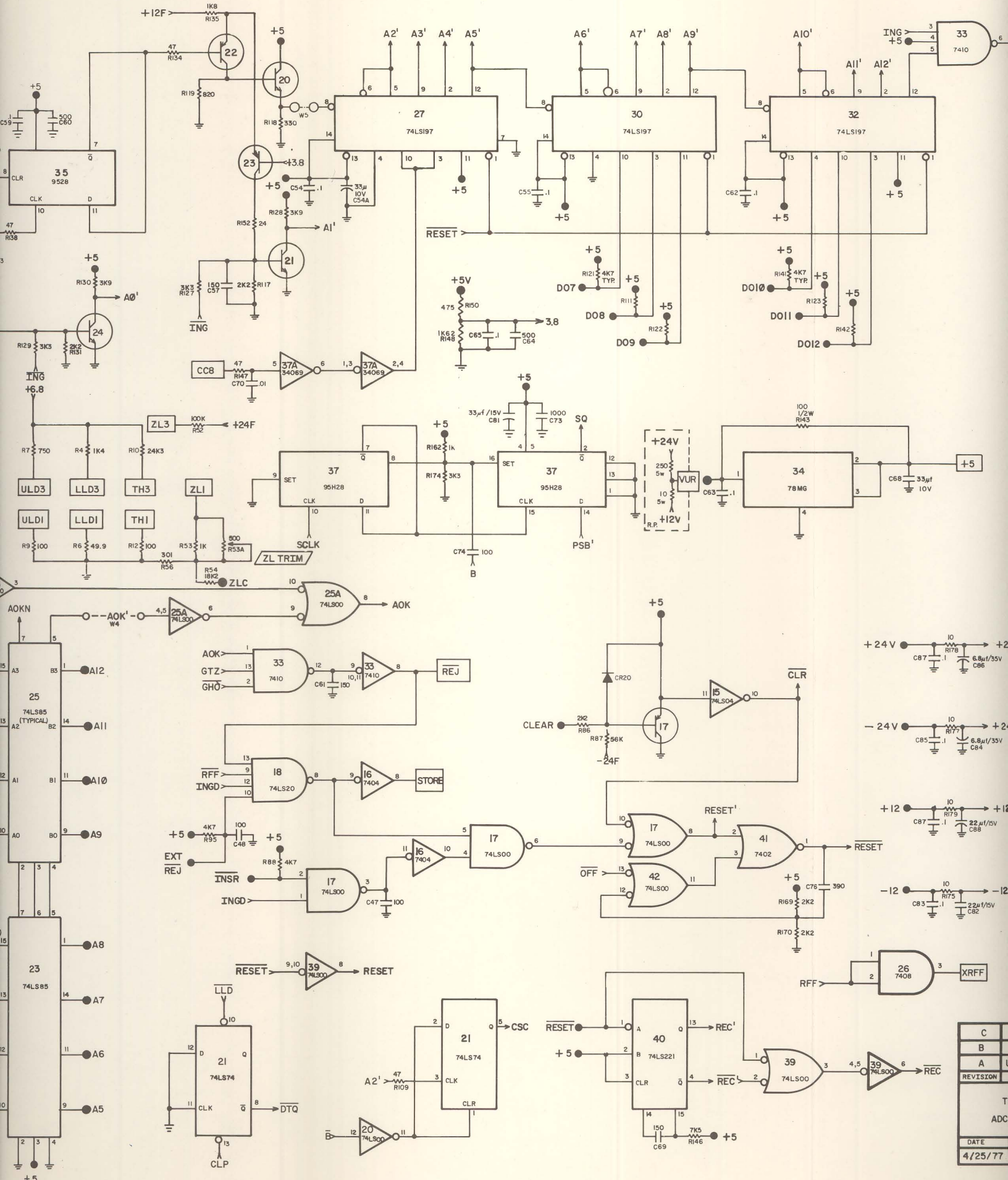

+12F
+24F
270K R16
3 LM311
+5
2K2 R78
ULD
ULD2
1K R8
.1 C6
C5
-12F
+5
4K7 R79
EXT REJ
R80 3K3
100K R77
CR17
15
-24F
B
42 74LS00
REC
REC'
CLP
14 74LS00
ULD
13 74LS20
16 7404
SCA'
OFF
20 74LS00
+12F
2 LM311
C10 .1
3K3 R74
LLD
500 C43
LLD2
1K R5
C4 .1
C3 .1
-12F
+5
CR22
2K2 R96
3K3 R94
ACN
100K R93
19
-24F
PRE
19 7474
CLK
CLR
PD
CLP
+5
2K2 R82
CR18
3K3 R84
CNC
100K R83
16 4126
14 74LS00
R106 1K5
LGS
+5
R18 1K
16 7404
OFF
OFF
PD
17 74LS00
+12F
4 LM306
C11 .1
1K R17
+5
R81 3K3
THS2
1K R8
C8 .1
C7 .1
-12F
CR6
3K3 R37
C44 390
14 74LS00
B
15 74LS04
THR
14 74LS00
DTI
RP
+12
V
+24F
+6.8
R23 27K
CR3
4
33µf 10V C13
C9A
MPS 6519
-24F
CLP
15 74LS04
+24F
R24 22K
8K2 R35
2K7 R21
18K R37
2K2 R29
CR4
CR8
C14
CR5
3
12 74LS27
LGS
1K5 R14
R18 3K3
1
+12F
C9 .1
INP
+5
499 R1
2K2 R3
499 R1
CR2
CR1
10 C2
R1 IS NOT LOADED FOR THE TN-1211A
1 LM310
+24F
140K R16
3K32 R15
RFF
2K7 R20
LGS
2K2 R19
C1 .1
-12F
2
5 CA 3018
8
TIS75
220 R33
10K R34
56K R31
C17 .1
CR10
CR11
R27 560K
R25 22K
R30 560K
-24F
40K2 R66
3.3 /10V C37
+12F
NOMINAL 20K R67
+6.8
TEST SELECT
10 LM301
C35 .1
14K3 R68
.1 C36
30 C34
-24F
470 *
W2
-13.6
-13.6S
* FOR STABILIZER
60K4 R61
C22
80K6 R60
* C33
* OPTION
+12F
9 LM301
C25 .1
33K2 R62
C27 .1
30 C26
-12F
6K34 R48
CG8
R50 4K7
CG9
CG10
CG11
CG12
6 34071 (TYP.)
4K7 R44
4K7 R43
4K7 R41
4K7 R42
B1
B2
B3
B4
B5
W1
DAC

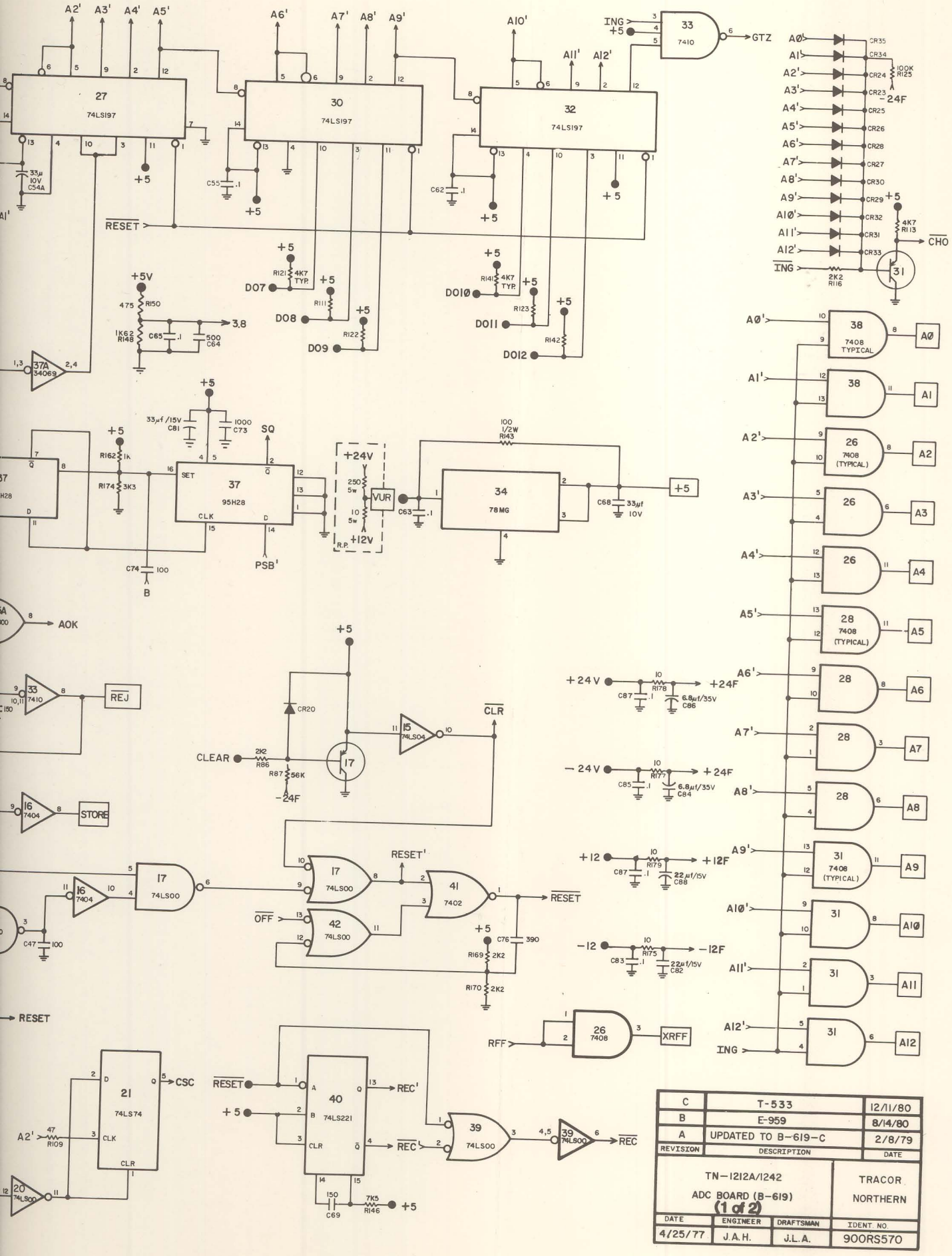

B
REC
42 74LS00
18 74LS20
EXT B
X PSB
SET B
ULD
13 74LS20
16 7404
18
CR21
-24F
+5
PRE
19 7474
CLK
CLR
RFF
PSB
ACN
CR22
19
PD
CLP
ZL
OFF
17 74LS00
LGS
+24
+12
-24
-12
+24F
+12F
-12F
+12
-12
CR35
CR34
CR24
CR23
CR26
CR25
CR28
CR27
CR30
CR29
CR32
CR31
CR33
A0'
A1'
A2'
A3'
A4'
A5'
A6'
A7'
A8'
A9'
A10'
A11'
A12'
ING
CHO
20
CR36
34 78MG
Vur
DTi
14 74LS00
15 74LS04
41 7402
EXT CNTL
EXT GATE
21
SCA'
SCA OUT
CR14
CR15
CR4
CR5
CR8
3
12 74LS27
LLD
PD
CR10
CR11
CR7
CR9
CSC
CG8
8 TIS75
7 TIS75
6 AST4260
5
9
7 DAC-08
6 34071 (TYP.)
COMP
13 2N2905
11 LM305
6.8V ADJ.
7V
8 LM311
10
10A LM306
ZL2
ZL (BIAS)
ZL STAB
ZERO ADJ.
WI
DA
4/2



TN-1211A/1241 (2 of 2) ADC BOARD (B-617)			TRACOR NORTHERN
DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
4/25/77	J.A.H.	S.M.B.	900RS569


+24F
R168 1K8
C78 .001
2K2 R67
.22 µH L1
5.5-18 C90
2N918
32
TEST SELECT
R166 1K
100 MHz Y1
R165 8K2
C77 .1
470 R176
-24F
+5
R156 680
1K R157
B
36 10102L
1000 C75
100 R158
R153 1K
SQ
36 10102L
560 R140
R155 470
820 R164
PSB
PSB'
C67 .1
R139 390
R149 1K
RESET
35 9528
CLR CLK D Q
24 R151
R154 1K
+12F
R137 6K8
MPS6519'S
+3.8
26
25
R136 1K
1K R133
RESET
C58 100
R120 390
C59 .1
500 C60
R130 3K9
A0'
R129 3K3
2K2 R131
ING
+6.8
ZL3
100K R52
+24F
R7 750
R4 1K4
R10 24K3
ULD3
LLD3
TH3
ZLI
ULDI
LLDI
THI
R9 100
R6 49.9
R12 100
R53 1K
500 R53A
301 R56
R54 18K2
ZLC
ZL TRI
CC8
47 R147
C70 .01
R135 1K8
47 R134
R119 820
R118 33
R152 24
3K3 R127
150 C57
2K2 R117
GSI3
R106 4K7
24 34069
25A 74LS00
AOKN
AOK'
W4
GSI2
R108 4K7 TYP.
34069 TYPICAL
GSI1
R107
GSI0
R105
GS9
R104
GSC
22 4069
25 74LS85 (TYPICAL)
A3 B3 A2 B2 A1 B1 A0 B0
AI2
AI1
AI0
A9
GS8
R103
GS7
R102
GS6
R101
GS5
R110
34069 (TYPICAL)
23 74LS85
A8
A7
A6
A5
+5
AOK
GTZ
GHO
33 7410
RFF
INGD
18 74LS20
EXT REJ
4K7 R95
100 C48
INSR
INGD
RESET
LLD
21 74LS74
D Q CLK
CLP
DTC


+12F
1K8 R135
47 R134
22
+5
20
R119 820
W5
R118 330
23
+13.8
C54 .1
33µ 10V C54A
R128 3K9
R152 24
21
AI'
3K3 R127
150 C57
2K2
R117
ING
A2' A3' A4' A5'
27 74LS197
A6' A7' A8' A9'
30 74LS197
A10' A11' A12'
32 74LS197
ING
33 7410
C55 .1
C62 .1
RESET
35 9528
CLR
CLK
D
Q
47 R138
R130 3K9
A0'
24
R129 3K3
2K2 R131
ING
+5V
475 R150
1K62 R148
C65 .1
500 C64
3.8
DO7
DO8
DO9
DO10
DO11
DO12
R121 4K7 TYP.
R111
R122
R141 4K7 TYP.
R123
R142
CC8
47 R147
C70 .01
37A 34069
+6.8
ZL3
100K R52
+24F
R7 750
R4 1K4
R10 24K3
ULD3
LLD3
TH3
ZLI
ULDI
LLDI
THI
R9 100
R6 49.9
R12 100
R53 1K
500 R53A
301 R56
R54 18K2
ZLC
SCLK
ZL TRIM
33µf/15V C81
1000 C73
SQ
37 95H28
R162 1k
R174 3K3
C74 100
B
PSB'
+24V
250 5w
VUR
10 5w
+12V
R.P.
C63 .1
100 1/2W R143
34 78MG
C68 33µf 10V
AOKN
AOK'
W4
25A 74LS00
AOK
25 74LS85 (TYPICAL)
AI2
AI1
AI0
A9
23 74LS85
A8
A7
A6
A5
GTZ
GHO
REJ
C61 150
RFF
INGD
18 74LS20
16 7404
STORE
EXT REJ
4K7 R95
100 C48
INSR
R88 4K7
17 74LS00
C47 100
CLEAR
2K2 R86
R87 56K
-24F
CR20
15 74LS04
CLR
RESET'
41 7402
OFF
42 74LS00
C76 390
R169 2K2
R170 2K2
+24 V
-24 V
-12
R178
R177
R179
R175
6.8µf/35V C86
6.8µf/35V C84
22µf/15V C88
22µf/15V C82
C87 .1
C85 .1
C83 .1
RESET
9,10 39 74LS00
LLD
21 74LS74
DTQ
CLP
RFF
26 7408
XRFF
A2'
R109
CSC
B
20 74LS00
RESET
+5
40 74LS221
REC'
REC
39 74LS00
C69 150
R146 7K5
C
B
A
REVISION
DATE
4/25/77

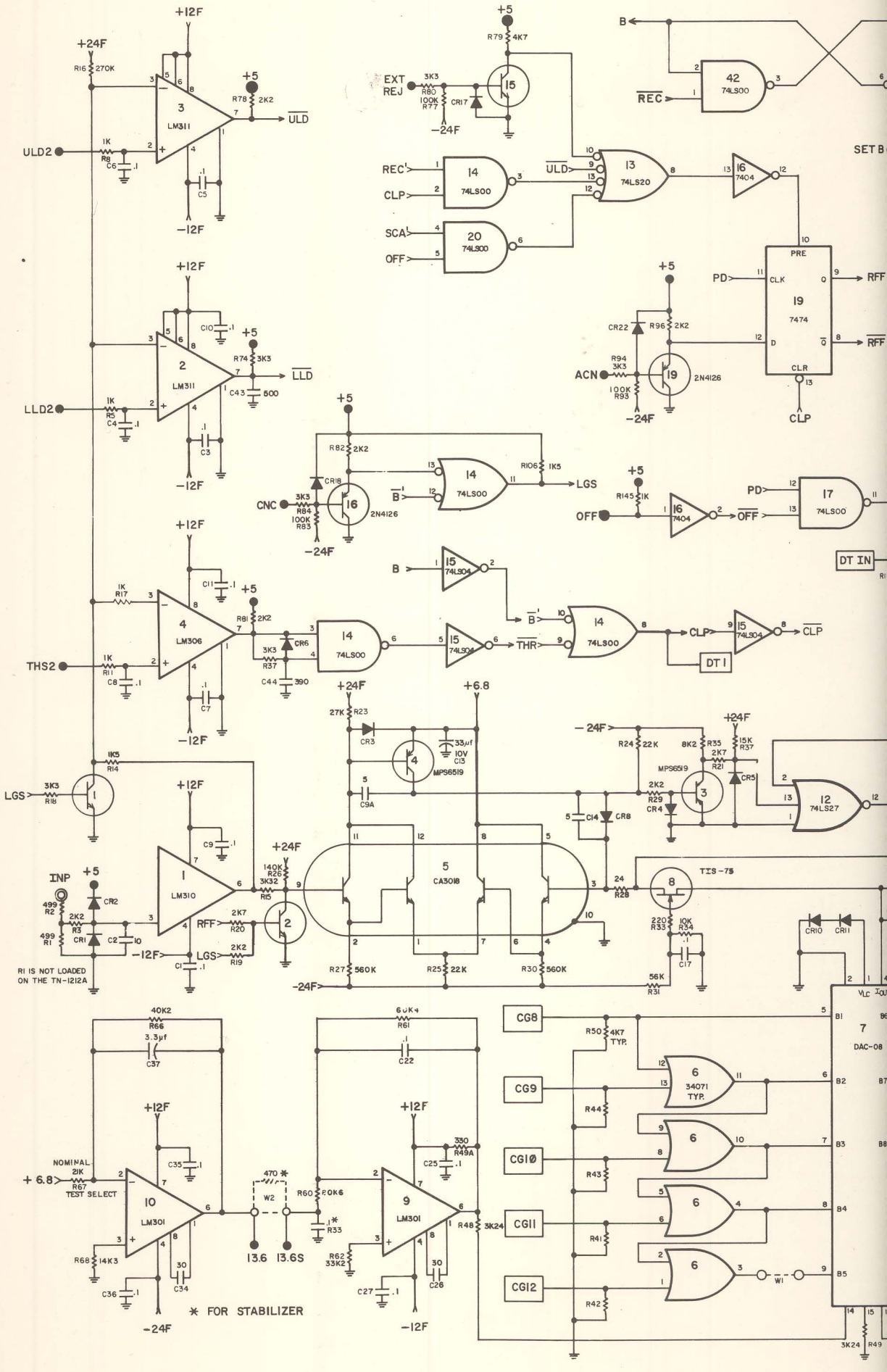


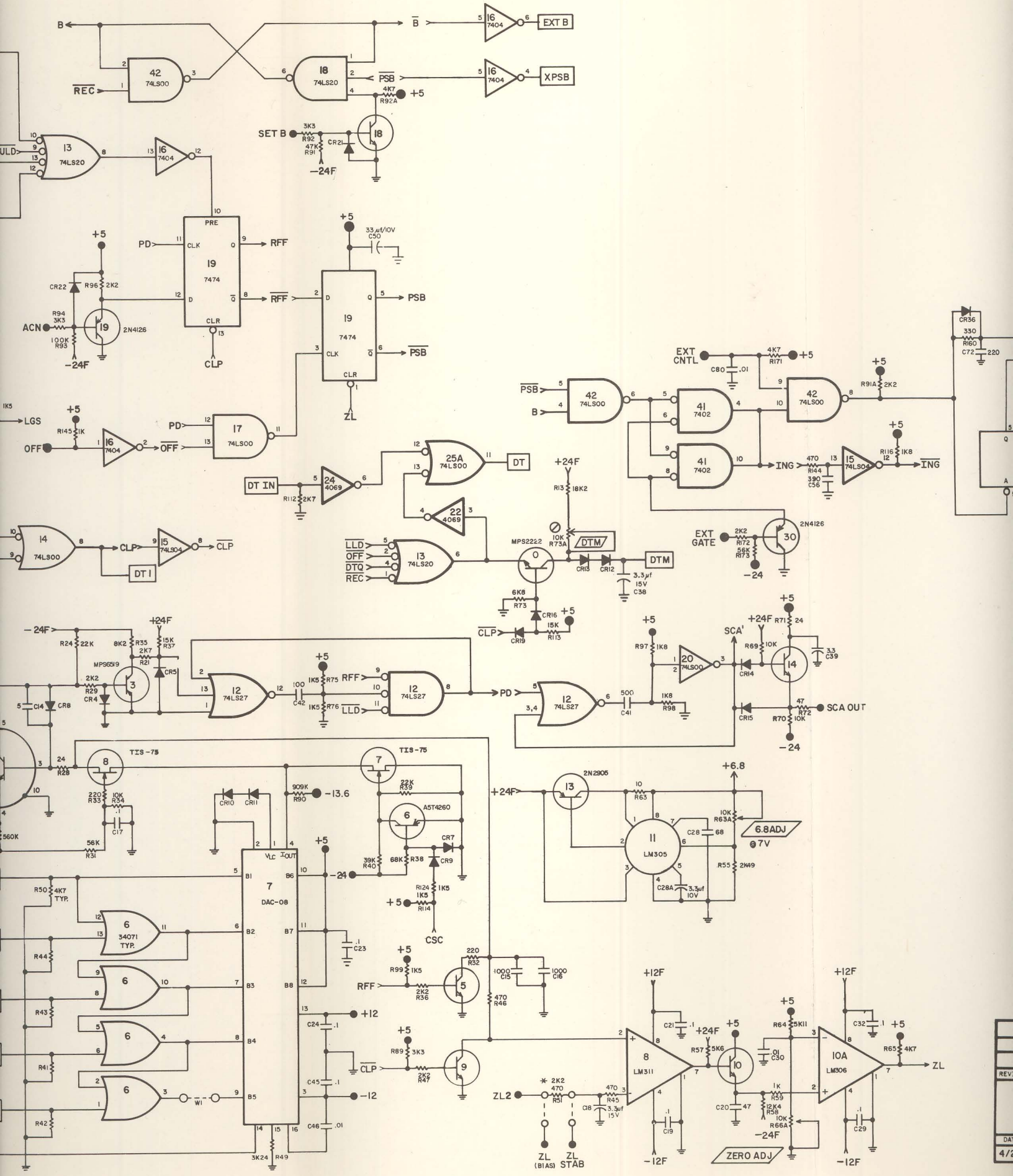
REVISION	DESCRIPTION	DATE
C	T-533	12/11/80
B	E-959	8/14/80
A	UPDATED TO B-619-C	2/8/79

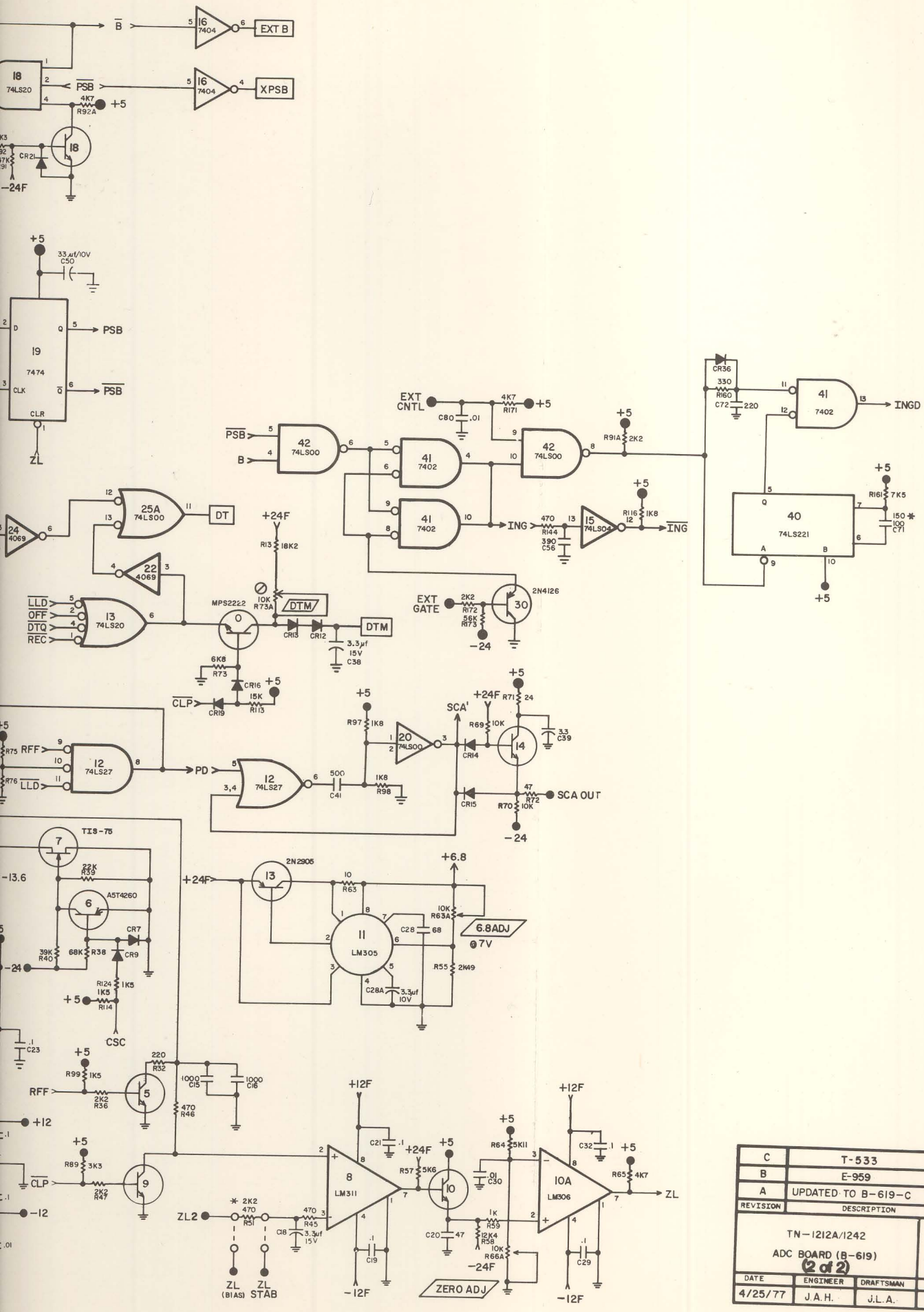
TN-1212A/1242
ADC BOARD (B-619)
(1 of 2)

TRACOR NORTHERN

DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
4/25/77	J.A.H.	J.L.A.	900RS570


+12F
+24F
R16 270K
3
LM311
+5
R78 2K2
ULD
ULD2
1K
R8
C6 .1
C5 .1
-12F
+5
R79 4K7
EXT REJ
3K3
R80
100K
R77
CR17
15
-24F
B
42
74LS00
REC
SET B
REC'
14
74LS00
CLP
SCA'
20
74LS00
OFF
ULD
13
74LS20
16
7404
PRE
PD
CLK
19
7474
D
CLR
RFF
RFF
CR22
R96 2K2
R94 3K3
ACN
100K
R93
19
2N4126
-24F
CLP
+12F
C10 .1
2
LM311
+5
R74 3K3
LLD
C43 500
LLD2
1K
R5
C4 .1
C3 .1
-12F
+5
R82 2K2
CR18
CNC
3K3
R84
100K
R83
16
2N4126
14
74LS00
R106 1K5
LGS
-24F
+5
R145 1K
OFF
16
7404
OFF
PD
17
74LS00
DT IN
+12F
C11 .1
4
LM306
+5
R81 2K2
1K
R17
THS2
1K
R11
C8 .1
C7 .1
-12F
3K3
R37
CR6
C44 390
14
74LS00
15
74LS04
THR
B
15
74LS04
B'
14
74LS00
CLP
15
74LS04
CLP
DT 1
+24F
27K R23
CR3
4
MPS6519
33µf
10V
C13
C9A
+6.8
-24F
R24 22K
8K2
R35
2K7
R21
+24F
15K
R37
MPS6519
3
CR5
2K2
R29
CR4
C14
CR8
12
74LS27
LGS
3K3
R18
1K5
R14
1
+12F
C9 .1
1
LM310
INP
+5
499
R2
2K2
R3
499
R1
CR2
CR1
C2 10
-12F
C1 .1
RFF
2K7
R20
LGS
2K2
R19
+24F
140K
R26
3K32
R15
2
5
CA3018
R27 560K
R25 22K
R30 560K
-24F
TIS-75
8
220
R33
10K
R34
.1
C17
56K
R31
CR10
CR11
RI IS NOT LOADED
ON THE TN-1212A
40K2
R66
3.3µf
C37
+12F
NOMINAL
2IK
+ 6.8
R67
TEST SELECT
C35 .1
10
LM301
R68 14K3
30
C34
C36 .1
-24F
470 *
W2
13.6
13.6S
60K4
R61
.1
C22
+12F
330
R49A
C25 .1
9
LM301
R60 20K6
.1 *
R33
R62
33K2
R48 3K24
30
C26
C27 .1
-12F
* FOR STABILIZER
CG8
CG9
CGIØ
CGI1
CGI2
R50 4K7
TYP.
6
34071
TYP.
R44
R43
R41
R42
7
DAC-08
B1
B2
B3
B4
B5
W1
3K24
R49


B
REC
42 74LS00
18 74LS20
EXT B
XPSB
SET B
3K3 R92
47K R91
CR21
-24F
+5
4K7 R92A
13 74LS20
16 7404
PRE
CLK
CLR
19 7474
PD
RFF
CLP
33 µf/10V C50
CR22 R96 2K2
ACN
R94 3K3
100K R93
19 2N4126
LGS
OFF
R145 1K
17 74LS00
14 74LS00
15 74LS04
DT I
DT IN
R112 2K7
24 4069
25A 74LS00
DT
22 4069
LLD
OFF
DTQ
REC
13 74LS20
MPS2222
R73A 10K
DTM
CR13
CR12
3.3µf 15V C38
6K8 R73
CR16
CR19
15K R113
EXT CNTL
C80 .01
R171 4K7
41 7402
R91A 2K2
ING
R144 470
C56 390
R116 1K8
CR36
R160 330
C72 220
EXT GATE
R172 2K2
R173 56K
30 2N4126
-24
R13 18K2
+24F
SCA'
R71 24
R69 10K
C39 33
CR14
SCA OUT
R70 10K
R72 47
CR15
R97 1K8
20 74LS00
C41 500
R98 1K8
12 74LS27
R75 RFF
R76 LLD
C42 100
R24 22K
R35 8K2
R37 15K
R21 2K7
MPS6519
R29 2K2
CR4
CR5
CR8
C14
TIS-75
R28 24
R33 220
R34 10K
C17 .1
R31 56K
560K
CR10
CR11
909K R90
-13.6
22K R39
A5T4260
CR7
CR9
39K R40
68K R38
R124 1K5
R114 1K5
CSC
7 DAC-08
VLC
IOUT
B1
B2
B3
B4
B5
B6
B7
B8
6 34071 TYP.
R50 4K7 TYP.
R44
R43
R41
R42
W1
3K24 R49
C23 .1
C24 .1
C45 .1
C46 .01
+12
-12
R99 1K5
2K2 R36
RFF
220 R32
1000 C15
1000 C16
470 R46
R89 3K3
2K2 R47
CLP
2N2905
+6.8
R63 10
R63A 10K
6.8ADJ @7V
11 LM305
C28 68
C28A 3.3µf 10V
R55 2K49
+12F
-12F
C21 .1
R57 5K6
C19 .1
8 LM311
10 LM310
C20 47
C30 .01
R64 25K11
R59 1K
R58 12K4
R66A 10K
ZERO ADJ
C32 .1
R65 4K7
10A LM306
C29 .1
ZL
ZL2
R51 2K2 470
R45 470
C18 3.3µf 15V
ZL (BIAS)
ZL STAB

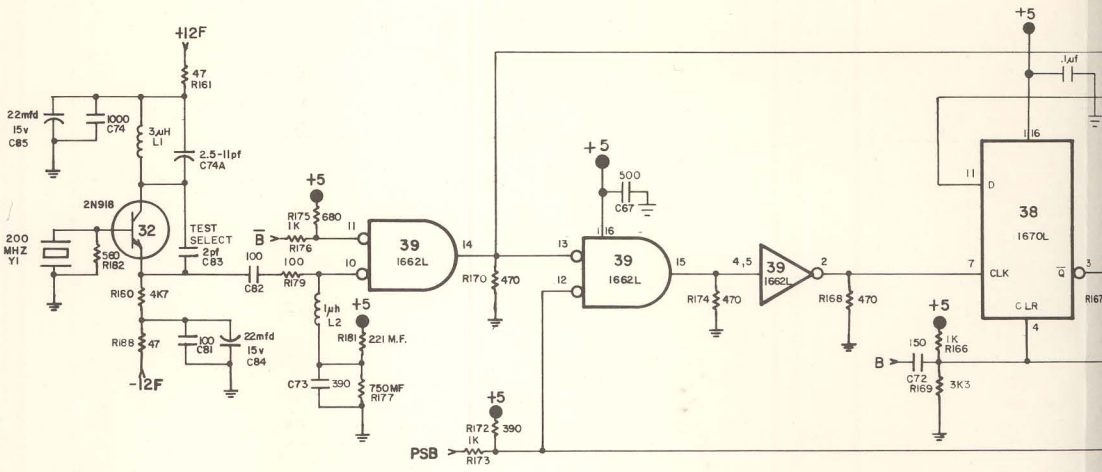


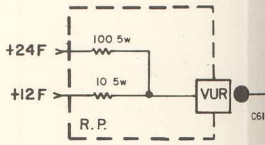
C	T-533	12/11/80
B	E-959	8/14/80
A	UPDATED TO B-619-C	2/8/79
REVISION	DESCRIPTION	DATE

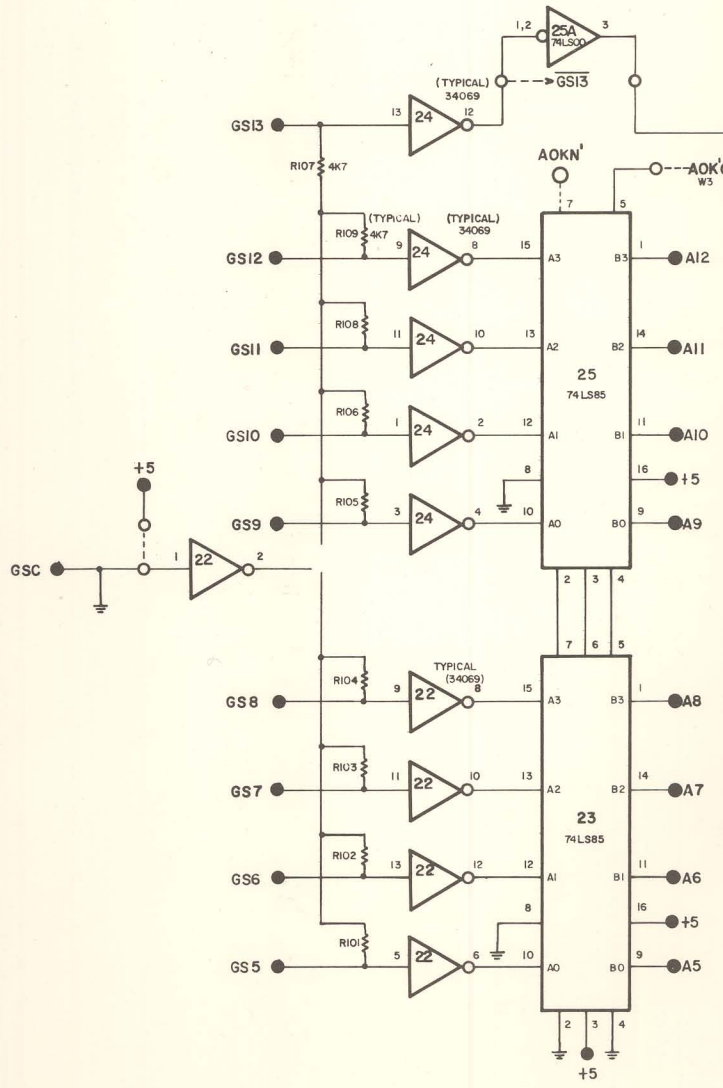
TN-1212A/1242
ADC BOARD (B-619)
(2 of 2)

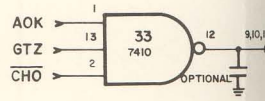
TRACOR NORTHERN

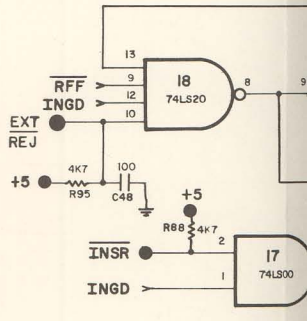
DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
4/25/77	J.A.H.	J.L.A.	900RS570





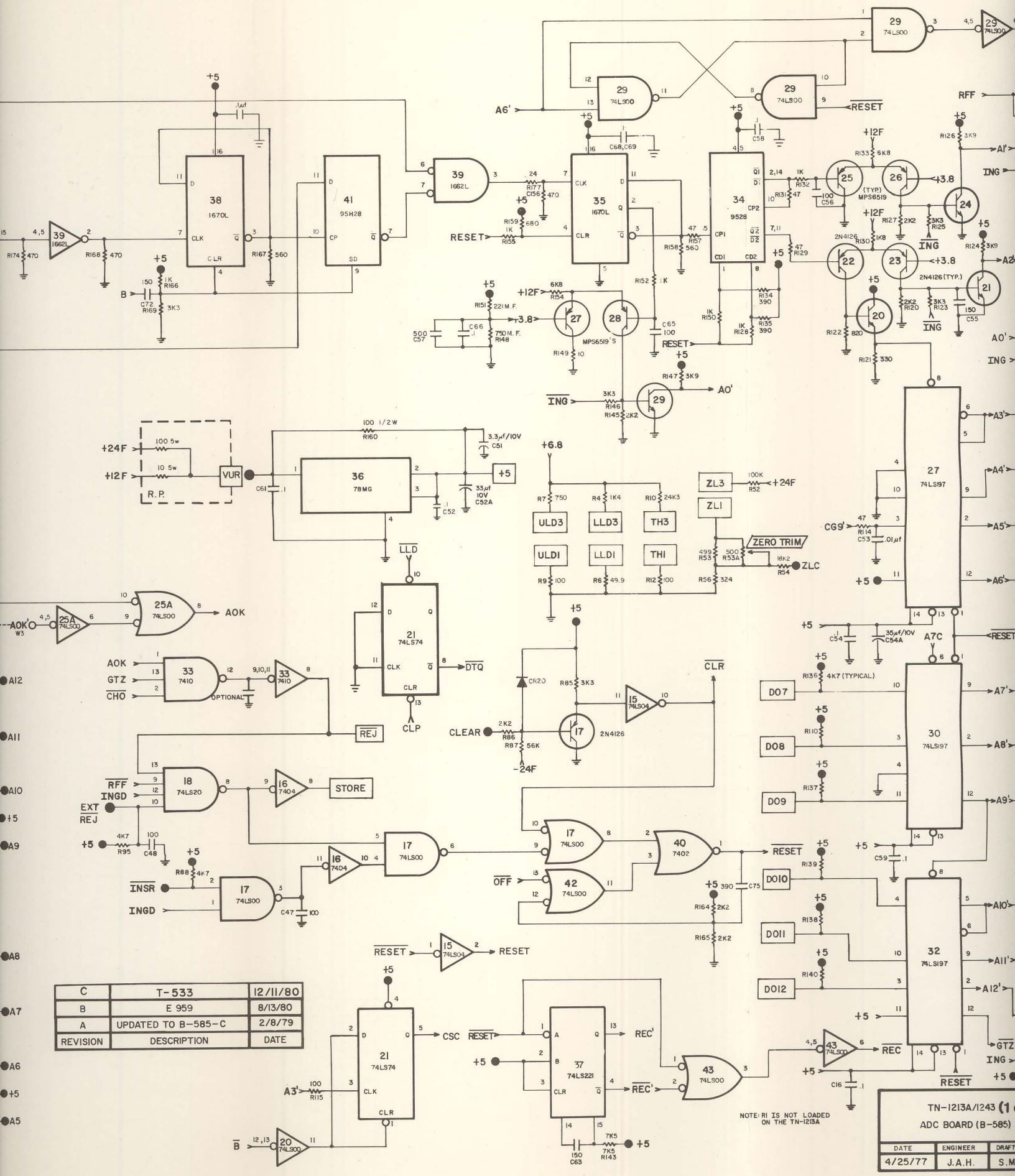






REVISION	DESCRIPTION	D
A	UPDATED TO B-585-C	2/
B	E 959	8/1
C	T-533	12/

B 12,13

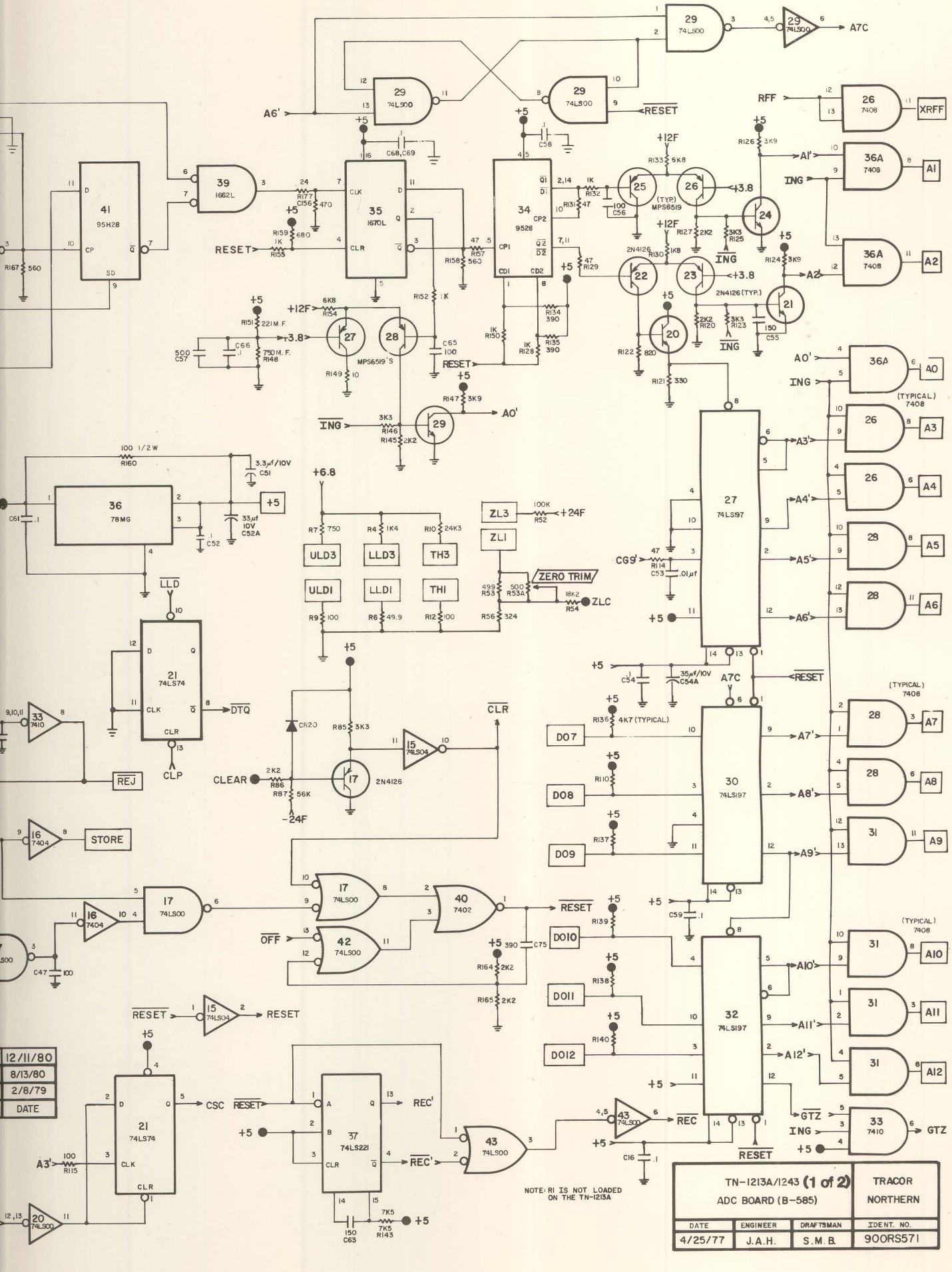


REVISION	DESCRIPTION	DATE
C	T-533	12/11/80
B	E 959	8/13/80
A	UPDATED TO B-585-C	2/8/79

TN-1213A/1243 (1

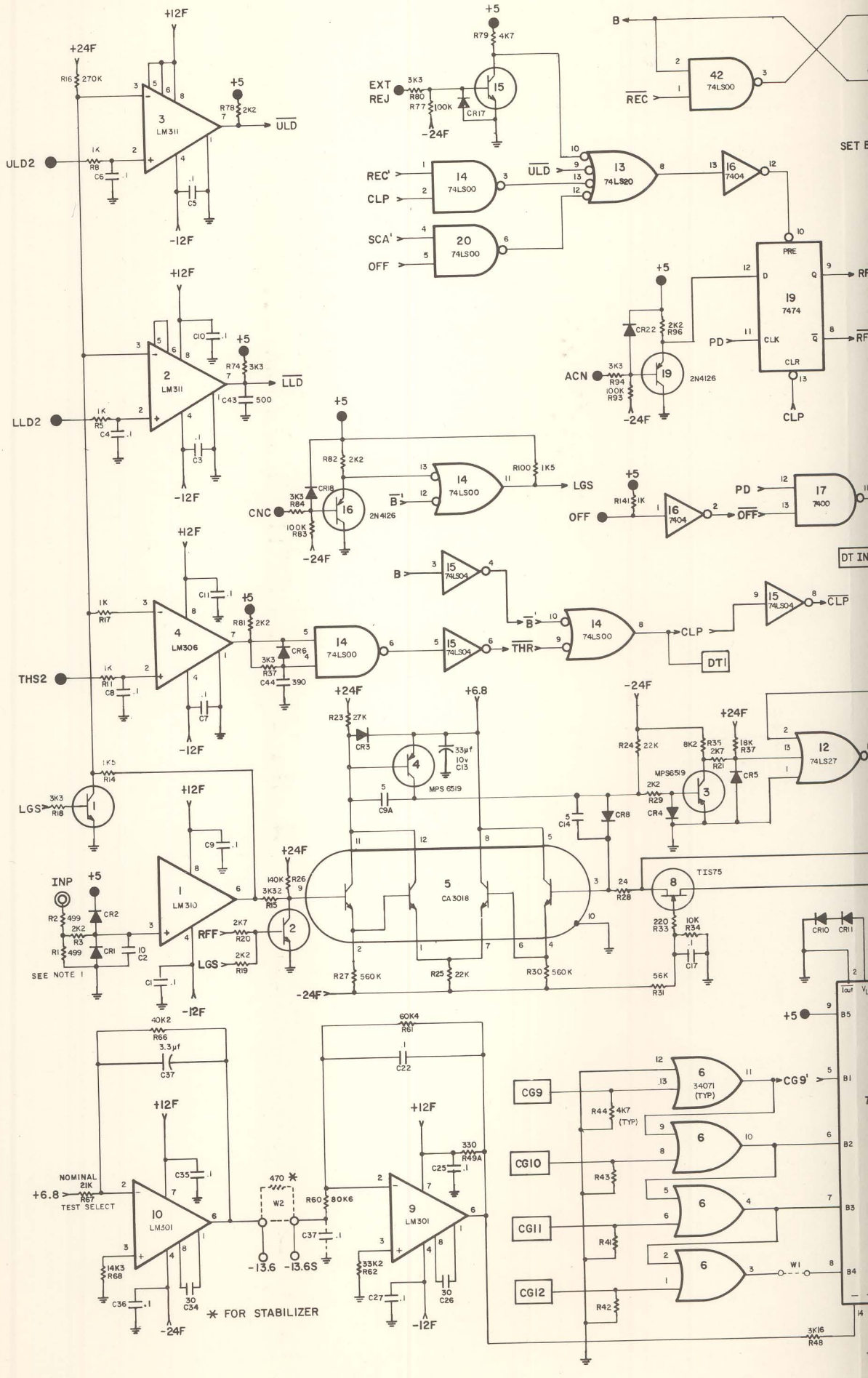
ADC BOARD (B-585)

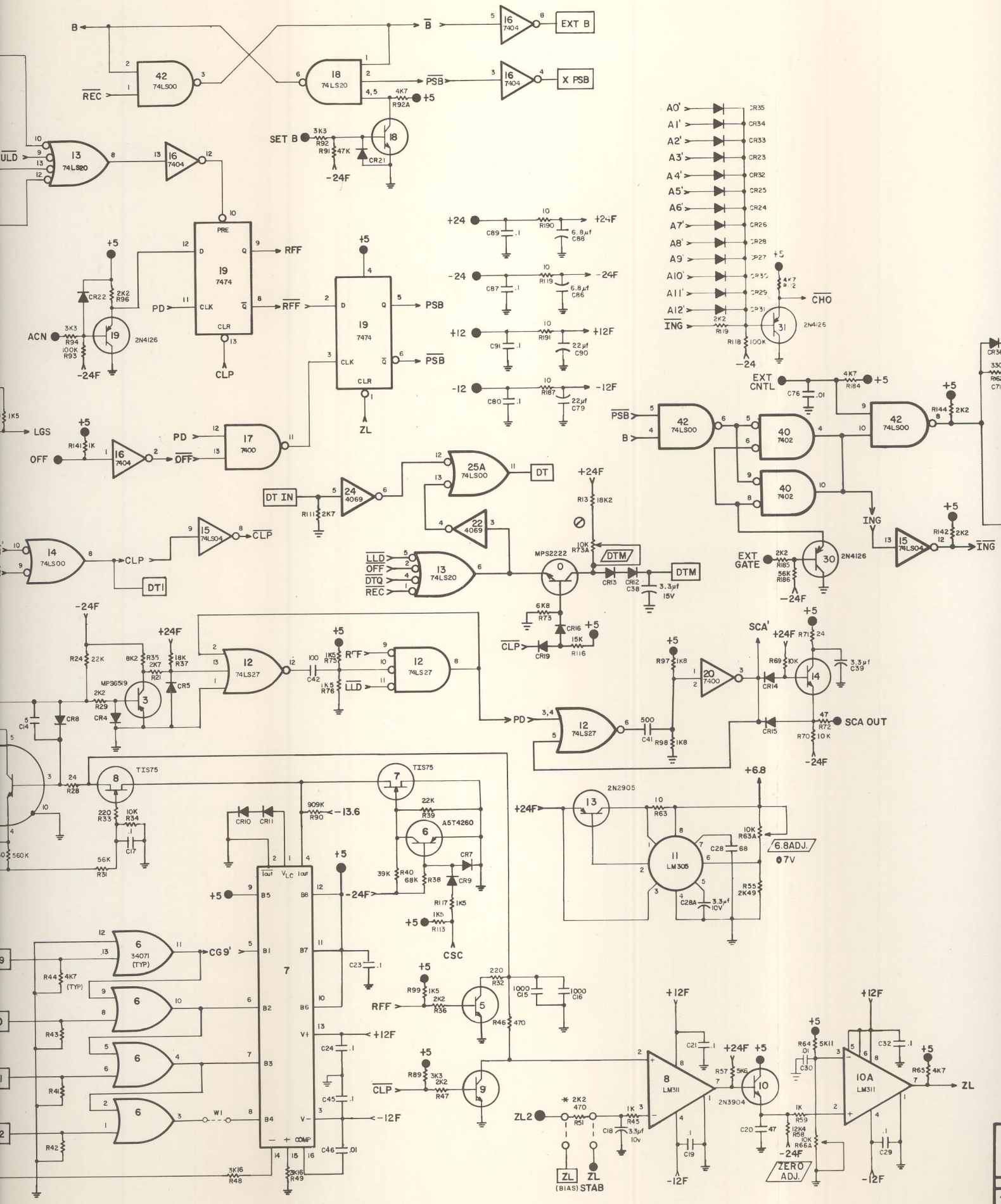
DATE	ENGINEER	DRAFT
4/25/77	J.A.H.	S.M

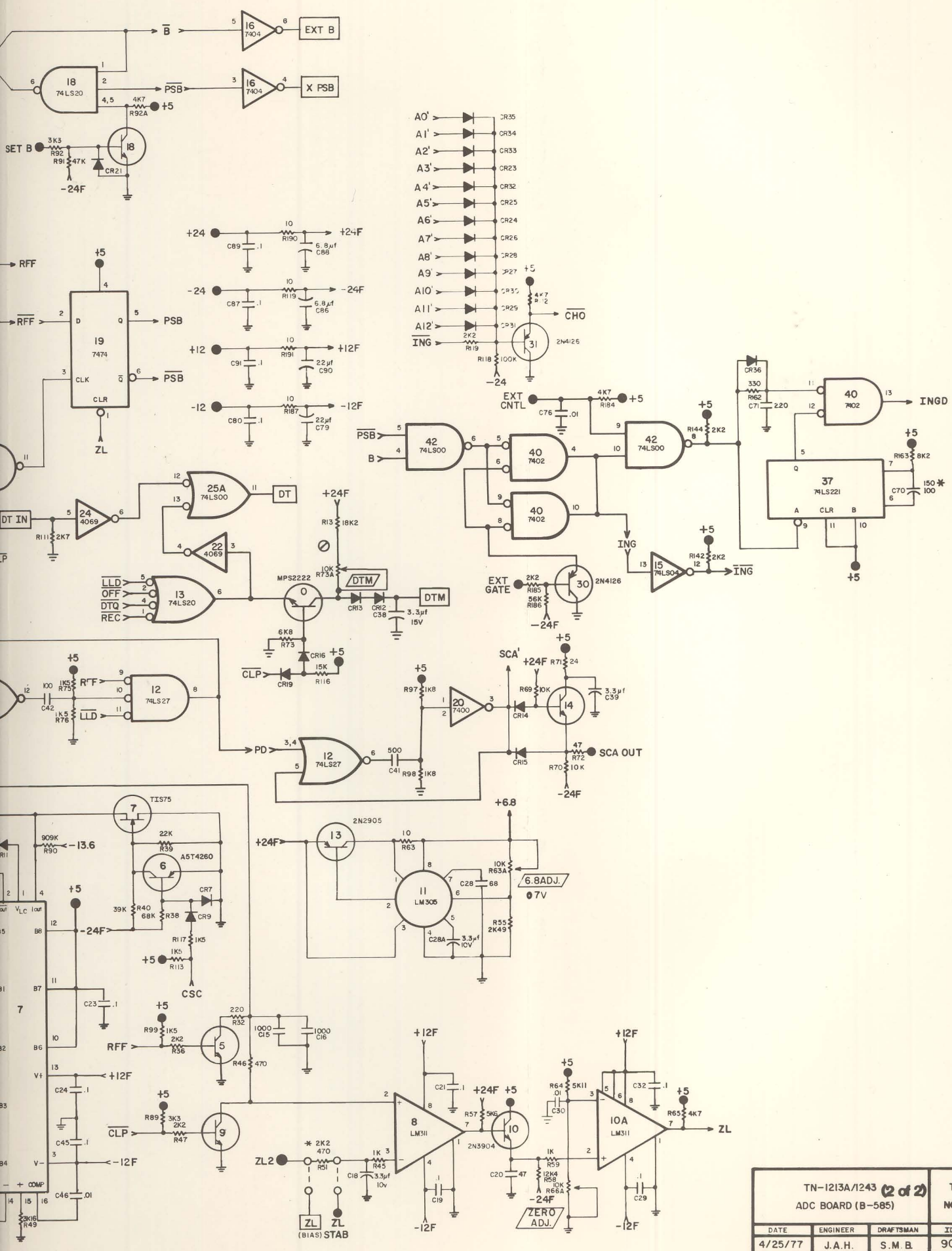


12/11/80
8/13/80
2/8/79
DATE

TN-1213A/1243 (1 of 2) ADC BOARD (B-585)			TRACOR NORTHERN
DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
4/25/77	J.A.H.	S.M.B.	900RS571


+12F
+24F
R16 270K
3
LM311
+5
R78 2K2
ULD
ULD2
1K
R8
C6 .1
C5 .1
-12F
+5
R79 4K7
EXT REJ
3K3
R80
R77 100K
CR17
15
-24F
B
42
74LS00
REC
SET E
REC'
CLP
14
74LS00
ULD
13
74LS20
16
7404
SCA'
OFF
20
74LS00
+12F
2
LM311
C10 .1
+5
R74 3K3
LLD
C43 500
LLD2
1K
R5
C4 .1
C3 .1
-12F
+5
PRE
19
7474
CLK
CLR
CR22
2K2
R96
PD
ACN
3K3
R94
100K
R95
19
2N4126
-24F
CLP
+5
R82 2K2
CR18
3K3
R84
CNC
16
2N4126
100K
R83
-24F
13
14
74LS00
R100 1K5
LGS
B'
+5
R141 1K
16
7404
OFF
OFF
PD
17
7400
DT IN
+12F
4
LM306
C11 .1
+5
R81 2K2
1K
R17
THS2
1K
R11
C8 .1
C7 .1
-12F
CR6
3K3
R37
C44 390
14
74LS00
15
74LS04
THR
B
15
74LS04
14
74LS00
CLP
15
74LS04
CLP
DTI
+24F
+6.8
R23 27K
CR3
4
MPS 6519
33µf
10v
C13
C9A
-24F
+24F
R24 22K
8K2
R35 2K7
18K
R37
R21
12
74LS27
MPS6519
3
2K2
R29
CR4
CR5
C14
CR8
1K5
R14
LGS
3K3
R18
1
+12F
C9 .1
+24F
INP
+5
R2 499
2K2
R3
R1 499
CR2
CR1
SEE NOTE 1
C2 10
1
LM310
140K R26
3K32
R15
2
RFF
2K7
R20
LGS
2K2
R19
C1 .1
-12F
5
CA3018
R27 560K
R25 22K
R30 560K
-24F
24
R28
8
TIS75
220
R33
10K
R34
.1
C17
56K
R31
CR10
CR11
+5
B5
B1
B2
B3
B4
40K2
R66
3.3µf
C37
+12F
NOMINAL
21K
+6.8
R67
TEST SELECT
10
LM301
C35 .1
470 *
W2
-13.6
-13.6S
R60 80K6
C37 .1
14K3
R68
C36 .1
30
C34
-24F
* FOR STABILIZER
60K4
R61
C22
+12F
330
R49A
C25 .1
9
LM301
33K2
R62
C27 .1
30
C26
-12F
CG9
CG10
CG11
CG12
6
34071
(TYP)
CG9'
R44 4K7
(TYP)
R43
R41
R42
W1
3K16
R48


B
REC
42 74LS00
18 74LS20
EXT B
X PSB
SET B
-24F
ULD
13 74LS20
16 7404
PRE
19 7474
CLR
CLP
RFF
PSB
ZL
ACN
2N4126
LGS
OFF
17 7400
PD
DT IN
24 4069
25A 74LS00
DT
22 4069
14 74LS00
15 74LS04
CLP
DTI
LLD
OFF
DTQ
REC
13 74LS20
MPS2222
DTM
CR13
CR12
3.3µf 15V
CR16
CR19
15K R116
6K8 R73
+24F
-24F
+5
MPS6519
CR4
CR5
CR8
12 74LS27
100 C42
1K5 R75
1K5 R76
RFF
LLD
PD
500 C41
1K8 R98
20 7400
CR14
CR15
SCA'
SCA OUT
R69 10K
R71 24
R72 10K
47
3.3µf C39
TIS75
220 R33
10K R34
.1 C17
56K R31
560K
R28
24
CR10
CR11
909K R90
-13.6
22K R39
A5T4260
CR7
CR9
39K R40
68K R38
1K5 R117
1K5 R113
CSC
CG9'
34071 (TYP)
R44 4K7 (TYP)
R43
R41
R42
W1
3K16 R48
3K16 R49
C23 .1
C24 .1
C45 .1
C46 .01
+12F
-12F
RFF
R93 1K5
2K2 R36
220 R32
1000 C15
1000 C16
R46 470
CLP
R89 3K3
2K2 R47
ZL2
2K2 470 R51
1K R45
C18 3.3µf 10v
ZL (BIAS)
ZL STAB
2N2905
10 R63
10K R63A
6.8ADJ.
7V
11 LM305
C28 68
C28A 3.3µf 10V
R55 2K49
+6.8
8 LM311
10 2N3904
R57 5K6
C21 .1
C19 .1
C20 47
10A LM311
R64 5K11
.01 C30
C32 .1
C29 .1
R65 4K7
R59 1K
R58 12K4
R66A 10K
ZERO ADJ.
A0'
A1'
A2'
A3'
A4'
A5'
A6'
A7'
A8'
A9'
A10'
A11'
A12'
ING
CHO
CR35
CR34
CR33
CR23
CR32
CR25
CR24
CR26
CR28
CR27
CR30
CR29
CR31
4K7 R192
2K2 R119
100K R118
31 2N4126
+24
-24
+12
-12
R190
R119
R191
R187
6.8µf C86
22µf C90
22µf C79
C89 .1
C87 .1
C91 .1
C80 .1
EXT CNTL
4K7 R184
C76 .01
EXT GATE
2K2 R185
56K R186
30 2N4126
42 74LS00
40 7402
R144 2K2
R142 2K2
CR36
330 R162
C71 220
DATE
4/25/7



TN-1213A/1243 (2 of 2) ADC BOARD (B-585)			TRACOR NORTHERN
DATE	ENGINEER	DRAFTSMAN	IDENT. NO.
4/25/77	J.A.H.	S.M.B.	900RS571

Tracor Northern

2551 West Beltline Highway • Middleton, Wisconsin 53562 • (608) 831-6511 • TWX-910-280-2521