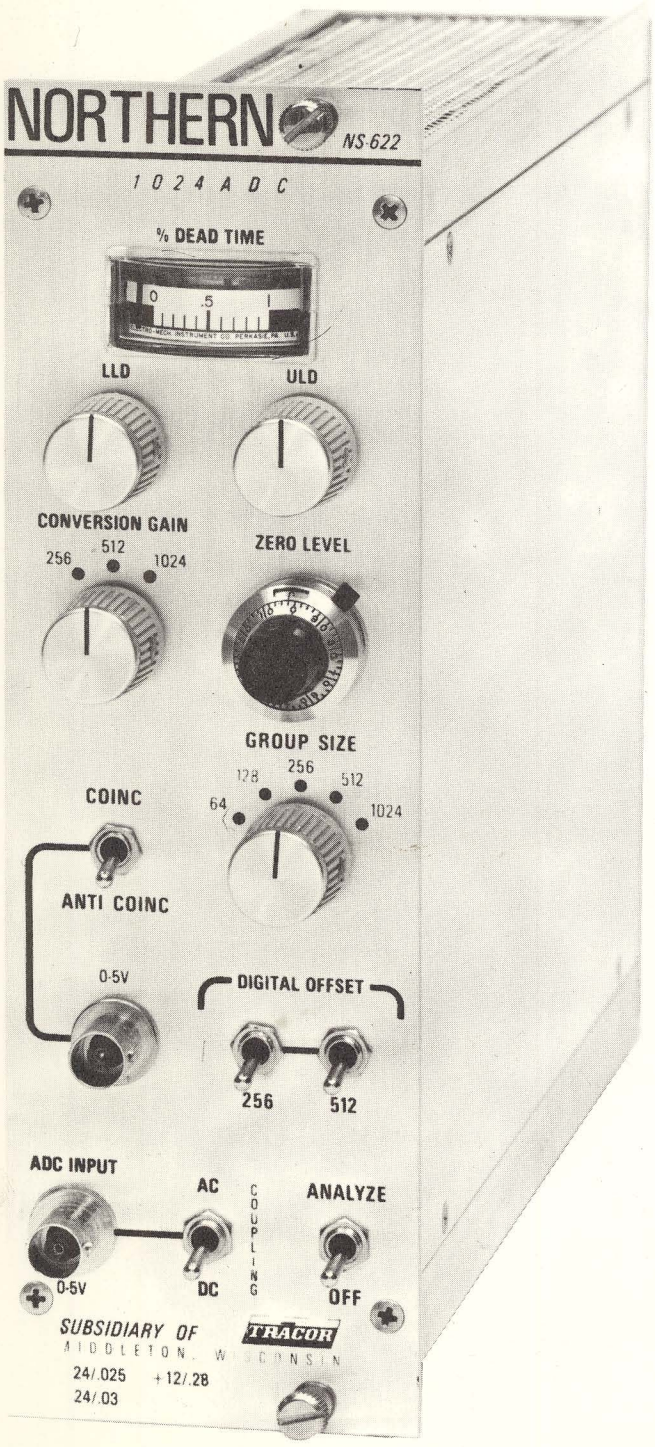
NS-622
ANALOG TO DIGITAL CONVERTER (ADC)
AND
ADC SECTION OF NS-633
PULSE HEIGHT ANALYZER

INSTRUCTION MANUAL

NORTHERN SCIENTIFIC, INC.
2551 WEST BELTLINE, P. O. BOX 66
MIDDLETON, WISCONSIN 53562
Phone (608) 836-6511
A SUBSIDIARY OF TRACOR


NORTHERN
NS·622
1024 ADC
% DEAD TIME
0
.5
1
LLD
ULD
CONVERSION GAIN
256
512
1024
ZERO LEVEL
GROUP SIZE
128
256
512
64
1024
COINC
ANTI COINC
0-5V
DIGITAL OFFSET
256
512
ADC INPUT
AC
COUPLING
DC
0-5V
ANALYZE
OFF
SUBSIDIARY OF
TRACOR
24/.025
+12/.28
24/.03

CONTENTS

I. INTRODUCTION

This manual covers the NS-622 Analog-to-Digital Converter (ADC) and the ADC section of the NS-633 Pulse Height Analyzer. Both units use the same printed-circuit board and nearly identical circuitry in the ADC's. In general this manual will not differentiate between units unless circuit differences exist. The design of the NS-633 is such that the ADC and memory are almost completely independent units. A second manual covers the memory/control section of the NS-633, and also contains operating instructions for pulse height analysis.

Except for address scaler size this ADC uses the same system design as larger, more sophisticated units manufactured by Northern Scientific. Rear panel connectors, logic levels, and pin assignments are the same as other NSI ADC's so that units are completely interchangeable.

The converter is of the familiar Wilkinson type with peak detection used to start the conversion process. Digitizing is performed at 50 MHz into a 10-bit scaler for resolution up to 1024 channels. Integrated circuits are used extensively to improve stability and reliability. Operation from the standard NIM supply voltages is accomplished by using internal regulators to drop the NIM voltages to proper levels for the DTL and TTL integrated circuits used.

II. GENERAL SYSTEM DESCRIPTION

Figure 1 is a block diagram of a typical acquisition system employing this ADC. Figure 2 is a timing diagram showing the relative time scale for the major signals involved in the analysis of an analog input.

Incident radiation at the detector is converted to an electrical signal which is amplified and shaped by the amplifier. The output of the amplifier connects to the ADC input where it triggers the ADC and starts conversion of the analog input into a digital address. Once the ADC has accepted a signal for conversion it is insensitive to other inputs until it has been cleared (reset).

Briefly, conversion of the analog input is accomplished in the following manner. The positive input pulse from the amplifier is applied to a stretcher circuit which charges a capacitor to the peak amplitude of the input signal. When the capacitor is fully charged a linear gate at the ADC input is closed, blocking ADC response to any other input. At the same time a gate is opened which allows 50 MHz clock pulses to start advancing a 10-bit scaler. Also at this time logic circuits turn on a current source which linearly discharges the stretcher capacitor back to zero. When the capacitor reaches zero the 50 MHz gate is closed and the 10-bit scaler contains a binary number whose magnitude is directly proportional to the amplitude of the analog input pulse. The binary number (address) is then presented to the memory unit for data storage. When storage is complete the memory unit sends a clear signal to the ADC. The clear signal resets the ADC, opens its linear gate; and the ADC is available to convert another input.

The complete connection between ADC and memory unit consists of three signals in addition to the 10-bit address. Signal STORE is generated approximately 1 usec after the ADC conversion is complete. The address is presented to the memory until 1 usec before STORE but presentation of an address does not always mean it will be followed by a STORE. During the 1 usec, acceptance tests are performed on the address and only if these tests are passed will a STORE follow 1 usec later. The tests performed are: address underflow (address less than zero when using digital zero offset), channel zero test (channel zero is reserved for live time and data

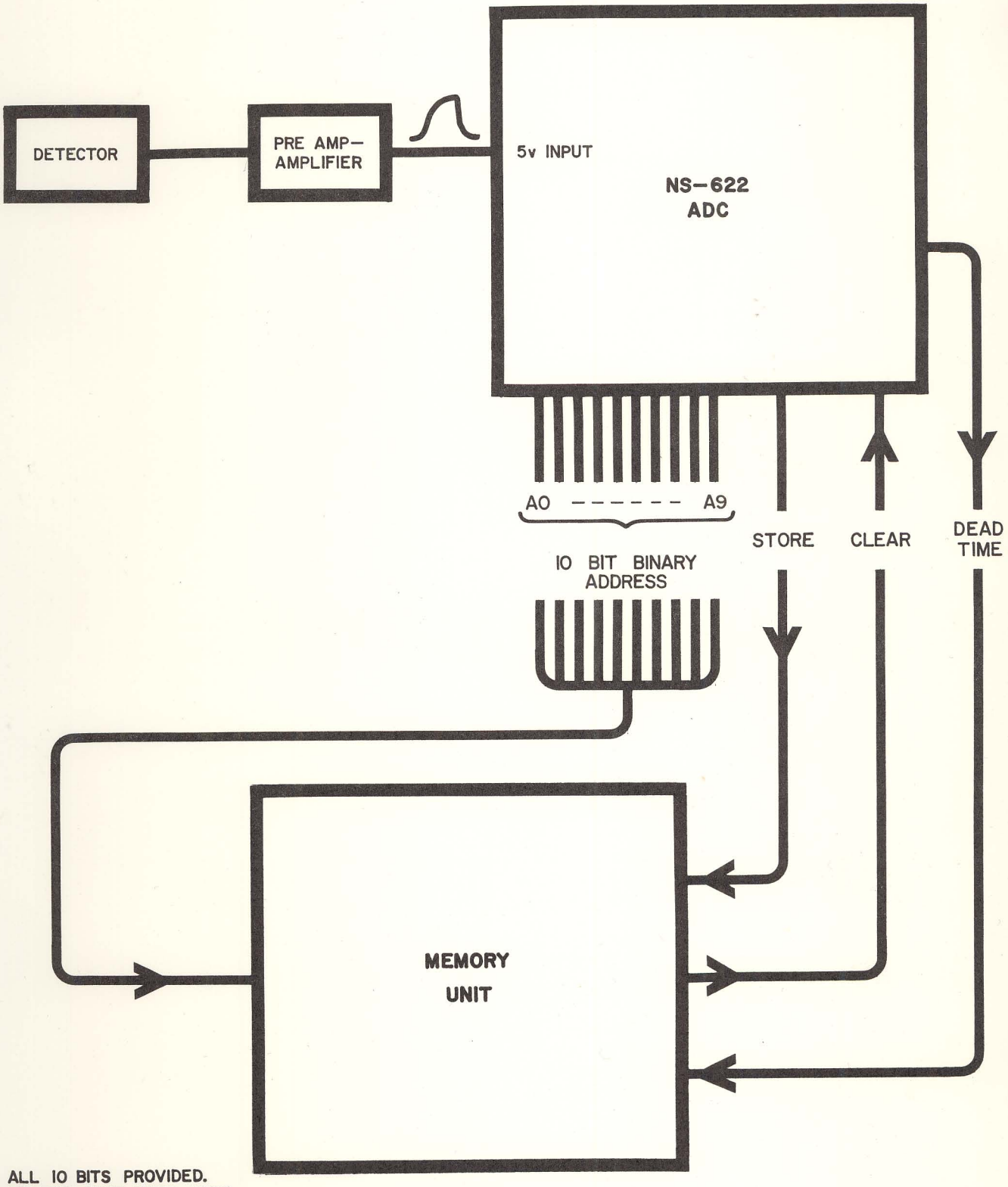
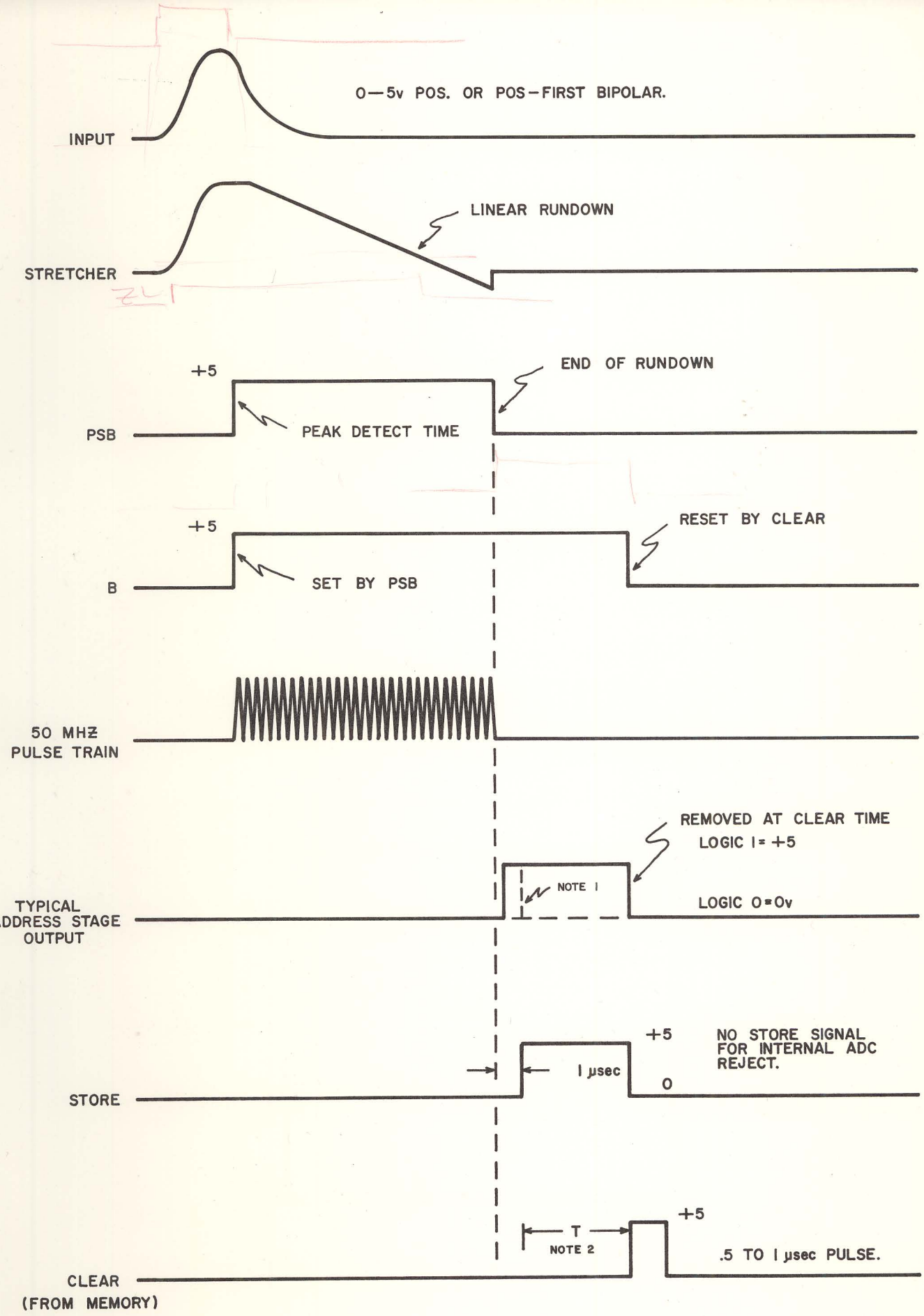


FIG. 1
BLOCK DIAGRAM OF SIMPLIFIED SYSTEM



NOTE 1

ADDRESS OUTPUT RETURNS TO 0V IN 1 μsec UNDER INTERNAL REJECT CONDITIONS.

FIG. 2
ADC TIMING

NOTE 2

TIME T IS DETERMINED BY MEMORY UNIT. ADDRESS AND STORE REMAIN UNTIL CLEAR IS SENT.

must not be stored there), and address overflow (address greater than memory size available). In the event the address as generated fails any one of the three tests it will not be stored and the ADC will automatically be reset by internal circuitry.

When the address passes the acceptance tests it is followed by a STORE command. The memory unit is designed to respond to this signal and transfer the address to its input register. At the end of data-transfer the memory unit sends a CLEAR to the ADC. This resets the ADC and allows it to accept another pulse for conversion. Both the address and STORE are dc signals and will remain indefinitely until a CLEAR is received. This arrangement greatly simplifies connection to any memory unit with no restrictions on transfer time. The acceptance tests performed on the address with automatic ADC reset under reject conditions also reduce the number of signals required to complete connection.

The third signal sent to the memory unit is signal DT. The one state of this signal starts with triggering of the ADC by an analog input and ends 3 usec after the ADC is reset, either internally by address reject, or by a CLEAR from the memory unit. DT represents the complete dead time for the ADC, the time it is not available to accept an input for conversion. This signal can be used by the memory unit for live timer operation. In the NS-633 signal DT is used on the ADC board to gate a clock which comes from the memory section. For live time operation the ADC and memory unit are both used to store live time counts. This is covered in detail in the section on Circuit and System Design.

III. OPERATING CONTROLS AND SPECIFICATIONS

A. INPUTS

1. ADC Analog Input

a. Range: 0-5V. Full scale with respect to the conversion gain is 4V. The additional 25% over range can be utilized by offsetting the zero intercept by 25%.

b. Polarity: Positive unipolar or positive-first bipolar.

c. Rise Time: .1 to 5 usec.

d. Fall Time: .1 to 10 usec; up to 30 usec is permissible but the linearity of the lower 5% of the range will be degraded.

e. Input Impedance: 10K ohm.

f. Coupling: Switch selected, ac (capacitive) or dc (direct).

2. COINC Input

a. Positive 5V signal performs either coincidence or anti coincidence function depending on position of COINC-ANTI COINC switch.

b. Input Impedance: 3.3K ohm, dc connected.

c. Refer to section on Operation for timing requirements.

B. DISCRIMINATORS

1. LOWER LEVEL

a. Function: Sets lower limit on signals to be converted by ADC. Signals below the lower level add no dead time to system operation.

b. Range: 0-100% of the full-scale conversion as set by the CONVERSION GAIN switch.

c. Coupling: dc to ADC input (ADC in turn may be either ac or dc coupled depending on position of COUPLING switch).

d. Stability: Maximum 200 ppm/^{o}C or 24 hrs at constant temperature, typically 50 ppm.

2. UPPER LEVEL

a. Function: Sets upper limit on signals to be converted by ADC. Dead time for signals above the upper limit is equal

to signal time above the lower level threshold.

b. Range: 5 to 125% of full-scale conversion.

c. Coupling: Same as lower level discriminator.

d. Stability: Max 200 ppm/^{o}C or 24 hrs, typically 50 ppm.

C. ZERO LEVEL CONTROLS

1. Analog ZERO LEVEL

a. Function: Adjusts the level of the analog input which corresponds to channel 0 (extrapolated).

b. Range: -0.5 to 10%. Range refers to extrapolated zero intercept of a plot of channel number versus analog input amplitude.

c. Stability: 100 ppm/^{o}C max, 50 ppm/^{o}C typical; 200 ppm/24 hrs at constant temperature; referred to full scale analog input.

2. DIGITAL ZERO OFFSET

a. Function: Digitally subtracts selected offset from converted address.

b. Positions: 0, 256, 512, 768 channels.

c. ADC Dead Time: Independent of digital offset for a given analog input.

d. Remarks: Underflow conversions (addresses less than 0 after offset subtraction) are rejected within the ADC; no STORE is generated and ADC is internally reset.

D. CONVERSION GAIN

1. SWITCH

a. Function: Sets the number of channels corresponding to full scale analog input of 4V. Switch selects magnitude of current effecting linear rundown of stretcher capacitor.

b. Positions: 256, 512, 1024 channels per 4V input.

c. Stability: 200 ppm/^{o}C max, 50 ppm/^{o}C typical; 200 ppm/24 hrs at constant temperature, referred to full scale analog input.

E. GROUP SIZE Switch (NS-622 only)

1. Function: Digitally sets upper limit on channel number to be stored in memory unit. Addresses greater than selected number are automatically rejected within the ADC.
2. Range: 32 to 1024 channels in binary increments.
3. Remarks: Reject occurs when group size overflow is sensed after conversion. When digital offset is used, overflow is sensed on group size above channel zero. Group size in NS-633 is wired to be a fixed 256 channels.

F. ANALYZE OFF Switch (NS-622 only)

1. ANALYZE Position: Normal operating position.
2. OFF Position: ADC is in dc reset condition.

G. POWER REQUIREMENTS (NS-622 only)

1. +24 : 25 mA.
2. -24 : 30 mA.
3. +12 : 280 mA.
4. -12 : none.

H. REAR PANEL CONNECTORS/SIGNALS (NS-622 only)

NS-630 Memory Unit

a. Size: 26 pin Amp.
b. Signals: Address, STORE, CLEAR, DT, plus several control input/outputs.
c. Levels: Logic one = +5V, Logic zero = 0V, DTL/TTL compatible.

IV. OPERATION

A. General

This section covers operation of the NS-622 ADC and the NS-630 Memory Unit in pulse height analysis. Operation of the combined units is not unlike the conventional pulse height analyzer found in a single package. The discussion here will pertain to the ADC connected to the Northern Scientific NS-630 Memory Unit but the front-panel adjustments of the ADC are essentially the same when operating it in the NS-633 Pulse Height Analyzer.

B. Initial Set Up and Operation With The NS-630 Memory Unit

Listed below are the switch positions and signal requirements which will ensure proper operation of the ADC and the NS-630 Memory Unit. It is assumed that the NS-630 Memory Unit has been adjusted for pulse height analysis mode of operation. If there is any question about proper switch positions for this mode, refer to the NS-630 manual. This set up is for simple, straightforward nuclear pulse height analysis and does not utilize the full capabilities of the system. Sections which follow cover the controls individually so that maximum acquisition efficiency can be achieved under more complex modes of operation.

1. Turn off the power on all units.
2. Connect the ADC to the memory unit using the cable supplied.
3. Connect the signal source to the ADC BNC input labeled ADC INPUT. Signal must be positive unipolar or positive first bipolar. Set the coupling switch on the ADC front panel to ac.
4. Set COINC/ANTI COINC switch to ANTI COINC.
5. Set ULD full clockwise.
6. Set LLD one quarter turn from full CCW position.
7. Set ZERO LEVEL at 100 small dial divisions.
8. Set CONVERSION GAIN to the switch position which corresponds to the memory unit size available.
9. Set the GROUP SIZE switch to the same position as the CONVERSION GAIN switch.

10. Place all DIGITAL OFFSET switches in the OFF position.
11. Now energize the NS-630 Memory Unit and the power supply in the NIM bin.
12. Place the ANALYZE OFF switch on the ADC to the ANALYZE position.
13. Control system with the START MEASURE and STOP pushbuttons on the NS-630. The above procedure sets up the ADC for analysis of the entire range from threshold to full scale. The ZERO LEVEL is set near 0-0 intercept and the lower level discriminator is set for approximately maximum sensitivity. Either the ADC ANALYZE OFF switch or the memory START MEASURE and STOP pushbuttons can be used to control analysis. The controls on the memory unit are preferred, however, because they also control operation of the clock/live timer in the memory unit. Accurate live time can be realized only when the memory unit pushbuttons are used to control analysis.

C. Lower and Upper Level Discriminators

The lower and upper level discriminators are connected directly to the ADC input and are used to bracket the range of analog signals to be converted by the ADC. Internally both discriminators are directly coupled to the ADC input. Also, the range of the lower level discriminator extends below zero so that the full CCW position of the front panel control will cause the discriminator to be triggered 100% of the time. This is indicated by 100% deflection on the dead time meter with no input signal. This is an improper operating point for the ADC, but this point was designed to accommodate small dc offsets of the input signal baseline when external restorers and dc input connection are used. The lower level discriminator is set for maximum sensitivity at the point where the dead time meter just drops from 100% back to zero with no input signal. Operation at maximum sensitivity should be avoided, however, because any small drift in the system may cause the lower level discriminator to trigger 100% of the time. The maximum sensitivity point should be found experimentally and then the

control should be adjusted to be positioned one-eighth turn above this point.

The upper level discriminator inhibits conversion of any signals above the upper level threshold. ADC dead time can be reduced considerably by adjusting the upper level threshold to be just above the maximum signal of interest. At low count rates this adjustment is not important but at high count rates considerable system dead time can be eliminated by proper setting of this control.

The upper and lower level discriminators should be adjusted to bracket a region of interest when using digital zero offset. With the discriminator set to convert the entire full scale spectrum considerable dead time is used in converting signals which are later rejected by underflow and overflow tests performed after conversion. After the region of interest is once selected with the DIGITAL OFFSET and GROUP SIZE controls, the upper and lower level thresholds should be adjusted to fall just outside the region of interest which has been bracketed digitally. Operation in this manner provides double selection of the region of interest. The discriminators provide analog selection and reduce ADC dead time while the GROUP SIZE/DIGITAL OFFSET controls provide for logic functions which precisely select the region to be stored in the memory unit.

D. Zero Level Adjustment

Zero level is defined as that analog input level which corresponds to channel zero (extrapolated) in the stored analysis. Using the front panel ZERO LEVEL Helipot any analog input from zero through .4 volts can be adjusted to correspond to channel zero in the memory unit. The ZERO LEVEL control is analogous to the bias level on a biased amplifier; signals below the zero level are not converted by the ADC just as signals below bias level are not amplified. As the ZERO LEVEL control is turned clockwise the channel number for a given energy is reduced. This has the effect of shifting the entire spectrum to lower channels when viewed from channel zero through full scale. From the standpoint of the spectrum stored in the memory unit there is no difference in the results obtained using the analog ZERO LEVEL control or the DIGITAL OFFSET switches. The main difference

in the two, however, is that the analog zero level control does reduce the amount of dead time required for a given conversion. The digital offset switches operate on the address after conversion. That is, for a given energy, the conversion time is independent of the digital offset switch positions. Using analog offset, however, the dead time is inversely proportional to the magnitude of offset. From a dead time standpoint only, analog adjustment is preferred over digital offset of zero level. However, digital offset does provide a convenient means of shifting the spectrum some fraction of the full scale conversion gain since offset, conversion gain, and memory group sizes are all in binary increments. The speed of the NS-622 is such that conversion times are low even with digital offset. For medium count rates the increased dead time is not significant, especially if the lower and upper level discriminators are adjusted properly to bracket the region-of-interest selected.

One final word on the analog zero level control at this time is in order. While the analog zero level control performs the same function as the bias level on a biased amplifier, the disadvantages associated with biased amplifiers are not found in the ADC. It is normal for a biased amplifier to bias off the lower portion of the input signal with a resultant change in pulse shape for signals above the bias level. The NS-622 ADC, however, employs a different design technique whereby the signal as seen by the pulse stretcher is independent of the ZERO LEVEL control setting. The significant advantages of this technique are that the ADC linearity is independent of zero level adjustment, and also the ADC stability is not dependent on zero level setting. See the next section on System and Circuit Design for details on how this is accomplished.

E. Conversion Gain

Front panel switch positions on the CONVERSION GAIN switch indicate the address generated for a 4 volt analog input signal. This switch then effectively adjusts the resolution of the ADC since the number of discrete channels for a given analog input is a function of this switch position. Internally this switch adjusts the magnitude of the rundown current which effects linear discharge of the stretcher capacitor. If the entire energy

range from zero to full scale is to be analyzed, the CONVERSION GAIN switch is set to the number which corresponds to the size of the available memory. The ADC may be operated at higher resolution settings than this but only by viewing a smaller portion of the entire spectrum. For example, if a 256 channel memory is the size in use then in order to view the entire voltage range from zero to 4 volts the CONVERSION GAIN must be operated at the 256 position. The CONVERSION GAIN may be operated at a setting of 1024 however if only one-fourth of the spectrum is to be stored. The CONVERSION GAIN switch is adjusted first for the resolution desired; then either the ZERO LEVEL control or DIGITAL OFFSET is used to shift the region of interest into channels 0 through 255. CONVERSION GAIN should be adjusted to provide the resolution desired over the dynamic range required by the region of interest.

F. GROUP SIZE Switch (NS-622 only)

The GROUP SIZE switch is essentially a digital upper level discriminator adjustment and sets the maximum address which will be stored in the memory unit. This is accomplished by testing each conversion for an address greater than the number selected on the front panel GROUP SIZE switch. Addresses above the number selected cause STORE to be inhibited and the ADC to be reset internally. The overflow tests are performed after conversion so that digital offset is subtracted before the tests are performed. This means that the group size as selected refers to the number of channels above zero. Conversions below channel zero are also rejected when underflow is sensed in the ADC.

In normal single parameter analysis the GROUP SIZE switch position corresponds to the memory size available. If the NS-630 is being used at something less than full memory (quarters, halves), the switch position should still correspond to the size of the memory being used. Switch positions corresponding to very small group sizes, 64 channels for example, is provided for two parameter analysis in a 64 x 64 configuration of two ADC's. Where only 64 channels along one axis are being used, digital offset will most probably be employed. The DIGITAL OFFSET and GROUP SIZE

switches provide for selecting a 64 channel region of interest with the ADC operating at much higher resolution.

G. Coincidence, Anti-Coincidence Operation

A front panel BNC is provided on the ADC for acceptance of a 0-5V signal for coincidence or anti-coincidence operation of the ADC. A toggle switch next to the BNC controls the operating mode. Connection is direct so that this input may be used as an auxiliary start-stop control of the ADC using a logic signal. Circuitry is such that this input can also be used for time coincidence or anti-coincidence operation of the ADC.

Requirements for pulse coincidence operation are as follows. With the toggle switch in the COINC position the ADC is inhibited from accepting any analog input for conversion. This is accomplished by holding a linear gate at the stretcher input closed. Analog input signals accompanied by a positive 5 volt pulse will be accepted by the ADC for conversion. All other logic functions, both analog and digital in nature, will still apply to the subsequent conversion. The lower and upper level discriminators, zero level control, digital offset and group size functions operate in normal fashion so that acceptance of a signal by the ADC does not necessarily mean it will be stored. Timing requirements for the application of the 5 volt coincidence signal are fairly straightforward and non critical. Pulse rise time for the coincidence input should be somewhere in the range between 50 and 250 nanoseconds. The coincidence pulse must arrive at the input no later than one-half microsecond before the analog input signal reaches its peak amplitude. There is no delay line in the ADC so that an external delay line may be necessary to allow time for the external coincidence circuitry to make its decision. Application of the coincidence input opens the ADC linear gate and the signal passes through the open gate and connects to the stretcher circuitry. When the signal reaches peak amplitude the peak detector is triggered. At peak detect time the linear gate is closed even if the coincidence input remains.

The duration of the coincidence input must be long enough to hold the linear gate open until it is closed by the ADC at peak detect time. The

suggested pulse duration is one-half microsecond greater than baseline-to-peak time of the analog input signal.

During the conversion process the ADC busy signal keeps the linear gate closed and additional coincidence inputs have no affect on the conversion. Once the ADC is reset, either by internal reject of a conversion or at the time a CLEAR signal is received from the memory unit, the coincidence input is again operative.

Pulse requirements for anti-coincidence operation of the ADC are less stringent than for the coincidence mode. To inhibit an analog input, the anti-coincidence input must be +5V at peak detect time and for approximately 400 nanoseconds thereafter. Pulse durations longer than the 400 nanosecond minimum, or pulses applied before peak detect time have no detrimental affect on operation. Pulses approximately two microsecond duration applied at the same time the analog signal is applied are suggested when analyzing one to two microsecond input pulses. The dead time for an analog input which is inhibited is equal to the input's time above the lower level discriminator threshold. The COINC input can be used as an auxiliary analyze-stop control for the ADC. The anti-coincidence input signal is not included in ADC dead time however, so that accurate live time operation cannot be realized if this mode of operation is used to control analysis.

H. Analyzing dc or Slow ac Signals

Either dc or slow ac signals can be analyzed with the NS-622 ADC by sampling at the ADC input. The following front panel switch positions should be used for operating in this mode. Place the COUPLING switch to the dc position, and the COINC/ANTI COINC switch to the COINC position. A positive 5 volt pulse source is required to strobe the ADC input. The pulse duration should be a minimum of one microsecond and a maximum of 4 microseconds. Operation is as follows. With the COINC/ANTI COINC switch in the COINC position the linear gate of the ADC is held closed. The dc applied at the front panel is connected to the linear gate but is blocked. Application of the 5 volt, one microsecond pulse at the coincidence input opens the linear gate for one microsecond. This effectively generates a

one microsecond pulse at the linear gate with a peak amplitude equal to the dc input. The ADC converts the one microsecond pulse in identical fashion to normal pulse inputs. All front panel controls, both analog and digital, are operative in this mode.

For analysis of slow ac signals the ADC front panel controls are set up the same as for dc signals. The ADC operated in this mode will convert only the positive portion of the ac input. Internal circuitry clips the negative portion of bipolar inputs and coincidence pulses applied will not produce conversions. If analysis of the entire signal is required, the ac signal must be superimposed on a dc pedestal such that the input to the NS-622 is always positive with respect to ground. As with dc inputs, all front panel controls remain operative so that the discriminators, zero level and region of interest selection controls can be used to bracket a region of interest. Once the ADC has accepted an input for analysis, the busy signal holds the linear gate closed until the ADC is ready to accept another pulse. Application of additional coincident inputs will not affect the conversion of the accepted input.

V. SYSTEM AND CIRCUIT DESIGN

A. General

This section provides detailed coverage of the ADC logic circuits, signal timing and circuit design. Block diagrams and timing diagrams are provided to facilitate explanation of the basic operation. Transistor and integrated circuit numbers are used on the block diagram to simplify cross referencing the logic blocks and circuits. The schematic is accompanied by a physical layout which shows the location of the transistors and integrated circuits with their numbers. Major signals as they appear on the schematic and block diagrams are also labeled on the printed circuit boards to aid signal tracing. A section just prior to the schematics contains general notes which explain the symbols used on our schematics and block diagrams. A few minutes spent studying this section will greatly simplify understanding the various signal sources and loads throughout the ADC. A list of major signals and their functions is included to cover the signals which may be omitted in the text. Although brief, this list does explain the function of all major signals found in the ADC.

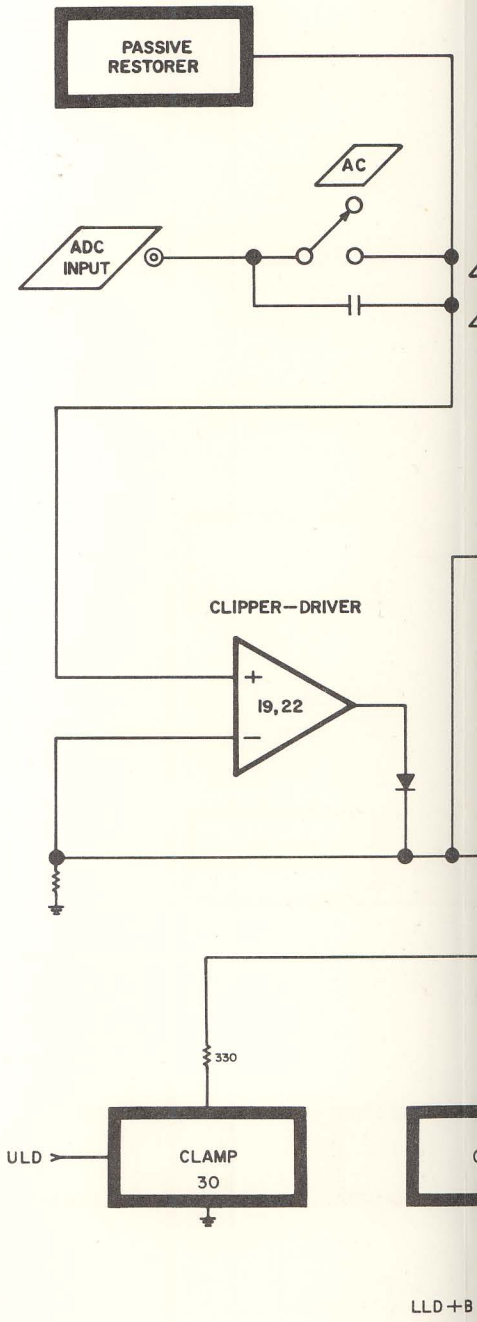
In the discussion of the system and circuit design which follows no attempt was made to discuss the block diagrams and schematic separately. Rather, the block diagrams and systems are discussed in detail and reference is made to individual circuits only where their complexity warrants further discussion. The system is separated into two sections to simplify explanation. The first section will deal with the basic component parts of the ADC. The second section will deal primarily with logic functions which occur after the conversion process and involve the store and reset circuitry of the ADC.

B. The Basic ADC Circuitry

1. ADC Input Circuits

Refer to the block diagram, Figure 3, for the circuits covered in this section. Figure 4 is a timing diagram of the analog and logic signals for the basic ADC.

The ADC INPUT BNC connects to the COUPLING switch and then to


PASSIVE
RESTORER
AC
ADC
INPUT
CLIPPER—DRIVER
+
19,22
−
330
ULD
CLAMP
30
LLD+B

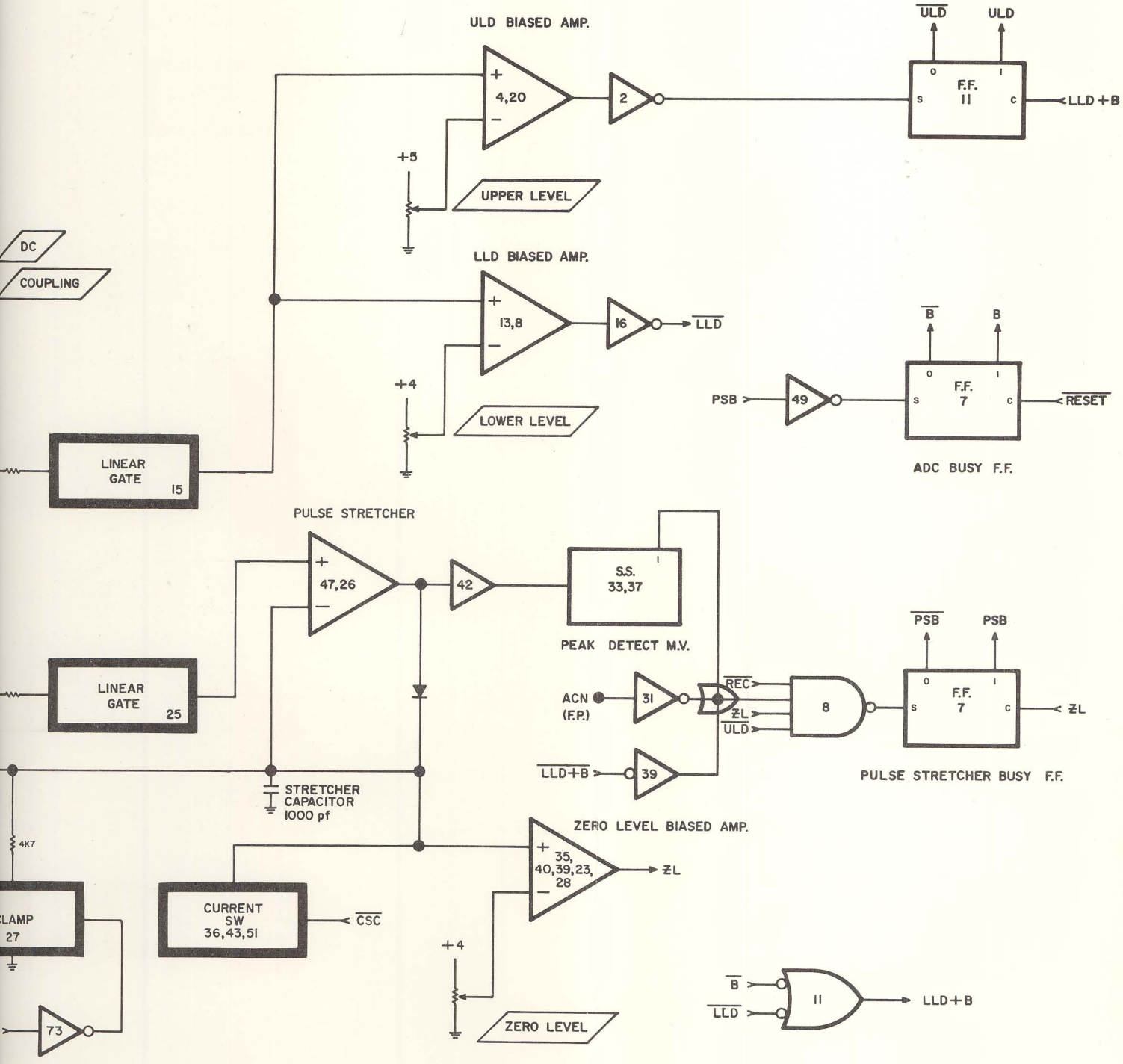


FIG. 3
BLOCK DIAGRAM OF ANALOG CIRCUITS AND STRETCHER LOGIC CIRCUITS.

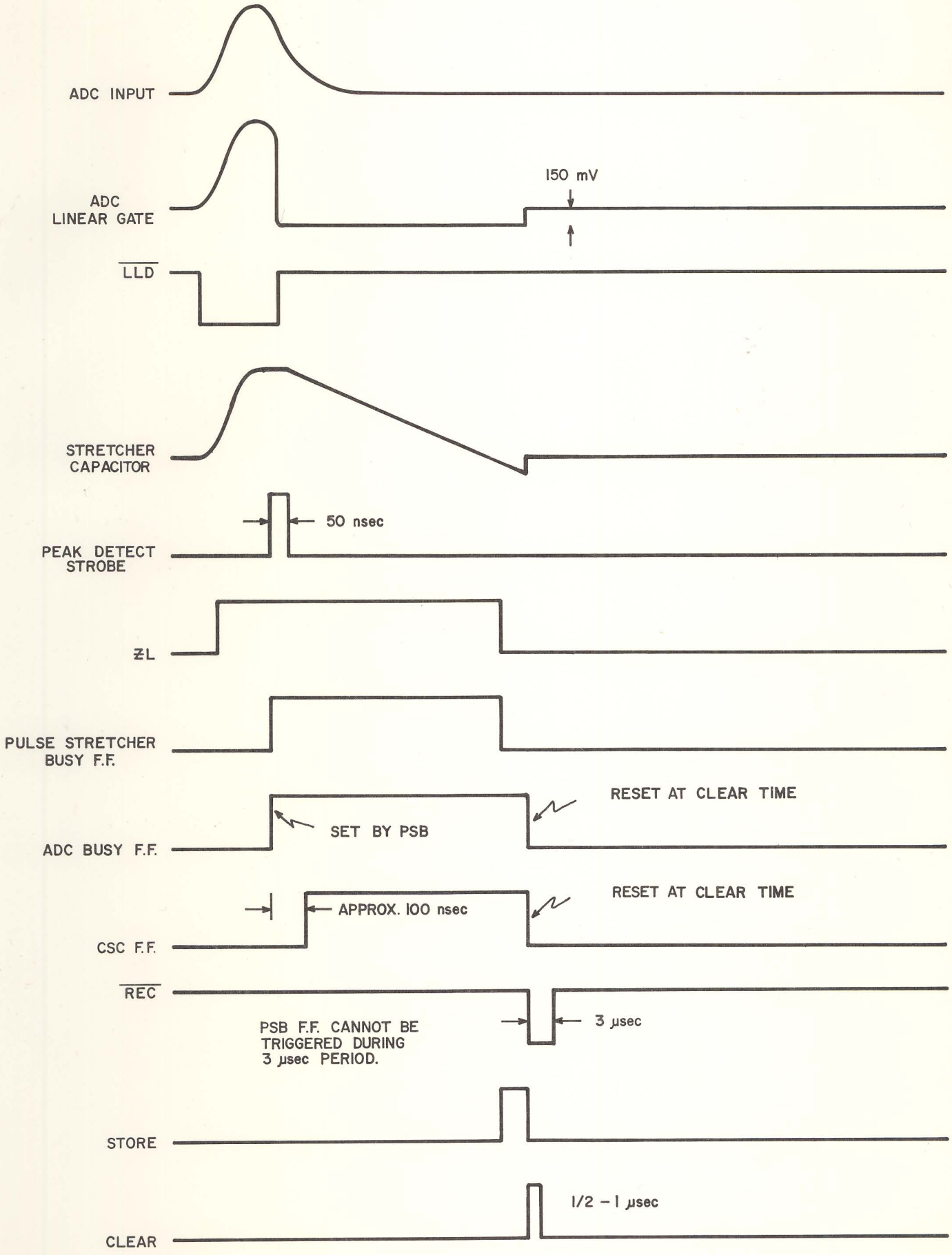


FIG. 4
TIMING FOR A BOARD SIGNALS
WITH RESPECT TO STORE-CLEAR

the input circuitry on the printed circuit board. The COUPLING switch provides for switching from capacitive coupling to direct coupling. The capacitor value as provided is a compromise between a value which produces minimum signal differentiation, and the value which provides shortest recovery time of the baseline. The .012 uf value is near optimum for pulse inputs in the 1-2 usec range. If longer pulses at low count rate are being analyzed ADC performance may be improved by increasing the capacitor size. The best value for a given count rate/pulse shape will have to be determined experimentally using system resolution and/or count rate shift as a guide for the optimum value.

An operational amplifier composed of transistors Q19 and Q22 form the input circuitry to the ADC. This amplifier is operated as a gain-of-one voltage follower with the loop closed by a diode from the collector of transistor Q22 to pin 3 of Q19. Closing the loop with a diode provides low output impedance for positive signals only. Negative signals are clipped at approximately -.7 volts at pin 3 of transistor Q19. The output of this loop connects to both the stretcher/peak-detector circuitry and to the lower and upper level discriminators. Each signal path is equipped with a linear gate, transistor Q15 for the discriminators and transistor Q25 for the ADC's stretcher.

2. Stretcher/Peak Detector Circuitry

Another operational amplifier composed of transistor Q26 and Q47 form the pulse stretcher for the ADC. The amplifier is operated as a gain-of-one voltage follower with the circuit modified to perform pulse stretching. The incoming positive pulse is applied to pin 9 of transistor Q26. The amplifier loop is closed by means of a diode from the collector of Q47 to the inverting input of the amplifier at pin 3 of Q26. The stretcher capacitor is also located at pin 3. As the input signal goes positive the diode conducts and pin 3 follows the input signal up to peak amplitude. As the signal passes through peak amplitude pin 3 remains at peak voltage due to the stretcher capacitor. The loop now opens because of the

polarity reversal at the diode closing the loop. The collector of Q47 swings negative with respect to ground and turns on transistor Q42 which amplifies the negative signal. The amplified signal at the collector of Q42 is used to trigger the peak-detect monostable composed of transistors Q33 and Q37. The multivibrator output at the collector of Q33 is used as a peak-detect strobe which connects to pin 13 of IC8, a four-input NAND gate. The collector of Q37 is also parallel connected to transistors Q31 and Q32. Assume for the moment that Q31 and Q32 are turned off and pins 9, 10 and 12 on IC8 are positive. Under these conditions a positive 50 nanosecond pulse will be generated at Q33 collector at peak-detect time. Pin 8 of IC8 will switch negative for 50 nanoseconds and set the pulse stretcher busy flip-flop composed of two two-input NAND gates found in IC7. Signals $\overline{\text{PSB}}$ and PSB, the outputs of the flip-flop are used to trigger logic circuits which effect a conversion. To prevent the start of conversion either the peak-detect strobe can be inhibited, or the PSB flip-flop can be held in a dc reset state. Both techniques are used by various circuits which will be covered individually in later sections. At this time it is important to understand the relationship of the peak-detect strobe with respect to the pulse stretcher, and the function of the pulse stretcher busy flip-flop. A peak-detect strobe represents the first logic signal derived from the analog input. The remaining logic circuitry can be treated with logic description rather than circuit description.

Several other circuits are connected to the stretcher capacitors and these circuits will be discussed later.

3. The Lower Level Discriminator

The output signal from the input driver connects to the lower level discriminator through a series resistor. Transistor Q15 acts as a linear gate at the discriminator input. The quiescent condition of the linear gate is with Q15 turned off such that an analog input is applied to both the lower and upper level discriminators. Transistor Q13 operates as a biased amplifier with the positive analog signal compared with a

positive bias at pin 3. The bias level is set by the front panel lower level discriminator control. Signals above LLD BIAS turn on the left Darlington pair causing transistor Q8 to conduct and generate a positive voltage at its collector. This is coupled to Q16 and signal $\overline{\text{LLD}}$ at Q16 collector switches to ground. Signal $\overline{\text{LLD}}$ connects to only one place, pin 12 of IC11. When $\overline{\text{LLD}}$ switches to ground pin 11 of IC11 switches positive and generates the leading edge of LLD + B. When pin 11 goes positive transistor Q73 is turned on. This in turn turns off transistor Q27. Transistor Q27 with the series 4.7K resistor in its collector acts as a shunt to rapidly discharge the stretcher capacitor. All signals are connected to the stretcher capacitor whether or not they are above the lower level and upper level discriminator thresholds. Unless the lower level discriminator has been triggered, however, the stretcher capacitors will not remain charged to the peak input amplitude but will be discharged through Q27.

The signal at pin 11 of IC11 is inverted by another section of IC11 with the inverted output appearing at pin 3. Until the lower level discriminator threshold is exceeded pin 3 is positive. The positive signal is diode-resistor coupled to the base of transistor Q32 which is saturated. The collector of Q32 is connected to the output of the peak-detect multivibrator. Transistor Q32 will keep the output of the multivibrator clamped to ground unless the lower level discriminator has been triggered.

When the input signal exceeds the lower level threshold two functions are performed. First, the clamp across the stretcher capacitor is removed, and second, the peak detect monostable is permitted to generate a positive output pulse which will trigger the stretcher busy flip-flop and begin the conversion.

4. The Upper Level Discriminator

Another biased amplifier composed of transistors Q4 and Q2 is used as the upper level discriminator. Discriminator bias is determined by the front panel control setting and ranges from approximately .2 volts to

+5 volts. Signals above the discriminator threshold cause transistor Q2 to conduct and turn on transistor Q20. The collector of Q20 switches negative and sets the Reject flip-flop. The Reject flip-flop is composed of two two-input NAND gates in IC11. The outputs of the flip-flop, signals ULD and $\overline{\text{ULD}}$, perform the following functions. Signal ULD is resistor coupled to the base of transistor Q30. Q30 acts as a second shunt across the stretcher capacitor. When signal ULD goes positive Q30 saturates and the stretcher capacitor has effectively 330 ohms placed across it. This causes the stretcher capacitor to discharge on the trailing edge of the input signal, and in fact, the capacitor voltage follows the input signal down to the baseline. The Reject flip-flop is reset when the input signal passes through the lower level discriminator threshold and LLD + B switches to 0V. With the flip-flop reset Q30 is turned off, removing the very low impedance shunt from the stretcher capacitor. However, at the same time Q27 is turned back on by the recovery of signal $\overline{\text{LLD}}$. The higher resistance shunt path provided by Q28 will then return the stretcher capacitor to approximately 0 volts.

Signal $\overline{\text{ULD}}$ connects to pin 9 of IC8 where it prevents triggering of the PSB flip-flop in the event the peak detect monostable is triggered. This inhibits the start of an ADC conversion.

5. The Zero Level Circuitry

Refer to the block diagram and the schematic for the zero level circuitry discussed here. Transistors Q35, 40, 39, 23, and 28 form a biased amplifier which is used as the zero level discriminator. The input to the biased amplifier connects directly to the stretcher capacitor. The output of the circuitry which appears at the collector of Q28 is essentially a logic function at this point because of the very high gain after the biased amplifier. The bias for the amplifier is derived from the front panel ZERO LEVEL control and connects to pin 3 of Q35. The voltage at pin 3 ranges from 0 to +.4 volts depending on the front panel Helipot adjustment. Signal ZL at the collector of Q28 connects to pin 10 of IC7, the PSB flip-flop, and to pin 10 of IC8. Signal ZL acts as a dc

reset for the flip-flop when ZL is at zero. Signal ZL goes positive as the signal at the ADC stretcher exceeds the zero level bias. This removes the dc reset on the PSB flip-flop, and normally occurs somewhere on the leading edge of the input signal. When the input signal reaches peak amplitude the peak detect monostable is triggered and the PSB flip-flop is set. In the event ZL is not in the one state at peak detect time (signals below the zero level bias) the peak detect monostable will not set the PSB flip-flop due to its dc reset. Therefore, the leading edge of signal ZL acts as a logic function whereby no conversions will be started unless ZL is positive at peak detect time. For input signals above the zero level bias linear rundown will begin approximately .6 microsecond after PSB is triggered. At some instant in the linear rundown the voltage at the stretcher capacitor will pass through the zero level bias on its way toward the baseline. At this time signal ZL returns to the zero state and resets PSB flip-flop. The trailing edge of PSB is used to close the gate which terminates the scaling of the 50 MHz clock into the address scaler. Thus, the zero level discriminator performs a dual function. First, only signals above zero level bias are permitted to allow triggering of the PSB flip-flop, and second, the final encoded address is a function of the time that ZL returns to the zero state. This in turn is a function of the zero level bias. Figure 5 shows an input signal of 4V with three different zero level bias settings. The first setting corresponds to a bias greater than the input signal. ZL is not generated and no conversion of the input results. The second condition is with the zero level bias set for approximately half signal amplitude. Note the pulse train duration and the address of the converted signal. The third condition shows the zero level bias set approximately for zero; that is, such that the slope intercept is at zero-zero. Again, note the number of address advance pulses and the final address generated. It can be seen from these diagrams that in all cases the input pulse shape as seen by the stretcher is the same. The final encoded address however

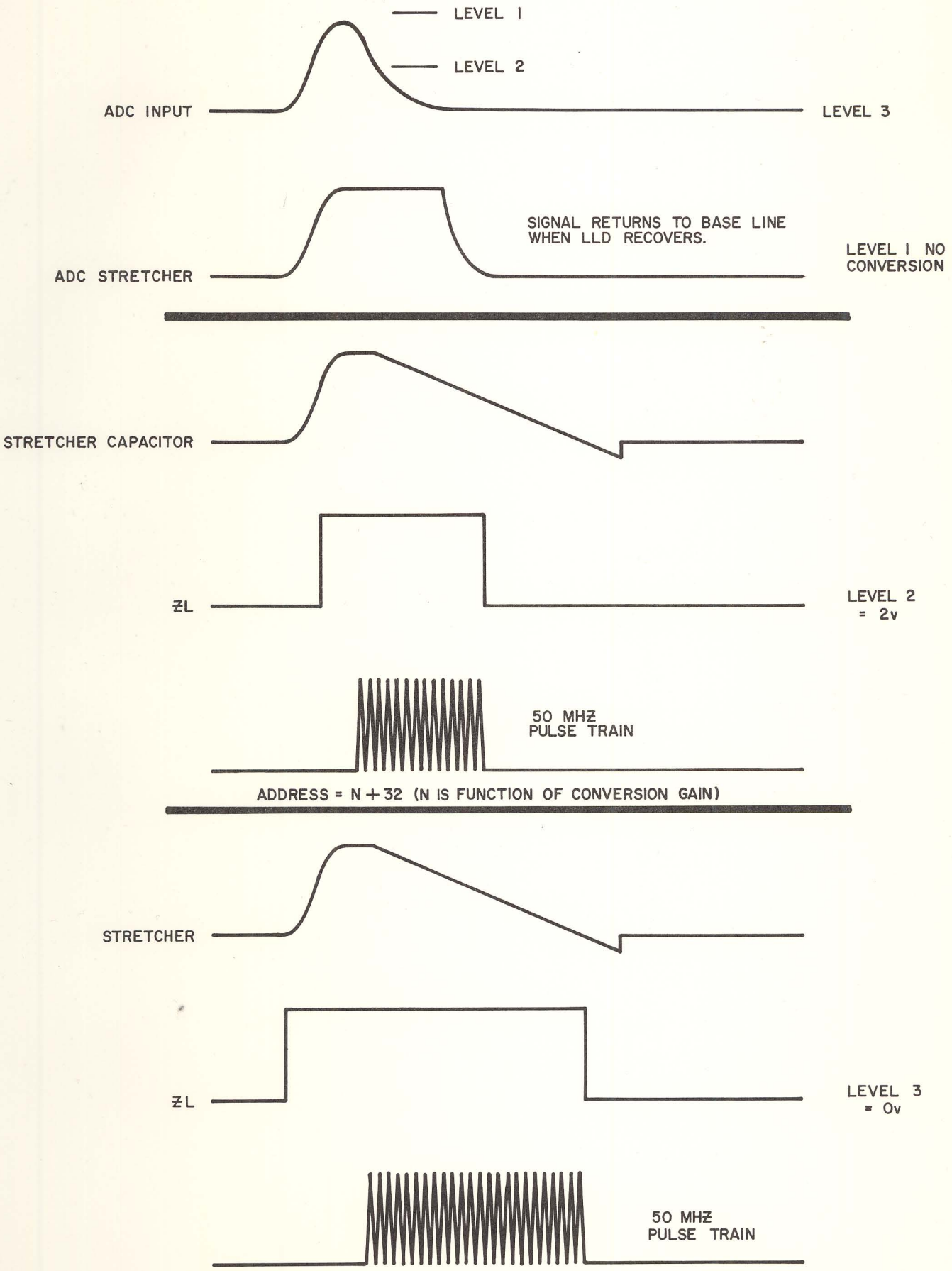

LEVEL 1
LEVEL 2
ADC INPUT
LEVEL 3
SIGNAL RETURNS TO BASE LINE WHEN LLD RECOVERS.
ADC STRETCHER
LEVEL 1 NO CONVERSION
STRETCHER CAPACITOR
ZL
LEVEL 2 = 2v
50 MHZ PULSE TRAIN
ADDRESS = N + 32 (N IS FUNCTION OF CONVERSION GAIN)
STRETCHER
ZL
LEVEL 3 = 0v
50 MHZ PULSE TRAIN
ADDRESS = 2N + 32, N = SAME NUMBER AS IN LEVEL 2 ABOVE.

FIG. 5

is a function of the zero level bias. Operation of the zero level circuitry in this manner provides all the advantages of biased amplifier operation without the disadvantages normally associated with them. The signal as connected to the ADC stretcher and other analog circuitry in the ADC is the same for any zero level bias. ADC stability and linearity are essentially independent of zero bias setting.

6. Rundown Current Switch and Conversion Switching

Approximately 100 nanoseconds after PSB is generated a constant current is applied to the stretcher capacitor to provide linear discharge of the capacitor. Transistor Q36 is a very high beta dual NPN transistor. One half of the transistor is used as a diode for temperature compensation of the other half which is operated in common base mode. The magnitude of the rundown current is controlled by the front panel CONVERSION GAIN switch. This switch controls the resistance between the emitter of Q36 and -20.4V. The resistance values are designed to yield the proper rundown current so that the address encoded from a nominal 4V input signal corresponds to the switch positions. In the quiescent state the current established by the switched-in resistor is conducted through transistor Q43. Signal $\overline{\text{CSC}}$ goes to the 0V when the rundown is to begin. The standing current in Q43 switches to Q36 and linear rundown begins. The rundown current remains switched on until the address as converted is either stored or rejected within the ADC. Later sections deal with a more detailed description of the timing of the ADC logic signals. At this time it is important to know only that signal $\overline{\text{CSC}}$ goes to 0V approximately 100 nanoseconds after PSB flip-flop is set. Signal $\overline{\text{CSC}}$ returns to its quiescent positive state when the ADC is reset, either internally under reject conditions or at the time a clear signal is received from the memory unit.

7. 50 MHz Oscillator and Address Scaler

Two 2N2369 transistors Q53 and Q54 are used in the 50 MHz oscillator. The oscillator output at the emitter of Q54 connects to an inverter/buffer in IC13. The output at pin 14 is inverted by another section of IC13

with 50 MHz appearing at pin 11. Both the true and complement 50 MHz are required for proper timing of the logic signals with respect to the clock.

Gating of the clock is performed in the base circuit of transistor Q52, the address scaler input-driver. Signal $\overline{ASG}$ switches to ground when address encoding is to begin, and Q52 acts as an inverter-driver for the 50 MHz clock signal applied to its base. At the end of conversion $\overline{ASG}$ returns to its quiescent positive condition and Q52 saturates, terminating scaler advance.

The address scaler comprises eleven JK flip-flops of TTL integrated circuits in seven packages. Ten of the flip-flops are used for address encoding and the eleventh is used for address underflow and 1024 overflow information. The first and second scaler stages are Sylvania SUHL II types rated at 50 MHz and all other stages are dual TTL types from the 7400 family. Note that the output of the second address scaler stage IC15 connects as a carry to two flip-flops. One flip-flop of the two contained in IC16 is used as an address scaler stage generating A_2 and $\overline{A_2}$. The other half of the dual flip-flop is used as the Current Source Control (CSC) flip-flop. This flip-flop is set when the "carry" from pin 11 of the second stage switches to ground. Signal $\overline{CSC}$ connects to the rundown current switch to control linear rundown. Following sections will discuss the timing of the logic signals in more detail. Note this flip-flop is dc reset by signal B when the Busy flip-flop is reset at CLEAR time.

There are 10 NPN transistors, numbers Q55 through Q64, which act as inverters for the address scaler outputs and also as buffers for the IC scaler stages. Two signals connect to the base of each inverter stage. One signal is the complement output of the scaler flip-flop, the other is signal $\overline{ING}$. $\overline{ING}$ is positive at all times except immediately after rundown. Signal $\overline{ING}$ is generated at the emitter of transistor Q71 and is equal to $\overline{B} \cdot PSB$. The output of IC12 pin 12 is at zero volts between the time PSB recovers and the ADC is reset, either internally or externally at CLEAR time. The ten buffers are held saturated by $\overline{ING}$

until pin 12 of IC12 switches to 0V. With $\overline{\text{ING}}$ at 0V the outputs of the IC scaler stages determine whether their respective buffer transistors are saturated or off. Thus, the encoded address as contained in the IC scaler is presented to the memory unit when the control of the buffers is switched from $\overline{\text{ING}}$ to the scaler at the end of conversion.

8. Conversion Logic Timing

Previous sections discussed individual circuits and logic blocks without any attempt to tie them all together in the system design. This section will cover the sequence of events from the arrival of the analog input through the end of conversion. Refer to Figure 6 which shows the timing of the major signals which will be discussed here. To simplify discussion, the ADC is assumed to be operated in the following manner. The upper and lower level discriminators are set for conversion of entire range from zero to full scale. The ZERO LEVEL control is set for approximate 0-0 intercept. The conversion gain and group size switches are set to the memory size available. The ADC is operated in a normal fashion; this precludes coincidence operation; no digital offset is used, and finally the ADC is analyzing normal pulses rather than dc or slow ac signals.

The incoming positive signal connects first to the gain-of-one voltage follower. The output of the voltage follower connects to the pulse stretcher and to the lower and upper level discriminators. As the signal starts positive the lower level discriminator triggers and removes the clamp across the stretcher capacitor. Simultaneously the clamp which inhibits the peak detect monostable output is removed. The positive signal across the stretcher capacitor is coupled to the zero level discriminator and it triggers generating positive signal ZL. With ZL in the one state the PSB flip-flop can now be triggered when peak detection occurs. The signal continues positive and all the proper logic levels have been established, awaiting peak detection to start the conversion. When the pulse reaches maximum amplitude the charging current to the stretcher capacitors drops to zero. Shortly thereafter the input signal

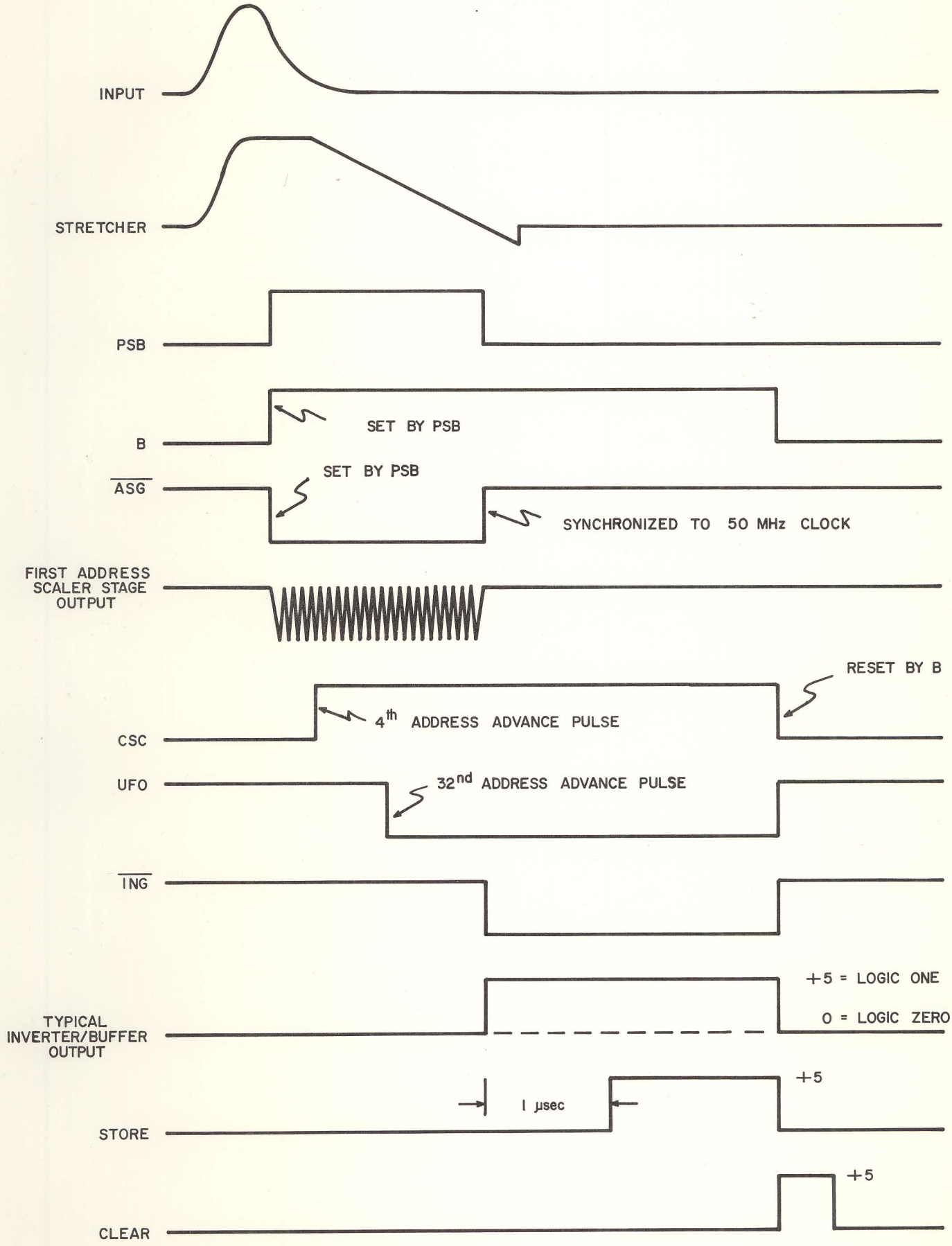

INPUT
STRETCHER
PSB
B
SET BY PSB
ASG
SET BY PSB
SYNCHRONIZED TO 50 MHz CLOCK
FIRST ADDRESS SCALER STAGE OUTPUT
RESET BY B
CSC
4th ADDRESS ADVANCE PULSE
UFO
32nd ADDRESS ADVANCE PULSE
ING
+5 = LOGIC ONE
0 = LOGIC ZERO
TYPICAL INVERTER/BUFFER OUTPUT
+5
1 μsec
STORE
+5
CLEAR

FIG. 6

starts down and peak detection occurs. A 50 nanosecond peak detect strobe is generated and this triggers the PSB flip-flop, setting it to the one state. Signal PSB goes positive and $\overline{PSB}$ goes to 0 volts. PSB sets the ADC Busy flip-flop and signal $\overline{B}$ goes to ground. This prevents the clamp on the stretcher capacitor from being turned back on until the flip-flop is reset. Signal $\overline{B}$ also generates signal LGS which closes the linear gates for the stretcher and discriminators. This holds the discriminators and the stretcher inoperative until this conversion-STORE sequence is complete. PSB is inverted (IC13) and its output is differentiated and the resultant pulse sets the Address Scaler Gate control flip-flop, IC12. The output of this flip-flop, signal $\overline{ASG}$, (connected to the driver at the input to the first stage of the address scaler) switches to the zero state. The 50 MHz clock signal is gated on and the scaler advances at a 50 MHz rate. Four clock pulses after scaling begins, the carry output of the second address scaler stage switches to ground. This sets stage A2 and also sets the CSC flip-flop. Signal CSC connects to the rundown current switch and turns on the rundown current.

With no digital offset, address stages A5 through A9 will be in the "set" state and stages A0 through A4 will be "reset" when scaling begins. After 31 clock pulses all address stages will be in the one state. One pulse later all address stages switch to the zero state. At this time a carry pulse from the last address stage A9 sets the UFO flip-flop and signal UFO switches to ground. The address scaler at this time is in channel 0. It is important to recognize that the address scaler begins from an equivalent address of -32; that is, it takes 32 pulses from the 50 MHz clock to place the address scaler in channel 0. The scaler requires .64 microsecond to arrive at channel 0 due to this built-in digital offset of 32 channels. The design of the analog circuitry is such that with the ZERO LEVEL control set for 0-0 there are exactly 32 channels of equivalent pedestal built into the analog circuitry. Even with no front panel digital offset, the address transferred to the memory unit differs from the number of address-advance pulses by a fixed quantity of 32.

The 32 channel digital offset serves two purposes. First, the turn-on of the rundown current is synchronized to the 50 MHz clock by scaling 4 address-advance pulses before setting the CSC flip-flop. No attempt is made to synchronize opening of the address scaler gate with the 50 MHz clock. The triggering uncertainty in the first stage has no effect on the ADC synchronization. For good channel profile it is essential that start of rundown current be well synchronized to the clock. This is accomplished by scaling in 4 pulses from the clock before signal CSC is generated. The first 2 address stages actually perform the synchronization. By the time the scaler has scaled 4 clock pulses the transitions are well synchronized to the clock.

At this time the sequence of events which began the conversion process have been covered. The address scaler has been advanced to channel 0 by scaling 32 address advance pulses. The conversion process now continues until the voltage at the stretcher capacitor reaches the zero level bias. Signal ZL at this time returns to zero volts and resets the PSB flip-flop. Signal $\overline{\text{PSB}}$ is ANDed with 50 MHz to form a reset pulse for the Address Scaler Gate Control flip-flop. When $\overline{\text{PSB}}$ switches positive the next 50 MHz clock pulse resets the flip-flop and signal $\overline{\text{ASG}}$ switches positive. With $\overline{\text{ASG}}$ positive the 50 MHz gate at the address scaler is closed and address encoding is terminated. Since signal $\overline{\text{ASG}}$ is switched by a 50 MHz clock pulse the trailing edge of the conversion process is also synchronized to the clock. This again improves the channel profile of the ADC.

Now that the address has been generated it is presented to the memory unit and to the "acceptance test" logic circuitry. This is accomplished in the following way. Signal $\overline{\text{ING}}$ switches to 0 volts when PSB returns to 0V and the NPN inverter-buffer transistors are allowed to switch to the states determined by their respective scaler stages. This presents the address to both the memory unit and the acceptance test logic circuitry.

This completes the basic conversion process. The address as

presented will either be transferred to the memory unit or rejected by the acceptance test circuitry which is covered in the next section.

C. STORE, CLEAR, Reject and Digital Offset Logic Circuits

1. General

This section deals with the sequence of events which immediately follows the end of the conversion. This includes the address acceptance tests followed by a STORE or internal reset of the ADC. Integrated circuits are used almost exclusively in this area so that no separate block diagram is provided. The schematic takes the form of a block diagram and will be used for this discussion.

2. STORE Command

From a logic standpoint STORE utilizes only two signals in the ADC, the pulse stretcher busy output PSB and the ADC busy output, signal B. At this time refer to the schematic and find the signal $\overline{\text{PSB}}$ on pin 9 of IC2. The output at pin 8 is again inverted in IC2 with the inverted output on pin 6. Pin 6 has a shunt-connected capacitor of 1000 pf to ground which delays the positive output signal such that it passes through the "one" state approximately 1 microsecond after PSB returns to zero. IC3 contains a two-input gate with inputs on pins 1 and 2. Signal B on pin 1 goes positive at the start of conversion. Signal $\overline{\text{PSB}}$-delayed on pin 2 reaches the one state approximately 1 microsecond after PSB returns to zero. Pin 3 switches to ground 1 microsecond after the end of conversion. This signal is inverted and the output appears at pin 11 of IC3. This output connects to two NAND gates. If the inputs at pins 2 and 4 on IC4 are positive when pin 5 goes positive, the output of this gate at pin 6 will switch to ground. This negative transition is coupled to pin 9 of IC3 and a positive output, STORE, appears at pin 8 of the same section. Signal STORE connects to the rear panel and then to the memory unit. Note that output pin 6 of IC4 also connects to pin 9 of IC4, a two-input NAND gate. If pin 2 or 4 is at zero when pin 5 of IC4 goes positive, pin 6 will remain positive. The inputs to pins 9 and 10 of IC4 will now both be positive and pin 8,

the output of the gate, will switch to ground. This connects to the trigger input on a single shot multivibrator which is triggered and generates signals RESET and $\overline{\text{RESET}}$. These signals reset all the logic circuits in the ADC to prepare it for accepting another input signal. Thus, when pin 5 of IC4 goes positive one of two logic functions will occur. Either a STORE will be generated if pins 2 and 4 are both positive, or the ADC will be immediately reset by the triggering of IC5. When a STORE is generated the reset multivibrator must be triggered by a CLEAR which is inverted by transistor Q17. The CLEAR is generated by the memory unit at the end of data-transfer.

Pins 2 and 4 on IC4 are reject inputs. If either of these pins is at zero at the end of conversion the single shot will be triggered internally with no STORE generated. Pin 2 connects to the rear panel and provides an auxiliary means of rejecting analyses. This input is provided for users convenience in adapting the ADC to complex systems. Signal $\overline{\text{REJ}}$ on pin 4 is the ORed output of three reject tests, any one of which can cause reject of the conversion. Transistor Q65 generates $\overline{\text{REJ}}$ and its base circuit contains the three signals which initiate an internal reject-clear sequence. One of the reject inputs is derived from emitter follower Q72. Signal OFO connects to the base of Q72 and is the overflow signal. This signal is derived from a diode OR gate contained on the front panel GROUP SIZE switch (NS-622 only), a special progressive-open type. The outputs from the address inverter buffers connect to this switch in addition to their rear panel connection to the memory unit. Only stages A6 through A9, which represent the more significant bits, are so connected. The switch position shown is for a group size of 128 channels. Address 128 and greater will have at least one of the stages from A7 through A9 in the one state. If any address stage connected by the switch is in the one state signal OFO is positive. This signal then connects to the base of emitter follower Q72 and turns on Q65. Signal $\overline{\text{REJ}}$ switches to zero such that when pin 5 of IC4 goes positive the reset multivibrator will be triggered. The base circuit of

Q65 has two additional signals connected to it. One is a 10-input diode AND gate and the other is signal UFO. In the memory unit channel zero is reserved for live time storage so it is important that no STORE command be generated for this channel. For channel zero all address stages are reset and $\overline{A_0}$ through $\overline{A_{12}}$ are all positive. Signal STROBE goes to +5 volts at the end of conversion. If all 10 address scaler stages are in the zero state transistor Q65 is turned on and signal $\overline{REJ}$ switches to ground. This inhibits STORE and the ADC is reset internally. The function of signal UFO which also connects to the base of Q65 will be discussed in the next section under Digital Zero Offset.

3. Digital Offset Circuitry

Refer to the schematic and note that address scaler stages A8 and A9 have both reset and set inputs. The set and reset signals are generated in IC10. For no digital offset the "set" inputs will be used on address stages A8 and A9. A front panel switch associated with each address stage controls the state of its respective stage when a reset pulse is generated at CLEAR time. The 512 switch controls address stage A9 and sends a reset pulse rather than a set pulse when the switch is "on". In similar fashion the reset state of stage A8 is determined by the front panel switch labeled 256. Two NAND gates are associated with both the A8 and A9 address scaler stages, one generating a reset pulse, the other a set pulse for the respective stage. For purposes of explanation refer to IC10 pins 3 and 6, the set and reset pulses for address stage A9. The RESET pulse, either internally generated at reject time or by a CLEAR input, is applied to pins 2 and 4 of IC10. A9S and A9R connect to the front panel digital offset switch labeled 512. With the switch off A9S will be open and A9R will be connected to ground. When RESET goes positive, pin 3 on IC10 switches to ground and sets the address scaler stage. With the switch "on" for 512 channels of digital offset, pin 1 is grounded and pin 5 is opened. Now when the RESET pulse is applied to the gates, pin 6 will switch to ground while pin 3 remains positive. This resets the address scaler stage.

The manner in which digital offset is accomplished can be best explained by using two examples. The first will use no digital offset while the second will have 512 digital offset. Assume for the moment then that both digital offset switches are off. When the address scaler is cleared stages A5 through A9 will be set; that is, the true outputs will all be in the one state. Stages A0 through A4 on the other hand will all be reset with the true outputs all in the zero state. The underflow flip-flop contained in IC20 will also be reset and signal UFO will be positive. Assume the address scaler gate is opened and that the scaler begins scaling. 31 address advance pulses later all stages A0 through A9 will be in the one state. One more address advance pulse will reset stage A0 which will propagate a carry to A1 and reset it. This in turn will propagate a carry to stage A2 resetting it. The process continues such that a carry is propagated through the 10 stages of the address scaler. A carry is also propagated to the Underflow flip-flop at this time. Signal UFO switches to 0V and the address scaler is in channel zero. If the address scaler were to stop here the Channel Zero reject gate would inhibit storage. If the address scaler continues to advance beyond channel zero and does not exceed group size it will be stored in the memory unit. Under these conditions the address as presented differs from the number of clock pulses by 32.

Now let's switch in 512 channels of digital offset. With the front panel switch "on" address stage A9 will always be cleared to the zero state so that 32 address advance pulses will put stages A0 through A8 in the zero state and a carry will propagate to stage A9 and set it to the one state. At this time no carry is propagated to the UFO flip-flop by A9. If conversion ceases at this time the channel zero reject gate will not reject the conversion but signal UFO will remain positive and keep signal $\overline{\text{REJ}}$ at ground, rejecting the conversion. Assume conversion continues for 511 additional address advance pulses. Now stages A0 through A9 will all be in the one state. Remember that this is the

condition corresponding to 31 address advance pulses with no digital offset. With one additional pulse stages A0 through A9 will be switched to the zero state and a carry will propagate to the UFO flip-flop removing signal UFO from Q65. However, at this time, the channel zero reject gate will still reject this conversion. All conversions generating more than 32 plus 512 address advance pulses will be stored as long as they do not exceed the group size switched in on the front panel.

The ADC is designed with a built in 32 channel digital offset. This offset is compensated for in the analog circuitry. It can be shown that the number of address advance pulses required to place the address scaler in channel zero is equal to 32 plus the digital offset switched in on the front panel. Digital offset can be thought of in another way. The address scaler can be thought of as being initially reset to a negative number. Also all negative-number conversions will automatically be rejected by the logic circuitry. Thus a digital offset of 512 can be thought of as a minus 512 condition of the address scaler. No storage will occur until the scaler has been advanced through the negative number and this means a minimum of 512 plus 32 address advance pulses. Note that for a given analog input the amount of offset does not affect the conversion dead time. At high count rates and high resolution settings of the conversion gain switch it is ofttimes wise to consider using analog offset with the ZERO LEVEL control for reduced dead time. With 50 MHz digitizing rate however, the analog control may be worthwhile only in extremely high count rate/resolution experiments.

4. Dead Time Signal and ADC Recovery Circuitry

Any time the ADC is busy and not capable of accepting an input for conversion it is considered "dead" to an input. For proper live time operation the time base clock must be gated off during these dead periods. To generate the dead time signal the logic functions which represent dead time are ORed into one signal which is used for live time operation. Refer to the schematic and find transistors Q10 and

Q14. The base of Q10 contains a diode OR gate with inputs LLD+B and REC. The two transistors act as a current switch. When the ADC is busy the standing current in Q10 is switched to Q14. The current pulses are integrated by the capacitor in the collector of Q14 and the dead time meter indicates the average dead time. When the current is switched from Q10 to Q14 transistor Q9 turns off, its collector goes positive, and signal DT is generated. DT is inverted by IC2 and connects to pin 12 of IC2 where it is ANDed with the live time clock pulse from the NS-633 memory unit.

The NS-622 ADC has signal DT connected to the rear panel for external live timer operation. The live time logic on the schematic is utilized in the NS-633 only.

Signal REC (a part of dead time) is the output of a monostable which is triggered by the reset monostable. $\overline{\text{REC}}$ connects to the peak detect strobe gate, pin 12 of IC8. Any peak detect output which occurs within 3 usec (the duration of REC) of an ADC reset signal is prevented from starting a conversion. This prevents conversion of partial pulses which may be present when the ADC is cleared.

5. Live Time Storage (NS-633 only)

A clock pulse from the memory section is connected to the LTC input in the base of Q3. The pulse is differentiated and inverted with a positive output at the collector of Q5. If the ADC is not busy pin 11 of IC2 will switch to zero and set the Live Time F.F. when a clock pulse arrives. With the ADC busy the positive clock pulse produces no further logic sequence.

When the Live Time flip-flop is set signal LTF goes positive. This is inverted by IC3 with a negative output on pin 6. This immediately generates a STORE and bypasses the normal STORE-CLEAR logic. $\overline{\text{LTF}}$ connects to IC6 pin 1 and keeps signal $\overline{\text{ING}}$ positive. With $\overline{\text{ING}}$ positive all address inverter outputs will be zero regardless of address scaler state. Thus, an LTF STORE is guaranteed to be in address channel 0.

Signal $\overline{\text{LTF}}$ also connects to pin 4 on IC11. When $\overline{\text{LTF}}$ goes to zero

pin 6 of IC11 goes positive and saturates Q30, placing the 330 ohm resistor across the stretcher capacitor. This quickly discharges any charge the capacitor may have gained because of LTF triggering on the leading edge of an input pulse.

Live time storage occurs in channel 0 in the memory unit. As far as the memory is concerned there is no distinction between live time and data storage. When the memory unit sends a CLEAR the ADC and Live Time flip-flop are both reset.

VI. SERVICING

Servicing of the ADC can be accomplished without a memory unit. All ADC functions can be checked with a good stable pulser capable of generating a zero to 5 volt positive pulse in the range of 1 to 2 microseconds duration. A scope with a 50 MHz bandpass is the minimum which can be used on most of the fast logic circuitry. The module will have to be bench operated so that an extender cable between the module and the bin power supply is required.

To disassemble the module for servicing use the following procedure. Remove the two Phillips-head screws on the front panel in the upper right and lower right corners. Do the same on the rear panel. Remove the right hand side of the module and the upper and lower shields. The printed circuit board is now exposed for servicing. To replace components the board need not be removed from the module. To replace components the left cover of the module must be removed to expose the bottom side of the printed circuit board.

The ADC has been described in some detail in the previous section, System and Circuit Design. This section coupled with the schematics and timing diagrams should greatly assist trouble shooting. In general, all components used in the ADC are stock items with large electronic distributors. Sheets are included in the manual preceding the schematic which show the pin numbers for the integrated circuits along with their types. The connector tabulations list the signals, connectors, and pin numbers where these signals appear. Where practicable, signals are labeled on the printed circuit boards as they appear on the schematic and connector tabulations. A short time spent with the connector tabulations, the list of major signals and their functions, and the general notes preceding the schematics will be a very good investment once trouble shooting is undertaken. The factory may be contacted for assistance in servicing if difficult problems are encountered.

MAJOR SIGNALS AND THEIR FUNCTIONS

Signal	Function
A0 through A9	10 bit address which connects to memory unit. Logic zero = 0V, logic one = +5V.
A8R	Control signal which connects to F.P. DIGITAL OFFSET switch. Signal is +5 when "256" switch is off, ground when switch is on.
A8S	Same as A8R with exception that signal is +5 when switch is on, and 0V when switch is off.
A9R	Same function as A8R for 512 switch.
A9S	Same function as A8S for 512 switch.
ACN	Connects to COINC BNC in the ANTI COINC position of the mode switch. Positive signal inhibits conversion by preventing PSB flip-flop from being triggered.
$\overline{\text{ASG}}$	Address scaler gate control flip-flop output. Flip-flop is set by PSB, allowing address scaler to scale at 50 MHz. Reset by PSB · 50 MHz so that trailing edge gating is synchronized to clock.
B	Output of ADC busy flip-flop. Flip-flop is set by PSB and reset by RESET. This signal is major component of dead time signal, connects to STORE logic, and holds ADC linear gates closed while in the one state.
CLEAR	Rear panel input to the ADC to reset the ADC after data transfer. Requirements: positive 3-10V pulse, 1/2 to 1 usec duration. Input impedance: 3.3K dc connected.
CNC	Connects to COINC BNC in the COINC position of the mode switch, and to +5 in the ANTI COINC position of the mode switch. Positive input opens linear gate to allow ADC conversion. See section on COINC operation for more details.
$\overline{\text{CSC}}$	Current source control F.F. output. Connects to run-down-current switch and starts linear rundown when switched to the one state. Flip-flop is set by carry from the second stage of address scaler and reset by the ADC Busy F.F. output, signal B.
DT	Dead Time signal appearing on rear panel connector. Signal is +5 whenever the ADC is busy converting an input or whenever it is insensitive to an input. Used in the memory unit for dead time correction in the live timer.
DTM	Dead Time Meter drive signal. Connects to F.P. Meter.

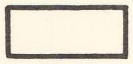
Ext B	Buffered output of ADC Busy F. F. available on ADC rear panel. Logic zero = 0V, logic one = +3V.
Ext Cont	Rear panel input provided to disable normal STORE-REJECT logic. Used by NS-641 Two Parameter Adapter to disable ADC logic.
Ext Gate	Input provided to force channel 0 by saturating address inverter/buffer transistors. Used by NS-641 Two Parameter Adapter for storage of Singles and/or Live Time counts.
Ext PSB	Buffered output of Pulse Stretcher Busy F. F. available on ADC rear panel. Logic zero = 0V, logic one = +3V.
Ext REJ	Rear panel input provided to reject a conversion. Input requirements: +5V signal must be applied at peak detect time to inhibit conversion.
Ext $\overline{\text{REJ}}$	Rear panel input provided to inhibit STORE and cause internal ADC reset. Input requirements: To inhibit STORE this input must be at 0V when PSB returns to 0V and for at least 2 usec thereafter. External source must sink approximately 2. 5 mA at 0V.
LGS	Linear Gate Source. LGS = B + OFF + $\overline{\text{CNC}}$. The linear gates for the ADC stretcher and discriminators are closed whenever LGS is in the one state.
OFF (NS-622)	Connects to Front Panel ANALYZE-OFF switch. Ground in ANALYZE switch position, +5V in the OFF position. Holds ADC in dc reset condition. Also used by NS-630 Memory Unit and NS-641 Two Parameter Adapter to hold timing scalers reset until analysis begins.
PSB	Pulse Stretcher Busy F. F. output. Set by peak detect strobe and reset by ZL in the zero state. Triggers and/or controls several ADC logic functions at the start and end of conversion which is indicated by the leading and trailing edges of this signal respectively.
$\overline{\text{REC}}$	3 usec output of Recovery Single Shot. Inhibits start of conversion within 3 usec after ADC is reset.
STORE	Positive 5V signal which indicates conversion complete and acceptable address for storage in the memory. STORE and address remain until a CLEAR is received by the ADC.
UFO	Underflow F. F. output. Signal is positive until address scaler has advanced through channel 0. Provides automatic reject of conversions below channel 0 when using digital offset.

REAR PANEL

26M ADC CONNECTOR

PIN	SIGNAL
A	A0
E	A1
K	A2
P	A3
U	A4
Y	A5
$\overline{c}$	A6
C	A7
H	A8
M	A9
S	
W	
$\overline{a}$	
B	DT
F	STORE
L	CLEAR
R	OFF
V	B EXT
Z	$\overline{\text{REJ}}$
$\overline{d}$	EXT CONTROL
D	EXT REJ
J	EXT GATE
N	SET B
T	PSB
X	
$\overline{b}$	GND

GENERAL NOTES

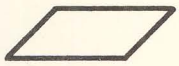


Designates signal source which connects to loads off this schematic/board and may also have loads on this schematic/board.

Designates signal from a source not on this schematic/board.

Designates source for a signal used only on this schematic/board.

Designates load for signal used only on this schematic/board.



Designates front and rear panel labeling.

All NPN transistors are 2N2369 or S2830 (2N2369 with minimum beta of 30) unless otherwise marked.

All PNP transistors are 2N3638, unless otherwise marked.

Pin numbers on Integrated Circuits are as viewed from the top of the IC.

All resistors are 1/4 watt 5%, unless otherwise marked.

R47 Resistor whose value is .47 ohms.

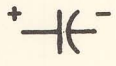
4K7 Resistor whose value is 4700 ohms.

4M7 Resistor whose value is 4.7 megohm.

MF designates precision metal film 1/4 w $\pm$ 1% resistors, unless otherwise specified.

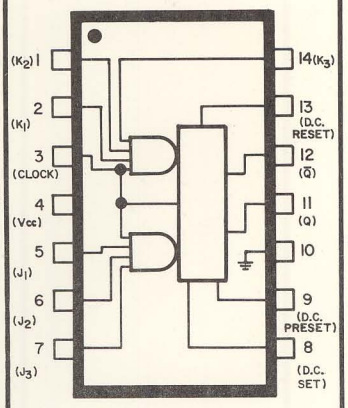
All diodes are Fairchild IN4150 or equivalent, unless otherwise specified.

Capacitance values shown are in picofarads unless otherwise specified.



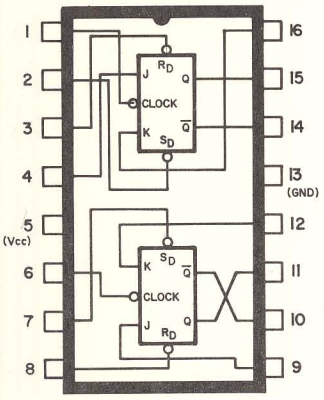
Polarized capacitors are as shown.

SF203



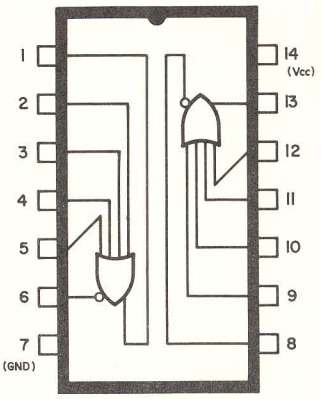
50 MHz
J-K FLIP-FLOP

7476



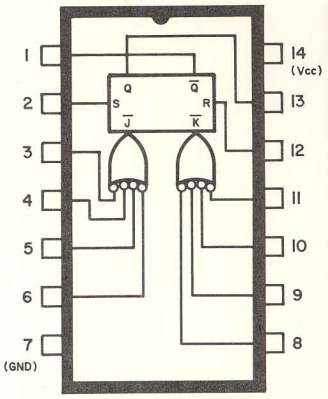
DUAL J-K FLIP-FLOP

MC1023



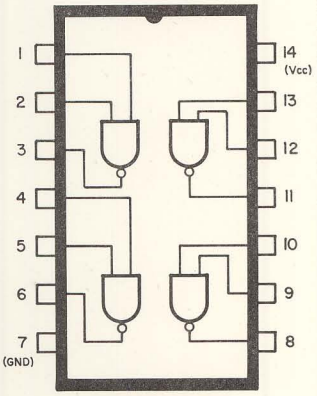
2-4 INPUT
CLOCK DRIVER

MC1027



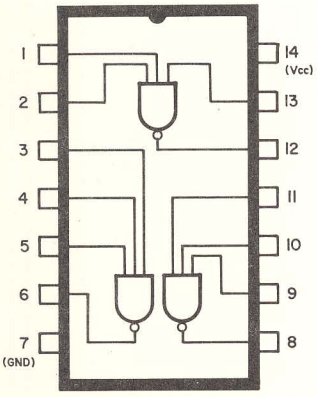
120 MHz
J-K FLIP-FLOP

7400



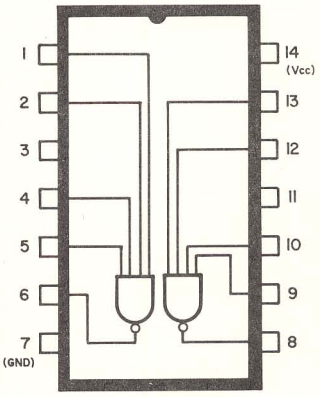
4-2 INPUT
NAND GATE

7410



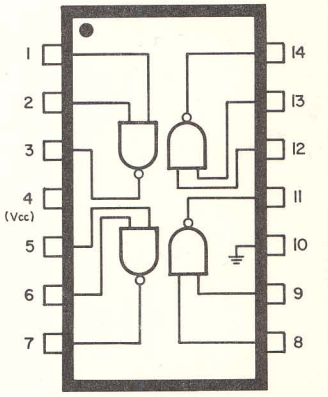
3-3 INPUT
NAND GATE

7420



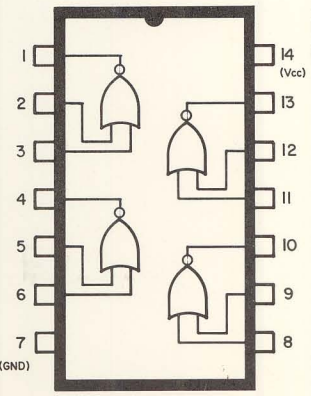
2-4 INPUT
NAND GATE

RG3222



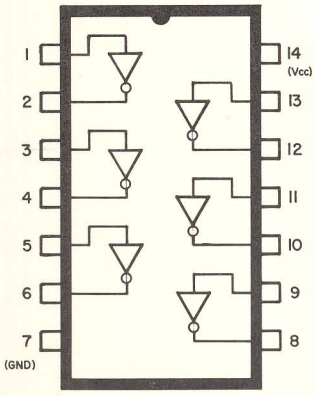
75 MHz
TTL

7402



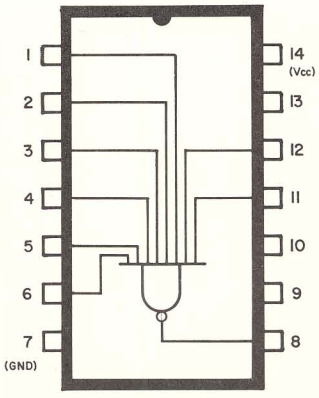
4-2 INPUT
POSITIVE NOR GATES

7404



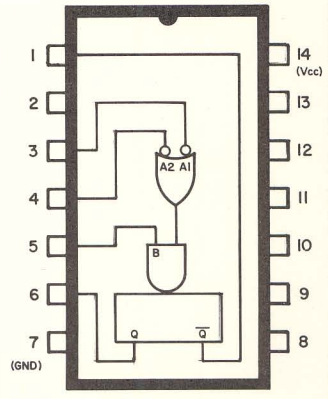
HEX INVERTERS

7430



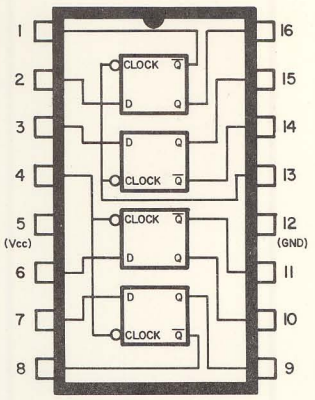
8-INPUT
POSITIVE NAND GATES

74121



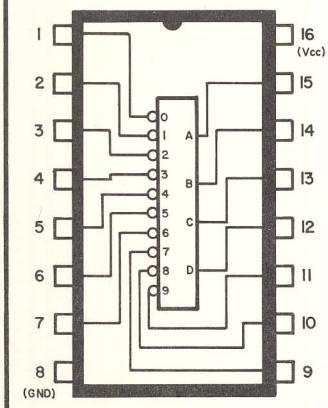
MONOSTABLE MULTIVIBRATORS

7475



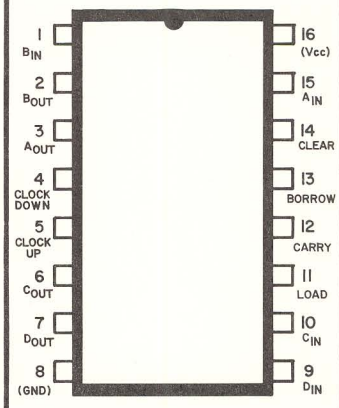
4 BIT BISTABLE LATCHES

7442



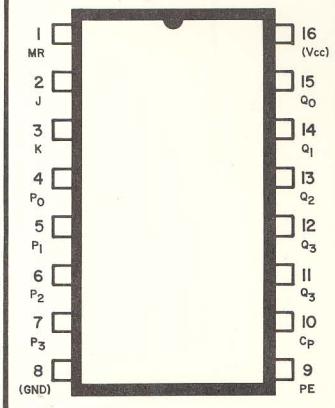
4 LINE–TO–10–LINE DECODERS

8560 8563



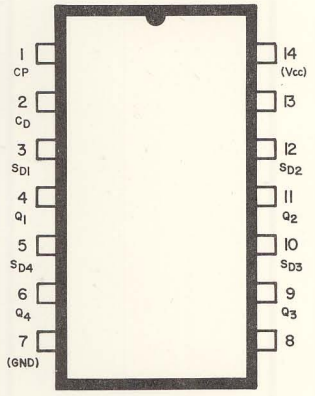
UP/DOWN DECADE COUNTER
UP/DOWN BINARY COUNTER

9300



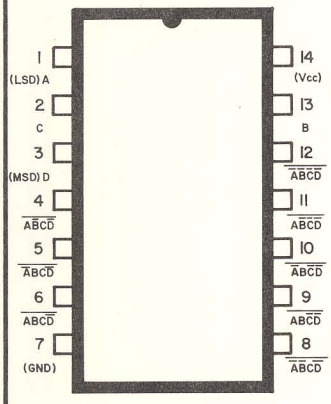
4–BIT SHIFT REGISTER

839



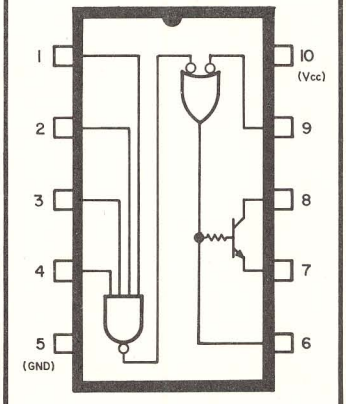
DIVIDE–BY
SIXTEEN COUNTER

8250



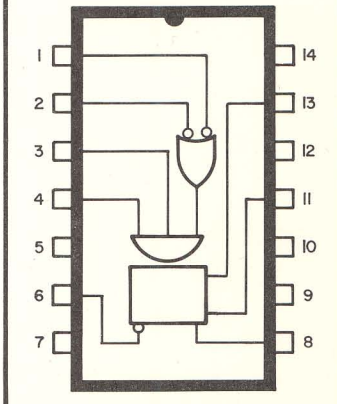
BINARY–TO–OCTAL DECODER

SH2002–P



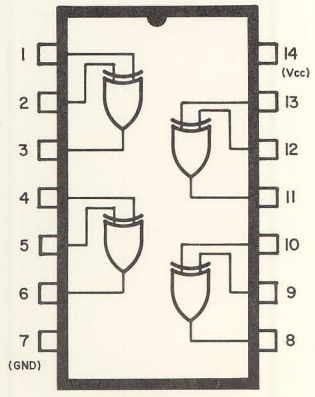
HIGH POWER DRIVER

9601

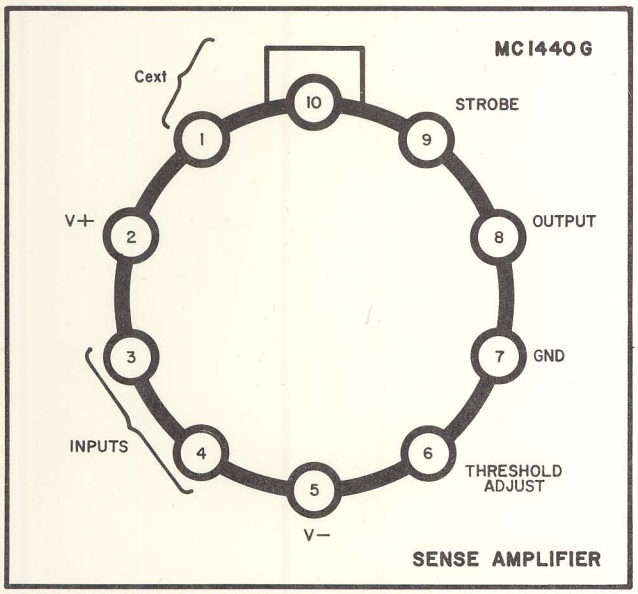


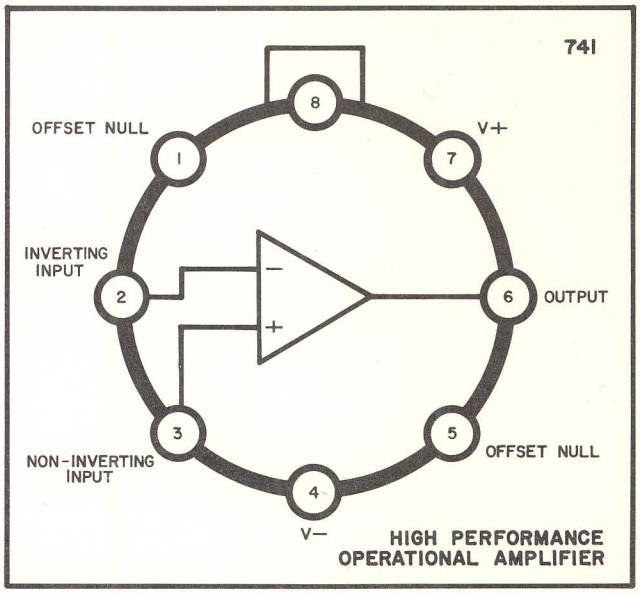
RETRIGGERABLE MONOSTABLE
MULTIVIBRATOR

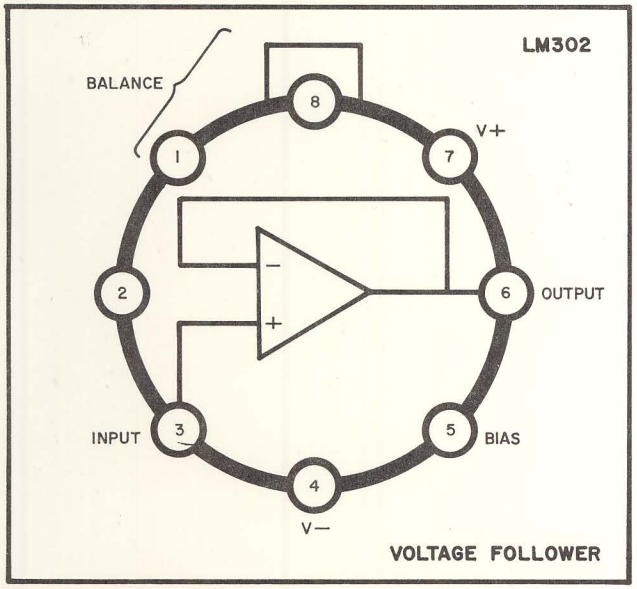
1812–P

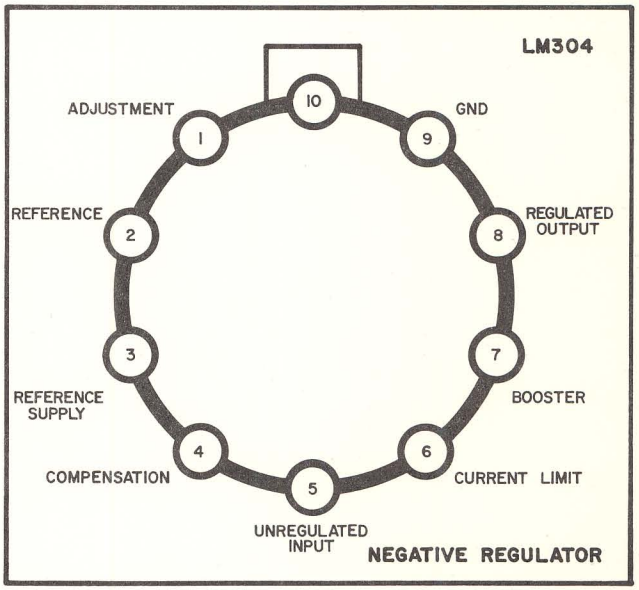


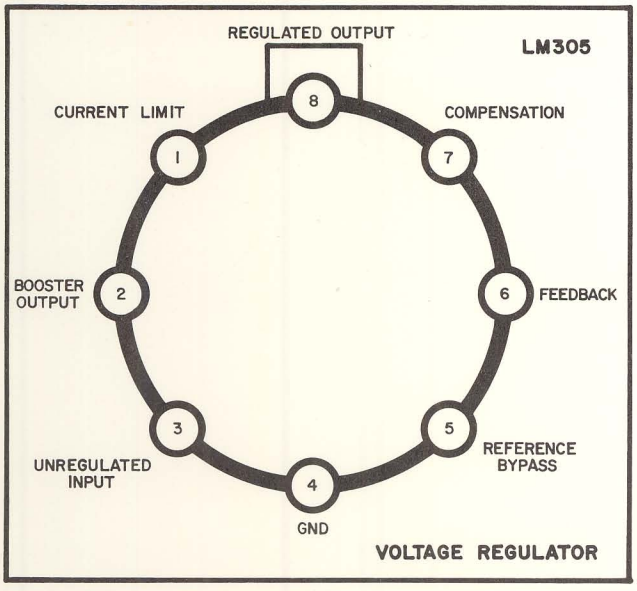
4–2 INPUT
EXCLUSIVE OR GATE

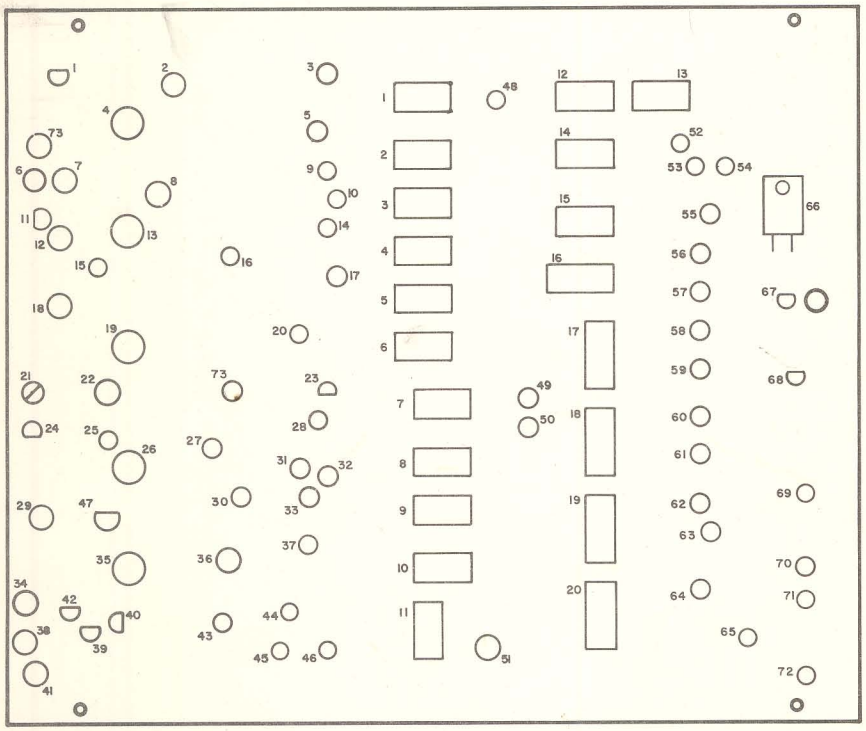

MC1440G
Cext
10
STROBE
1
9
V+
2
8
OUTPUT
3
7
GND
INPUTS
4
6
THRESHOLD ADJUST
5
V−
SENSE AMPLIFIER


741
8
OFFSET NULL
1
7
V+
INVERTING INPUT
2
6
OUTPUT
3
5
NON-INVERTING INPUT
OFFSET NULL
4
V−
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

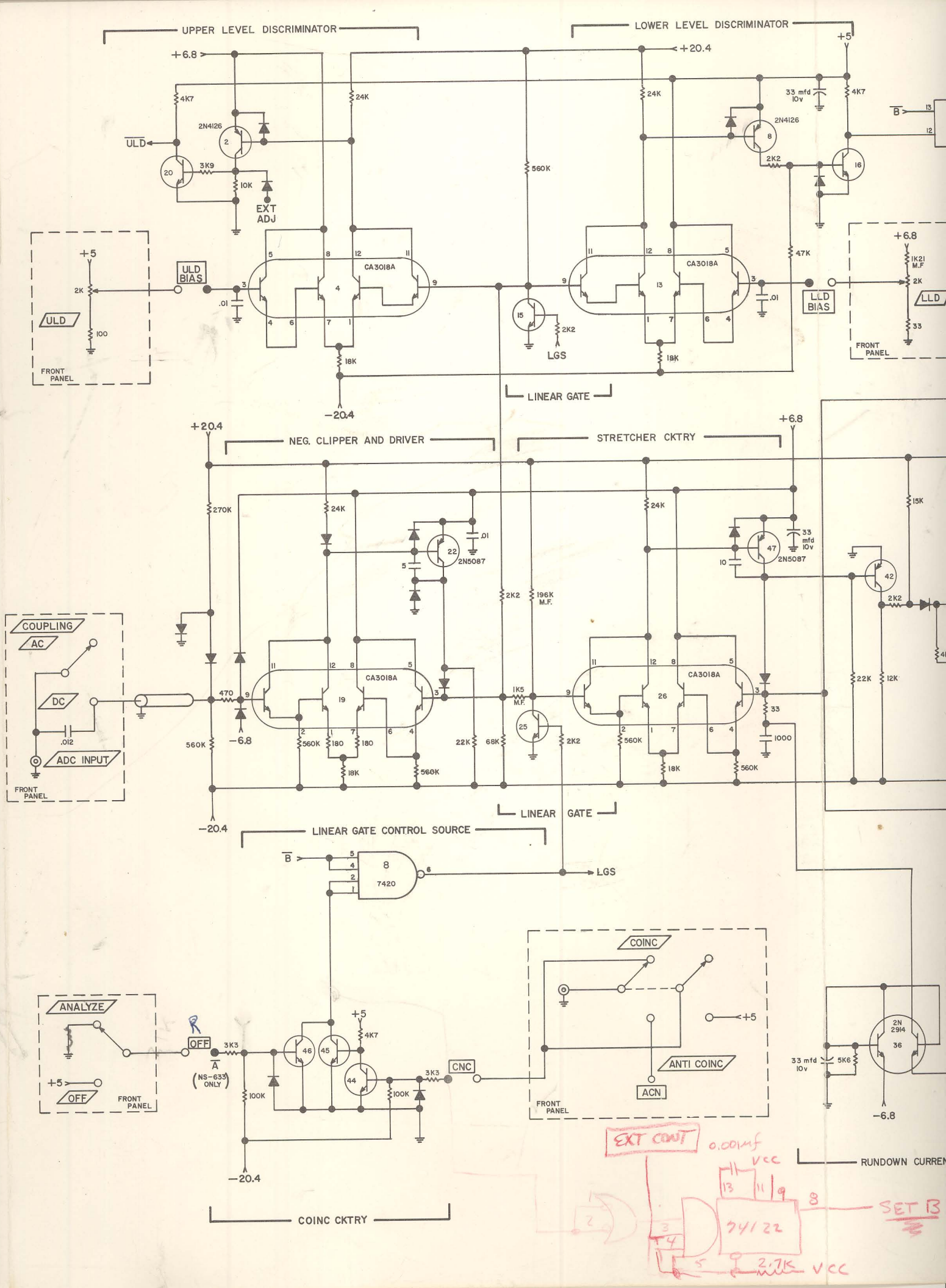

LM302
BALANCE
8
1
7
V+
2
6
OUTPUT
INPUT
3
5
BIAS
4
V−
VOLTAGE FOLLOWER

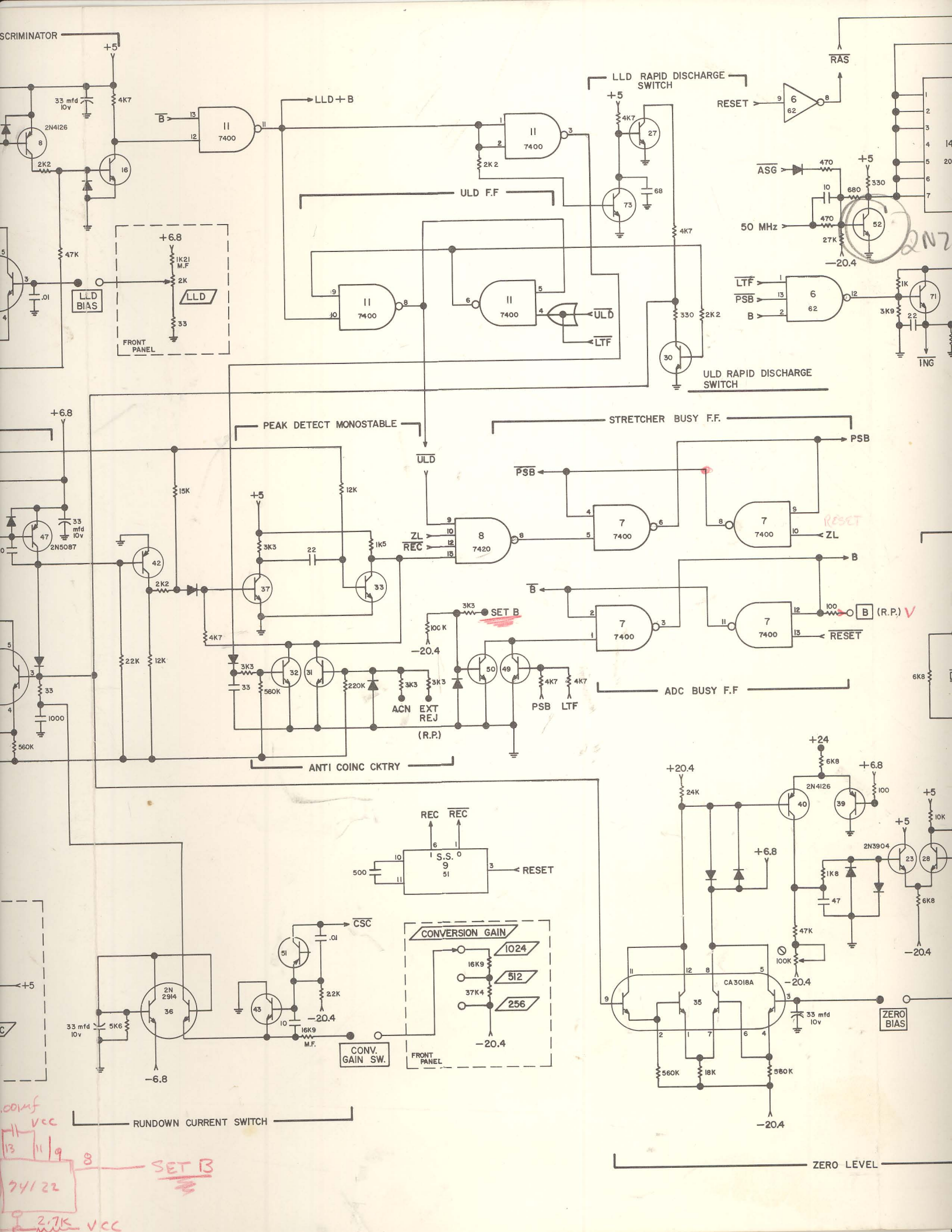

LM304
ADJUSTMENT
10
GND
1
9
REFERENCE
2
8
REGULATED OUTPUT
3
7
REFERENCE SUPPLY
BOOSTER
4
6
COMPENSATION
CURRENT LIMIT
5
UNREGULATED INPUT
NEGATIVE REGULATOR

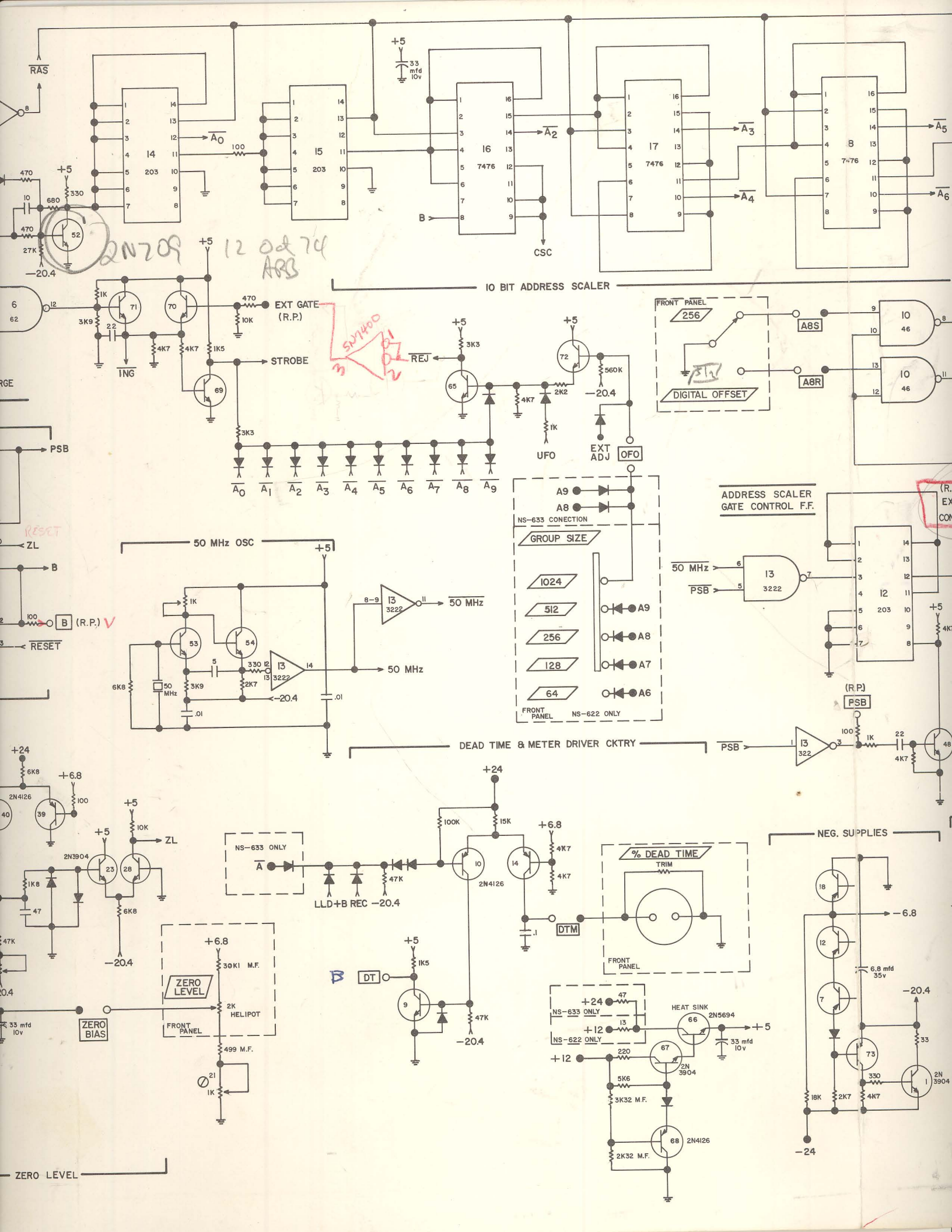

REGULATED OUTPUT
LM305
8
CURRENT LIMIT
COMPENSATION
1
7
BOOSTER OUTPUT
2
6
FEEDBACK
3
5
UNREGULATED INPUT
REFERENCE BYPASS
4
GND
VOLTAGE REGULATOR

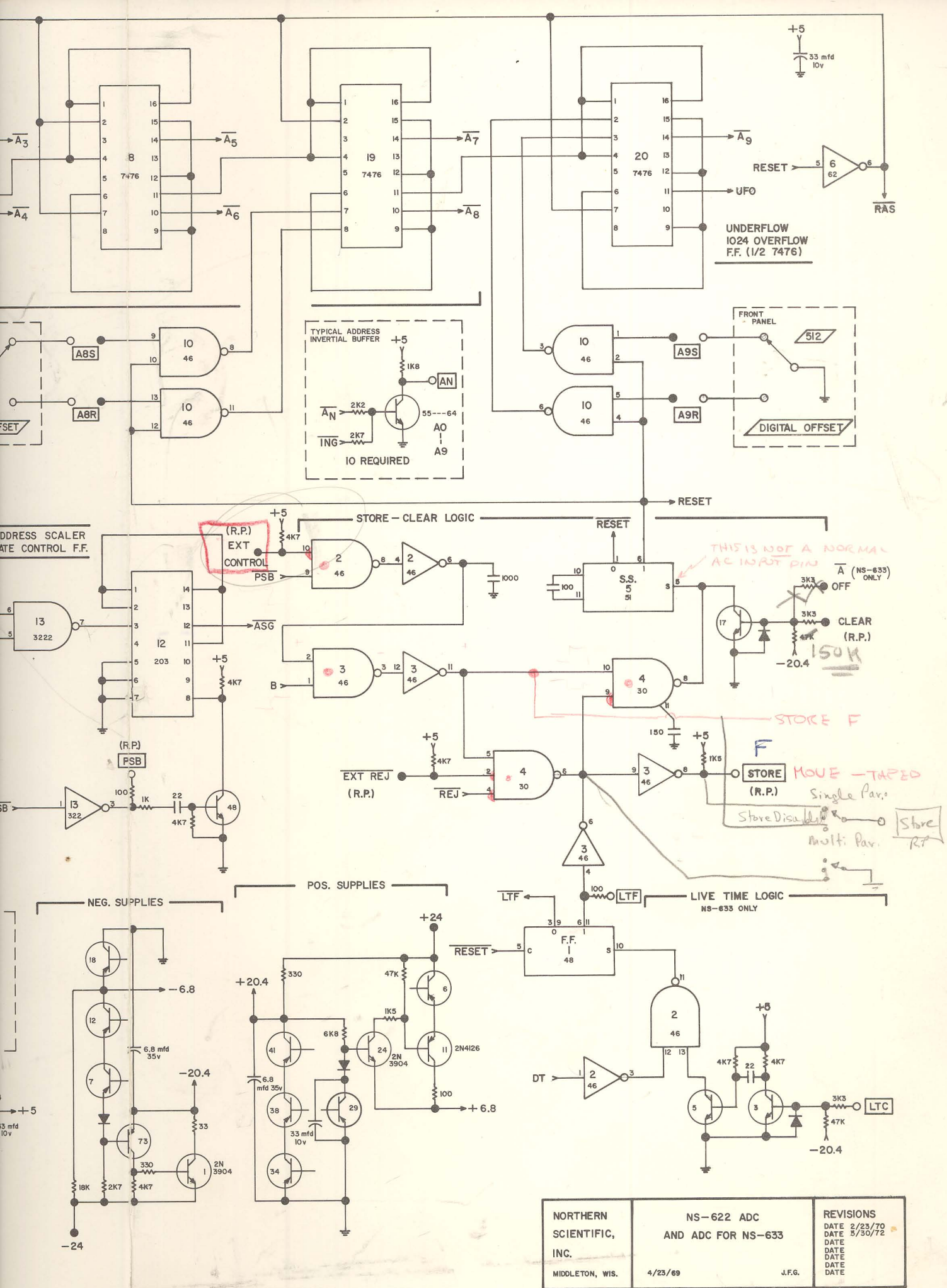


PHYSICAL LAYOUT OF TRANSISTORS


UPPER LEVEL DISCRIMINATOR
LOWER LEVEL DISCRIMINATOR
+6.8
+20.4
+5
4K7
24K
2N4126
ULD
3K9
10K
EXT ADJ
560K
33 mfd 10v
2K2
B
ULD BIAS
CA3018A
.01
18K
LGS
47K
LLD BIAS
LLD
1K21 M.F
33
FRONT PANEL
LINEAR GATE
-20.4
NEG. CLIPPER AND DRIVER
STRETCHER CKTRY
270K
2N5087
196K M.F.
15K
COUPLING
AC
DC
.012
ADC INPUT
470
-6.8
1K5 M.F.
22K
68K
12K
1000
LINEAR GATE CONTROL SOURCE
7420
ANALYZE
OFF
(NS-633 ONLY)
100K
46
45
44
CNC
COINC
ANTI COINC
ACN
2N 2914
5K6
EXT CONT
0.001mf
Vcc
74122
SET B
2.7K


SCRIMINATOR
+5
33 mfd 10v
4K7
2N4126
2K2
47K
.01
LLD BIAS
+6.8
1K21 M.F
2K
LLD
33
FRONT PANEL
B
7400
LLD+B
2K2
LLD RAPID DISCHARGE SWITCH
ULD F.F
68
4K7
330
2K2
ULD
LTF
ULD RAPID DISCHARGE SWITCH
RESET
RAS
ASG
470
330
680
10
50 MHz
27K
-20.4
LTF
PSB
B
1K
3K9
22
ING
PEAK DETECT MONOSTABLE
STRETCHER BUSY F.F.
PSB
ZL
REC
7420
15K
12K
1K5
3K3
22
2K2
4K7
22K
33
1000
560K
100 K
SET B
220K
560K
ACN
EXT REJ
(R.P.)
ADC BUSY F.F
B
(R.P.) V
RESET
6K8
ANTI COINC CKTRY
REC
S.S.
500
RESET
CSC
CONVERSION GAIN
1024
512
256
16K9
37K4
16K9 M.F.
CONV. GAIN SW.
FRONT PANEL
5K6
2N 2914
2.2K
-6.8
RUNDOWN CURRENT SWITCH
+24
+20.4
24K
6K8
2N4126
100
2N3904
10K
1K8
47
47K
100K
CA3018A
33 mfd 10v
ZERO BIAS
560K
18K
ZERO LEVEL
.001mf
Vcc
SET B
74122
2.7K
Vcc


10 BIT ADDRESS SCALER
50 MHz OSC
DEAD TIME & METER DRIVER CKTRY
ADDRESS SCALER GATE CONTROL F.F.
NEG. SUPPLIES
ZERO LEVEL
EXT GATE (R.P.)
STROBE
REJ
UFO
EXT ADJ
OFO
DIGITAL OFFSET
GROUP SIZE
NS-633 CONECTION
FRONT PANEL
NS-622 ONLY
% DEAD TIME
TRIM
ZERO LEVEL
ZERO BIAS
HELIPOT
HEAT SINK
LLD+B REC
RAS
CSC
DTM
PSB
RESET
ZL



NORTHERN SCIENTIFIC, INC. MIDDLETON, WIS.	NS-622 ADC AND ADC FOR NS-633 4/23/69 J.F.G.	REVISIONS DATE 2/23/70 DATE 5/30/72 DATE DATE DATE DATE DATE