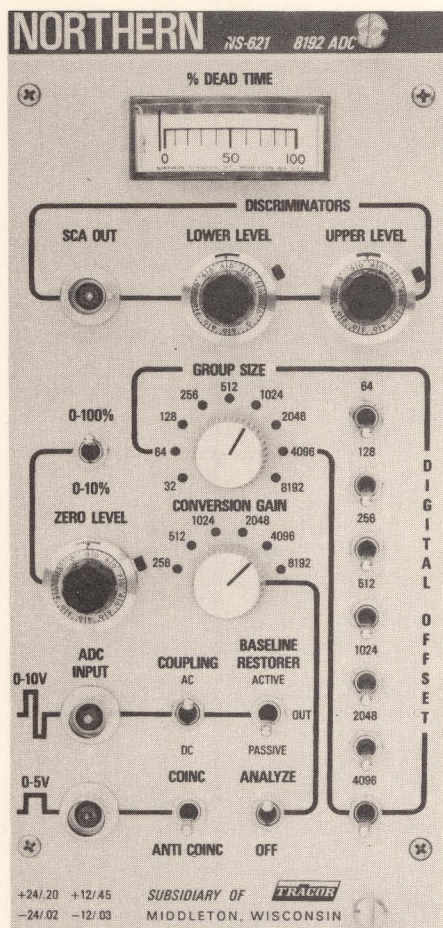


NS-621, 50 MHz and NS-623, 100 MHz

ANALOG TO DIGITAL CONVERTER



I N S T R U C T I O N M A N U A L

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I. INTRODUCTION

This manual covers both the NS-621 and NS-623 Analog-to-Digital Converters (ADC's). Both models are essentially identical from an operator's standpoint. Internally, both models use the same analog circuitry; only the integrated circuit types used in the converter logic are different. Logic input/output signals and connectors are identical to previous Northern Scientific modular ADC's and these models are interchangeable with older units.

As with previous Northern Scientific ADC's, the familiar Wilkinson conversion technique is employed. This method consists of charging a capacitor to the peak amplitude of an input pulse. At the conclusion of the charging process the capacitor is discharged linearly to zero. During the linear discharge a periodic pulse train (clock) is scaled into a binary scaler. The final binary address is directly proportional to the peak amplitude of the analog pulse since the scaling time is directly proportional to peak amplitude. The NS-621 uses a 50 MHz clock for address encoding and the NS-623 uses 100 MHz. Both scalers are 13-bit capacity (8192 channels).

Extensive use of the latest linear integrated circuits (IC's) is made in these designs for improved linearity and stability. In the NS-621 new Schottky-Clamped TTL are used for the high speed logic circuits. The NS-623 utilizes new Temperature-Compensated emitter-coupled logic (ECL) IC's in the high speed logic circuits. Both ADC's use a new adjustment-free logic scheme for the conversion process which provides reliable, stable performance with no special circuit precautions or component selection.

These ADC's operate from standard NIM supplies of $\pm 24V$ and $\pm 12V$. Internal regulators provide the required power supply voltages for the linear and digital IC types.

II. GENERAL SYSTEM DESCRIPTION

The essentials of a data acquisition system using one of these ADC's are shown in Figure 1. Incident radiation at the detector is converted to an electrical signal which is amplified and shaped before connecting to the ADC for conversion. The ADC accepts the analog signal and converts it into a binary address which is proportional to the peak amplitude of the input signal. At the end of conversion the address is transferred to a memory unit, either our NS-630 or NS-636 Memory Unit, or a computer which has been suitably interfaced. At the end of transfer the ADC is reset and allowed to perform another conversion.

In addition to the basic function of converting an analog input into a binary address, the ADC performs several logic functions which greatly simplify its adaptation to any memory system. Memory systems are available in a variety of sizes; the NS-636 Memory Unit ranges from 1024 to 8192 channels. Computers equipped with larger memories can utilize the full 13 bit (8192) address available from the ADC. Unless steps are taken to ensure ADC-to-Memory size compatibility storage of erroneous data (e.g., address overflows) will result. Several logic functions are included in the ADC's to preclude storage of erroneous data due to address overflow, underflow, partial pulses, etc. Because these logic functions ensure system-size compatibility only two logic signals are required to connect the ADC to any memory system. Of course, these two are in addition to the parallel connection of address data.

Figure 2 shows a timing diagram of the major signals involved in the conversion-data transfer-reset sequence. Signal **STORE** is generated approximately 1 uSec after conversion is complete. During the 1 uSec delay several tests are performed on the address: overflow, underflow (when using digital zero offset), and channel 0 (reserved for live-time storage). **STORE** is generated only if the address passes the acceptance tests performed, and then remains with the address data until a **CLEAR** is sent to the ADC from the memory unit. **CLEAR** is normally generated

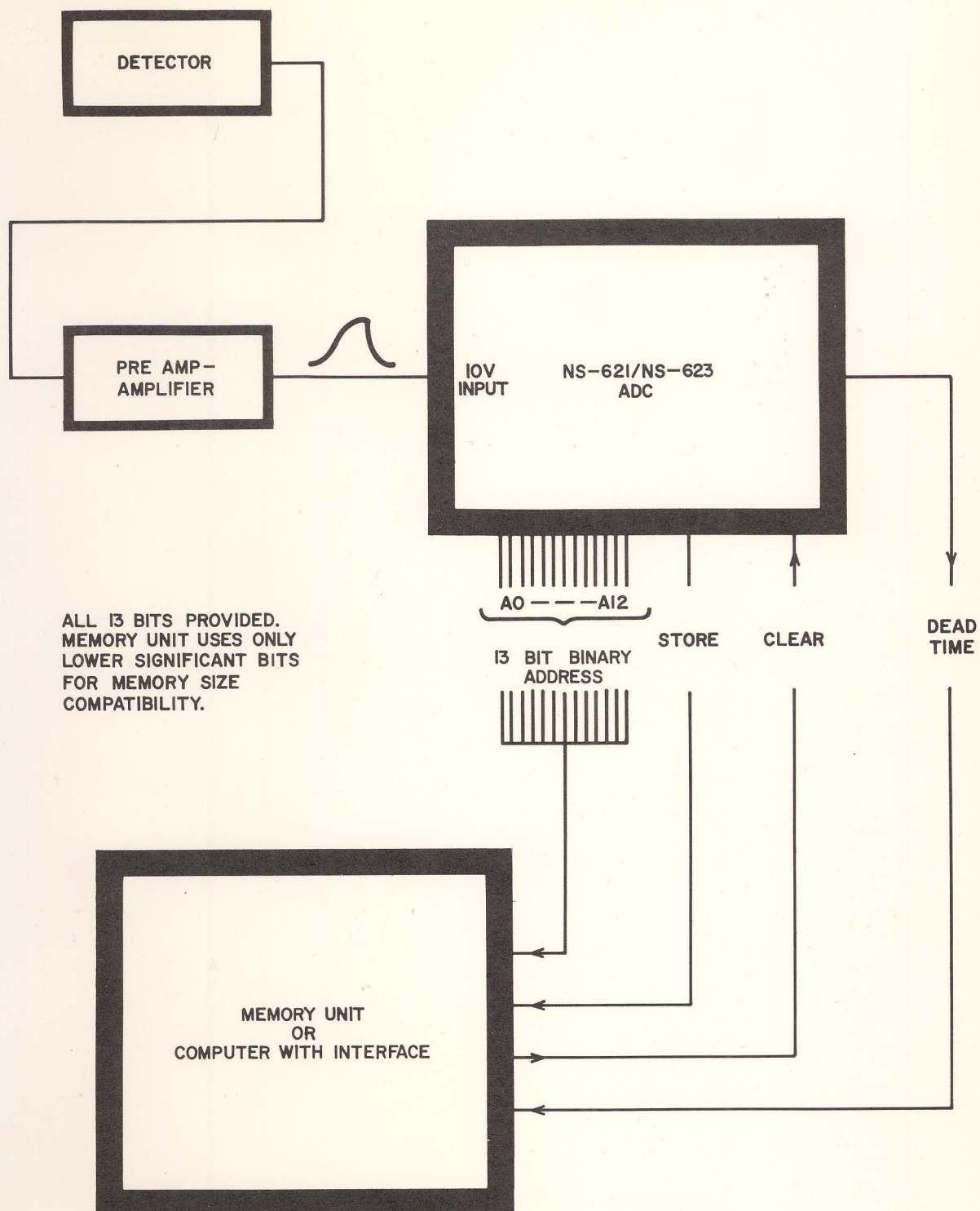
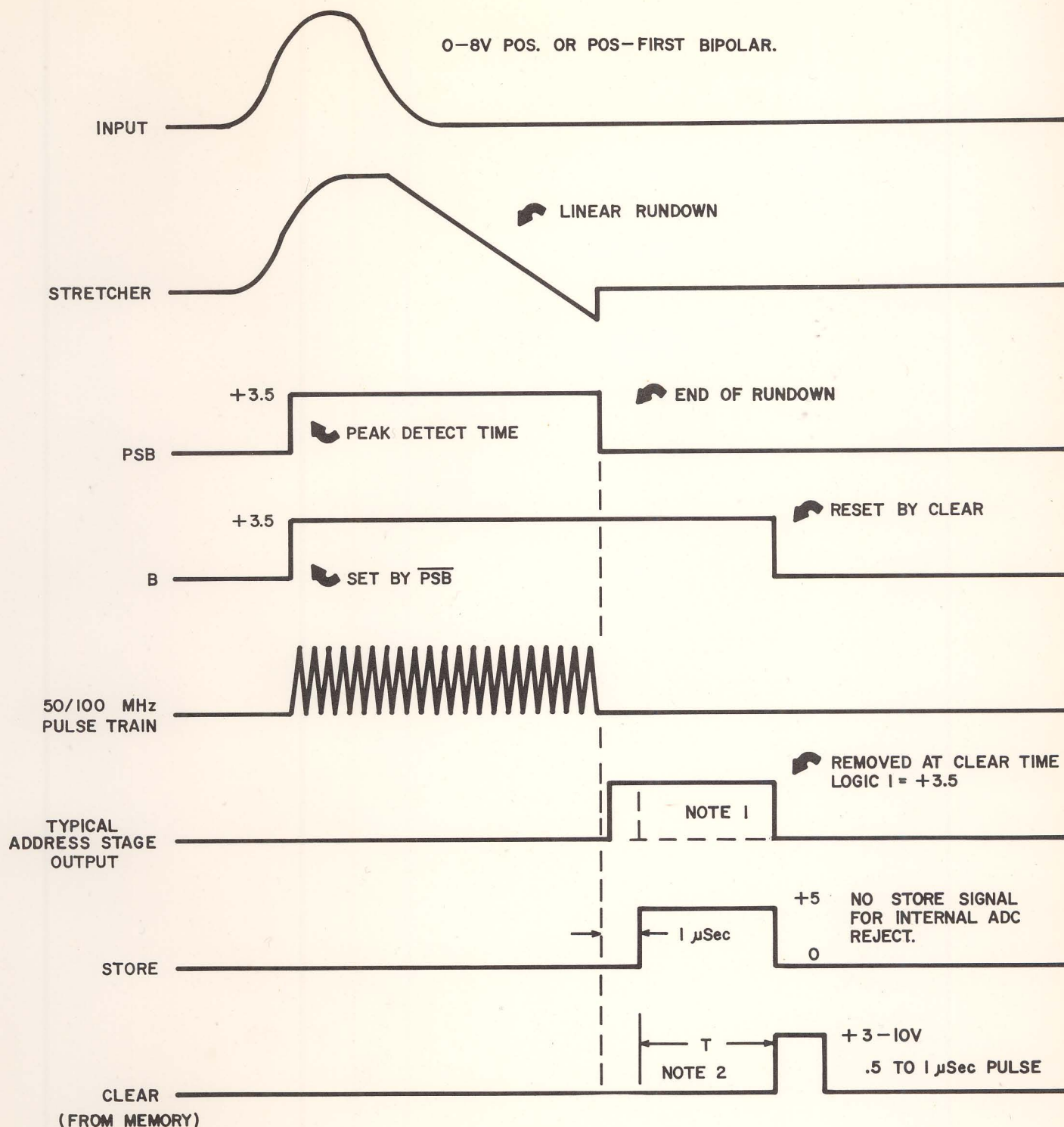


FIG. 1
BLOCK DIAGRAM OF SIMPLIFIED SYSTEM



NOTE 1
ADDRESS OUTPUT RETURNS TO 0V IN 1 μSec UNDER INTERNAL REJECT CONDITIONS.

NOTE 2
TIME T IS DETERMINED BY MEMORY UNIT OR COMPUTER. ADDRESS AND STORE REMAIN UNTIL CLEAR IS RECEIVED BY ADC.

FIG. 2
ADC TIMING

at the end of data transfer to the memory's input register, but there is no restriction on timing. Multiplexing of ADC's or other time-sharing operation of the computer/memory may preclude immediate response to a STORE signal. The address and STORE will remain until the memory is available to transfer data and generate the requisite CLEAR to reset the ADC.

If the generated address fails the acceptance tests performed at the end of conversion a STORE is inhibited. An internally generated clear signal resets the ADC immediately, removing the address. It is important that any interface logic for computer applications remain unresponsive to the address lines unless accompanied by a STORE signal. Under "reject" condition the address will be presented for approximately 1 uSec and then removed without any STORE generated or CLEAR required for ADC reset.

Several input/output signals are provided in the standard ADC which are not required by a simple, straightforward, data acquisition system. Operation of multiparameter systems, multiplex operation, or more complex computer systems will require these signals, however. Refer to the section describing Major Signals and Their Functions for more information.

III. OPERATING CONTROLS AND SPECIFICATIONS

A. INPUTS

1. ADC Analog Input

- a. Range: 0-10V. Full scale with respect to the conversion gain is 8V. The additional 25% over range can be utilized by offsetting the zero intercept by 25%, extending ADC resolution to its maximum, one part in 10,000.
- b. Polarity: Positive unipolar or positive-first bipolar.
- c. Rise Time: .1 to 5 uSec.
- d. Fall Time: .1 to 10 uSec; up to 30 uSec is permissible but the linearity of the lower 5% of the range will be degraded.
- e. Input Impedance: 1Kohm, DC connected to gnd.
- f. Coupling: Switch selected, AC (capacitive) or DC (direct).

2. COINC Input

- a. Positive 5V signal performs either coincidence or anti coincidence function depending on position of COINC-ANTI COINC. switch.
- b. Input Impedance: 3.3Kohm, DC connected.
- c. Refer to section on Operation for timing requirements.

B. DISCRIMINATORS

1. LOWER LEVEL

- a. Function: Sets lower limit on signals to be converted by ADC. Signals below the lower level add no dead time to system operation.
- b. Range: 0-100% of the full-scale conversion as set by the CONVERSION GAIN switch.
- c. Coupling: DC to ADC input (ADC in turn may be either AC or DC coupled depending on position of COUPLING switch).
- d. Stability: Maximum 100 ppm/ $^{\circ}$ C or 24 hours at constant temperature, typically 50 ppm.

2. UPPER LEVEL

- a. Function: Sets upper limit on signals to be converted by ADC. Dead time for signals above the upper limit is equal to signal time above the lower level threshold.

- b. Range: 5 to 125% of full-scale conversion.
- c. Coupling: Same as lower level discriminator.
- d. Stability: Max 100 ppm/ $^{\circ}$ C or 24 hours, typically 50 ppm.

C. ZERO LEVEL CONTROLS

1. Analog ZERO LEVEL

- a. Function: Adjusts the level of the analog input which corresponds to channel 0 (extrapolated).
- b. Range: -0.5 to 10% or 100%, switch selected. Range refers to extrapolated zero intercept of a plot of channel number versus analog input amplitude.
- c. Stability: 100 ppm/ $^{\circ}$ C max, 20 ppm/ $^{\circ}$ C typical; 100 ppm/24 hours at constant temperature; referred to full scale analog input.

2. DIGITAL ZERO OFFSET

- a. Function: Digitally subtracts selected offset from converted address.
- b. Positions: 0, 64, 128, 8127 channels.
- c. ADC Dead Time: Independent of digital offset for a given analog input.
- d. Remarks: Underflow conversions (addresses less than 0 after offset subtraction) are rejected within the ADC; no STORE is generated and ADC is internally reset.

D. CONVERSION GAIN

1. SWITCH

- a. Function: Sets the number of channels corresponding to full scale analog input of 8V. Switch selects magnitude of current effecting linear rundown of stretcher capacitor.
- b. Positions: 256, 512, 1024, 2048, 4096, 8192 channels per 8V input.

- 2. Stability: 100 ppm/ $^{\circ}$ C max, 50 ppm/ $^{\circ}$ C typical; 100 ppm/24 hours at constant temperature, referred to full scale analog input.

E. BASELINE RESTORERS

1. Passive
 - a. Type: Robinson.
 - b. Inputs: Unipolar or bipolar acceptable.
 - c. Recovery Time: 50 uSec to .05%, 150 uSec to .01%.
2. Active
 - a. Type: Operational Amp with diode feedback.
 - b. Inputs: Positive unipolar only.
 - c. Recovery Time: 3 uSec to .01%.
3. OUT (COUPLING sw. must be in DC position)
 - a. Restorer: None.
 - b. Function: Provided for DC connection of ADC for external baseline restorers.

F. GROUP SIZE Switch

1. Function: Digitally sets upper limit on channel number to be stored in memory unit. Addresses greater than selected number are automatically rejected within the ADC.
2. Range: 32 to 8192 channels in binary increments.
3. Remarks: Reject occurs when group size overflow is sensed after conversion. When digital offset is used, overflow is sensed on group size above channel zero.

G. ANALYZE OFF Switch

1. ANALYZE Position: Normal operating position.
2. OFF Position: ADC is in DC reset condition.

H. POWER REQUIREMENTS

1. +24: 20 mA.
2. -24: 20 mA.
3. +12: 450 mA.
4. -12: 30 mA.

I. REAR PANEL CONNECTORS/SIGNALS

1. Memory Unit
 - a. Size: 26 pin Amp.

b. Signals: Address, STORE, CLEAR, DT, plus several control input/outputs.

c. Levels: Logic one = +3V

Logic zero = 0V

2. Stabilizer/

a. Size: 26 pin Amp.

b. Signals: None in standard unit. Units equipped with Stabilizer have ADC address, ADC busy, and correction signals in this connector.

IV. OPERATION

A. General

This section covers operation of the ADC's and the NS-630 or NS-636 Memory Units in pulse height analysis. Operation of the combined units is not unlike the conventional pulse height analyzer found in a single package. The discussion here will pertain to the ADC connected to a Northern Scientific Memory Unit but the front-panel adjustments of the ADC are essentially the same when operating with a computer for data storage.

B. Initial Set Up and Operation with The Memory Unit

Listed below are the switch positions and signal requirements which will ensure proper operation of the ADC and the Memory Unit after initial connection. It is assumed that the Memory Unit has been adjusted for pulse height analysis mode of operation. If there is any question about proper switch positions for this mode, refer to the respective manual. This set up is for simple, straightforward nuclear pulse height analysis and does not utilize the full capabilities of the system. Sections which follow cover the controls individually so that maximum acquisition efficiency can be achieved under more complex modes of operation.

1. Turn off the power on all units.
2. Connect the ADC to the memory unit using the cable supplied.
3. Connect the signal source to the ADC BNC input labeled ADC INPUT. Signal must be positive unipolar or positive first bipolar. Set the coupling switch on the ADC front panel to AC. Set the baseline restorer to PASSIVE.
4. Set COINC/ANTI COINC switch to ANTI COINC.
5. Set ULD full clockwise.
6. Set LLD at 10 dial divisions position.
7. Set ZERO LEVEL at 100 small dial divisions and the toggle switch in the 0-10% position.
8. Set CONVERSION GAIN to the switch position which corresponds to the memory unit size available.
9. Set the GROUP SIZE switch to the same position as the CONVERSION GAIN switch.

10. Place all DIGITAL OFFSET switches off (down).
11. Now energize the Memory Unit and the power supply in the NIM bin.
12. Place the ANALYZE OFF switch on the ADC to the ANALYZE position.
13. Control system with the START MEASURE and STOP pushbuttons on the Memory Unit. The above procedure sets up the ADC for analysis of the entire range from threshold to full scale. The ZERO LEVEL is set close to 0-0 intercept and the lower level discriminator is set for approximately maximum sensitivity. Either the ADC ANALYZE OFF switch or the memory START MEASURE and STOP pushbuttons can be used to control analysis. The controls on the memory unit are preferred, however, because they also control operation of the clock/live timer in the memory unit. Accurate live time can be realized only when the memory unit pushbuttons are used to control analysis.

C. Lower and Upper Level Discriminators

The upper and lower level discriminators are connected directly to the ADC input and are used to bracket the range of analog signals to be converted by the ADC. Internally, both discriminators are directly coupled to the ADC input. Also, the range of the lower level discriminator extends below 0 volts so that the full CCW position of the lower level discriminator Helipot will cause the discriminator to be triggered 100% of the time. This is indicated by 100% deflection on the dead time meter with no input signal. This is an improper operating point for the ADC, but this point was designed to accommodate small DC offsets of the input signal baseline when external restorers and DC input connection are used. The lower level discriminator is set for maximum sensitivity at the point where the dead time meter just drops from 100% back to zero with no input signal. Operation at maximum sensitivity should be avoided, however, because any small drift in the system may cause the lower level discriminator to trigger 100% of the time. The

maximum sensitivity point should be found experimentally and then the Helipot should be adjusted to approximately 5 small dial divisions above this point.

The upper level discriminator inhibits conversion of any signal above the upper level threshold. ADC dead time can be reduced considerably by adjusting the upper level threshold to be just above the maximum signal of interest. At low count rates this adjustment is not important but at high count rates considerable system dead time can be eliminated by proper setting of this control.

The upper and lower level discriminators should be adjusted to bracket a region of interest when using digital zero offset. With the discriminator set to convert the entire full scale spectrum considerable dead time is used in converting signals which are later rejected by underflow and overflow tests performed after conversion. After the region of interest is once selected with the DIGITAL OFFSET and GROUP SIZE controls, the upper and lower level thresholds should be adjusted to fall just outside the region of interest which has been bracketed digitally. Operation in this manner provides double selection of the region of interest. The discriminators provide analog selection and reduce ADC dead time while the GROUP SIZE/DIGITAL OFFSET controls provide for logic functions which precisely select the region to be stored in the memory unit.

D. Zero Level Adjustment

Zero level is defined as that analog input level which corresponds to channel zero (extrapolated) in the stored analysis. Using the front panel ZERO LEVEL Helipot any analog input from zero through 8 volts can be adjusted to correspond to channel zero in the memory unit. The ZERO LEVEL control is analogous to the bias level on a biased amplifier; signals below the zero level are not converted by the ADC just as signals below bias level are not amplified. As the ZERO LEVEL control is turned clockwise the channel number for a given energy is reduced. This has the effect of shifting the entire spectrum to lower channels when viewed from channel

zero through full scale. From the standpoint of the spectrum stored in the memory unit there is no difference in the results obtained using the analog ZERO LEVEL control and the DIGITAL OFFSET switches. The main difference in the two, however, is that the analog zero level control does reduce the amount of dead time required for a given conversion. The digital offset switches operate on the address after conversion. That is, for a given energy, the conversion time is independent of the digital offset switch positions. Using analog offset, however, the dead time is inversely proportional to the magnitude of offset. From a dead time standpoint only, analog adjustment is preferred over digital offset of zero level. However, digital offset does provide a convenient means of shifting the spectrum by a binary fraction of the full scale conversion gain. Offset, conversion gain, and memory group sizes are all in binary increments. The speed of the ADC is such that conversion times are low even with digital offset. For medium count rates the increased dead time is not significant, especially if the lower and upper level discriminators are adjusted properly to bracket the region-of-interest selected.

One final word on the analog zero level control at this time is in order. While the analog zero level control performs the same function as the bias level on a biased amplifier, the disadvantages associated with biased amplifiers are not found in the ADC. It is normal for a biased amplifier to bias off the lower portion of the input signal with a resultant change in pulse shape for signals above the bias level. These ADC's, however, employ a different design technique whereby the signal as seen by the pulse stretcher is independent of the ZERO LEVEL control setting. The significant advantages of this technique are that the ADC linearity is independent of zero level adjustment, and also the ADC stability is not dependent on zero level setting. The next section on System and Circuit Design provides details on how this is accomplished.

E. Conversion Gain

Front panel switch positions on the CONVERSION GAIN switch indicate the address generated for nominal 8 volt analog input signal. This switch

then effectively adjusts the resolution of the ADC since the number of discrete channels for a given analog input is a function of this switch position. Internally this switch adjusts the magnitude of the rundown current which effects linear discharge of the stretcher capacitor. If the entire energy range from zero to full scale is to be analyzed, the CONVERSION GAIN switch is set to the number which corresponds to the size of the available memory. The ADC may be operated at higher resolution settings than this but only by viewing a smaller portion of the entire spectrum. For example, if a 1024 channel memory is the size in use then in order to view the entire voltage range from zero to 8 volts the conversion gain must be operated in the 1024 position. The conversion gain may be operated at a setting of 8192 however if only one-eighth of the spectrum is to be stored. The CONVERSION GAIN switch is adjusted first for the resolution desired; then either the ZERO LEVEL control or DIGITAL OFFSET is used to shift the region of interest into channels 0 through 1024. CONVERSION GAIN should be adjusted to provide the resolution desired over the dynamic range required by the region of interest.

F. GROUP SIZE Switch

The GROUP SIZE switch is essentially a digital upper level discriminator adjustment and sets the maximum address which will be transferred to the memory unit. This is accomplished by testing each conversion for an address greater than the number selected on the front panel GROUP SIZE switch. Addresses above the number selected cause STORE to be inhibited and the ADC to be reset internally. The overflow tests are performed after conversion so that digital offset is subtracted before the tests are performed. This means that the group size as selected refers to the number of channels above zero. Conversions below channel zero are also rejected when underflow is sensed in the ADC.

In normal single parameter analysis the GROUP SIZE switch position corresponds to the memory size available. If the NS-630 or NS-636 is being used at something less than full memory (quarters, halves), the switch

position should correspond to the size of the memory group being used. Switch positions corresponding to very small group sizes, 32 and 64 channels for example, are provided for two parameter analysis in a 32 x 32 or 64 x 64 configuration of two ADC's. Where only 32 or 64 channels along one axis are being used, digital offset will most probably be employed. The DIGITAL OFFSET and GROUP SIZE switches provide for selecting a 32 or 64 channel region of interest with the ADC operating at much higher resolution.

G. Baseline Restorers

A choice of either active or passive baseline restoration is provided in the ADC. If the ADC is to be operated with external baseline restoration the COUPLING can be switched to DC and both internal restorers can be switched out. The OUT position is also used when the ADC is converting DC or slow AC signals. One of the restorers must be switched in with the COUPLING switch in the AC position. The choice of baseline restorers under normal operating conditions is left to the user with the following guidelines. For bipolar pulses the passive restorer must be used along with AC coupling. For unipolar input pulses at low count rates the passive restorer will yield a somewhat higher resolution than the active. In general, because the passive restorer will accept bipolar inputs, proper pole-zero, or delay line clipping adjustments are not so critical as for the active restorer. The disadvantages of the passive restorer are as follows. First, the recovery to true baseline for a well-adjusted unipolar input is considerably longer than with the active baseline restorer. Second, the input impedance at the ADC input is a function of signal level. This is characteristic of passive restorers and is due to the non-linear diode turn-off. In these ADC's the impedance change introduces a small zero level shift and differential non linearity in the lower 3% of the analog input range. In many applications this small non linearity is offset by the improved resolution afforded by baseline restoration. The degree of non linearity is a function of both pulse shape and pulse duration. The coupling capacitor as installed at the factory is a compromise between best linearity on the low end and fastest recovery. The recovery time of the restorer can be improved by reducing the capacitor from its

normal .022 microfarad down to .005 or even .001 microfarad. Reducing the capacitor size, however, will make the low end non linearity and zero level shift more pronounced. In fact, the non linearity may extend into the lower 5% of the range. For a given pulse shape the non linearity will remain constant and repeatable so that differential linearity checks could be performed and subsequent correction factors applied to the analyses.

The active baseline restorer employs an operational amplifier with diode-connected feedback at the ADC input. The impedance to positive signals is very high while the impedance to negative signals is very low due to the operational amplifier. Because of the high impedance to positive inputs there is very little charge gained on the coupling capacitor during the normal pulse input. When the signal returns to zero the charge gained is quickly discharged through the low impedance at the op. amp. input. The impedance ratio is such that the charge gained on the positive input is completely lost within three microseconds after the input pulse returns to baseline. While the active restorer provides for very rapid discharge of the capacitor and return of the ADC input to zero, it has some disadvantages when operating with normal nuclear pulse amplifier outputs. First, the input signal must return to zero very accurately because any excursion below the baseline will cause the capacitor to gain an erroneous charge very quickly. Second, amplifier noise is not unipolar in nature, that is, while the pulse out of the amplifier may be unipolar, the noise makes excursions both positive and negative with respect to the baseline. The baseline restorer will keep the coupling capacitor charged to the average negative excursion made by system noise. The net effect is that the baseline itself is determined by noise, and in the final analysis the resolution of the system may be poorer than if the passive baseline restorer were used. Under high count rate conditions the active baseline restorer will definitely improve the resolution over what will be achieved with a passive restorer. At some count rate there is a crossover between the loss of resolution due to the baseline not returning to zero and the average charge maintained due to

amplifier noise. In general, the active baseline restorer should be used only with amplifiers equipped with pole zero cancellation so that the output pulse returns to the baseline very closely. The characteristics of the active restorer are such that it does not introduce the non linearity associated with the passive restorer in the lower 3 to 5% of the input range. After careful adjustment of the amplifier, the best operating position of the restorer switch should be determined experimentally. At low count rates there is no question but that the passive restorer will be preferred over active. At medium count rates with carefully adjusted amplifier there may be some advantage to the active restorer. At high count rates the active restorer will definitely prove superior to the passive in high resolution systems, after careful pole zero cancellation adjustments.

H. Coincidence, Anti-Coincidence Operation

A front panel BNC is provided on the ADC for acceptance of a 0-5V signal for coincidence or anti-coincidence operation of the ADC. A toggle switch next to the BNC controls the operating mode. Connection is direct so that this input may be used as an auxiliary start-stop control of the ADC using a logic signal. Circuitry is such that this input can also be used for time coincidence or anti-coincidence operation of the ADC.

Requirements for pulse coincidence operation are as follows. With the toggle switch in the COINC position the ADC is inhibited from accepting any analog input for conversion. This is accomplished by holding a linear gate at the stretcher input closed. Analog input signals accompanied by a positive 5 volt pulse will be accepted by the ADC for conversion. All other logic functions, both analog and digital in nature, will still apply to the subsequent conversion. The lower and upper level discriminators, zero level controls, digital offset and group size functions operate in normal fashion so that acceptance of a signal by the ADC does not necessarily mean it will be transferred to memory. Timing requirements for the application of the 5 volt coincidence signal are fairly straightforward and non critical. Pulse rise time for the coincidence input should be somewhere in the range between 50 and 250 nanoseconds. The coincidence pulse must arrive at the input no

later than one-half microsecond before the analog input signal reaches its peak amplitude. There is no delay line in the ADC so that an external delay line may be necessary to allow time for the external coincidence circuitry to make its decision. Application of the coincidence input opens the ADC linear gate and the signal passes through the open gate and connects to the stretcher circuitry. When the signal reaches peak amplitude the peak detector is triggered. At peak detect time the linear gate is closed even if the coincidence input remains.

The duration of the coincidence input must be long enough to hold the linear gate open until it is closed by the ADC at peak detect time. The suggested pulse duration is one half microsecond greater than baseline-to-peak time of the analog input signal.

During the conversion process the ADC busy signal keeps the linear gate closed and additional coincidence inputs have no effect on the conversion process. Once the ADC is reset, either by internal reject of a conversion or at the time a CLEAR signal is received from the memory unit, the coincidence input is again operative.

Pulse requirements for anti-coincidence operation of the ADC are less stringent than for the coincidence mode. To inhibit an analog input, the anti-coincidence input must be +5V at peak detect time and for approximately 400 nanoseconds thereafter. Pulse durations longer than the 400 nanosecond minimum, or pulses applied before peak detect time, have no effect on operation. Pulses approximately two microsecond duration applied at the same time the analog signal is applied are suggested when analyzing one to two microsecond input pulses. The dead time for an analog input which is inhibited is equal to the analog input time above the lower level discriminator threshold. The COINC input can be used as an auxiliary analyze-stop control for the ADC. The anti-coincidence input signal is not included in ADC dead time however, so that accurate live time operation cannot be realized if this mode of operation is used to control analysis.

I. Analyzing DC or Slow AC Signals

Either DC or slow AC signals can be analyzed by the ADC by sampling

at its input. The following front panel switch positions should be used for operating in this mode. Place the COUPLING switch to the DC position, the BASELINE RESTORER to the OUT position and the COINC/ANTI COINC switch to the COINC position. A positive 5 volt pulse source is required to strobe the ADC input. The pulse duration should be a minimum of one microsecond and a maximum of 4 microseconds. Operation is as follows. With the COINC/ANTI COINC switch in the COINC position the linear gate of the ADC is held closed. The DC applied at the front panel is connected to the linear gate but is blocked. Application of the 5 volt, one microsecond pulse at the coincidence input opens the linear gate for one microsecond. This effectively generates a one microsecond pulse at the linear gate with a peak amplitude equal to the DC input. The ADC converts the one microsecond pulse in identical fashion to normal pulse inputs. All front panel controls, both analog and digital, are operative in this mode.

For analysis of slow AC signals the ADC front panel controls are set up the same as for DC signals. The ADC operated in this mode will convert only the positive portion of the AC input. Internal circuitry clips the negative portion of any input and coincidence pulses applied will not produce conversions. If analysis of the entire signal is required, the AC signal must be superimposed on a DC reference such that the input to the ADC is always positive with respect to ground. As with DC inputs, all front panel controls remain operative so that the discriminators, zero level and region of interest selection controls can be used to bracket a region of interest. Once the ADC has accepted an input for analysis, the busy signal holds the linear gate closed until the ADC is ready to accept another pulse. Application of additional coincident pulses will not affect the conversion of the accepted input.

V. SYSTEM AND CIRCUIT DESIGN

A. General

This section provides detailed coverage of the ADC logic circuits, signal timing and circuit design. Block diagrams and timing diagrams are provided to facilitate explanation of the basic operation. Transistor and integrated circuit numbers are used on the block diagram to simplify cross referencing of logic blocks to the circuits. Each schematic is accompanied by a physical layout which shows the location of the transistors and integrated circuits with their numbers. A section just prior to the schematics contains general notes which explain the symbols used on our schematics and block diagrams. A few minutes spent studying this section will greatly simplify understanding the various signal sources and loads throughout the unit. The circuitry contained on the ADC boards uses two schematics to show all circuitry. In addition there is another schematic showing all front panel controls and switches. Where practicable, the front panel controls, sometimes simplified, are resown on the board schematics to further aid circuit understanding. Finally, a list of major signals and their functions is included to cover the signals which may be omitted in the text. This list explains the function of all major signals found in the NS-621/623.

In the discussion of the system and circuit design which follows no attempt was made to discuss the block diagram and schematics separately. Rather, the block diagram and systems are discussed in detail and reference is made to individual circuits only where their complexity warrants further discussion. The system is separated into two sections to simplify explanation. The first section will deal with the basic component parts of the ADC. The second section will deal primarily with logic functions which occur after the conversion process and involve the store and reset circuitry of the ADC.

B. The Basic ADC Circuitry

1. ADC Input Circuits

Refer to the block diagram, Figure 3 and the A Board schematic for the circuits covered in this section. Figure 4 is a timing diagram of the analog and logic signals for the basic ADC.

The signal connected to the ADC INPUT BNC is attenuated by a factor of two by two metal film precision resistors mounted on the front panel. This means that all the analog circuitry in the ADC operates on a 0 to 5 volt signal rather than the 0 to 10 volt input. The resistor values may be changed by the user if he desires some input range other than 0 to 10 volts. If the resistors are changed to give different attenuation ratios the Thevenin source impedance should be below 500 ohms. The junction of the attenuating resistors connects to the coupling switch where either capacitive or direct coupling is selected. From there the signal connects directly to the ADC input and to the baseline restorer selection switch. The center-off position of this switch disconnects both baseline restorers and leaves the ADC input free. With no baseline restorer connected the coupling switch must be in the DC position to provide a DC return for the ADC input circuitry.

The passive baseline restorer is composed of two back-to-back diodes with one referenced to ground. A screwdriver adjustment is provided to adjust diode drops to be exactly equal such that with the baseline restorer connected the ADC reference is at ground. The active baseline restorer is composed of an operational amplifier, transistors 7 and 22. Again, a screwdriver adjustment is provided to adjust the baseline reference to be ground. The active baseline restorer operates in the following manner. Pin number 9 of transistor 7 is the input of a darlington differential transistor pair, and is the inverting input of an operational amplifier whose feedback loop is closed by the diode between the collector of transistor 22 and pin 9. In the

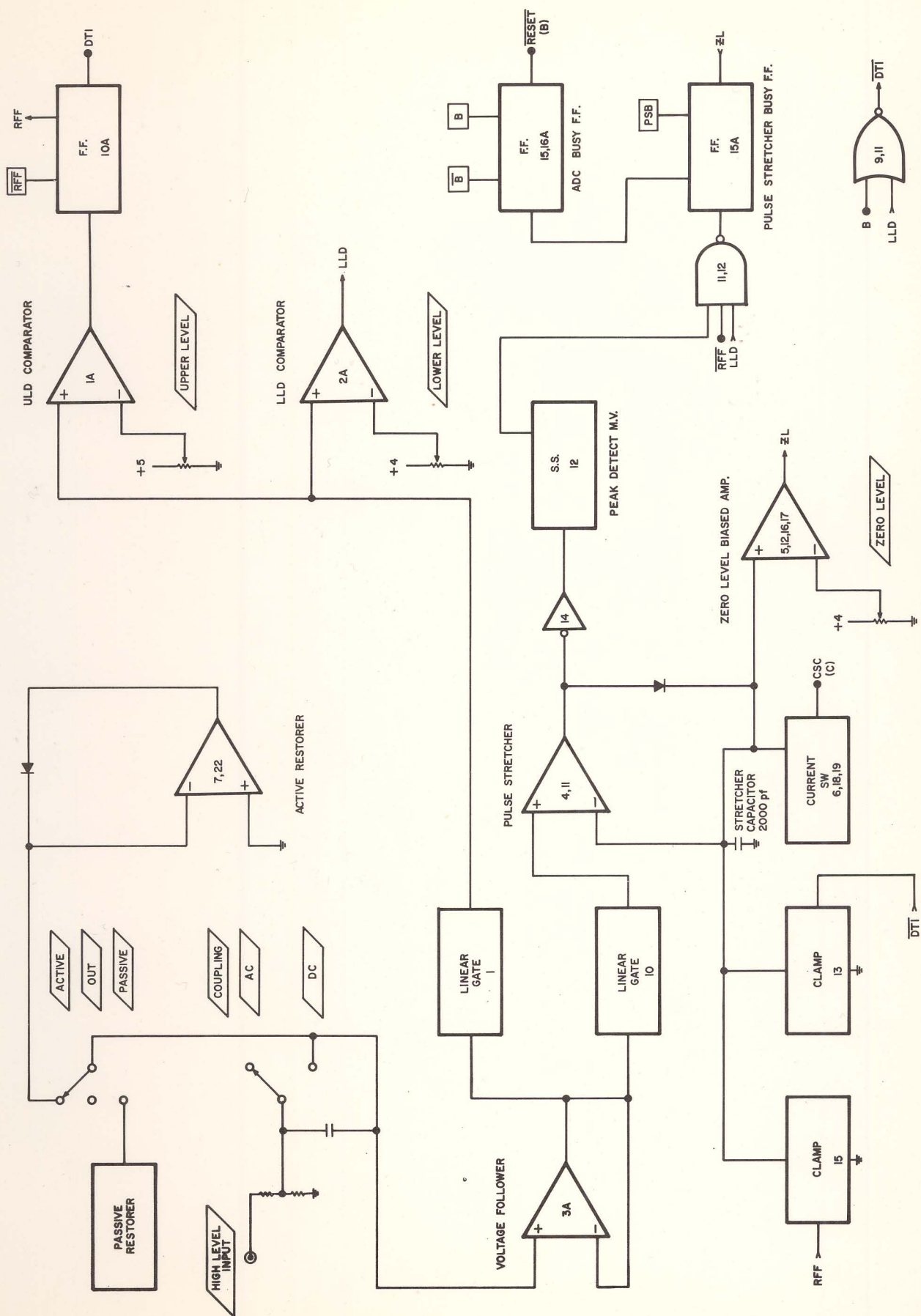


FIG. 3
BLOCK DIAGRAM OF A BOARD CIRCUITS

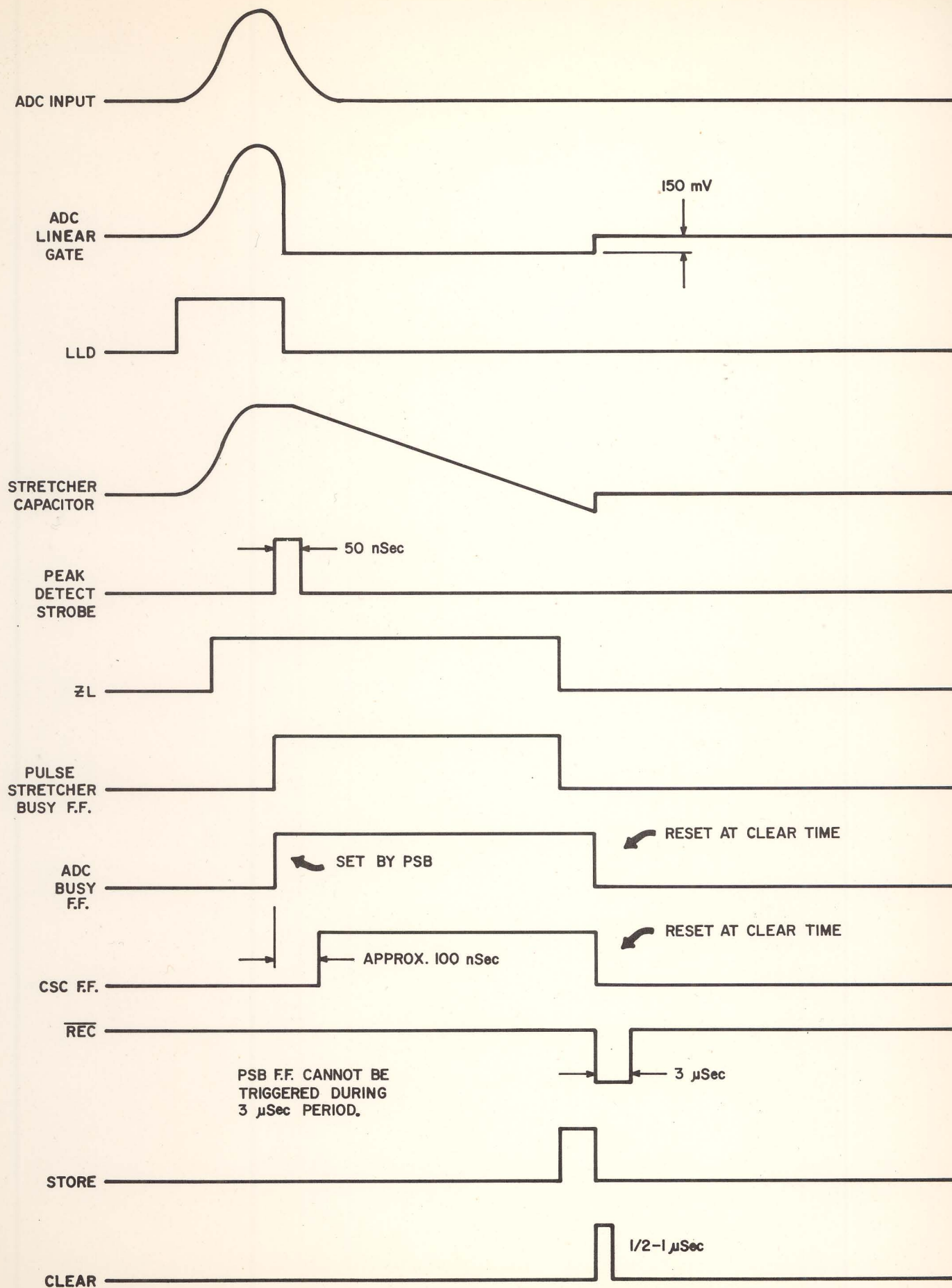


FIG. 4
TIMING FOR A BOARD SIGNALS WITH RESPECT TO STORE-CLEAR

quiescent state, the only current through the diode is the base current into pin 9, approximately 1/2 microamp. Positive input signals are inverted by the restorer and the collector of transistor 22 swings negative, turning off the diode which closed the feedback loop. For positive inputs the amplifier operates essentially open loop and the input impedance at pin 9 is very high because of the darlington connected input transistors. When the input signal returns to zero and tries to swing negative the amplifier amplifies this negative excursion and the positive output at 22 collector causes the diode to conduct and clamp pin 9 at ground. The coupling capacitor at the ADC input discharges very rapidly through the diode. The impedance ratios and time constants are such that the capacitor is completely discharged in approximately 3 microseconds.

An LM-310 operational amplifier forms the input circuitry to the ADC. This IC type is a gain-of-one voltage follower by design. The output of this stage connects to both the stretcher/peak-detector circuitry and to the lower and upper level discriminators. Each signal path is equipped with a linear gate, transistor 1 for the discriminators, and transistor 10 for the ADC's stretcher.

2. Stretcher/Peak Detector Circuitry

Another operational amplifier composed of transistor 4 and 11 form the pulse stretcher for the ADC. The amplifier is operated as a gain-of-one voltage follower with the circuit modified to perform pulse stretching. The incoming positive pulse is applied to pin 9 of transistor 4. The amplifier loop is closed by means of a diode from the collector of 11 to the inverting input of the amplifier at pin 3 of transistor 4. The stretcher capacitors are also located at pin 3. As the input signal goes positive the diode conducts and pin 3 follows the input signal up to peak amplitude. As the signal passes through peak amplitude pin 3 remains at peak voltage due to the stretcher capacitors. The loop now opens because of the polarity reversal at the diode closing the loop. The collector of 11 swings negative with respect to ground

and turns on transistor 14 which amplifies the negative signal. The amplified signal at the collector of 14 is used to trigger the peak-detect monostable found in IC12A. The output at pin 13 of IC12A is used as a peak-detect strobe. The strobe is ANDed with LLD in IC11A. The output at pin 8 ($\overline{\text{PDS}}$) triggers the single channel monostable for signals above the lower level discriminator threshold. The peak-detect-strobe signal (PDS) at IC14A pin 3 connects to a NAND gate, IC14A pin 4, where ADC conversions are controlled by mode signal $\overline{\text{OFF}}$ at pin 5 of IC14A. Signal $\overline{\text{OFF}}$ is at zero when the front panel ANALYZE-OFF switch is in the OFF position so that no ADC conversions are triggered by logic circuitry which follows this gate.

Pin 6 of IC14A will switch negative for approximately 50 nanoseconds and set the pulse stretcher busy flip-flop composed of two two-input NAND gates found in IC15A. Signals $\overline{\text{PSB}}$ and PSB, the outputs of the flip-flop, are used to trigger logic circuits which effect a conversion. To prevent the start of conversion the peak-detect strobe is inhibited from triggering the PSB flip-flop. At this time it is important to understand the relationship of the peak detect strobe with respect to the pulse stretcher, and the function of the pulse stretcher busy flip-flop. A peak detect strobe represents the first logic signal derived from the analog input. The remaining logic circuitry can be treated with logic description rather than circuit description.

Several other circuits are connected to the stretcher capacitors and these circuits will be discussed later.

3. The Lower Level Discriminator

The output signal from the input voltage follower connects to the lower level discriminator through a series resistor. Transistor 1 acts as a linear gate at the discriminator inputs. The quiescent condition of the linear gate is with 1 turned off such that an analog input

is applied to both the lower and upper level discriminators. IC2A operates as a comparator with the positive analog signal compared with a positive bias at pin 3. The bias level is set by the front panel lower level discriminator Helipot. Signals above LLD BIAS generate a positive output which is coupled to IC9 for further amplification. Signal LLD connects to pin 12 of IC9A and generates the leading edge of DT1 when pin 12 goes positive. Signal DT1 also contains signal B which has been ORed with LLD in IC9A. DT1 is the major component of ADC dead time (due primarily to signal B, not LLD) which is used for live time correction. DT1 is inverted and the output $\overline{\text{DT1}}$ is at IC11A pin 6. $\overline{\text{DT1}}$ connects to the base of transistor 13 where it turns off the transistor when the lower level threshold is exceeded and keeps it off while the ADC is busy. Transistor 13 with the series 2.2K resistor in its collector acts as a shunt to rapidly discharge the stretcher capacitors. All signals are connected to the stretcher capacitors whether or not they are above the lower level and upper level discriminator thresholds. Unless the lower level discriminator has been triggered, however, the stretcher capacitors will not remain charged to the peak input amplitude but will be discharged through 13.

Signal LLD is used for one other function through its connection to pin 10 of IC11A. Analog input signals below the lower level discriminator threshold are not gated off but are allowed to drive the stretcher/peak detector circuit. Pin 9 of IC11A goes positive for approximately 50 nanoseconds when the peak amplitude of the input signal is detected. Unless signal LLD is positive at this time signal $\overline{\text{PDS}}$ remains positive and no further ADC logic signals are triggered.

To summarize, when the input signal exceeds the lower level threshold two functions are performed. First, the clamp across the stretcher capacitors is removed, and second, the peak detect monostable is permitted to trigger the pulse stretcher flip-flop and begin the conversion.

4. The Upper Level Discriminator

Another comparator, IC1A, is used as the upper level discriminator. Discriminator bias is determined by the front panel Helipot setting and ranges from approximately .2 volts to +5 volts. Signals above the discriminator threshold generate a positive output at pin 6 of IC9A. The output of IC9A, pin 14, sets the Reject flip-flop. The Reject flip-flop is composed of two, two-input NOR gates in IC10A. The outputs of the flip-flop, signals RFF' and \overline{RFF} , perform the following functions. Signal RFF' is resistor-coupled to the base of transistors 10 and 15. Transistor 15 acts as a second shunt across the stretcher capacitors. When signal RFF' goes positive 15 saturates and the stretcher capacitor has effectively 220 ohms placed across it. This causes the stretcher capacitor to discharge on the trailing edge of the input signal, and in fact, the capacitor voltage follows the input signal down to the baseline. The Reject flip-flop is reset when the input signal passes through the lower level discriminator threshold and $\overline{DT1}$ switches positive. With the flip-flop reset 15 is turned off, removing the very low impedance shunt from the stretcher capacitor. However, at the same time 13 is turned back on by the recovery of signal $\overline{DT1}$. The higher resistance shunt path provided by 13 will then return the stretcher capacitor to approximately 0 volts.

The Reject flip-flop connects to two more circuits. First, signal RFF' connects to pin 11 of IC12A where it prevents triggering of the PSB flip-flop for reject conditions. This inhibits the start of an ADC conversion. Signal \overline{RFF} also connects to the STORE-REJECT logic circuitry (IC18A) and acts as a logic back up in the event the PSB flip-flop does get triggered by a partial pulse. In this case the following sequence of events occurs. The PSB flip-flop will set the ADC Busy flip-flop. Signal $DT1$ is composed of $LLD + B$ and the Reject flip-flop is reset by $\overline{DT1}$. If for some reason the Busy flip-flop is set, the Reject flip-flop will not be reset when LLD recovers. Instead, the normal reject circuitry of the STORE REJECT logic will be activated.

As soon as a "reject" is sensed the internal reset circuitry will reset the Busy flip-flop. At the same time a STORE command is inhibited. Now the Reject flip-flop will be reset when $\overline{DT1}$ returns positive. Under normal operating conditions this sequence does not occur. Under high count rate/pulse pile up conditions the normal ADC logic sequence may be upset, however. The sequence of events involving \overline{RFF} and the ADC Busy flip-flop then take over to reset the ADC and inhibit storage of an erroneous conversion. Note that under normal operating conditions the dead time added to the system by signals which trigger the upper level discriminator are equal to the time the lower level discriminator is triggered. Signal DT1 which is a component of the ADC dead time will be positive only for the duration the lower level discriminator is triggered.

5. The Zero Level Circuitry

Refer to the block diagram and the schematic for the zero level circuitry discussed here. Another comparator, IC5A is used as the zero level discriminator. One input to the comparator connects directly to the stretcher capacitors. The output of the circuitry which appears at the collector of 16 is essentially a logic function at this point because of the very high gain after the comparator. The level for comparison is derived from the front panel ZERO LEVEL control and connects to pin 3 of IC5A. The voltage at pin 3 ranges from approximately 0 to +4 volts depending on the front panel Helipot adjustment. Signal ZL at the collector of 16 connects to only one point, pin 5 of IC15A, the PSB flip-flop. Signal ZL acts as a dc reset for the flip-flop when ZL is at zero. Signal ZL goes positive as the signal at the ADC stretcher exceeds the zero level bias. This removes the dc reset on the PSB flip-flop, and will normally occur somewhere on the leading edge of the input signal. When the input signal reaches peak amplitude the peak detect monostable is triggered and the PSB flip-flop is set. In the event ZL is not in the one state at peak detect time (signals below the zero level bias) the peak detect monostable

will not set the PSB flip-flop due to its dc reset. Therefore, the leading edge of signal ZL acts as a logic function whereby no conversions will be started unless ZL is positive at peak detect time. For input signals above the zero level bias linear rundown will begin approximately .6 microsecond after PSB is triggered. At some instant in the linear rundown the voltage at the stretcher capacitor will pass through the zero level bias on its way toward the baseline. At this time signal ZL returns to the zero state and resets the PSB flip-flop. The trailing edge of PSB is used to close the gate which terminates the scaling of the 50/100 MHz clock into the address scaler. Thus, the zero level discriminator performs a dual function. First, only signals above zero level bias are permitted to allow triggering of the PSB flip-flop, and second, the final encoded address is a function of the time that ZL returns to the zero state. This in turn is a function of the zero level bias. Figure 5 shows an input signal of 4V with three different zero level bias settings. The first setting corresponds to a bias greater than the input signal. ZL is not generated and no conversion of the input results. The second condition is with the zero level bias set for approximately half signal amplitude. Note the pulse train duration and the address of the converted signal. The third condition shows the zero level bias set approximately for zero; that is, such that the slope intercept is at zero-zero. Again, note the number of address advance pulses and the final address generated. It can be seen from these diagrams that in all cases the pulse shape as seen by the pulse stretcher is the same. The final encoded address however is a function of the zero level bias. Operation of the zero level circuitry in this manner provides all the advantages of biased amplifier operation without the disadvantages normally associated with them. The signal as connected to the ADC stretcher and other analog circuitry in the ADC is the same for any zero level bias. ADC stability and linearity are essentially independent of zero bias setting.

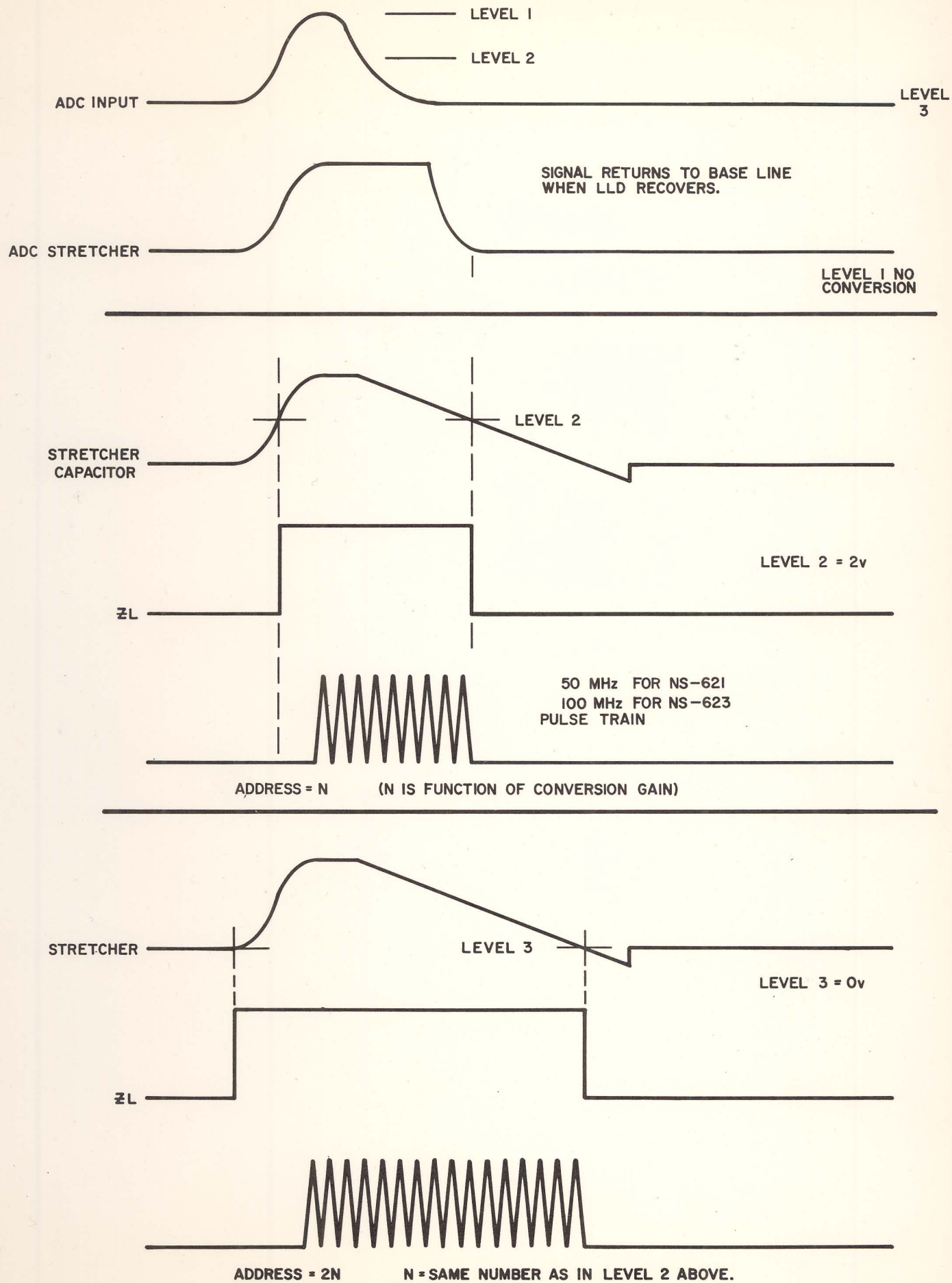


FIG. 5

6. Rundown Current Switch and Conversion Switching

Circuitry for this section is all contained on the A Board schematic. Approximately 100 nanoseconds after PSB is generated a constant current is applied to the stretcher capacitor to provide linear discharge of the capacitor. Transistor 6 is darlington connected for very high current gain. One darlington pair is used as a diode for temperature compensation of the other pair which operated in a common base mode. The CONVERSION GAIN switch on the front panel sets the resistance between the -13.6V reference supply and the emitter of the common-base darlington pair in 6. The switched-in resistor establishes the appropriate rundown current so that the full-scale address corresponds to the front panel CONVERSION GAIN switch position for an 8V ADC input. In the quiescent state the current established by the switched-in resistor is conducted through transistor 18. Signal CSC goes to the one state when the rundown is to begin. This saturates transistor 19 and the standing current in 18 switches to 6 and linear rundown begins. The rundown current remains switched on until the address as converted is either stored, or rejected within the ADC. Later sections deal with a more detailed description of the timing of the ADC logic signals. At this time it is important to know only that signal CSC goes to the one state approximately 100 nanoseconds after PSB flip-flop is set. Signal CSC returns to the zero state when the ADC is reset, either internally under reject conditions or at the time a clear signal is received from the memory section.

7. 50 MHz (NS-621) and 100 MHz (NS-623) Oscillators

The oscillator for the respective ADC type is found on the B Board. These boards are designed specifically for the respective ADC types and circuitry and IC types are considerably different. Refer to the B Board schematic for the following discussion.

The 50 MHz oscillator is found in IC4B in the NS-621. This IC type is a Schottky diode-clamped version of the standard 7400 quadruple

two-input NAND gate. The diode clamp provides near class A operation of the inverting gates which increases the switching speed considerably. One gate with inputs on pins 12-13 has a parallel resonant circuit connected to a bypassed 330 ohm resistor which connects to the gate output pin 11. The resistor provides a stable operating point for the oscillator circuit. A 50 MHz, third overtone, crystal connects directly from pin 11 to pins 12 and 13 on IC4B. The resonant circuit provides high impedance to 50 MHz only, causing oscillation only on the third overtone. The remaining gates in IC4B gate the 50 MHz and also buffer the oscillator from the scaler.

For the NS-623 100 MHz oscillator Motorola MECL II IC's are used. Refer to the B Board schematic and find IC4B. The input to one inverter in IC4B, pin 2, has a parallel resonant circuit connected to the junction of a 221 ohm and 750 ohm resistor. These resistors form a voltage divider which places the gate in its active region. The 100 MHz crystal is a fifth overtone type with oscillation at the proper overtone selected by the resonant circuit at the inverter input. The other inverter in IC4B acts as a buffer between the oscillator and the address scaler.

8. Address Scaler

The address scalars in the NS-621 and NS-623 are almost identical. However, the first two stages of the NS-623 are Fairchild ECL types while the NS-621 uses TTL exclusively.

In the NS-621 the first two address scaler stages are Schottky diode-clamped TTL for 50 MHz and 25 MHz scaling. The remaining 11 stages are standard TTL types.

In the NS-623 IC2B and IC5B are Fairchild temperature-compensated ECL types for 100 MHz and 50 MHz scaling. Transistors 1B through 7B transform the ECL levels to TTL levels for readout and/or further scaling in the 11 following TTL scaler stages.

Beyond the first two address stages the circuitry for the ADC's is

essentially the same. The discussion which follows applies to either unit with difference noted in the discussion.

The address scaler is composed of two flip-flops in IC5B followed by 12 flip-flops of TTL from the 7400 family. Note that the output of the third address scaler stage in 6B connects as a carry to two flip-flops. One flip-flop of the two is address scaler stage A₃. The other flip-flop is used as the Current Switch Control (CSC) flip-flop. This flip-flop is set when the "carry" from pin 15 of the third stage switches positive. Remember that signal CSC begins linear rundown. Following sections will discuss the timing of the logic signals in more detail. Note this flip-flop is dc reset by signal B when the Busy flip-flop is reset at CLEAR time.

There are 13 IC gates in IC's 1, 2, 3 and 14B (NS-621) or 1, 7, 10 and 13B (NS-623) which act as gated buffers for the address scaler outputs. Two signals connect to the inputs of the gated-buffer stages. One signal is the output of the scaler flip-flop, the other is signal $\overline{\text{ING}}$. $\overline{\text{ING}}$ is positive at all times except immediately after rundown. Signal $\overline{\text{ING}}$ is generated at pins 3 and 6 of IC9A and is equal to $B \cdot \overline{\text{PSB}}$. The thirteen buffers are held off by $\overline{\text{ING}}$ until the end of conversion. With $\overline{\text{ING}}$ at zero the outputs of the IC scaler stages determine whether their respective buffers are at logic zero or one. Thus, the encoded address as contained in the IC scaler is presented to the memory when the control of the buffers is switched from $\overline{\text{ING}}$ to the scaler at the end of conversion. Address output lines A0 through A12 remain at zero volts until the address is presented.

9. Conversion Logic Timing

Previous sections discussed individual circuits and logic blocks without any attempt to tie them all together in the system design. This section will cover the sequence of events from the arrival of the analog input through the end of conversion. Refer to Figure 6 which shows the timing of the major signals which will be discussed here. To simplify discussion, the ADC is assumed to be operated in the following manner. The upper and lower level discriminators are set for conversion of the

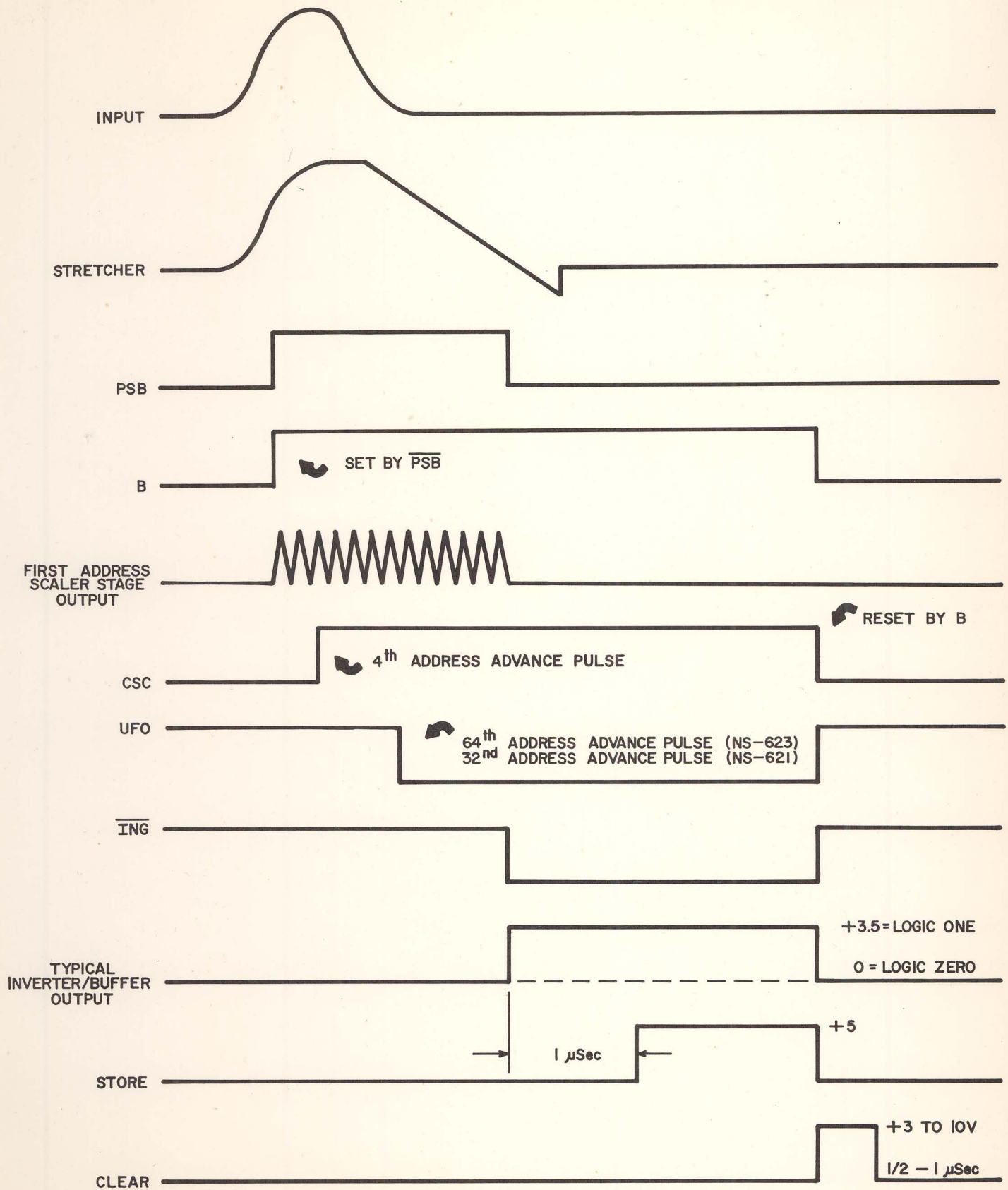


FIG. 6

entire range from zero to full scale. The ZERO LEVEL control is set for approximate 0-0 intercept. The conversion gain switch is set to the memory size. The ADC is operated in a normal fashion; this precludes coincidence operation; no digital offset is used, and finally the ADC is analyzing normal pulses rather than DC or slow AC signals.

The incoming positive signal connects first to the gain-of-one voltage follower. The output of the voltage follower connects to the pulse stretcher and to the lower and upper level discriminators. As the signal starts positive the lower level discriminator triggers and removes the clamp across the stretcher capacitor. Simultaneously the signal which inhibits the peak detect monostable output is removed. The positive signal across the stretcher capacitor is coupled to the zero level discriminator and it triggers generating positive signal ZL. With ZL in the one state the PSB flip-flop can now be triggered when peak detection occurs. The signal continues positive and all the proper logic levels have been established, awaiting peak detection to start the conversion. When the pulse reaches maximum amplitude the charging current to the stretcher capacitors drops to zero. Shortly thereafter the input signal starts down and peak detection occurs. A 50 nanosecond peak-detect strobe is generated and this triggers the PSB flip-flop, setting it to the one state. Signal PSB goes positive and $\overline{\text{PSB}}$ goes to 0 volts. $\overline{\text{PSB}}$ sets the ADC Busy flip-flop and signal $\overline{\text{B}}$ goes to ground. This prevents the clamp on the stretcher capacitor from being turned back on until the flip-flop is reset. Signal $\overline{\text{B}}$ also generates signal LGS which closes the linear gates for the stretcher and discriminators. This holds the discriminators and the stretcher inoperative until this conversion-STORE sequence is complete. Signal B is differentiated and the resultant pulse sets the CLOCK SYNCHRONIZING flip-flop, IC12B for the NS-621 and IC2B for the NS-623. The output of this flip-flop

switches to the one state and the clock signal is now connected to the input of the first address stage and it begins to scale. Four clock pulses later the carry output of 6B, the third address scaler stage, switches positive. This sets the CSC flip-flop. Signal CSC turns on the rundown current. With no digital offset, address stages A5 through A12 (A6 through A12 for the NS-623) will be in the "set" state and stages A0 through A4 (A0 through A5 for the NS-623) will be "reset" when scaling begins. After 31 clock pulses (63 for the NS-623) all address stages will be in the one state. One pulse later all address stages switch to the zero state. At this time a carry pulse from the last address stage A12 sets the UFO flip-flop and signal UFO switches to zero. The address scaler at this time is in channel 0. It is important to recognize that the address scaler has been reset to the equivalent of -32 (-64 for NS-623); that is, it takes 32 pulses from the 50 MHz clock (64 from the 100 MHz) to place the address scaler in channel 0. The scaler requires .64 microsecond to arrive at channel 0 due to this built-in digital offset. The design of the analog circuitry is such that with the ZERO LEVEL control set for 0-0 there are exactly 32 channels (64 for NS-623) of equivalent pedestal built into the analog circuitry. Even with no front panel digital offset, the address transferred to the memory unit differs from the number of address-advance pulses by a fixed quantity of 32 (64 for NS-623). The offset serves two purposes. First, the turn on of the rundown current is synchronized to the clock by scaling 4 address-advance pulses before setting the CSC flip-flop. No attempt is made to synchronize opening of the address scaler gate with the clock. The triggering uncertainty in the first stage has no effect on the ADC synchronization. For good channel profile it is essential that start of rundown current be well synchronized to the clock. This is accomplished by scaling in 4 pulses from the clock before signal CSC is generated. The first 3 address stages actually perform the synchronization. By the time the scaler has scaled 4 clock pulses the transitions are well synchronized to the clock.

The second function of the offset is in providing the ADC with settling time. At peak detect time several circuits are triggered and several logic transitions occur. The .64 uSec period before reaching address zero allows the analog circuitry and the zero level discriminator to settle to quiescent states before an acceptable address is converted.

At this time the sequence of events which began the conversion process have been covered. The address scaler has been advanced to channel 0 by scaling through the built-in offset. The conversion process now continues until the voltage at the stretcher capacitor reaches the zero level bias. Signal ZL at this time returns to zero and resets the PSB flip-flop. Signal PSB at zero starts clock pulses to scale in the clock synchronizing flip-flop. The output of the flip-flop switches positive in synchronization to the clock and gates off the clock to the address scaler.

Now that the address has been generated it is presented to the memory unit and to the "acceptance test" logic circuitry. This is accomplished in the following way. Signal \overline{ING} switches to zero when PSB returns to 0V and the buffers are allowed to switch to the states determined by their respective scaler stages. This presents the address to both the memory and the acceptance test logic circuitry.

This completes the basic conversion process. The address as presented will either be transferred to the memory or rejected by the acceptance test circuitry. This is covered in the next section.

C. Store, Clear, Reject and Digital Offset Logic Circuits

1. General

This section deals with the sequence of events which immediately follows the end of the conversion. This includes the address acceptance tests followed by a STORE or internal reset of the ADC. Integrated circuits are used almost exclusively in this area so that no separate block diagram is provided. The schematics take the form of a block diagram and will be used for this discussion.

2. STORE Command and ADC Reset

Signal STORE is the flag to the computer or memory unit signifying that a conversion is complete and that the address passed all tests whose limits are set by the front panel controls. STORE and address remain at the ADC output until a CLEAR is received from the computer or memory unit.

Refer to the A Board schematic and find where PSB connects to pin 12 of IC20A. The output of 20A at pin 13 is $\overline{\text{PSB}} \cdot \text{B}$, the conversion complete signal. This output is inverted by two gates in IC19A and generates $\overline{\text{ING}}$ on pins 3 and 6. $\overline{\text{ING}}$ goes to zero when conversion is complete and allows the address-scaler buffers (B Board) to present the address to both the rear panel output connector and to the front panel overflow circuitry on the GROUP SIZE switch. The address is tested for overflow at this time.

The output of IC20A pin 13 also connects to pins 5 and 6 of 20A through series 2K2 resistors. Pin 6 of this gate diode connects to the CHO gate (B Board) and tests the address for channel zero (reserved for live/clock time storage). If the address scaler stops in channel zero pin 4 of IC20A switches to zero signifying a "reject" condition. Pin 5 of this same gate diode connects to the underflow flip-flop (UFO) and pin 4 of IC20A switches to zero if the address scaler has not scaled to zero due to digital offset.

The conversion complete signal also connects to pin 12 of IC19A where it is inverted, and then inverted a second time by another gate in IC19A. The output of this second inverter at pin 8 is delayed approximately 1 uSec by the 1000 pF capacitor to ground. This delay in the conversion complete signal allows time for all the address tests to be completed and set up any reject signal.

The delayed conversion complete signal ties to pin 13 of IC18A and if all acceptance tests are passed the other inputs to this gate, $\overline{\text{OFO}}$, $\overline{\text{Z}}$, $\overline{\text{RFF}}$, $\overline{\text{RESET}}$, and $\overline{\text{EXT REJ}}$, will be positive. Pin 8 of IC18A switches to zero and is inverted to generate STORE at pin 3 of IC21A.

When pin 8 of 18A switches to zero the other NAND gate in IC18 is disabled at pin 5. If any reject is generated by the address; overflow, underflow, or channel zero for example, pin 8 of IC18A will not go to zero when "conversion complete" is applied to pin 13. Now both inputs to IC18A at pins 5 and 2 will be positive and the re-set monostable will be triggered. This resets the ADC with no STORE generated. Note, if STORE is generated pin 5 of IC18A will be at zero and the only way the ADC can be reset is by a CLEAR signal applied at the base of transistor 6.

3. Digital Offset Circuitry

Refer to the schematics for the front panel and the B Board for the circuitry in this section. Note that address scaler stages A6 through A12 have both reset and set inputs. For no digital offset the "set" inputs will be used on address stages A6 through A12. A front panel toggle switch associated with each address stage controls the state of its respective stage when a reset pulse is generated at CLEAR time. For example, the 4096 switch controls address stage A12, and sends a reset pulse rather than a set pulse when the switch is on (up). In similar fashion the reset state of stage A11 is determined by the front panel switch labeled 2048, A10 by 1024, A9 by 512, etc.

Refer again to the schematic and observe the digital offset reset logic. Two NAND gates are associated with each address scaler stage, one generating a reset pulse, the other a set pulse. For purposes of explanation refer to IC8, pins 2 and 3, the set and reset inputs for address stage A6. The RESET pulse, either internally generated at reject time or by a CLEAR input, is applied to pins 10 and 12 of 17A. A6S and A6R connect to the front panel digital offset switch labeled "64". With the switch down A6S will be open and A6R will be connected to ground. When RESET goes positive, pin 8 and 17A switches to ground and sets the address scaler stage. When the switch is "on" for 64 channels of digital offset pin 9 is grounded and pin 13 is opened. Now when the RESET pulse is applied to the gates pin 11 will switch

to ground while pin 8 will remain positive. This resets the address scaler stage.

The manner in which digital offset is accomplished can be best explained by using two examples. The first will use no digital offset while the second will have 4096 digital offset. Assume for the moment then that all digital offset switches are off. When the address scaler is cleared stages A6 through A12 will be set, that is, the true outputs will all be in the one state. Stages A0 through A5 on the other hand will all be reset with the true outputs all in the zero state. The underflow flip-flop contained in IC11A will also be reset and signal UFO will be positive. Assume the address scaler gate is opened and that the scaler begins scaling clock pulses. 31 address advance pulses later all stages A0 through A12 will be in the "one" state on the NS-621. For the NS-623 63 address advance pulses puts all stages in the "one" state. One more address advance pulse will reset stage A0 which will propagate a carry to A1 and reset it. This in turn will propagate a carry to stage A2, resetting it. The process continues such that a carry is propagated through the 13 stages of the address scaler. A carry is also propagated to the Underflow flip-flop at this time. Signal UFO switches to zero and the address scaler is in channel zero. If the address scaler were to stop here the Channel Zero reject gate would inhibit storage. If the address scaler continues to advance beyond channel zero and does not exceed group size it will generate STORE. Under these conditions the address as presented differs from the number of clock pulses by 32 clock pulses for the NS-621 and 64 clock pulses for the NS-623.

Now let's switch in 4096 channels of digital offset. With the front panel toggle switch "on" address stage A12 will always be cleared to the zero state so that either 32 or 64 (NS-621 and NS-623 respectively) address advance pulses will put stages A0 through A11 in the zero state and a carry will propagate to stage A12 where it will be set. At this time no carry is propagated to the UFO flip-flop. If conversion ceases

at this time the channel zero reject gate will not reject the conversion but signal UFO will remain positive and keep signal \overline{Z} at ground, rejecting the conversion. Assume conversion continues for 4095 additional address advance pulses. Now stages A0 through A12 will all be in the one state. Remember that this is the condition corresponding to 32 or 64 address advance pulses with no digital offset. With one additional pulse, stages A0 through A12 will be switched to the zero state and a carry will propagate to the UFO flip-flop removing the reject condition. However, at this time, the channel zero reject gate will still reject this conversion. All conversions generating more than 32 or 64 plus 4096 address advance pulses will generate a memory cycle as long as they do not exceed the memory group size.

The ADC is designed with built-in digital offset. This offset is compensated for in the analog circuitry. It can be shown that the number of address advance pulses required to place the address scaler in channel zero is equal to the digital offset switched in on the front panel plus the constant 32 or 64 for the NS-621 and NS-623 respectively. Digital offset can be thought of in another way. The address scaler can be thought of as being initially reset to a negative number. Also all negative-number conversions will automatically be rejected by the logic circuitry. Thus a digital offset of 4096 can be thought of as a minus 4096 condition of the address scaler. No memory cycle will occur until the scaler has been advanced through the negative number and this means a minimum of 4096 plus 32 or 64 address advance pulses. Note that for a given analog input the amount of offset does not affect the conversion dead time. At high count rates and high resolution settings of the conversion gain switch it is oftentimes wise to consider using analog offset with the ZERO LEVEL control for reduced dead time. With 50 or 100 MHz digitizing rate, however, the analog control may be worthwhile only in extremely high count rate/resolution experiments.

4. Dead Time Signal and ADC Recovery Circuitry

Signal DT is positive any time the ADC is busy and not capable of accepting another input for conversion. Signal DT1 is composed of $LLD + B$. DT1 connects to pin 5 of IC11A with the output appearing at pin 6 as $\overline{DT1}$. Pin 6 connects to pin 12 of IC11A and generates a portion of DT. At the time the ADC is reset, either internally or externally, an ADC recovery single shot, IC13A is triggered. This monostable is provided to allow the ADC 3 microseconds to recover from the transients generated by the address transfer. The ADC discriminators, stretcher, and logic circuits are enabled at reset time. However, any signal detected during the 3 microsecond period of the recovery multivibrator will not be converted. This 3 microsecond dead time must be included in ADC dead time for accurate live time operation. This is accomplished by connecting \overline{REC} to pin 13 of IC13A. Thus, the total dead time signal for a conversion begins with triggering of the lower level discriminator and extends for 3 microseconds after the reset pulse has been generated.

VI. SERVICING

Servicing of the ADC can be accomplished without a memory unit. All ADC functions can be checked with a good stable pulser capable of generating a zero to 10 volt positive pulse in the range of 1 to 2 microseconds duration. A scope with a 50 MHz bandpass is the minimum which can be used on most of the fast logic circuitry. A 100 MHz unit is preferred and is a must if waveforms in the 100 MHz circuitry are to be observed. The module will have to be bench operated so that an extender cable between the module and the bin power supply will be necessary.

To disassemble the module for servicing use the following procedure. Remove the two Phillips-head screws on the front panel in the upper right and upper left corners. Do the same on the rear panel. Loosen the four Phillips-head screws on the lower front and rear panels. Now separate the module sides at the top by rotating the sides down. Access to the bottom sides of the printed circuit boards can be gained by removing the metal sides.

The ADC has been described in some detail in the previous section, System and Circuit Design. This section coupled with the schematics and timing diagrams should greatly assist trouble shooting. In general, all components used in the ADC are stock items with large electronic distributors. Sheets are included in the manual preceding the schematics which show the pin numbers for the integrated circuits along with their types. The connector tabulations list the signals, connectors, and pin numbers where these signals appear. Where practicable, signals are labeled on the printed circuit boards as they appear on the schematics and connector tabulations. A short time spent with the connector tabulations, the list of major signals and their functions, and the general notes preceding the schematics will be a very good investment once trouble shooting is undertaken. The factory may be contacted for assistance in servicing if difficult problems are encountered.

MAJOR SIGNALS AND THEIR FUNCTIONS

<u>Signal</u>	<u>Function</u>
A0 through A12	13 bit address which connects to memory unit. Logic zero = 0V, logic one = +2.5 to 3.5V from TTL source.
A6R	Control signal which connects to F. P. DIGITAL OFFSET sw. Signal is +5 when "64" switch is up, ground when switch is down.
A6S	Same as A6R with exception that signal is +5 when switch is up and 0V when switch is down.
A7R through A12R	Same function as A6R for their respective switch/circuits.
A7S through A12S	Same function as A6S for their respective switch/circuits.
$\overline{A6R}$	1 uSec pulse from quiescent +3.5V to gnd. which resets the A6 stage of the address scaler.
$\overline{A6S}$	Same as $\overline{A6R}$ except pulse sets A6 stage.
$\overline{A7R}$ through $\overline{A12R}$	Same function as $\overline{A6R}$ for respective address scaler stages.
$\overline{A7S}$ through $\overline{A12S}$	Same function as $\overline{A6S}$ for respective address scaler stages.
ACN	Connects to COINC BNC in the ANTI COINC position of the mode switch. Positive signal inhibits conversion by preventing PSB flip-flop from being triggered.
B	Output of \overline{ADC} busy flip-flop. Flip-flop is set by \overline{PSB} and reset by Reset. This signal sets clock synchronizing flip-flop, is major component of dead time signal, connects to STORE logic, and holds ADC linear gates closed while in the one state.
CLEAR	Rear panel input to the ADC to reset the ADC after data transfer. Requirements: positive 3-10V pulse, 1/2 to 1 uSec duration. Input impedance: 3.3K dc connected.
CNC	Connects to COINC BNC in the COINC position of the mode sw., and to +5 in the ANTI COINC position of the mode sw. Positive input opens linear gate to allow ADC conversion. See section on COINC operation for more details.
CSC	Current source control F.F. output. Connects to rundown-current switch and starts linear rundown when switched to the one state. Flip-flop is set by carry from third stage of address scaler and reset by the ADC Busy F.F. output, signal B.

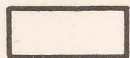
DT	Dead Time signal appearing on rear panel connector. Signal is +3.5 whenever the ADC is busy converting an input or whenever it is insensitive to an input. Used in the memory unit for dead time correction in the live timer.
DT1	Positive whenever LLD or B is positive. Major component of dead time signal. Used to control clamp across stretcher capacitor.
DTM	Dead Time Meter drive signal. Connects to F.P. Meter.
Ext B	Buffered output of ADC Busy F.F. available on ADC rear panel. Logic zero = 0V, logic one = +3.5V.
Ext Cont	Rear panel input provided to disable normal STORE-REJECT logic. Used by NS-641 Two Parameter Adapter to disable ADC logic.
Ext Gate	Input provided to force channel 0 on address output lines. Used by NS-641 Two Parameter Adapter for storage of Singles and/or Live Time counts.
Ext REJ	Rear panel input provided to reject a conversion. Input requirements: +5V pulse, 1/2 to 1 uSec duration. Pulse must be applied after the analog input signal triggers LLD, and before the end of conversion. Pulse sets Reject F.F. which inhibits STORE and automatically causes ADC reset. Dead time after pulse application is approximately 5 uSec for any analog input amplitude/conversion gain. This input can be used as a delayed anti coincidence input. Maximum delay to ensure reject for any amplitude/conversion gain is approximately 1.5 uSec after the analog input reaches peak amplitude.
Ext $\overline{\text{REJ}}$	Rear panel input provided to inhibit STORE and cause internal ADC reset. Input requirements: To inhibit STORE this input must be at 0V when PSB returns to 0V and for at least 2 uSec thereafter. External source must sink approximately 2.5 mA at 0V. Used by NS-409 and NS-454 Stabilizers.
LGS	Linear Gate Source. $\text{LGS} = \text{B} + \overline{\text{CNC}}$. The linear gates for the ADC stretcher and discriminators are closed whenever LGS is in the one state.
OFF	Connects to Front Panel ANALYZE-OFF switch. Ground in ANALYZE sw. position, +5V in the OFF position. Holds ADC in dc reset condition. Also used by NS-630/NS-636 Memory Units and NS-641 Two Parameter Adapter to hold timing scalers reset until analysis begins.
OFO	Signal generated on the front panel GROUP SIZE switch. OFO is positive for any address greater than group size selected by switch. This causes STORE to be inhibited and ADC to be reset internally.

PSB	Pulse Stretcher Busy F.F. output. Set by peak detect strobe and reset by ZL in the zero state. Triggers and/or controls several ADC logic functions at the start and end of conversion which are indicated by the leading and trailing edges of this signal respectively.
$\overline{\text{REC}}$	3 uSec output of Recovery Single Shot. Inhibits start of conversion within 3 uSec after ADC is reset.
RFF	Buffered Output of Reject F.F. which connects to rear panel. RFF is set by $\text{ULD} + \text{Ext REJ} + \text{ACN} \cdot \text{PDS}$ and is reset by DT1 when it returns to 0V. Used by the NS-641 Two Parameter Adapter.
STORE	Positive 5V signal which indicates conversion complete and acceptable address for storage in the memory. STORE and address remain until a CLEAR is received by the ADC.
UFO	Underflow F.F. output. Signal is positive until address scaler has advanced through channel 0. Provides automatic reject of conversions below channel 0 when using digital offset.
X PSB	Buffered output of Pulse Stretcher Busy F.F. available on ADC rear panel. Logic zero = 0V, logic one = +5V.
$\overline{\text{Z}}$	Zero signal which connects to STORE-REJECT logic. Signal is 0V when conversion is below channel 0 (due to UFO) or is at channel 0 (CH0 gate) so that STORE is inhibited and the ADC is automatically reset.

REAR PANEL
26M ADC CONNECTOR

<u>PIN</u>		<u>SIGNAL</u>
A ✓	26 x	A0
E ✓	16 x	A1
K ✓	15 x	A2
P ✓	14 x	A3
U ✓	12 x	A4
Y ✓	11 x	A5
\overline{c} ✓	10 x	A6
C ✓	8 x	A7
H ✓	7 x	A8
M ✓	6 x	A9
S ✓	4 x	A10
W ✓	3 x	A11
\overline{a} ✓	2 x	A12
B ✓	30 x	DT (Busy)
— F ✓	35 x	STORE
— L ✓	31 x	CLEAR
— R		OFF
V		EXT B
— Z		\overline{REJ}
\overline{d} ✓	33 x	EXT CONT
D		EXT REJ
J		EXT GATE
N		SET B
— T		X PSB
X		RFF
\overline{b} ✓	19 x	GND

GENERAL NOTES



Designates signal source which connects to loads off this schematic/board and may also have loads on this schematic/board.



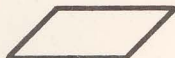
Designates signal from a source not on this schematic/board.



Designates source for a signal used only on this schematic/board.



Designates load for signal used only on this schematic/board.



Designates front and rear panel labeling.

All NPN transistors are 2N2369 or S2830 (2N2369 with minimum beta of 30) unless otherwise marked.

All PNP transistors are 2N3638, unless otherwise marked.

Pin numbers on Integrated Circuits are as viewed from the top of the IC.

All resistors are 1/4 watt 5%, unless otherwise marked.

R47

Resistor whose value is .47 ohms.

4K7

Resistor whose value is 4700 ohms.

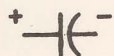
4M7

Resistor whose value is 4.7 megohm.

MF designates precision metal film 1/4 w \pm 1% resistors, unless otherwise specified.

All diodes are Fairchild IN4150 or equivalent, unless otherwise specified.

Capacitance values shown are in picofarads unless otherwise specified.



Polarized capacitors are as shown.

GENERAL NOTES



Designates signal source which connects to loads off this schematic/board and may also have loads on this schematic/board.



Designates signal from a source not on this schematic/board.



Designates source for a signal used only on this schematic/board.



Designates load for signal used only on this schematic/board.



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All resistors are 1/4 watt 5%, unless otherwise marked.

R47

Resistor whose value is .47 ohms.

4K7

Resistor whose value is 4700 ohms.

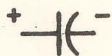
4M7

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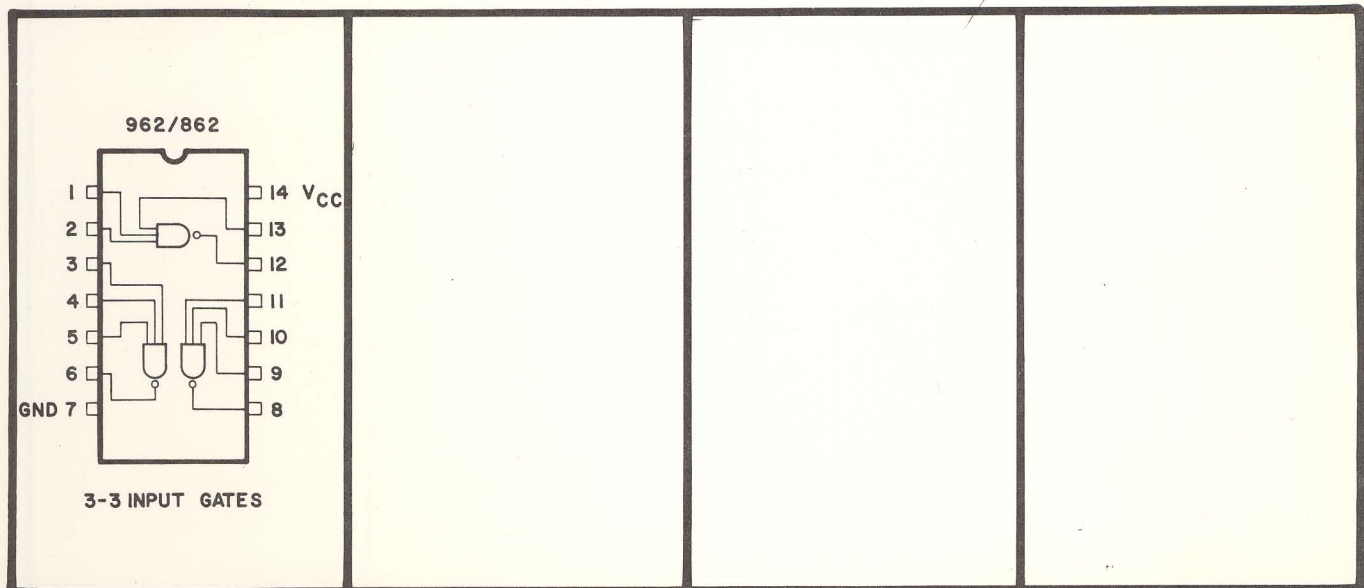
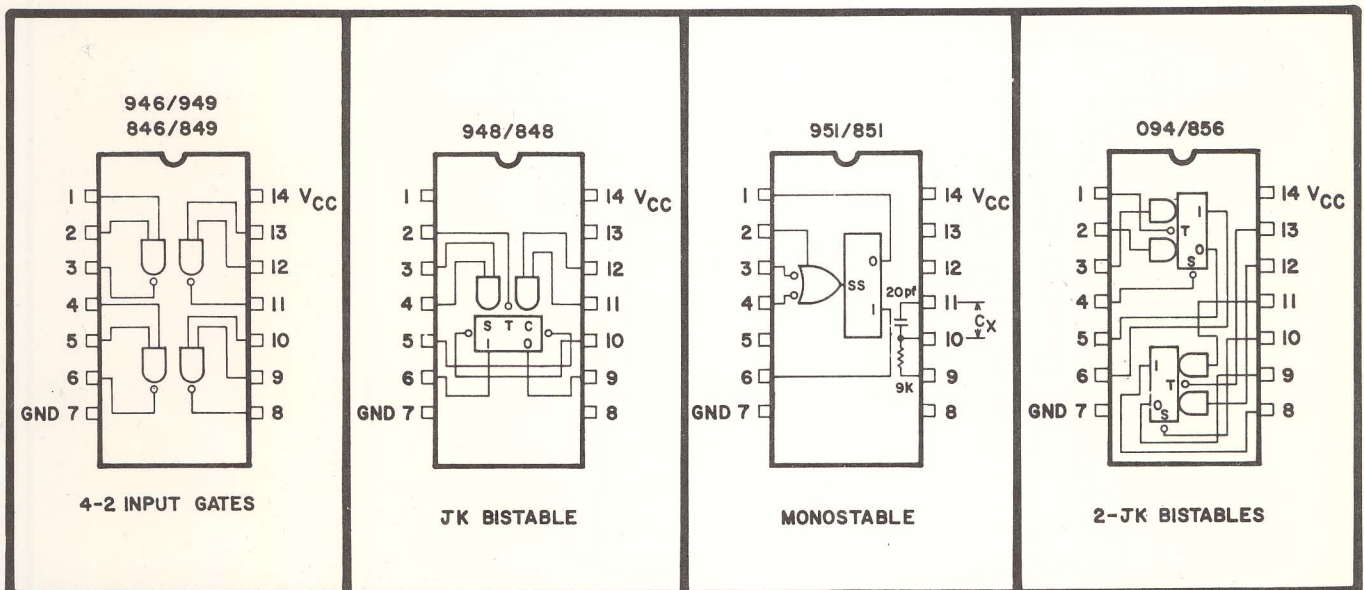
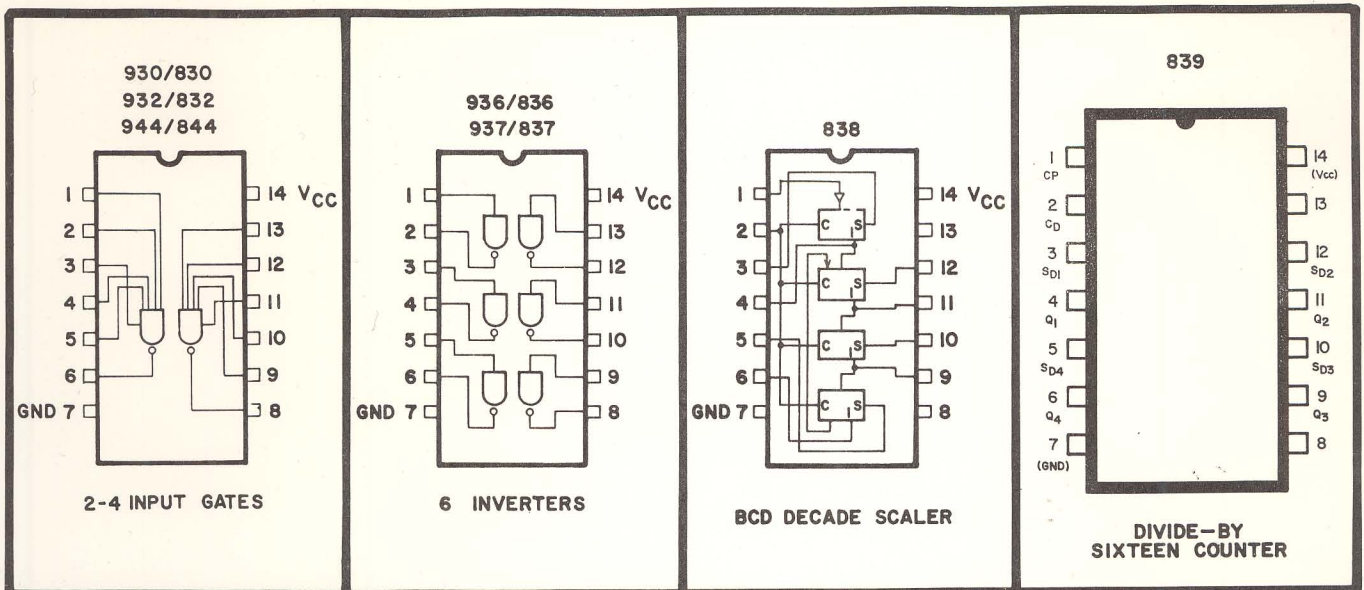
MF designates precision metal film 1/4 w $\pm 1\%$ resistors, unless otherwise specified.

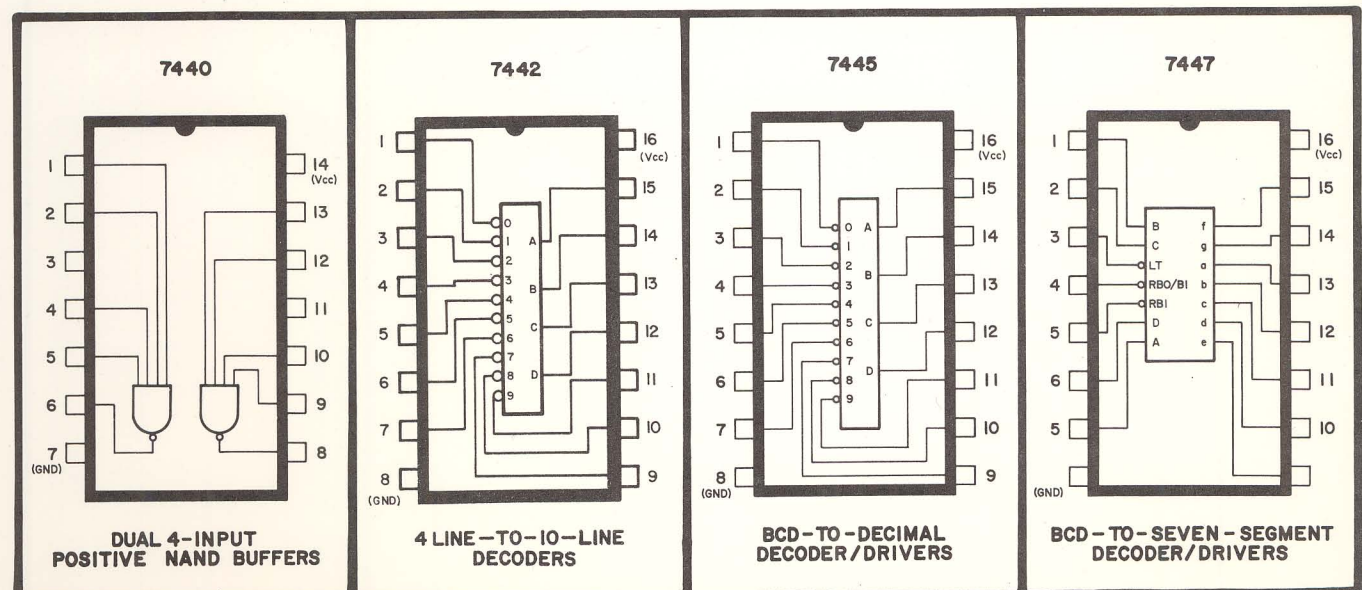
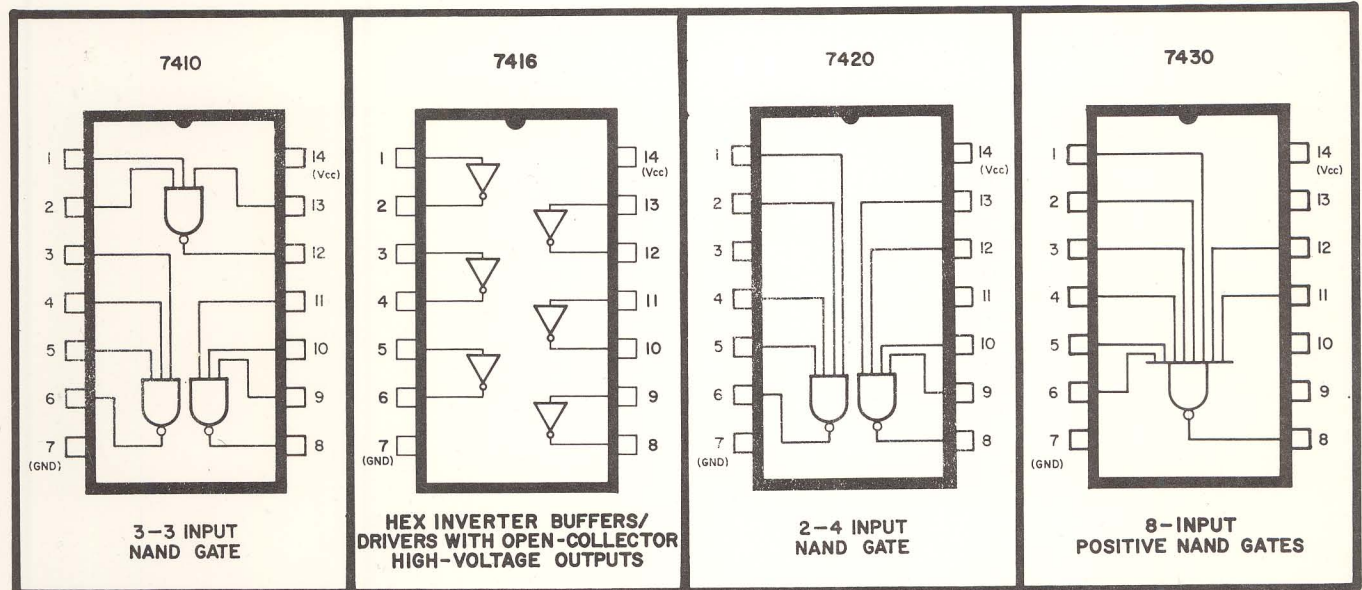
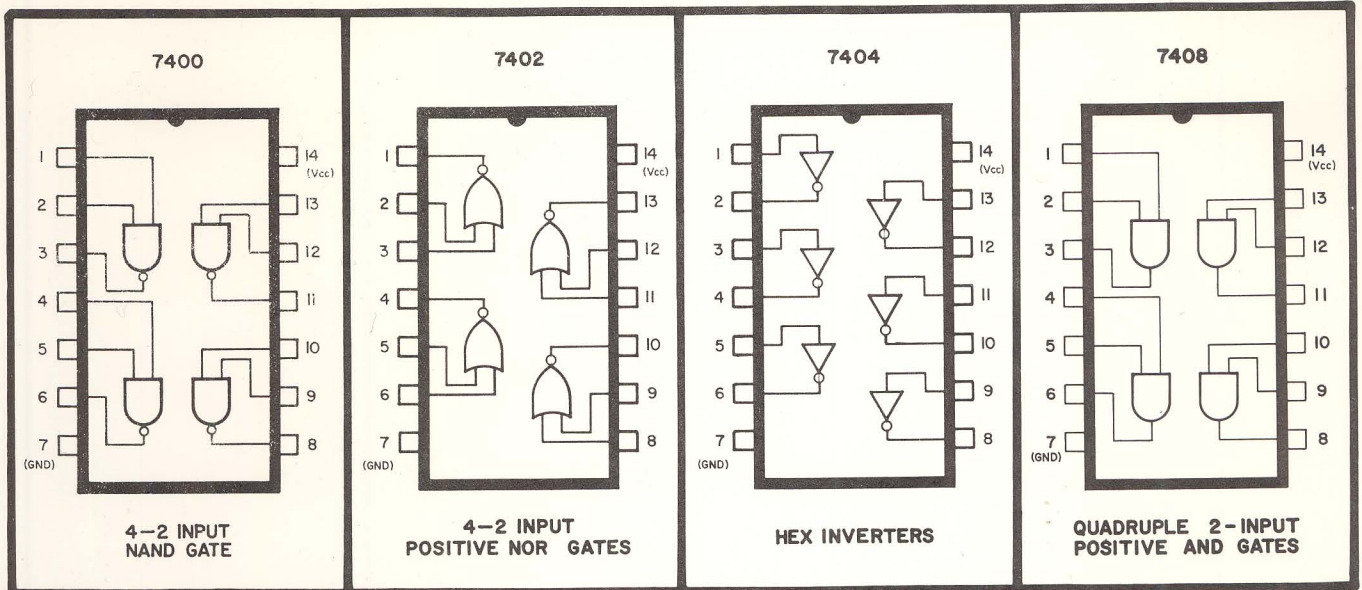
All diodes are Fairchild IN4150 or equivalent, unless otherwise specified.

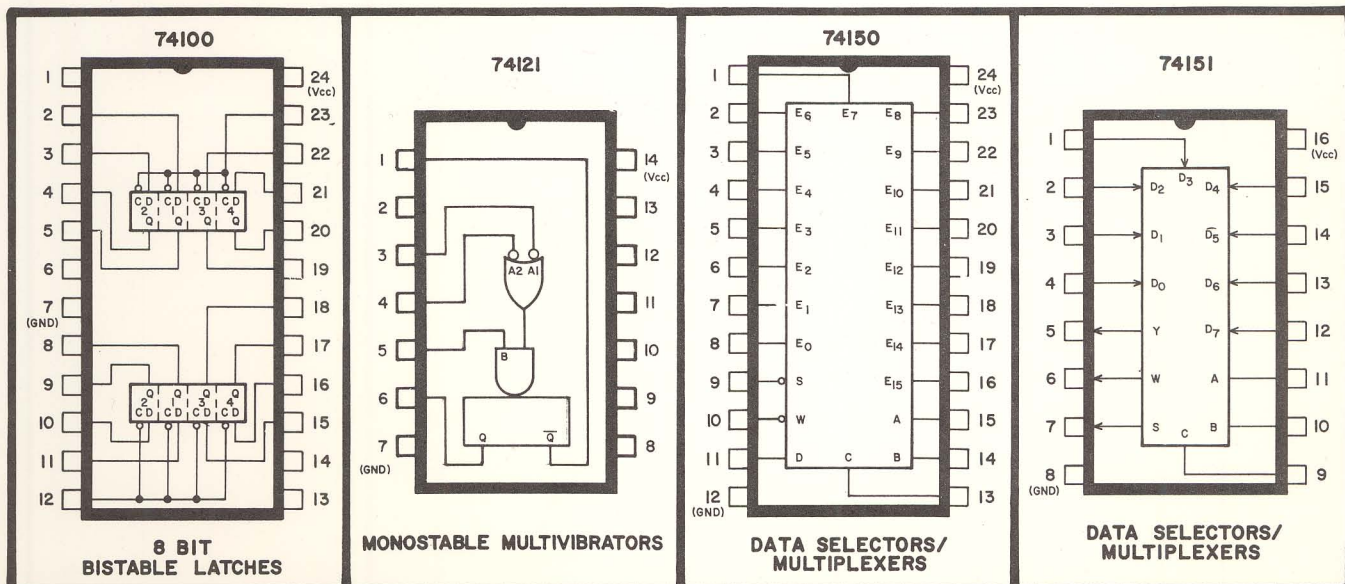
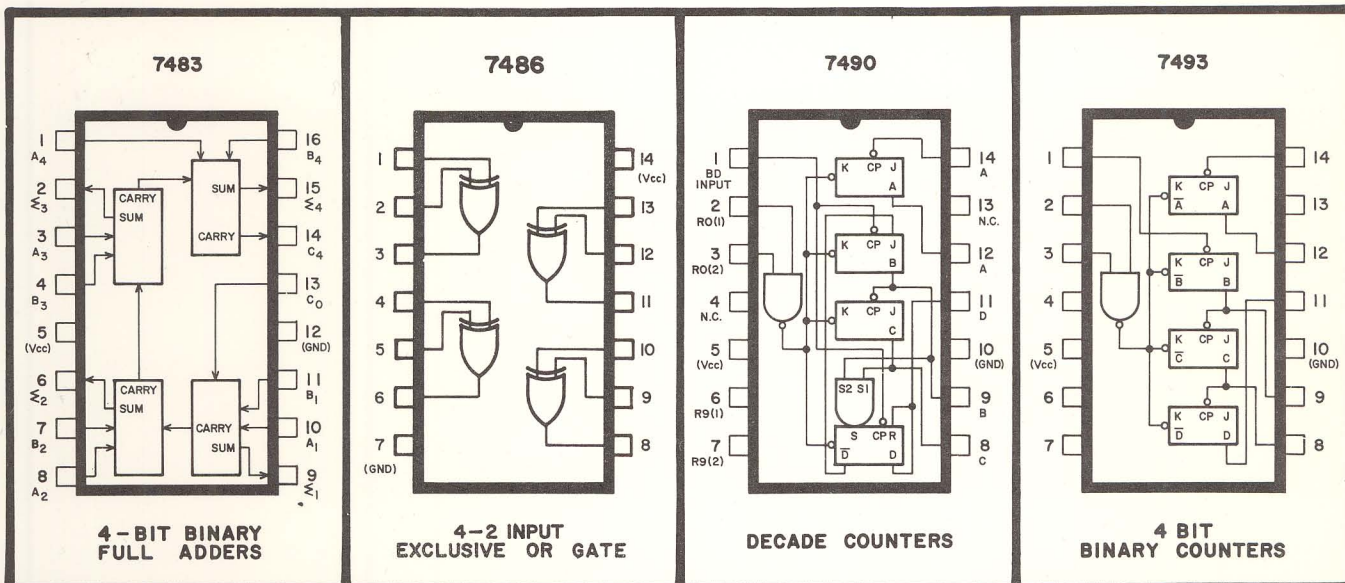
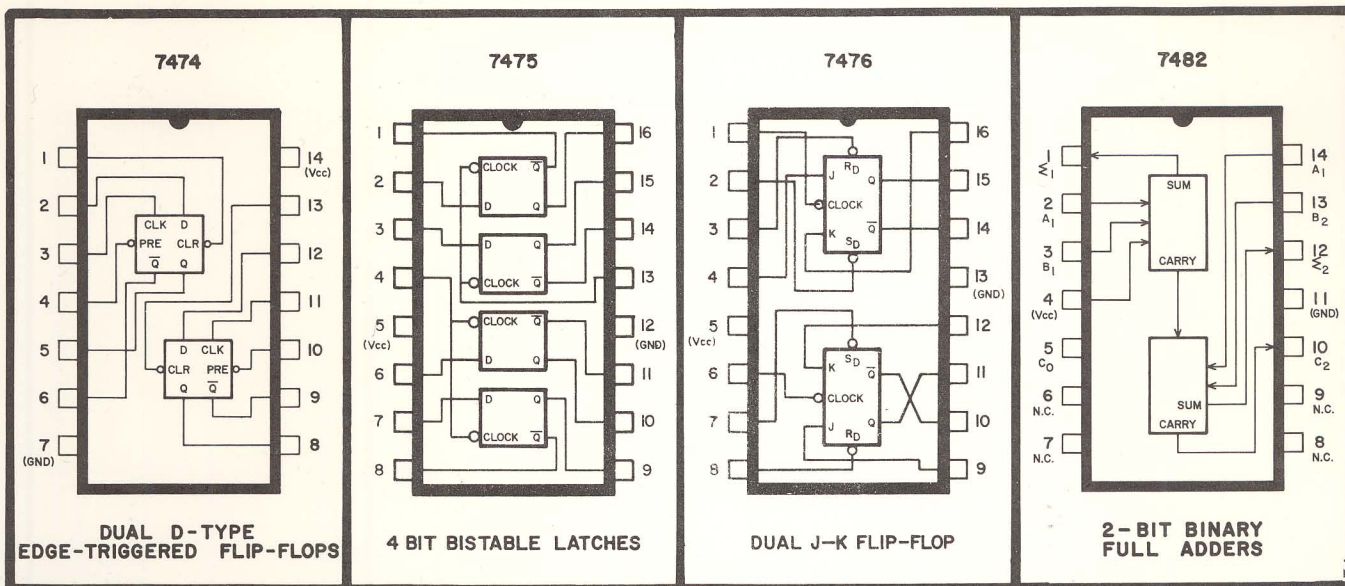
Capacitance values shown are in picofarads unless otherwise specified.



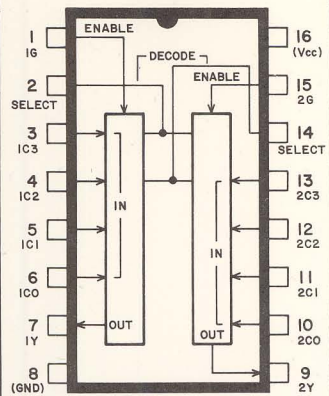
Polarized capacitors are as shown.





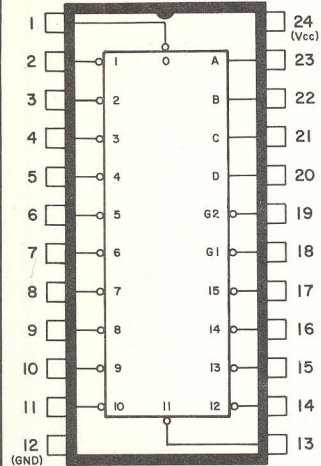


74153



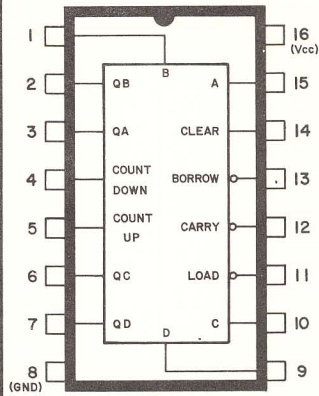
DUAL 4-LINE - TO - LINE
DATA SELECTORS/MULTIPLEXERS

74154



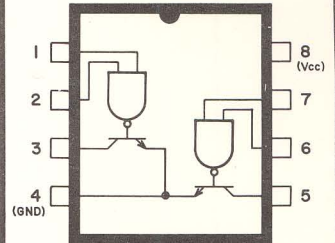
4 - LINE - TO - 16 LINE
DECODERS/DEMULPLEXERS

74192 - 74193



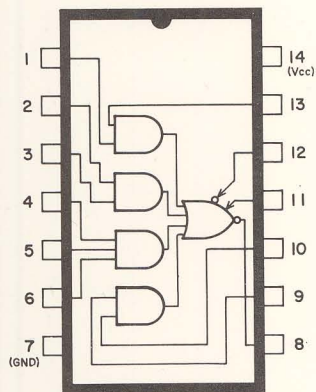
SYNCHRONOUS 4-BIT
UP/DOWN COUNTERS
(DUAL CLOCK WITH CLEAR)

75451



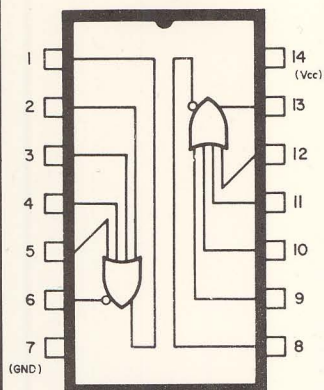
DUAL PERIPHERAL DRIVER

74H53

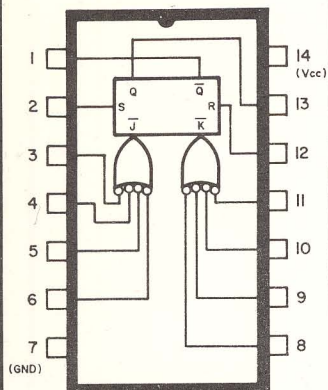


EXPANDABLE 2-2-2-3 INPUT
AND-OR-INVERT GATES

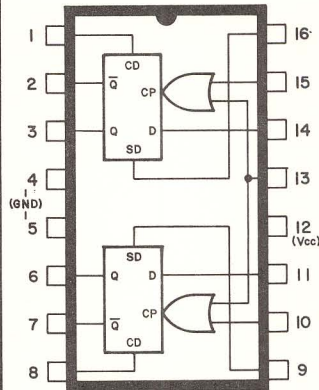
MC1023

2-4 INPUT
CLOCK DRIVER

MC1027

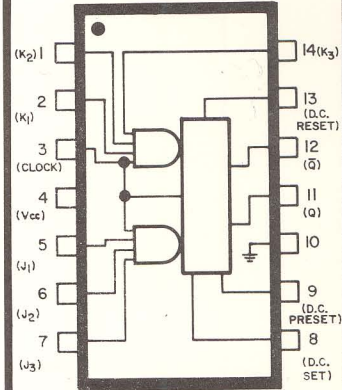
120 MHz
J-K FLIP-FLOP

9528

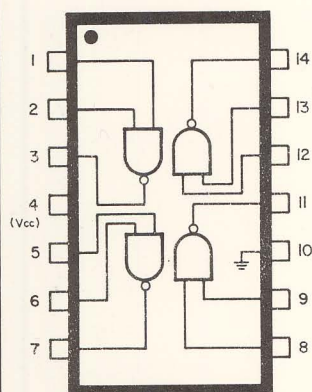


DUAL D FLIP-FLOP

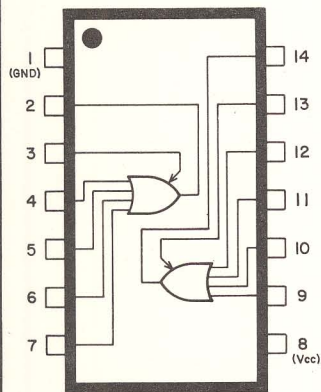
SF203

50 MHz
J-K FLIP-FLOP

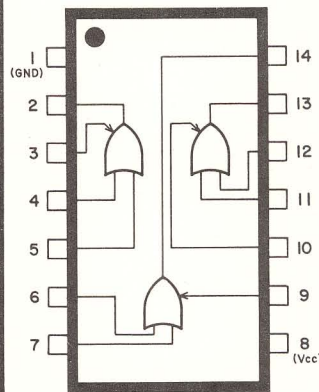
RG3222

75 MHz
TTL

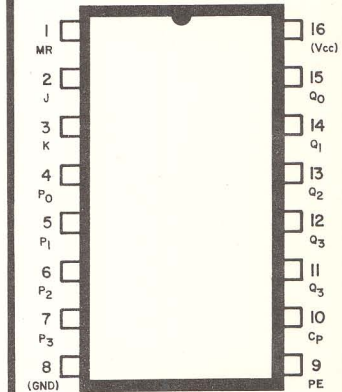
SP 334A

DUAL 4-INPUT
EXPANDABLE OR GATE

SP 375A

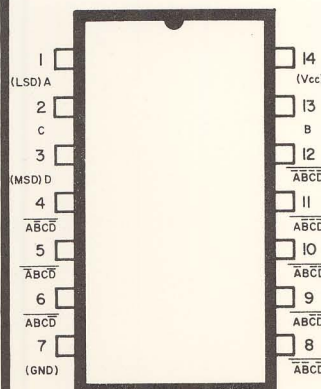
TRIPLE 2-INPUT
EXPANDABLE OR GATE

9300



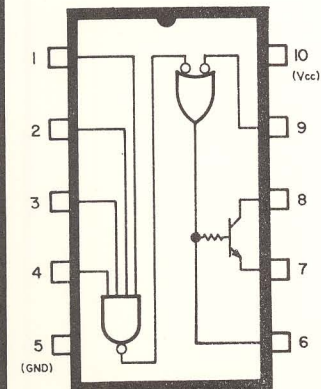
4-BIT SHIFT REGISTER

8250



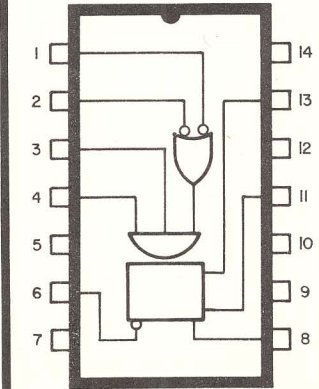
BINARY-TO-OCTAL DECODER

SH2002-P

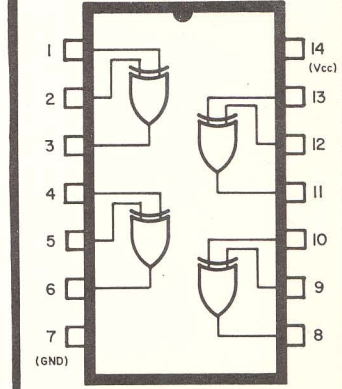


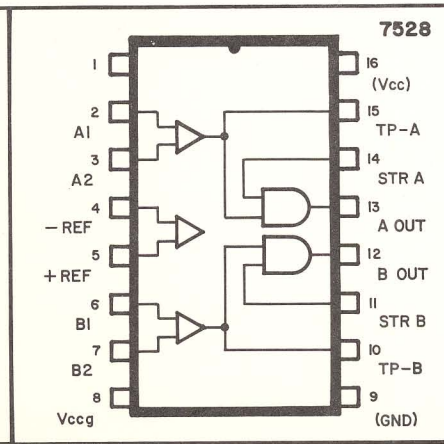
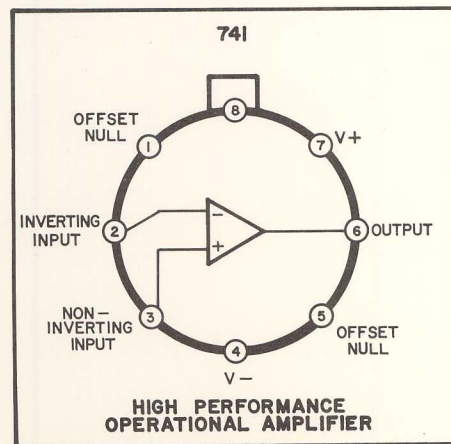
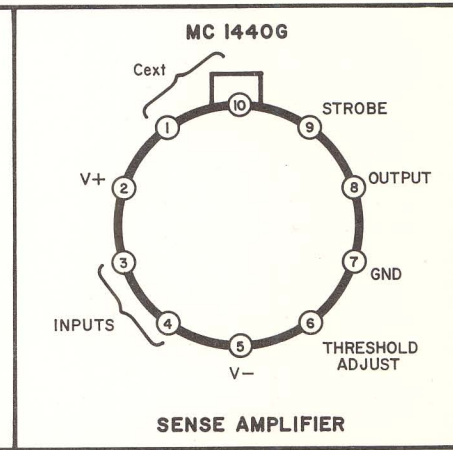
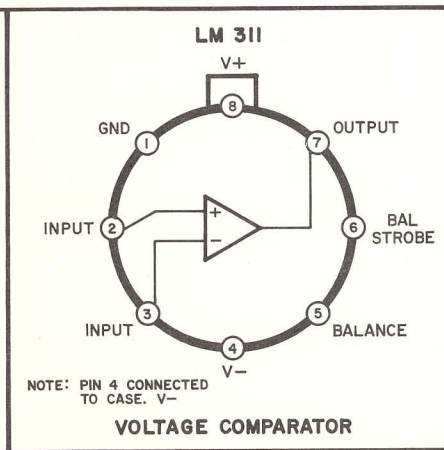
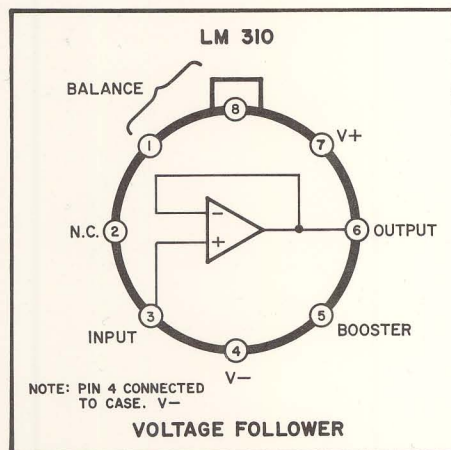
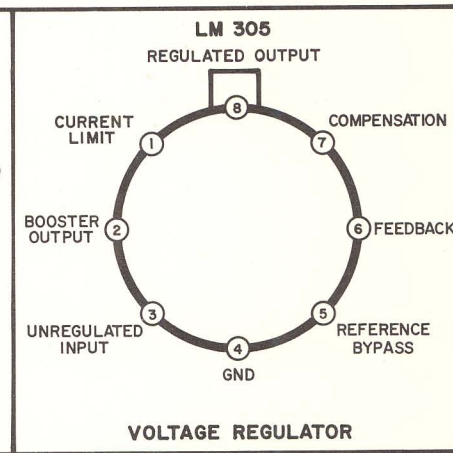
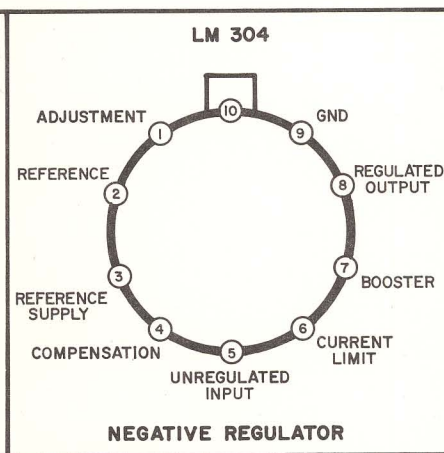
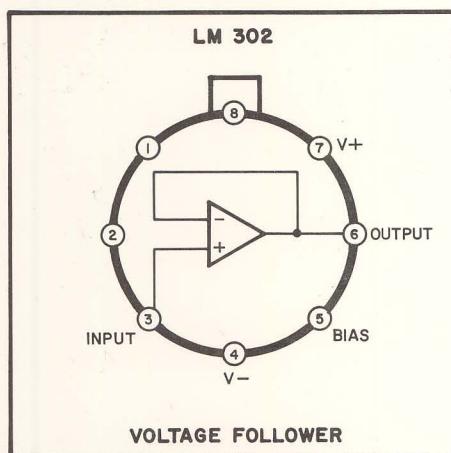
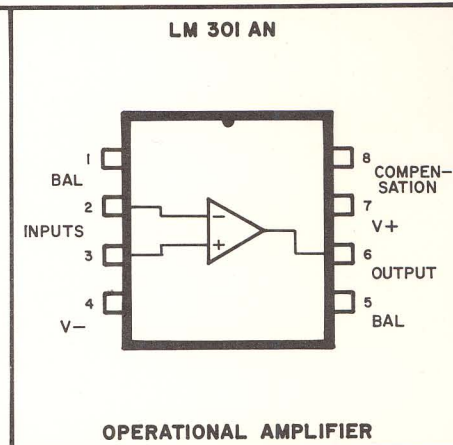
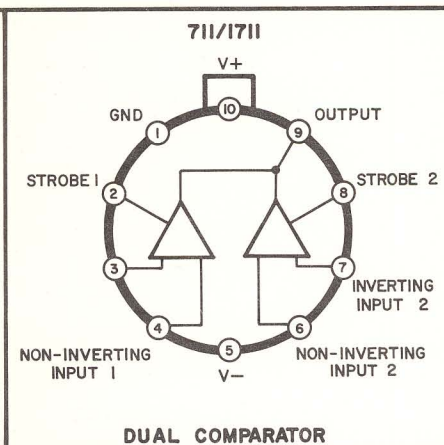
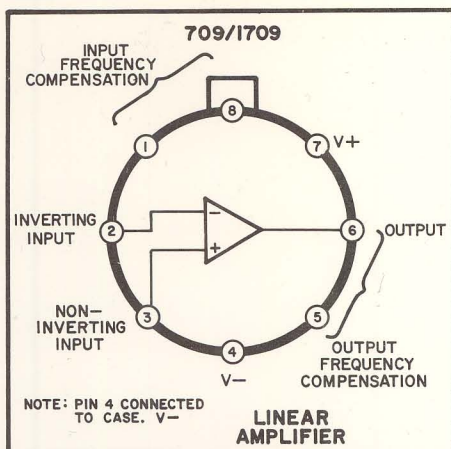
HIGH POWER DRIVER

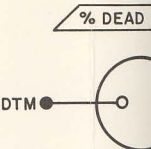
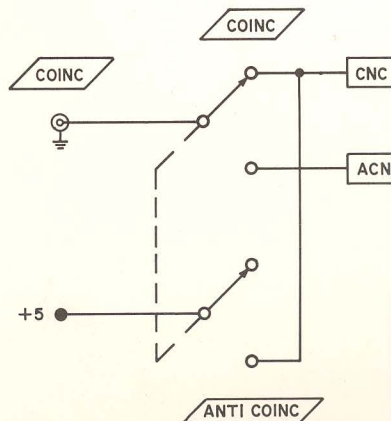
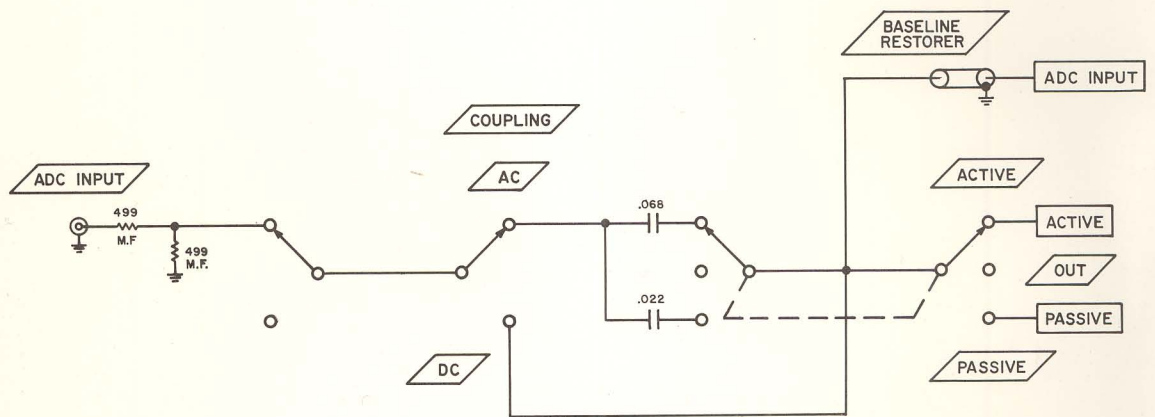
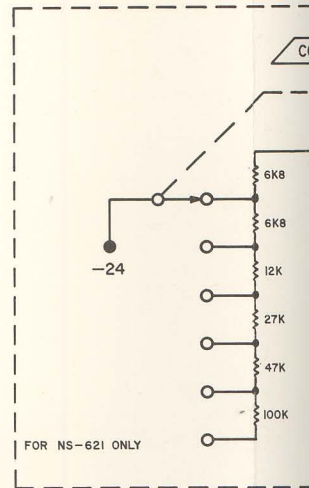
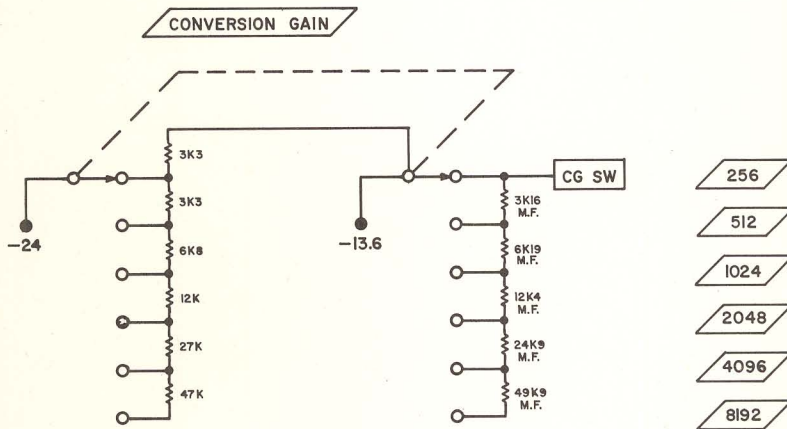
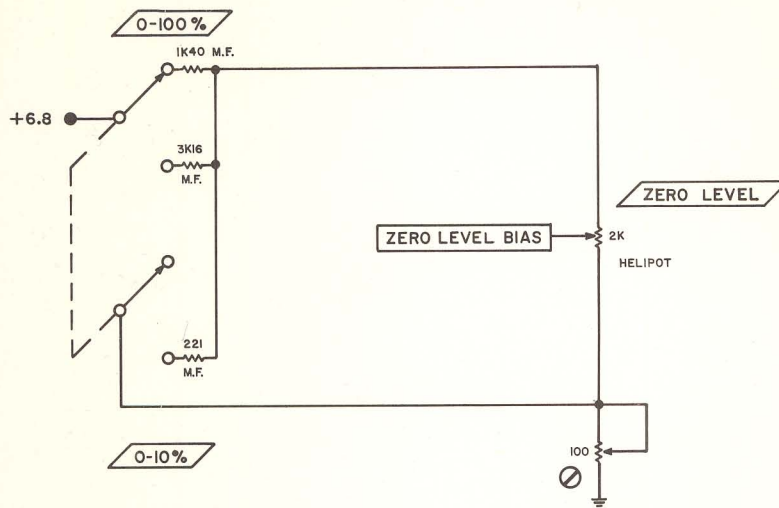
9601

RETRIGGERABLE MONOSTABLE
MULTIVIBRATOR

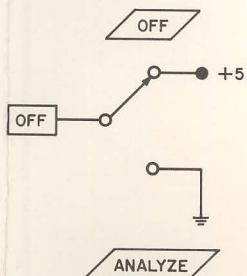
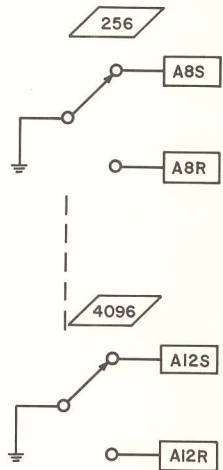
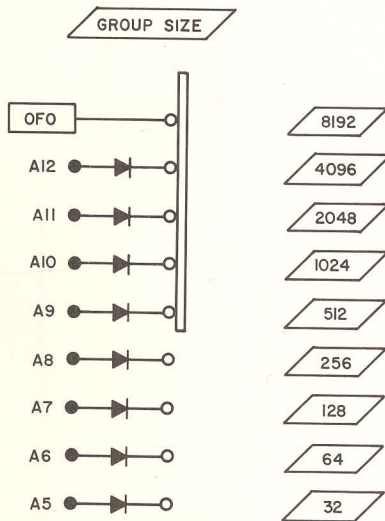
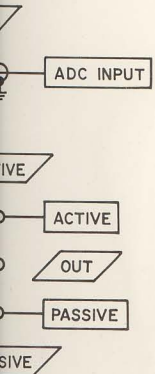
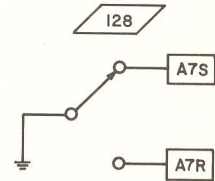
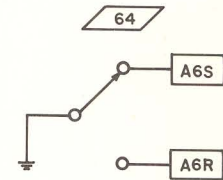
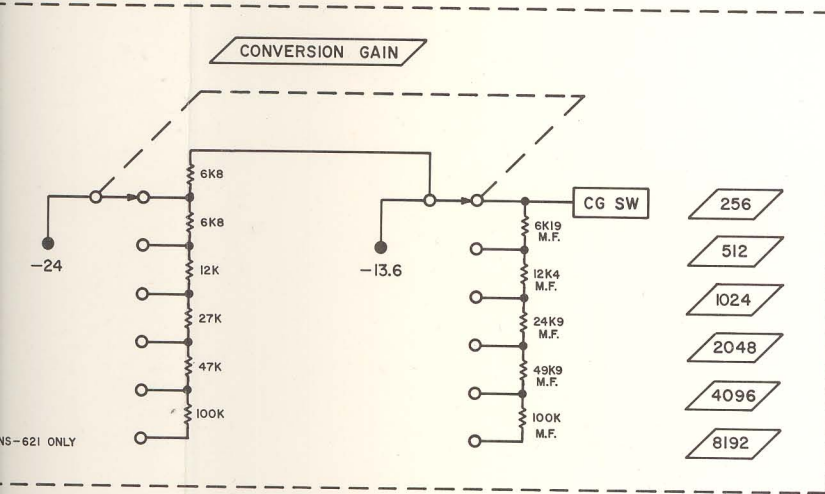
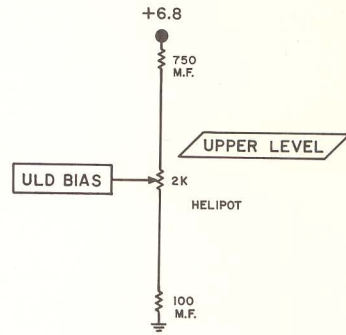
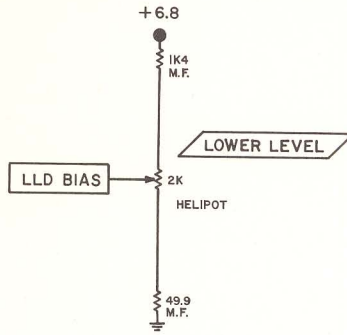
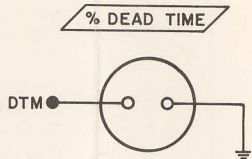
1812-P

4-2 INPUT
EXCLUSIVE OR GATE

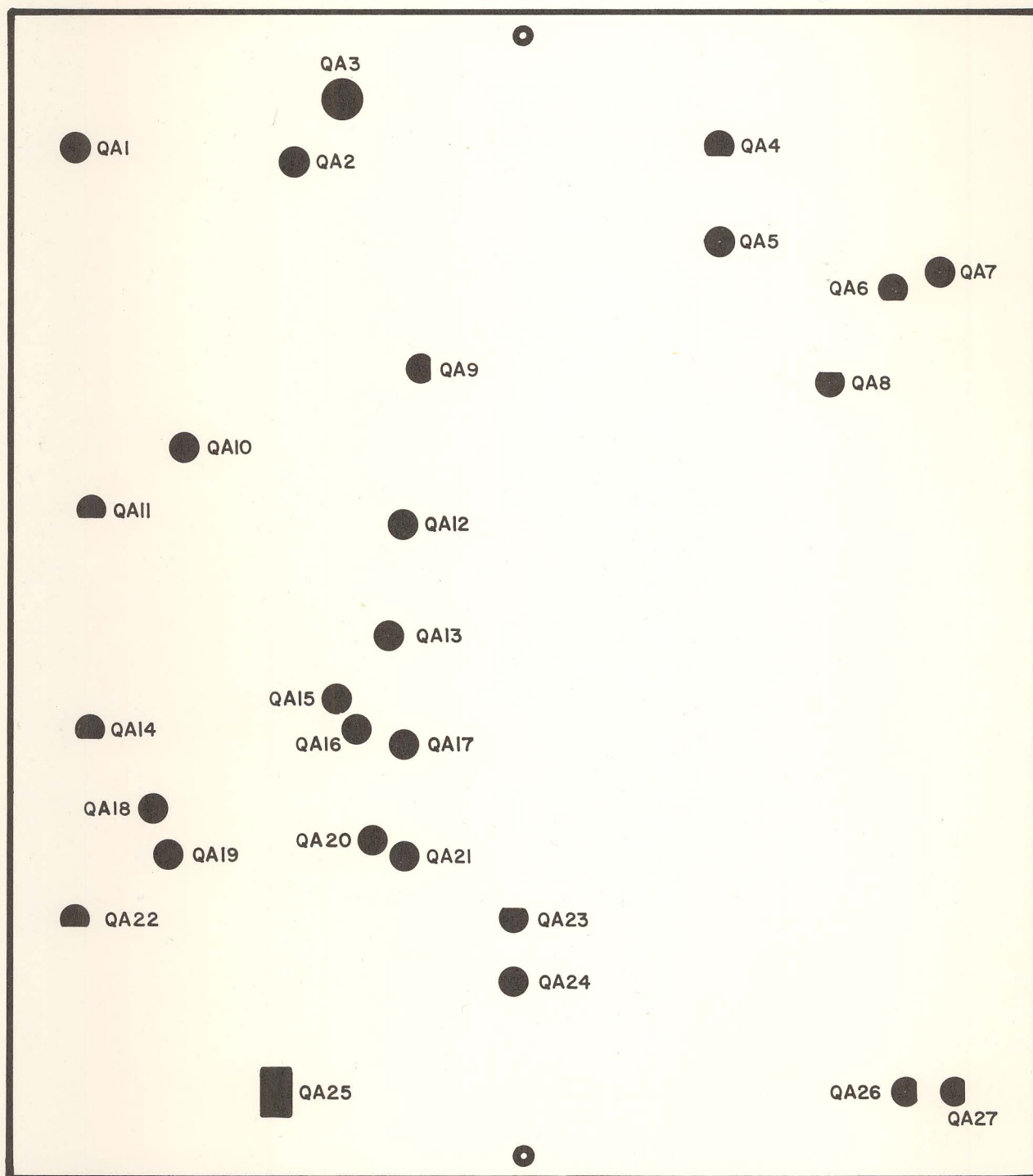




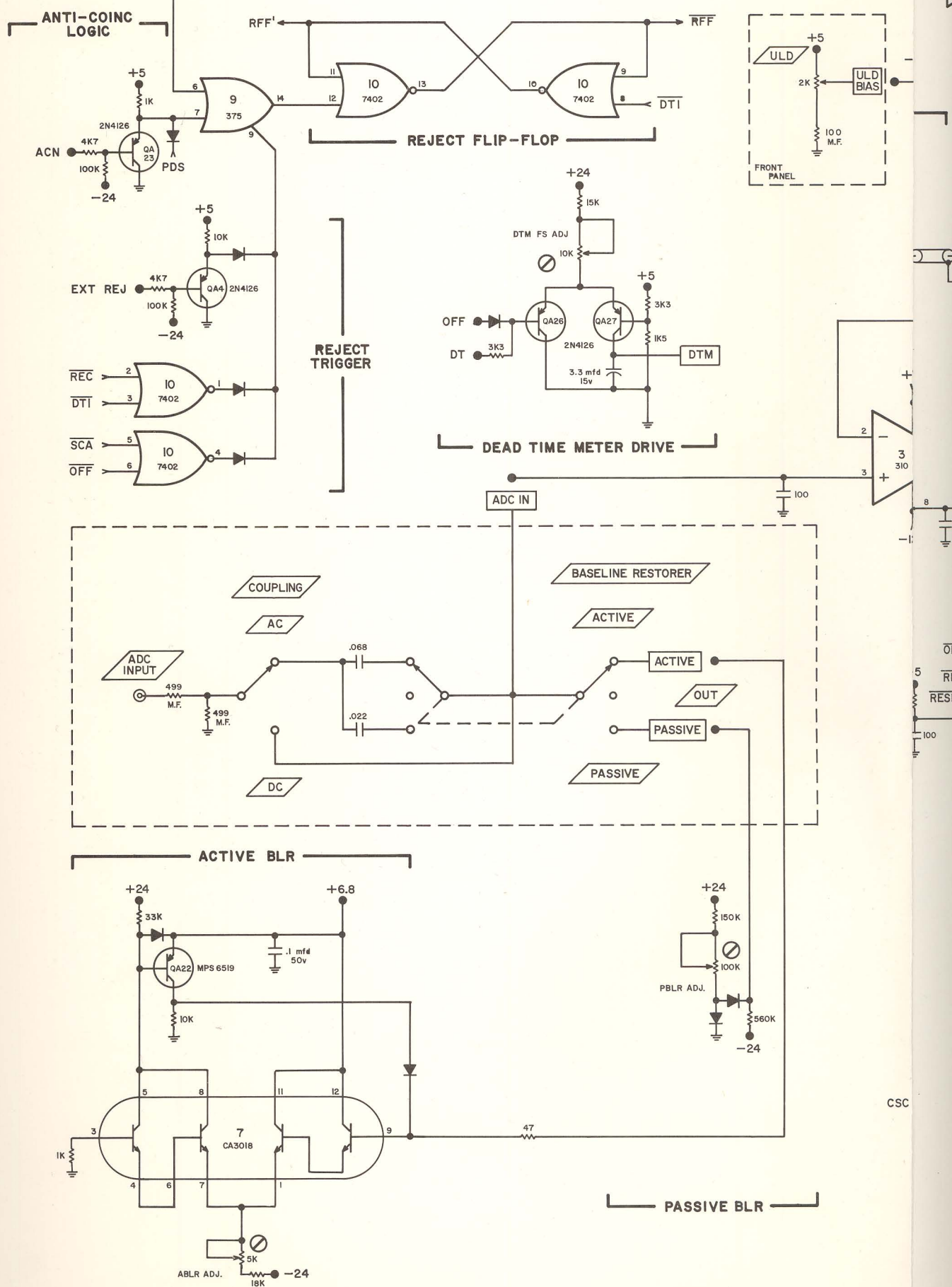
OFF

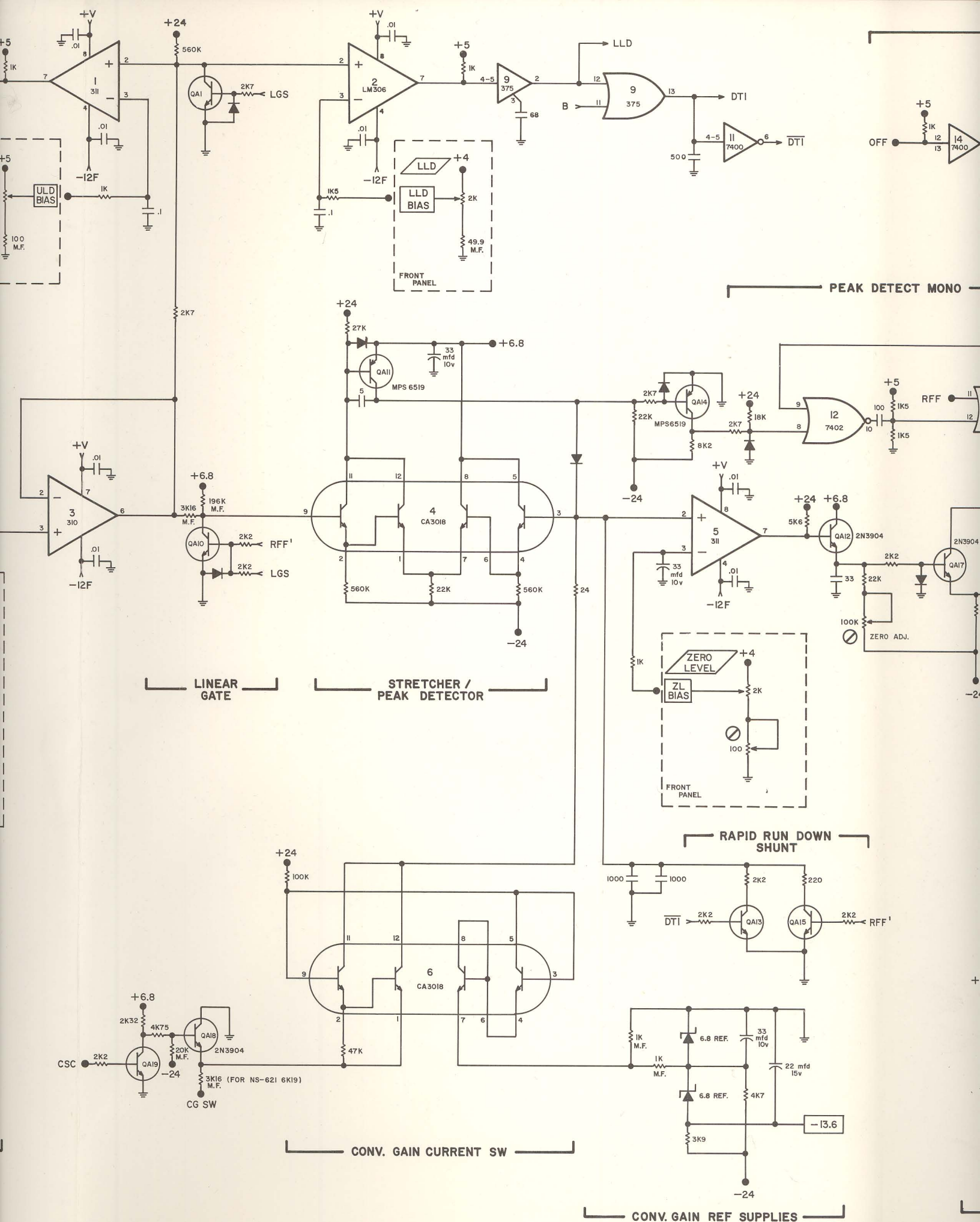


FRONT PANEL CONTROLS FOR NS-621 AND NS-623			NORTHERN SCIENTIFIC, INC.
DATE	SCALE	DRAFTSMAN	IDENT. NO.
4/27/70	2" = 1"	J. F. G.	S-50



PHYSICAL LAYOUT OF TRANSISTORS

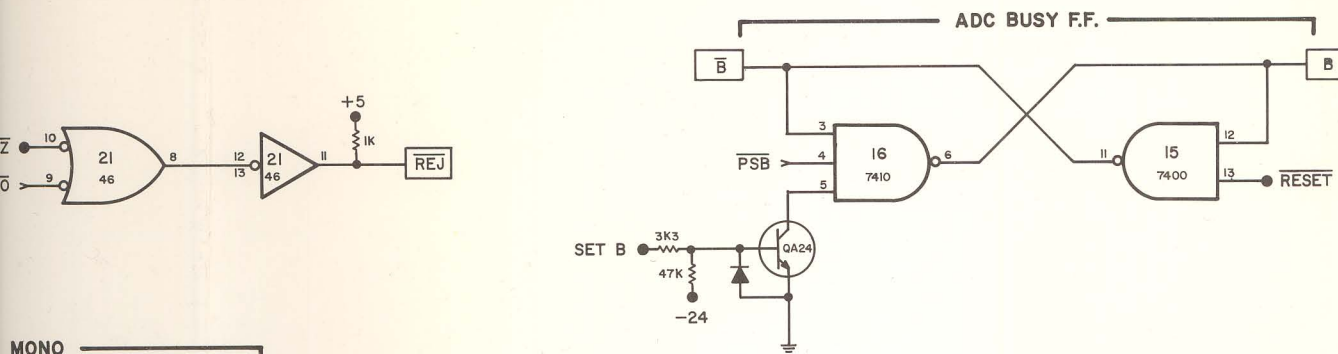




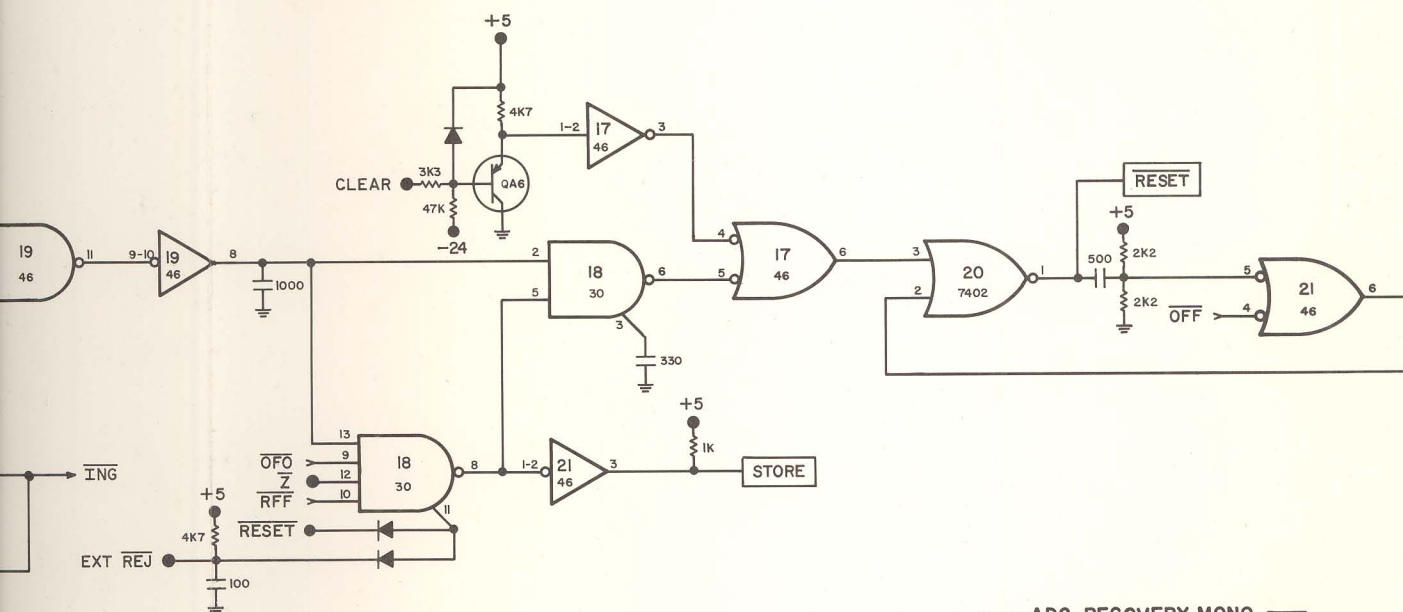
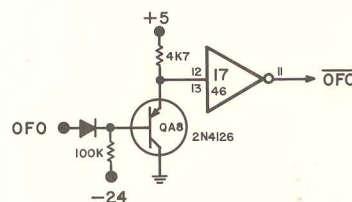
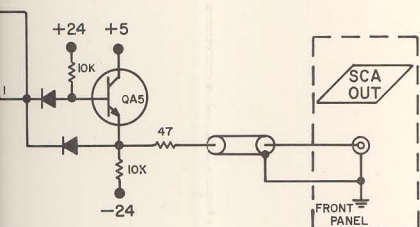


COINC LOGIC

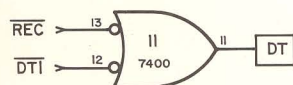
+ 6.8 V POWER SUPPLY



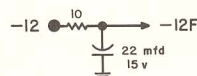
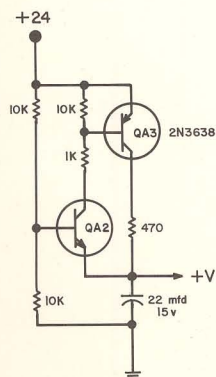
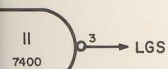
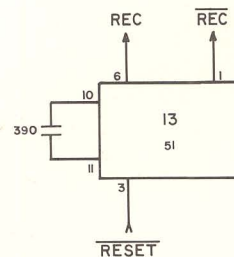
MONO



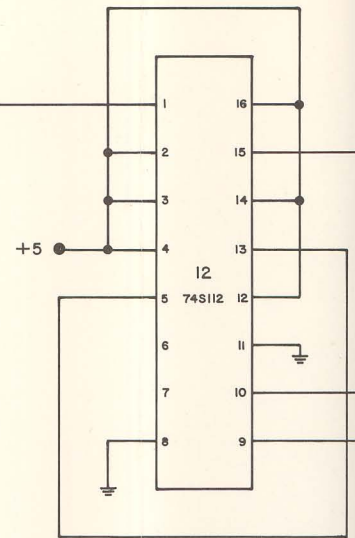
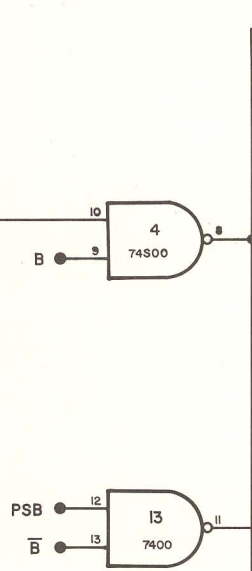
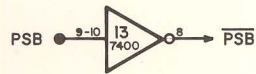
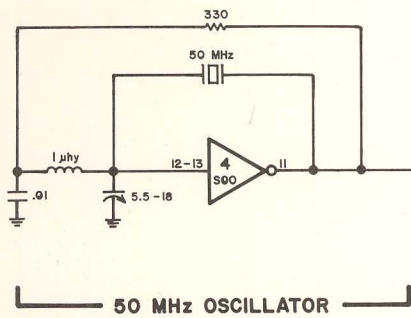
DEAD TIME SIGNAL



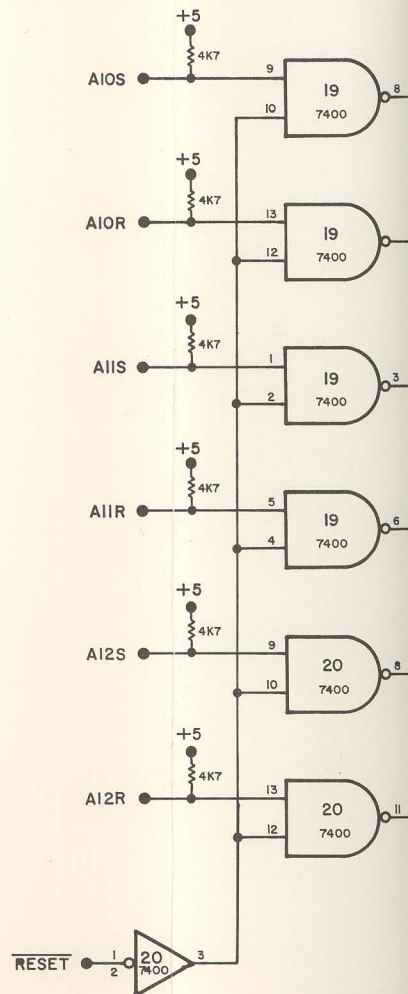
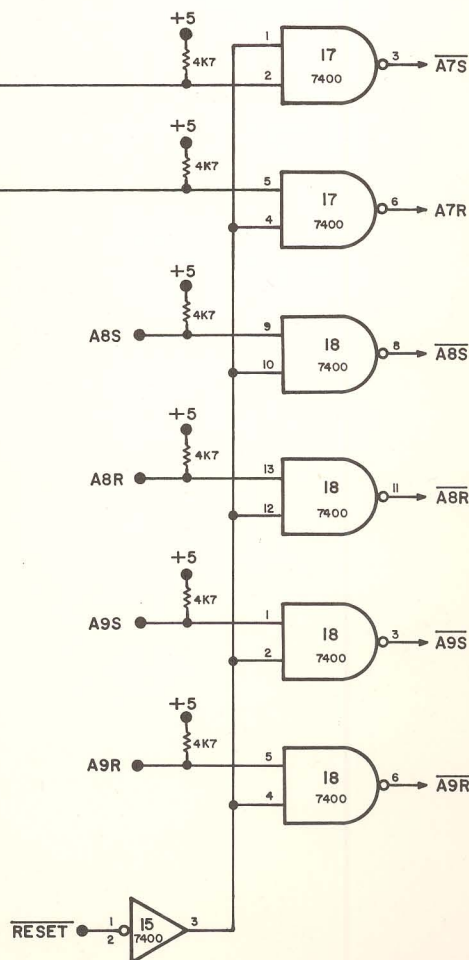
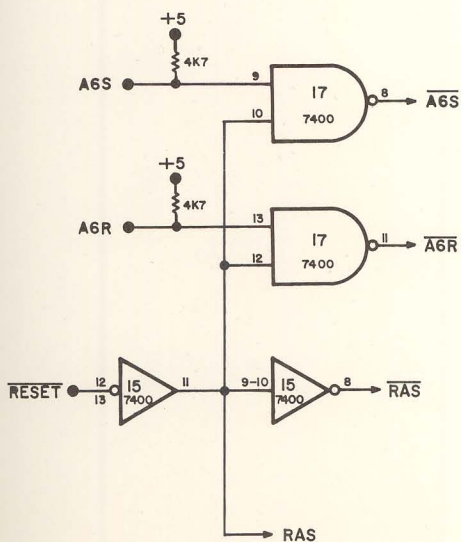
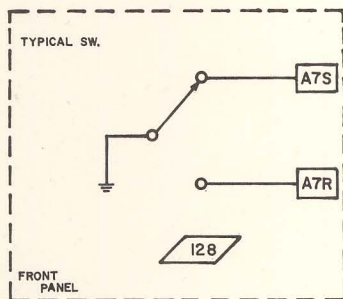
ADC RECOVERY MONO

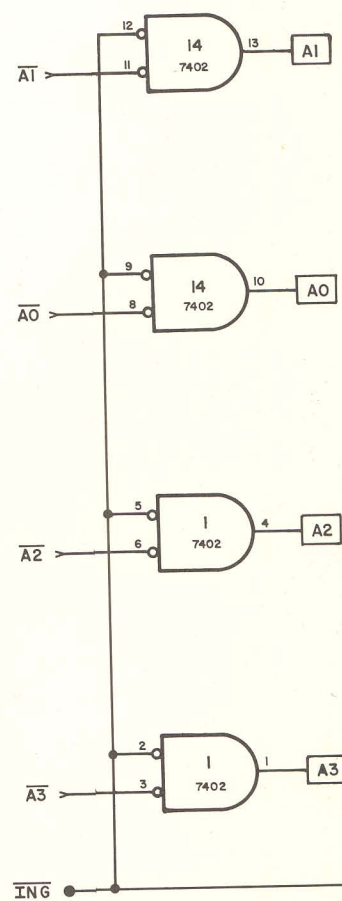
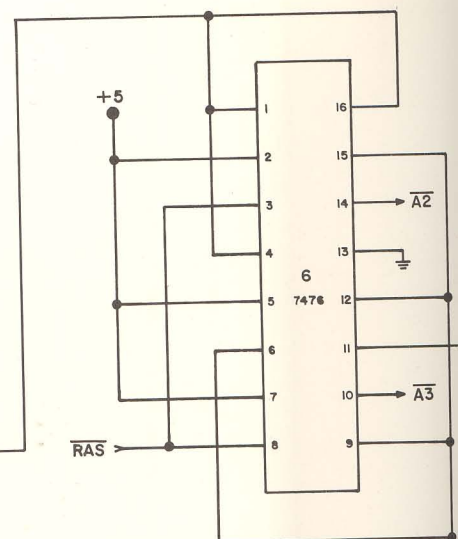


A BOARD FOR NS-621 AND NS-623			NORTHERN SCIENTIFIC, INC.
DATE	SCALE	DRAFTSMAN	IDENT. NO.
5/24/71	2" = 1"	J. F. G.	S-51

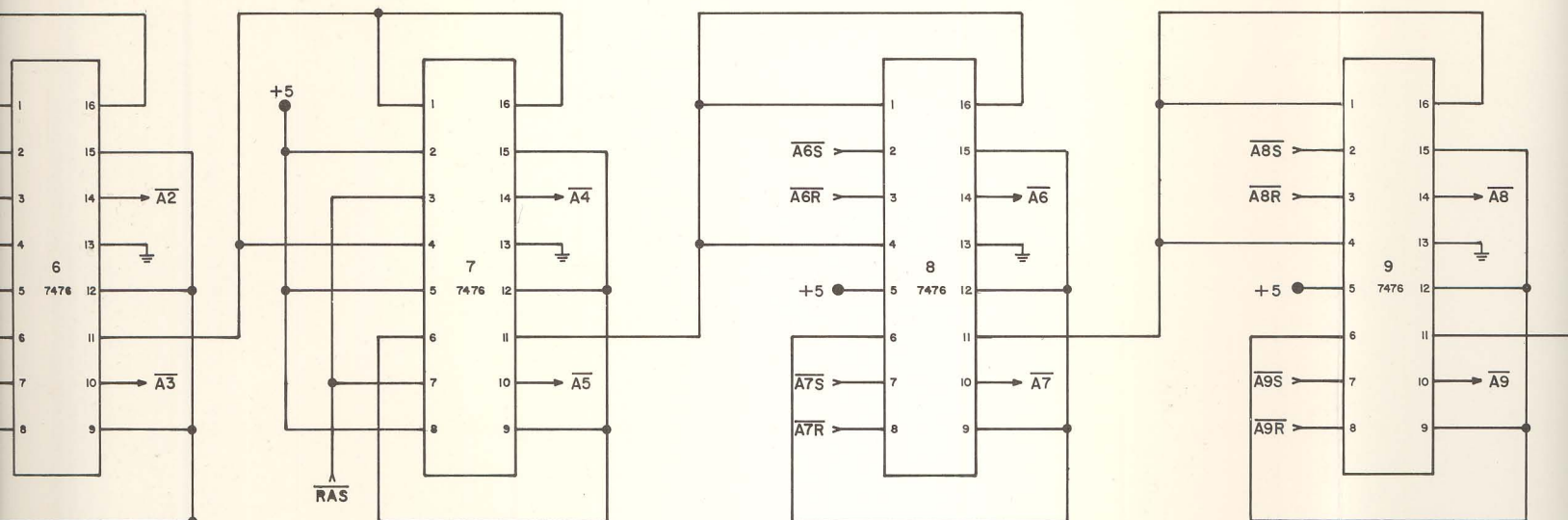


DIGITAL ZERO OFFSET RESET GATES

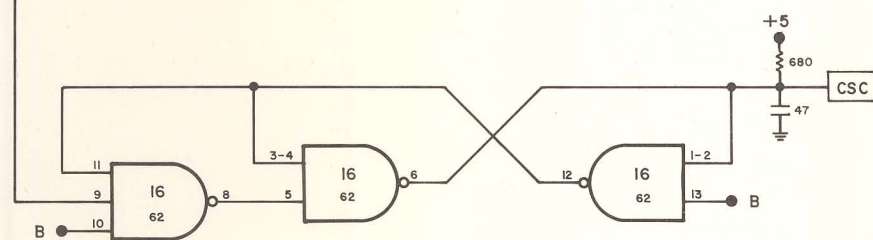




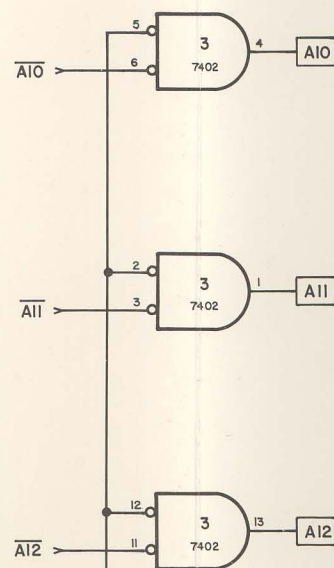
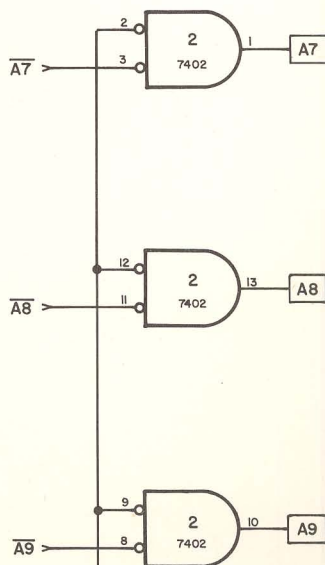
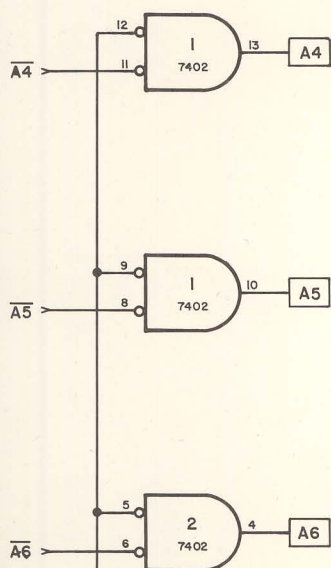
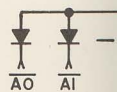
13 BIT ADDRESS SCALER

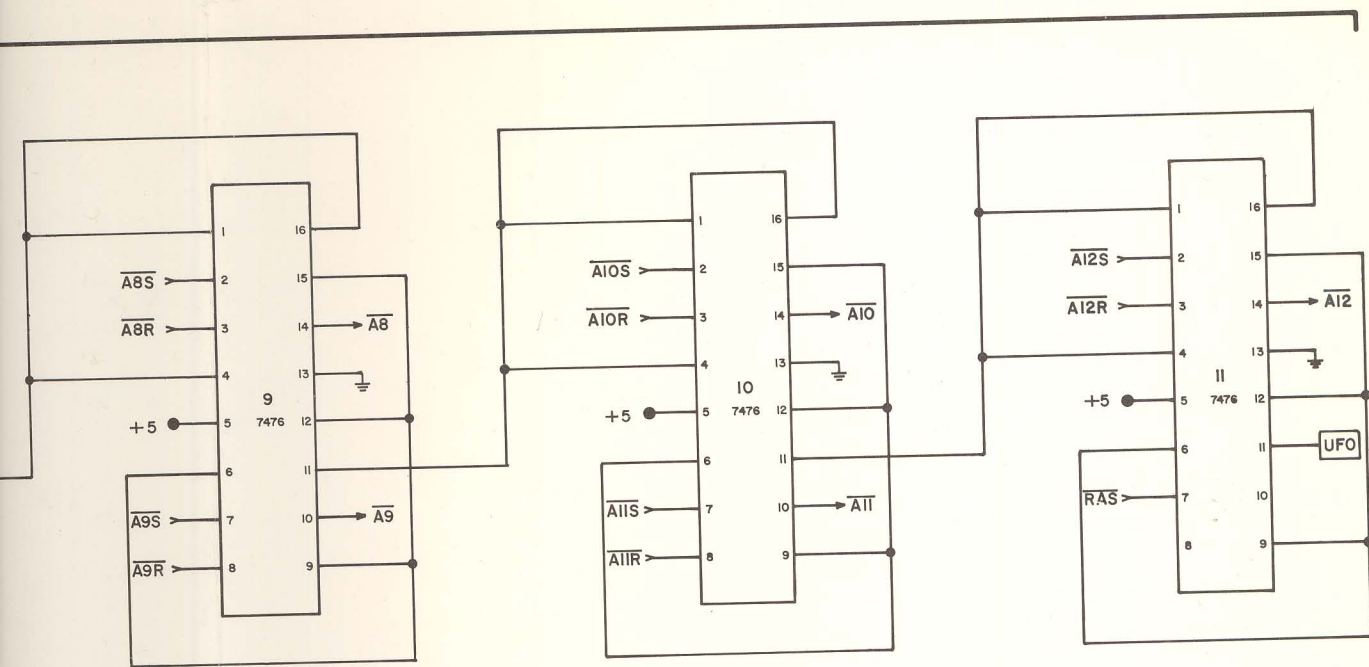


CONV GAIN CURRENT SW. CONTROL F.F.



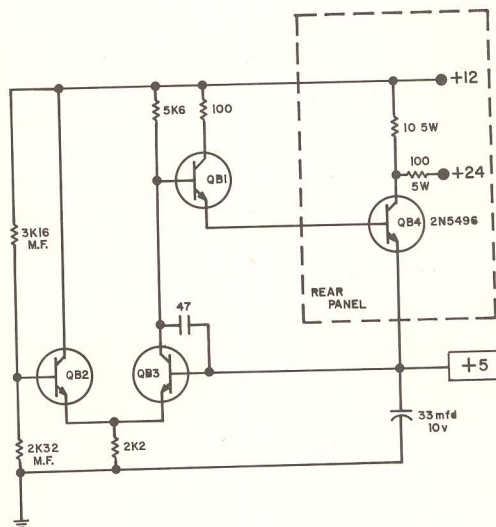
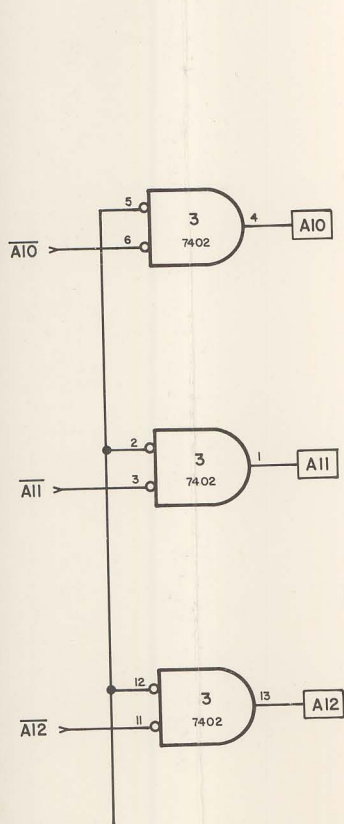
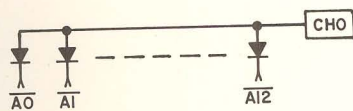
CHANNEL



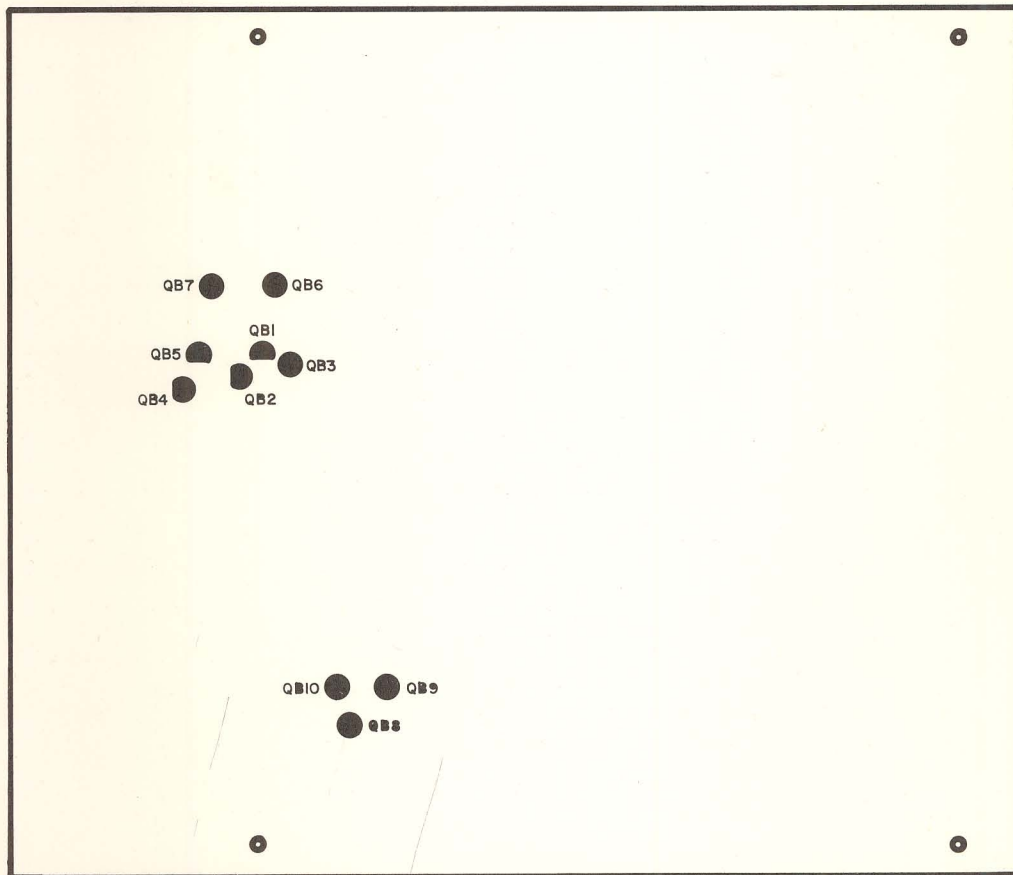


UNDERFLOW & 8192
OVERFLOW FLIP-FLOP

CHANNEL ZERO AND GATE

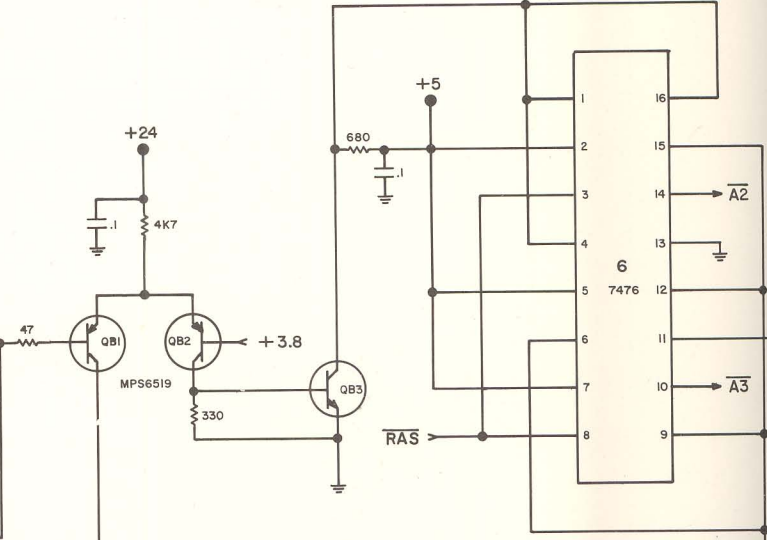
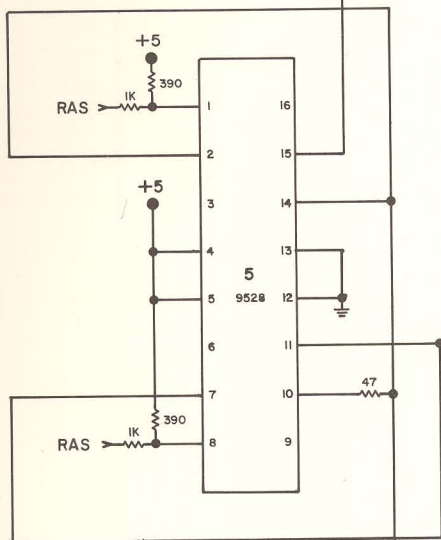
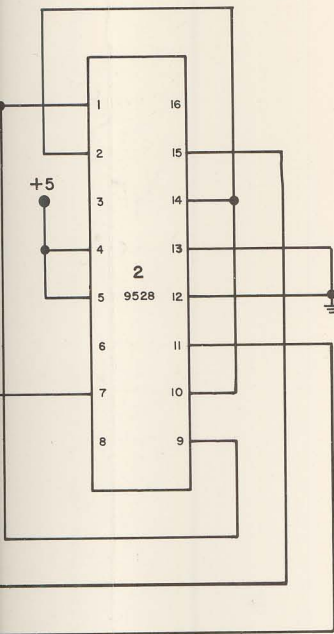
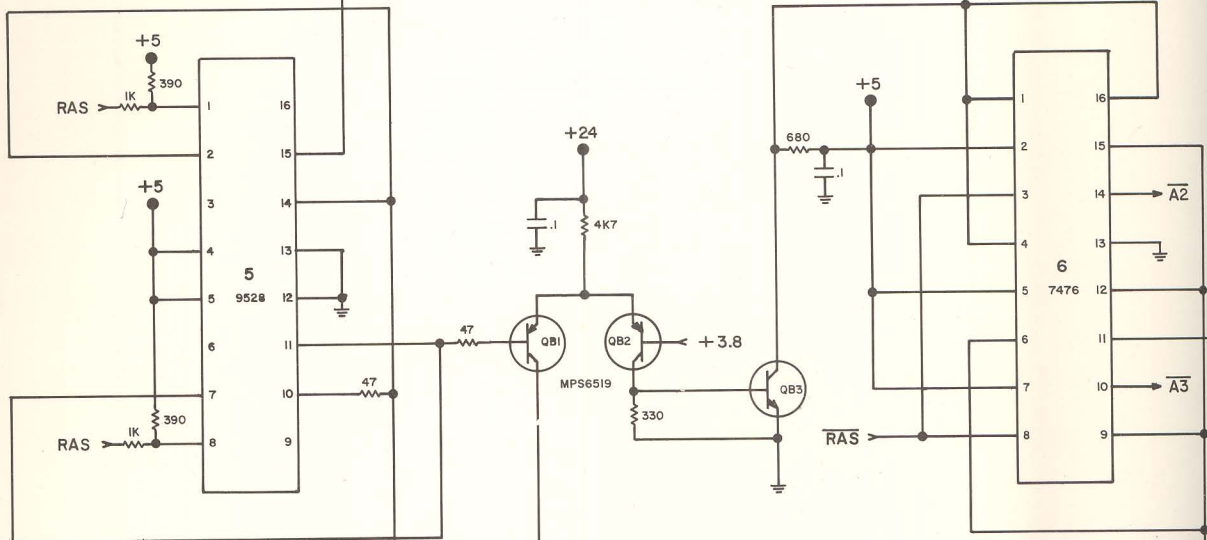
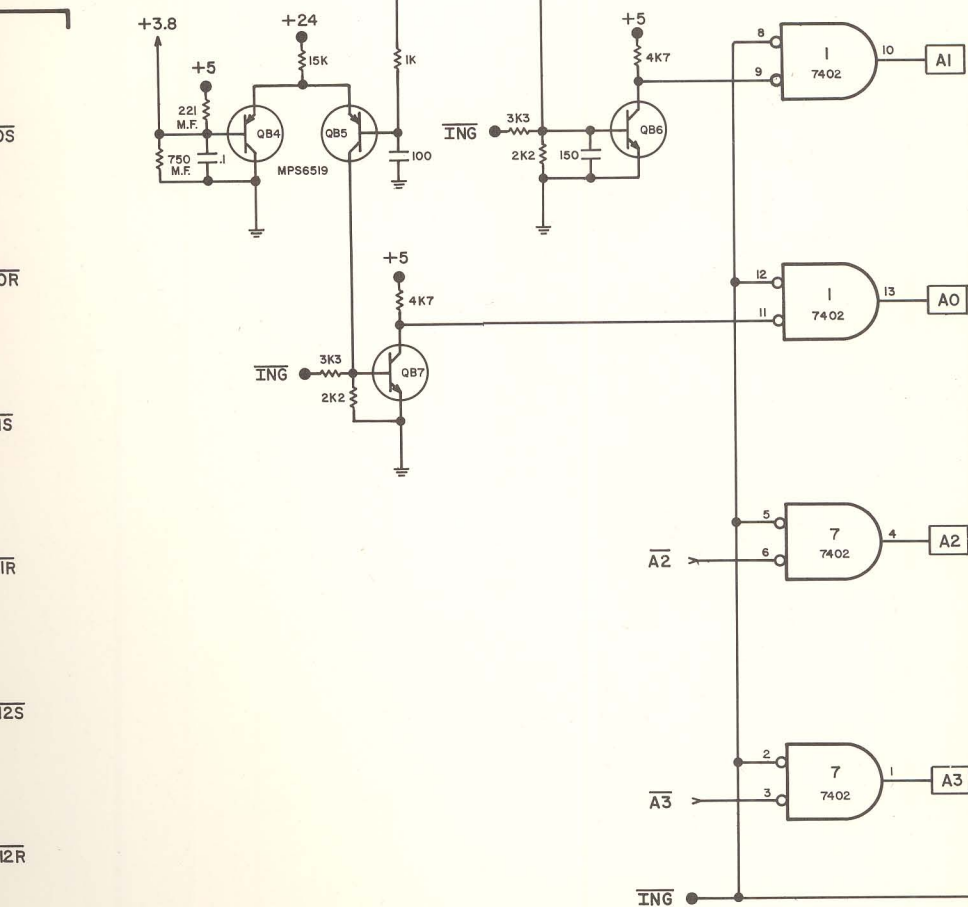
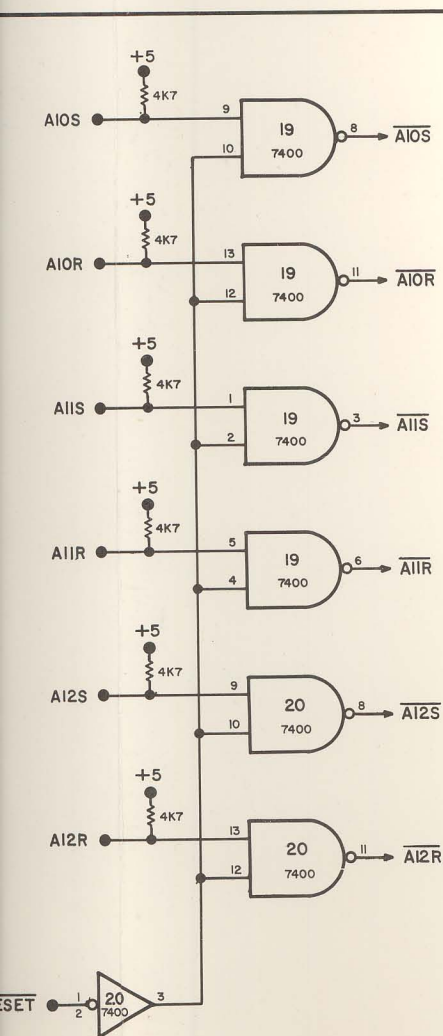


B BOARD FOR NS-621			NORTHERN SCIENTIFIC, INC.
DATE	SCALE	DRAFTSMAN	IDENT. NO.
10/27/72	2" = 1"	J. F. G.	S-52

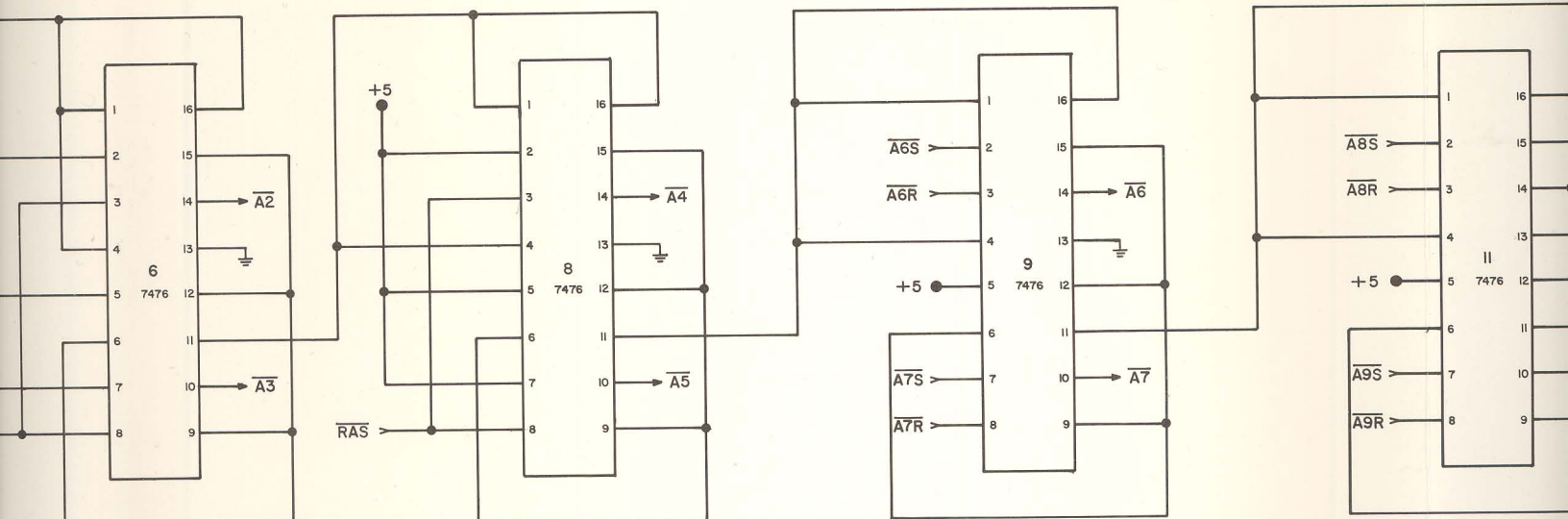


PHYSICAL LAYOUT OF TRANSISTORS

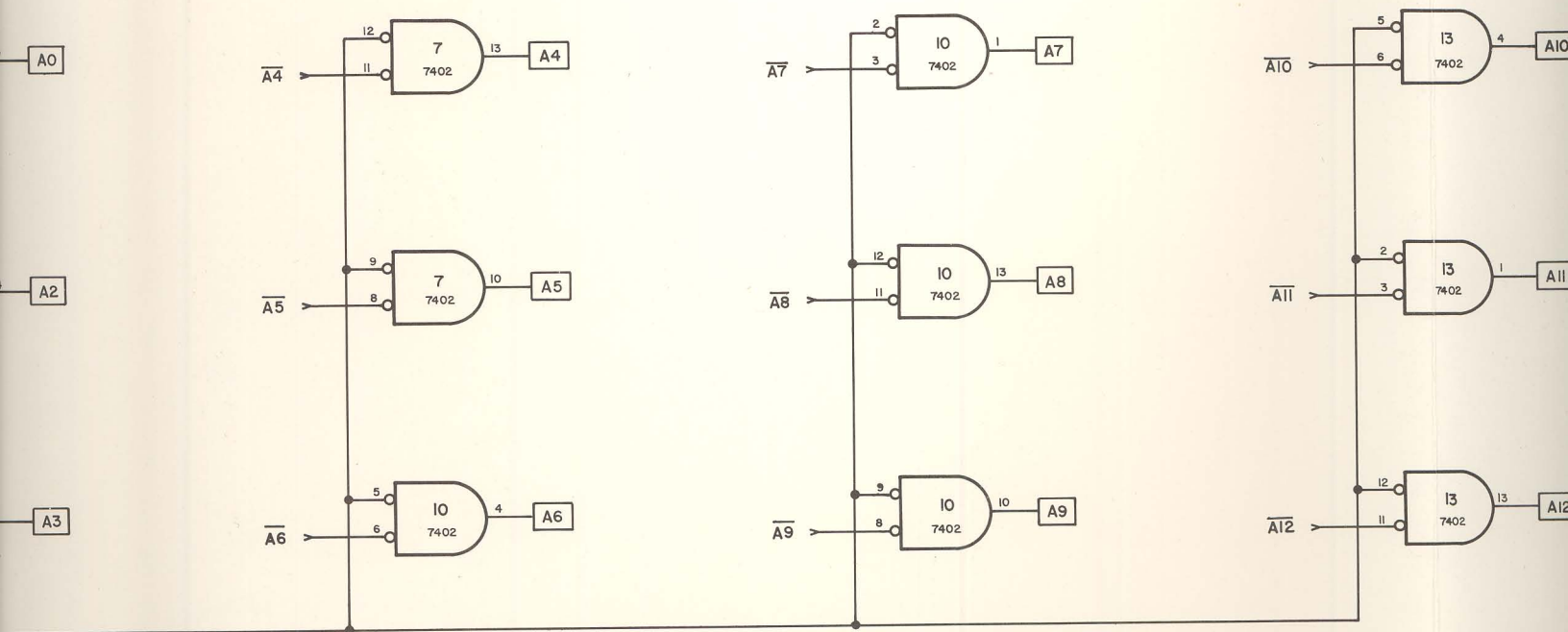
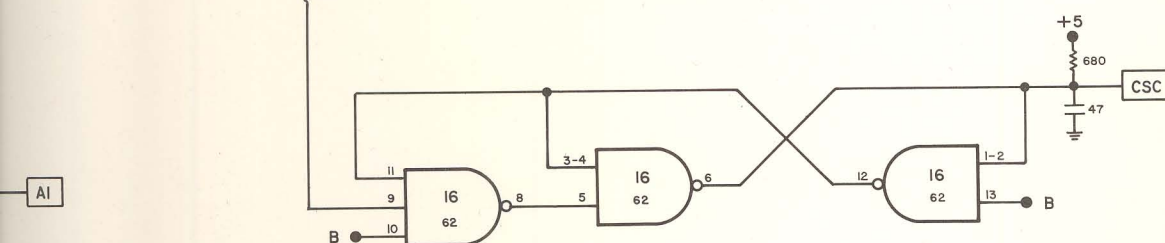
CLOCK SYNCHRONIZING FF'S

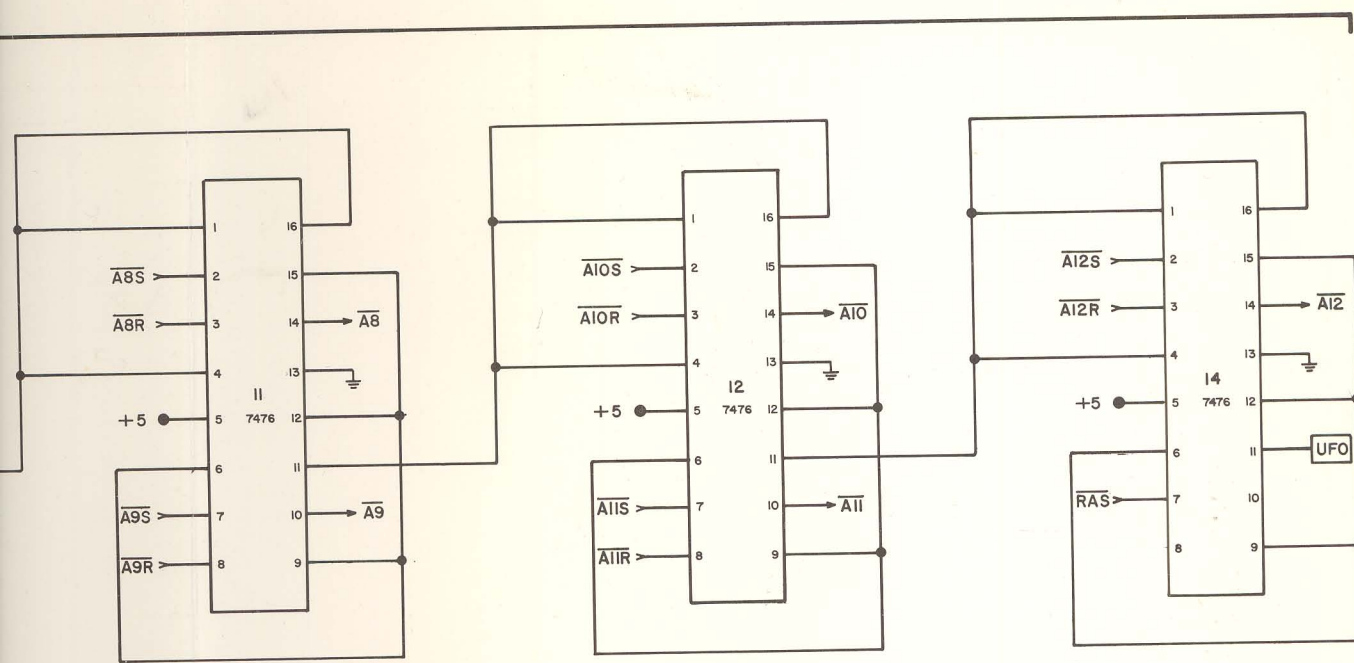


13 BIT ADDRESS SCALER



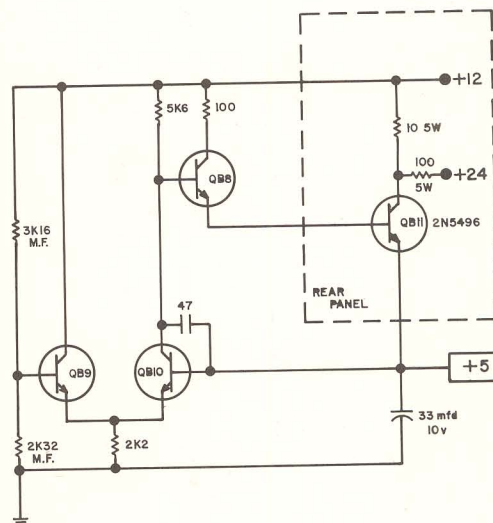
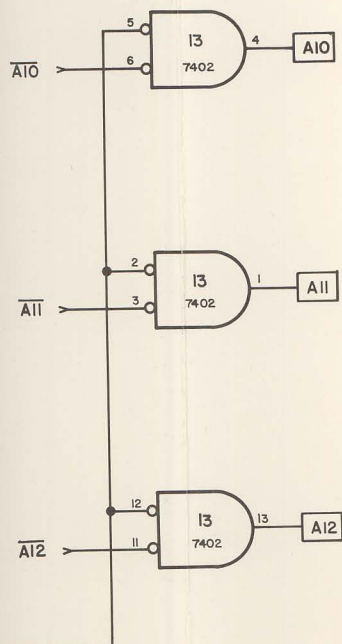
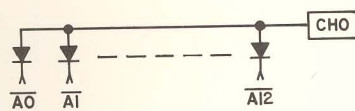
CONV GAIN CURRENT SW. CONTROL FF.





UNDERFLOW & 8192
OVERFLOW FLIP-FLOP

CHANNEL ZERO AND GATE



B BOARD FOR NS-623			NORTHERN SCIENTIFIC, INC.
DATE	SCALE	DRAFTSMAN	IDENT. NO.
9/17/71	2" = 1"	J. F. G.	S-53