

**Model GT304  
Serial I/O Board**

# User Manual

## Model GT304 Serial I/O Board

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MODEL 304

SERIAL I/O BOARD

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## FEATURES

- \* Direct Replacement for DLV11-J Serial I/O Board
- \* Totally Compatible with DEC Software
- \* All Standard DEC Features
- \* Each Port Independently Configured for Either EIA RS-232, RS-422, or RS-423
- \* Four Level Vector Interrupt Structure, Ideal for Multi-User Applications
- \* Channel 3 can be Independently Configured as System Console

## GENERAL

The Model 304 is a four channel serial I/O port for interfacing DEC's Q-bus to asynchronous serial data channels. The 304 is a direct replacement for the DEC four channel Serial I/O Board (Model DLV11-J). It is packaged on the standard 8.9" x 5.2" DEC style dual width board and is electrically and mechanically compatible with DEC's LSI-11, 11/2, and 11/23 Microcomputer Series.

Each channel consists of a UART which receives and converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. The UART's transmitter converts the computer's parallel data into serial form and automatically adds start, parity, and stop bits.

Each channel's data length can be configured for 7 or 8 bits. Parity is jumper selectable, odd or even, and parity checking and generation can be inhibited. Stop bits are jumper selectable; one or two.

The 304 can be used in a wide range of interface applications including printers, terminals, peripherals and remote data acquisition systems. Each channel can operate at one of nine jumper selectable data rates, from 150 to 38.4K baud, which are generated by an on-board clock. The user may also provide an external clock.

The line characteristics of each channel can be jumper configured to operate in accordance with EIA standard RS-232,

RS-422, or RS-423. Twenty milliamp current loop operation is possible when used in conjunction with the DEC DLV11-KA.

A unique feature of the 304 is the capability to support the LSI 11/23 four level interrupt structure. Channel 3 may also be configured as the system console, independent of the other three channels. Special pins are provided on each I/O connector which can be used to constantly assert the data terminal ready lines of the peripheral, and each channel can also be configured to provide a pulse output to control a paper tape reader.

### SPECIFICATIONS

Bus Interface	Q-bus, DEC LSI-11, 11/2 & 11/23 compatible
Data Characteristics	
(Each Channel)	
No. of Channels	4
Data Protocol	Asynchronous serial
Baud Rates	Jumper Selectable 150, 300, 600, 1.2K, 2.4K, 4.8K, 9.6K, 19.2K 38.4K, Ext.
Line Discipline	Jumper Selectable EIA RS-232C, RS-422, or RS-423
Data Bits	Jumper Selectable 7 or 8
Stop Bits	Jumper Selectable 1 or 2
Parity	Jumper Selectable Odd, Even, None
Addressing	
Base Address Range	Jumper Selectable 776000 <sub>8</sub> to 777740 <sub>8</sub>
Console Address	Jumper Selectable 777560 <sub>8</sub> Channel 3 Only
Interrupts	
Priority Level	Jumper Selectable LSI-11 & 11/2 Level 4, Jumper Selectable LSI-11/12 Level 4, 5, 6, or 7
Base Vector Range	Jumper Selectable 0 to 740 <sub>8</sub>
Console Vector	60 only when console option is enabled

## Mechanical & Environmental

Dimensions	DEC LSI-11 standard 8.9" x 5.2" half quad board
Power Requirements	5V @ 1 Amp, 12V @ .2 Amps
Bus Loading	1.5 Std. AC/1 Std. DC Load
Operating Temperature Range	0 to 55°C
Storage Temperature Range	0 to 75°C
Relative Humidity	To 85% non-condensing
Mating Connector	Amp #87133-5, Pin #87165-2

## Q-BUS INTERFACE

The Q-Bus Interface consists of address/data transceivers, an address comparator, console decode logic and I/O select and control logic.

During the addressing portion of a bus cycle, the Address/Data transceivers are in the receive mode. Address lines 12 through 5, gated by bus line BBS7, are compared to the base address setting selected by the address selection jumpers. When the correct address is asserted by the processor, the comparator output (BDSEL) is asserted. This in conjunction with the assertion of BSYNC is used by the Select and Control Logic (SCL) to select the appropriate on-board register for the remainder of the bus cycle.

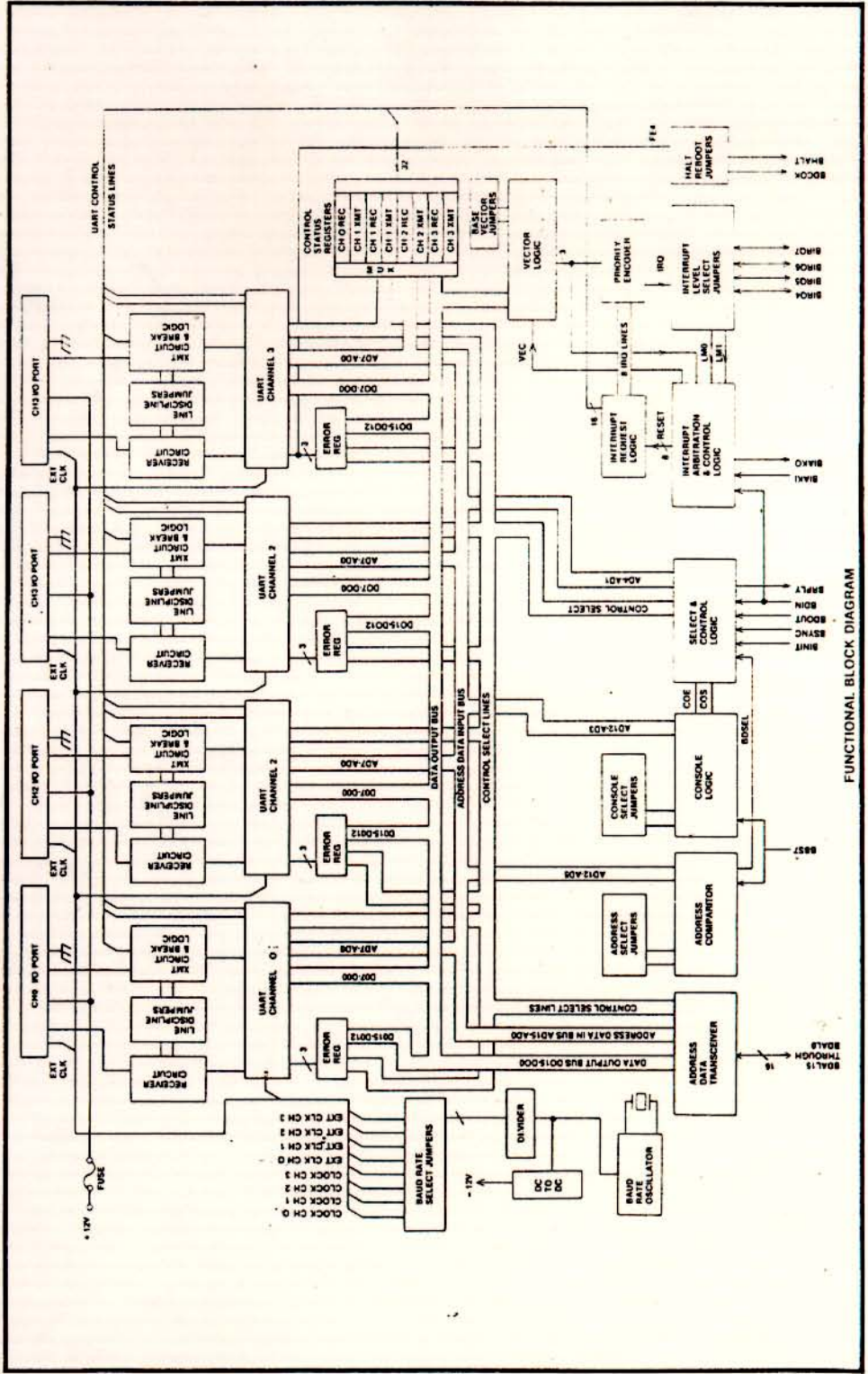
If the processor is performing a read, then the BDIN line is decoded in conjunction with the SCL to enable the tri-state buffers of the selected register, place the bus transceivers in their transmit mode, and then assert the BRPLY line.

If the processor is performing a write operation, then the register which is to be written to is selected during the Address/Data portion of the bus cycle and the BDOUT line is used to clock the latches of the receiving register, and to assert BRPLY.

## INTERRUPT LOGIC

The interrupt handling logic consists of interrupt request logic, a priority encoder, level circuit logic, arbitration control, and vector logic.

The interrupt request logic consists of eight latches; one for each transmit or receive CSR. In order to generate an interrupt, two requirements must be met. First, the interrupt



MODEL 304  
Functional Block Diagram

enable bit (Bit 6) in either the transmit or receive CSR must be set, and second, the appropriate condition flag must be set (Bit 7). These two logically anded signals clock the flop. The outputs of all eight flops are fed into the priority encoder. When the output of any flop goes high, the priority encoder generates a master interrupt request (IRQ). This signal is fed into the level select logic which in turn asserts the appropriate BIRQ lines. At the same time the arbitration logic monitors the bus to determine if a device on a higher interrupt level is requesting. If not, then when the interrupt grant signal BIAKI is received, the appropriate vector as determined by the priority encoder is placed on the bus, and if more than one channel is requesting, the channel of highest priority is cleared leaving the lower priority requests pending. Table 1 gives the priority level of each channel.

<u>Channel</u>		<u>Level</u>		<u>Vector Offset</u>
Channel 0	Receive	0	Highest Priority	Base Vector +0
Channel 1	Receive	1		Base Vector +10
Channel 2	Receive	2		Base Vector +20
Channel 3	Receive	3		Base Vector +30
Channel 0	Transmit	4		Base Vector +4
Channel 1	Transmit	5		Base Vector +14
Channel 2	Transmit	6		Base Vector +24
Channel 3	Transmit	7	Lowest Priority	Base Vector +34

TABLE 1

#### CONSOLE CHANNEL

When the console enable jumper is installed, Channel 3 will respond to the address of  $177560_8$ , and the receiver will always have a vector address of  $60_8$ . The transmitter vector will be  $64_8$ . The console mode of operation is independent of the board's base address.

#### UART

Each channel consists of a Universal Asynchronous Receiver Transmitter (UART) which receives and converts serial data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. If a transmission error is detected, the nature of the error is outputted to an error



register which is read when the receive data register is read. Upon receiving the last stop bit, the receiver full flag is set (Bit 7 of the receive CSR). If the receiver interrupt enable bit is set (Bit 6), then the receiver full flag will generate an interrupt request.

The UART's transmitter converts the computer's parallel data into a serial format and automatically adds start, parity, and stop bits. When the transmitter buffer is ready to receive a byte of data for transmission, the transmitter ready flag is set (Bit 7 of the transmitter CSR). If the transmitter interrupt enable bit is set (Bit 6), then the transmitter ready flag will generate an interrupt.

#### CONTROL STATUS REGISTER (CSR)

Each channel contains a 16 bit receiver CSR and a 16 bit transmitter CSR. Bit 7 is a read only bit used as a status flag and Bit 6 is a read/write bit used to enable an interrupt request when Bit 7 gets set.

Bit 7 of the receiver CSR is used to indicate that the receiver contains new data. Bit 7 is cleared by reading the receiver's data register or by a software reset. When Bit 6 is set, an interrupt request is generated when Bit 7 is set.

Bit 0 of the receiver CSR is used to transmit a reader run pulse. This bit is a write only bit and always reads zero.

Bit 7 of the transmitter CSR, when set, indicates the transmitter buffer is empty and ready to transmit new data. Setting Bit 6 will generate an interrupt whenever Bit 7 is set.

Bit 0, when set, will transmit a continuous break.

All unused CSR bits in both the transmitter and receiver CSR's will always read zero.

#### DATA REGISTERS

Each channel contains a Receiver Data Register (RDR) and a Transmitter Data Register (TDR). When data is received, it is placed in the RDR and Bit 7 of the Receiver CSR is set. The received data is obtained by reading this register and, thus, automatically clearing Bit 7.

Data to be transmitted is written to the TDR. This automatically clears Bit 7 of the Transmitter CSR. Here the data will remain until the transmitter is ready. The data is then placed into the transmitter setting Bit 7.

#### ERROR REGISTERS

Each channel contains a 4 bit error register which is comprised of Bits 15 through 12 of the RDR.

Bit 12 is the Parity Error (PE) Bit. A "1" indicates the receiver parity does not match the parity selected by the format jumpers. The PE bit remains set until parity matches on a succeeding character. When parity is inhibited, this bit always reads zero.

Bit 13 is the Framing Error (FE) Bit. A "1" indicates the first stop bit was invalid. The FE bit will stay set until the next valid character's stop bit is received.

Bit 14 is the Overrun Error (OE) Bit. A "1" indicates that the last character was not read from the RDR before a new character was received. The OE is reset at the next character's stop if Bit 7 of the Receive CSR cleared.

Bit 15 is the Error Flag (EF) and is the logical "oring" of the PE, FE, and OE bits. The setting of any error bit will set this bit.

#### EIA CIRCUIT

The EIA circuit for each channel consists of a differential line driver, line receiver, and a single ended line driver. Through the use of wire wrap jumpers, each channel can be configured to operate as RS-232C, RS-422, or RS-423.

Channels operating as RS-232C or RS-423 will configure the differential line receiver to operate single ended and utilize the single ended line driver. The slew rates of the line drivers are controlled by changing external resistors.

Channels which operate as RS-422 configure the differential line receiver for differential operation by adding a 100 ohm termination resistor, and utilize the differential line driver.

#### BAUD RATE GENERATOR

The baud rate generator consists of a crystal oscillator and divider. The oscillator base frequency is 614.4 kHz which is divided to yield the nine baud rate clocks. Each channel can operate at any one baud rate independent of the other channels.

## MODES OF OPERATION

Each channel of the 304 can operate in various line disciplines, data formats, and baud rates. The base address can be set so that the board can reside in any I/O page location. The vector can also be set to any address from  $0_8$  to  $774_8$ , and the interrupt level can be set to 4, 5, 6, or 7. All of these operation modes are configured by setting wire wrap jumpers. Table 2 is a summary of the jumper selectable modes which the board can be configured to.

TABLE 2

### Jumper Selectable Modes of Operation

<u>Mode Description</u>	<u>Mode Selection</u>
* Line Discipline	RS-232C, RS-422, or RS-423
* Baud Rate	150, 300, 600, 1200, 2400, 4800, 9600, 19.2K, 38.4K, External
* Serial Data Format	Data Bits, 7 or 8 Stop Bits, 1 or 2 Parity, Odd, Even, None
Base Address	$160000_8$ to $177740_8$
Vector Base Address	$0$ to $740_8$
Console	Enable Channel 4 as System Console Address CH 4 = $177560_8$ Vector CH4 = $60_8$
Halt/Reboot on Break	Channel 3
Interrupt Level	4, 5, 6, or 7

\* Channel to Channel Configurable

Jumper Installed Selects Option

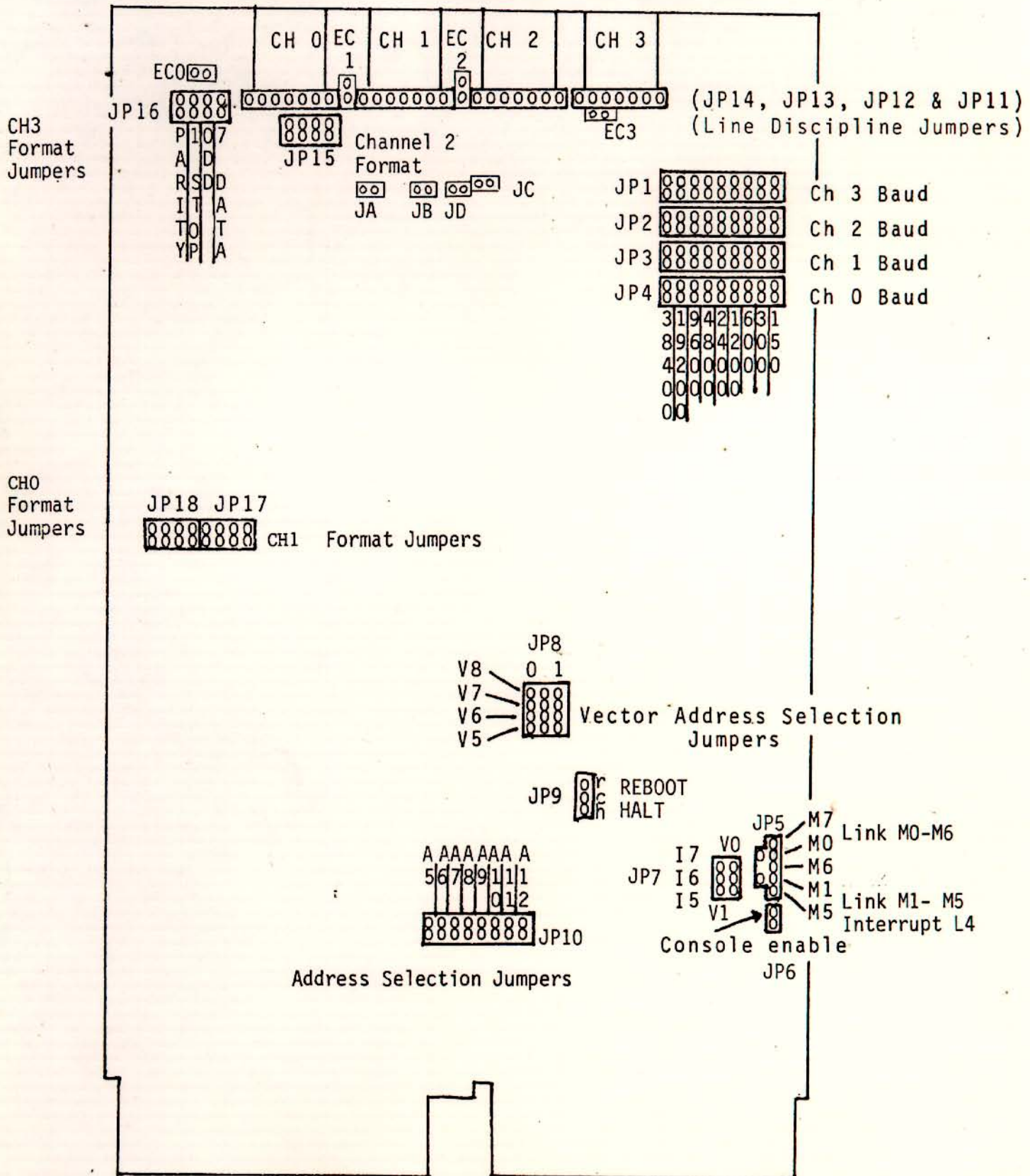


Figure 1 - Model 304 Jumper Layout

## FACTORY CONFIGURATION

The Model 304 is shipped configured as follows:

TABLE 3

Base Address	176500 <sub>8</sub>
Vector Base Address	300 <sub>8</sub>
CH3 Console Enabled	Yes
CH3 Halt on Break	Enabled
* Serial Data Format	1 Stop Bit, 8 Data Bits, No Parity
* Line Discipline	RS232C
* Baud Rate	9600
Interrupt Level	4 (LSI-11)
* All Channels	

## SETTING THE BASE ADDRESS

The 304's base address can be set to reside anywhere within the I/O page. The location of the base address jumper (JP10) is illustrated on Figure 1. To change the board's base address requires reconfiguring the base address jumpers.

Figure 2 illustrates the base address jumper post arrangement. The base address jumpers are arranged as eight pairs labeled A5 through A12. To set an address bit to a 1 requires no connection between the pair of jumper posts labeled for that bit. To set an address bit to a 0 requires installing a jumper between the pair of jumper posts for that bit.

As an example, the factory configured base address is 176500<sub>8</sub>. To set this base address requires installing jumpers at A5, A7, and A9 and removing any jumpers at A12, A11, A10, A8, and A6.

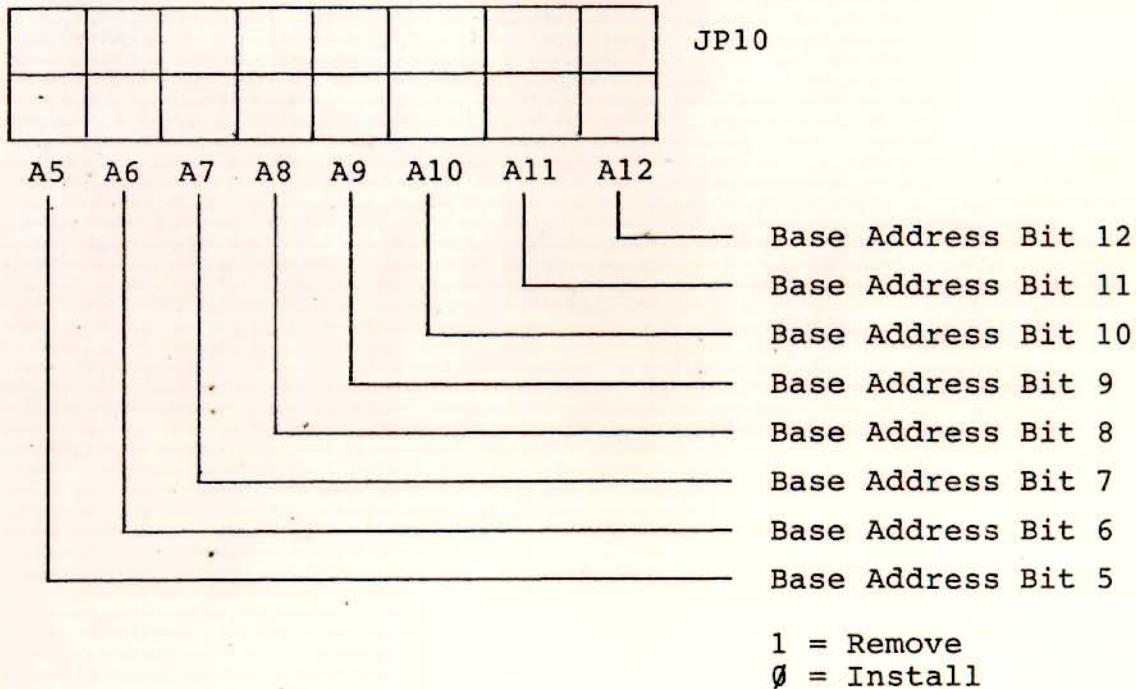


Figure 2 - Base Address Jumpers JP10

SETTING THE VECTOR ADDRESS

The 304's vector address can be set from Ø to 740<sub>g</sub>. The location of the vector selection jumpers (JP8) is illustrated on Figure 1. The vector selection jumpers are comprised of four sets of jumper posts, three across. Each set is labeled according to the vector bit which it controls.

Setting a vector bit to a 1 requires installing a jumper between the right post and the center post. To set a bit to a Ø requires installing a jumper between the left and center post. Figure 3 illustrates the vector selection jumper.

As an example, the factor configured base vector address is 300<sub>g</sub>. To select this vector address requires installing jumpers between the left and center posts at V8 and V5 and the right and the center posts of V6 and V7.

Vector Address Bit 8 - V8	0	0	0	JP8
Vector Address Bit 7 - V7	0	0	0	
Vector Address Bit 6 - V6	0	0	0	
Vector Address Bit 5 - V5	0	0	0	

Figure 3 - Vector Address Selection Jumpers JP8

TABLE 4  
Interrupt Level Selection Jumpers

<u>Level</u>	<u>Jumper Post JP5*</u>		<u>Jumper Post JP7**</u>		
	M1	M0	I5	I6	I7
4	M5	M6	R	R	R
5	V1	M6	I	R	R
6	V1	M7	R	I	R
7	V1	V0	R	I	I

\*Note: Install jumpers from jumper posts M1 and M0 to the jumper posts listed in each column according to the interrupt level desired. No other jumpers should be installed

\*\*Note: R = Remove  
I = Install

SETTING THE INTERRUPT LEVEL

Setting the 304's interrupt level is done by configuring jumper posts JP5 and JP7 according to Table 4. Figure 1 illustrates the location of these jumper posts and Figure 4 illustrates these jumper posts in greater detail.

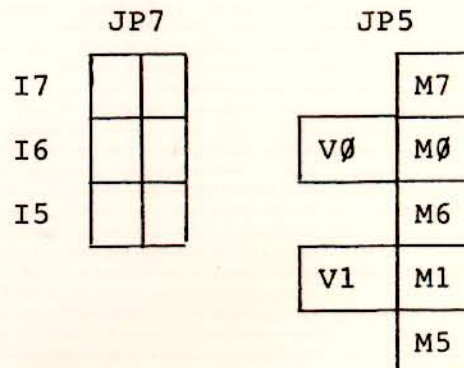


Figure 4 - Interrupt Level Selection Jumpers JP5 and JP7

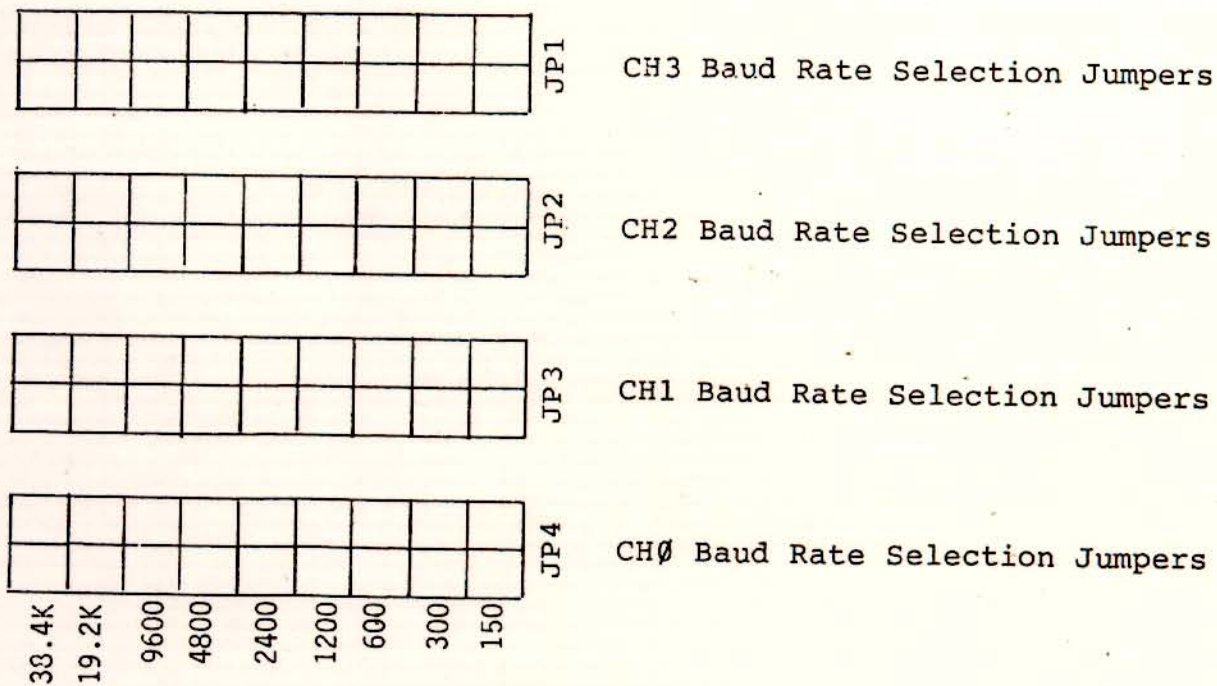


Figure 5 - Baud Rate Selection Jumpers



## SETTING THE BAUD RATE

Each channel can be set to operate at one of nine jumper selectable baud rates from 150 to 38.4K baud. Figure 5 illustrates the baud rate selection jumpers and Figure 1 illustrates their location on the 304.

In addition to the on-board baud rates, the user can use an external clock. The external clock is input through pin 1 of a channels I/O connector. The baud rate jumpers must also be completely removed from that channels baud rate jumper block and external clock jumper for that channel must be installed. These may be located by referring to Figure 1. Channel 0 through 3's external clock jumpers correspond to jumper post EC0 through EC3, respectively.

The baud rate jumpers are divided into four groups of nine pairs. Each group is used to select a baud rate for each channel, and each jumper pair for each baud rate. To set the baud rate requires installing a jumper at the appropriate jumper pair within the baud rate selection jumpers for the channel.

## ENABLING THE CONSOLE

Channel 3 can be enabled as the system console independent of the base and vector address settings. To enable this option requires installing jumper JP6. To disable this option requires removing jumper JP6. Refer to Figure 1.

When the console is enabled, Channel 3 will respond to addresses 177560<sub>h</sub> to 177566 and will output a vector of 60 and 64 for the receiver and transmitter interrupts, respectively. Caution should be employed when the console is enabled so as not to set the base address equal to 177540 or a conflict will exist between Channel 2 and Channel 3. When the console is disabled, all jumpers must be removed from JP9 (refer to Figure 1).

## SYSTEM HALT OR REBOOT

Any device communicating through Channel 3 can generate a system halt or power up initialization by outputting a "BREAK."

To generate a system halt on break requires installing a jumper at JP9 (Figure 1) from C to H. To generate a power fail reset, connect C to R. Refer to Figure 1 for jumper block JP9's location. Removing either jumper disables these functions completely.

## SETTING THE SERIAL DATA FORMAT

Each channel of the 304 can be configured to operate in the following data formats:

7 or 8 Data Bits  
1 or 2 Stop Bits  
Odd, Even, or with No Parity

Jumper posts JP18, JP17, JP15, and JP16 (Figure 1) are used to set the serial data format of Channels 0 through 3, respectively. The jumper configurations of the various options are illustrated in Figure 6. As an example, the 304 is shipped configured for eight data bits, one stop bit, and no parity. This requires installing the one stop bit jumper and removing all the rest.

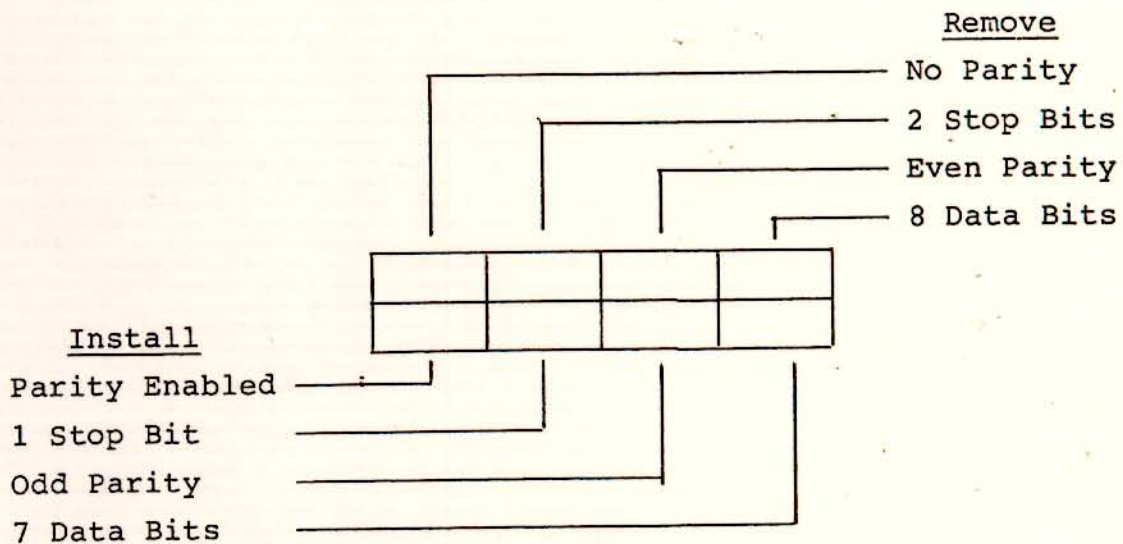


Figure 6 - Serial Data Format Jumper Block Detail

JP15(CH 2), JP16 (CH 3), JP17 (CH1) and JP18 (CH0)

## SETTING THE LINE DISCIPLINE

Each channel of the 304 can operate in any one of the following EIA line disciplines:

RS-232C  
RS-422  
RS-423

The jumper blocks used to configure Channels 0 through JP14, JP13, JP12, and JP11 (Figure 1), respectively. Table 9 illustrates the jumper configuration to set up each channel. As an example, the 304 is shipped from the factory with each channel set up to operate in RS-232C. This requires jumpering S+ to I+ and S- to I-. Figure 6 illustrates the layout of the line discipline jumper blocks.

TABLE 9

### Line Discipline Jumper Configuration

<u>Line Discipline</u>	<u>Jumper Configuration</u>
RS-232C	I+ to S+, I- to S-
* RS-422	I+ to D+, I- to D-
RS-423	I+ to S+, I- to S-

\* Add 100 ohm termination resistor, (RA, RB, RC, RD)

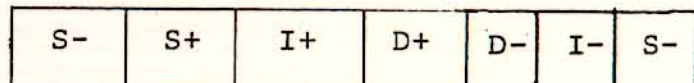


FIGURE 7

### Line Discipline Jumper Block Layout

JP14, JP13, JP12, JP11

When a channel is set up to operate in RS-422, a 100 ohm termination resistor must be installed at the input of the differential receiver. This is accomplished by installing jumpers JA through JD according to Table 10.

TABLE 10

RS-422 Resistor Installation Jumper Guide

Channel 0	Install Jumper JA
Channel 1	Install Jumper JB
Channel 2	Install Jumper JC
Channel 3	Install Jumper JD

During data communication over long data leads, it may be necessary to change the rise and fall times of the single ended line drivers used in RS-423 to reduce line reflections and the potential of data errors. R13 controls the transition time for Channels 0 and 1 and R14 controls Channels 2 and 3. The resistor installed at the factory is a 22K which sets the transition time at 2.2 $\mu$ s. Table 11 is a list of recommended resistor values as a function of baud rate which should be installed if line reflections become a problem.

TABLE 11

RS-423 Slew Rate Resistor Values

<u>Baud Rate</u>	<u>Resistor Value in Ohms</u>	<u>Nominal Transition Times</u>
150	1 Megohm	100 $\mu$ sec
300	1 Megohm	100 $\mu$ sec
600	1 Megohm	100 $\mu$ sec
1200	820K Ohm	82 $\mu$ sec
2400	430K Ohm	43 $\mu$ sec
4800	200K Ohm	20 $\mu$ sec
9600	100K Ohm	10 $\mu$ sec
19.2K	51K Ohm	5.1 $\mu$ sec
38.4K	22K Ohm	2.2 $\mu$ sec

## READER RUN PULSE

The reader run pulse is used to control a paper tape reader. To use this control requires connecting P to I- at the appropriate line discipline jumper block (Figure 1). Figure 6 illustrates the location of this jumper with the line discipline jumper block.

## SERIAL INTERFACE

Figure 1 illustrates the connector location for each channel.

### CONNECTOR DESCRIPTION

Each channel is interfaced through a 10 pin header. Figure 7 illustrates the pin-out location. The mating connector is manufactured by AMP, Inc. Table 12 lists the parts which are required to assemble the mating connector. The connector may be obtained through AMP, AMP distributors, or GTSC.

TABLE 12

#### Model 304 Connector Assembly Parts List

<u>AMP P/N</u>	<u>Description</u>	<u>Quantity/Connector</u>
87133-5	Connector Shell	1
87179-1	Key Pin	1
87165-2	Pins	9

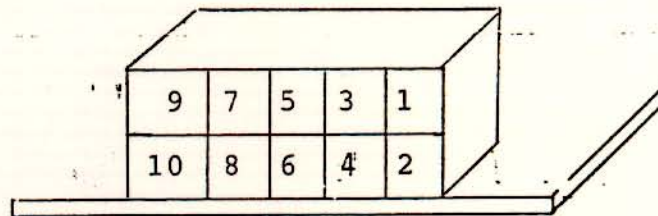


FIGURE 7

#### Model 304 Header Pin-out

The pin-out description of each header is as follows:

<u>Pin No.</u>	<u>Description</u>
N-1	Clock I/O
2	Signal Ground ✓
3	Transmit Data + ✓
4	Transmit Data -
5	Signal Ground ✓
Z-6	Key (No Pin)
7	Receive Data -
8	Receive Data + ✓
9	Signal Ground
N-10	+12 Volts (Fused)

When a channel is configured for RS-232C or RS-423, Pin 7 must be externally tied to signal ground. This is typically done by connecting Pin 7 to Pin 9. Pin 1 is the external clock input.

LINE DISCIPLINE, CABLE LENGTH & DATA RATES

The two basic methods for electronic communications are single ended transmission and differential transmission. RS-232 was developed for single ended transmission over short distances at slow data rates. RS-423 extends the maximum data rate and cable length beyond that of RS-232. It also provides for wave shaping dependent on data rate and wire length to control reflections.

For communications over long distances, differential transmissions (RS-422) should be used to nullify effects of ground shifts and noise signals which appear as common mode. Table 13 lists the maximum recommended cable length and data rates for each line discipline.

TABLE 13

Key Aspects of RS-232,  
RS-423 & RS-422

<u>Specification</u>	<u>RS-232C</u>	<u>RS-423</u>	<u>RS-422</u>
Mode of Operation	Single-ended	Single-ended	Differential
No. of Drivers & Receivers allowed on one line	1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers
Maximum Cable Length	50 feet	4000 feet	4000 feet
Maximum Data Rate	20 kb/s	100 kb/s	10 mb/s

## PROGRAMMING

Figure 8 illustrates the functions of the four 16 bit registers which comprise each channel. Thus, the Model 304 occupies 16 contiguous blocks in the I/O page \*. The registers which make up each channel are:

Receiver Control Status Register (RCSR)  
Receiver Data Register (RDR)  
Transmitter Control Status Register (TCSR)  
Transmitter Data Register (TDR)

Table 14 illustrates the relationship between each channel's registers and the base address. When the console is enabled, any attempt to address Channel 3 through an address other than the console address will cause a bus time out error.

Testing Bit 7 of the RCSR is used to indicate that the UART has received new data. Reading the RDR will clear Bit 7. Setting Bit 6 of the RCSR will enable the receiver interrupts. When Bit 7 is set, an interrupt will be generated.

Bit 0 of the RCSR is used to generate the reader run pulse by setting this write only bit. This action will also clear Bit 7 of the RCSR.

Bits 0 through 7 of the RDR contain the data received by the UART. Bits 12 through 15 indicate any errors which have occurred during the reception of data.

Bit 7 of the TCSR indicates the status of the transmitter. When this bit is set, the transmitter is ready to receive a new byte of data for transmission. When this bit is cleared (Bit 7 = 0), the transmitter is busy and no attempt to write the data to the TDR should be made. Setting Bit 6 of the TCSR will allow interrupts to be generated when Bit 7 is set.

Bit 0 of the TCSR is a read/write bit used to transmit a continuous break. A "1" written to Bit 0 will transmit a break (continuous 0), a zero clears the break transmission.

\* This only holds true if Channel 3 is not configured as the console.



Data which is to be transmitted is written to the TDR, but only if Bit 7 of the TCSR is set.

Table 15 lists the relationship between the vector jumper settings and each channel. Note, Channel 3's vector is that of the console when the console is enabled.

Table 16 illustrates the register and vector address when Channel 3 is configured as the system console.

TABLE 14

Register Address Offset

<u>Register Description</u>	<u>Base Address Offset (Octal)</u>
Channel 0 Receiver CSR	Base Address +0
Channel 0 Receiver Data Register	Base Address +2
Channel 0 Transmitter CSR	Base Address +4
Channel 0 Transmitter Data Register	Base Address +6
Channel 1 Receiver CSR	Base Address +10
Channel 1 Receiver Data Register	Base Address +12
Channel 1 Transmitter CSR	Base Address +14
Channel 1 Transmitter Data Register	Base Address +16
Channel 2 Receiver CSR	Base Address +20
Channel 2 Receiver Data Register	Base Address +22
Channel 2 Transmitter CSR	Base Address +24
Channel 2 Transmitter Data Register	Base Address +26
Channel 3 Receiver CSR	Base Address +30
Channel 3 Receiver Data Register	Base Address +32
Channel 3 Transmitter CSR	Base Address +34
Channel 3 Transmitter Data Register	Base Address +36

TABLE 15

Vector Address Offset

<u>Interrupt Request Description</u>	<u>Vector Base Address Offset</u>
Channel 0 Receive	0
Channel 0 Transmit	4
Channel 1 Receive	10
Channel 1 Transmit	14
Channel 2 Receive	20
Channel 2 Transmit	24
Channel 3 Receive	30
Channel 3 Transmit	34

TABLE 16

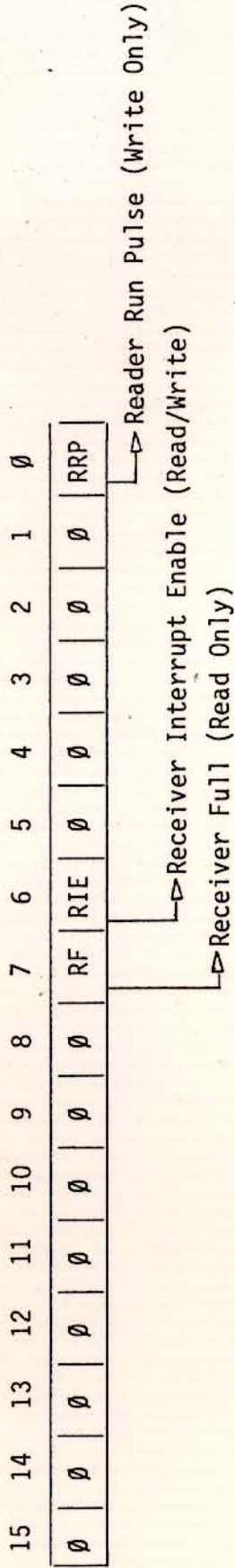
Console Register & Vector Addresses

When Console Option is Enabled

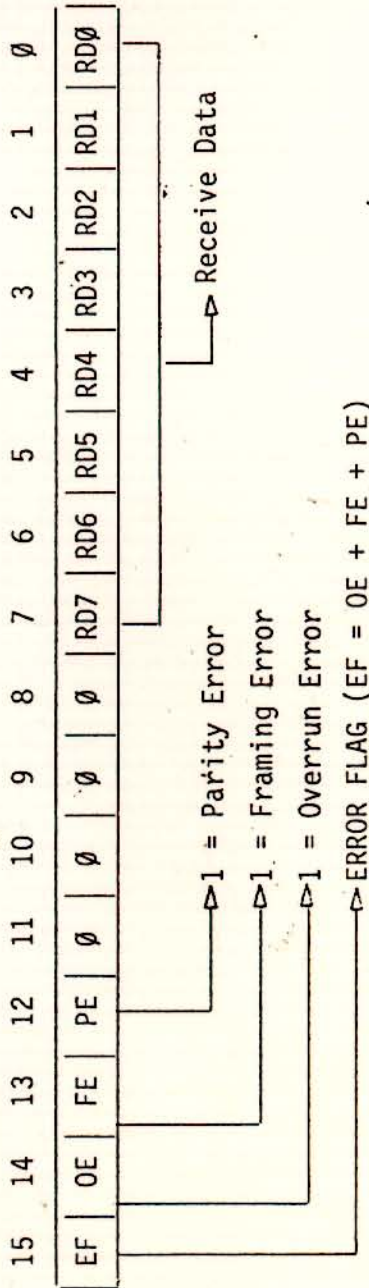
<u>Channel 3 Register Description</u>	<u>Register Address</u>
Receiver CSR	177560 <sub>8</sub>
Receiver Data Register	177562 <sub>8</sub>
Transmitter CSR	177564 <sub>8</sub>
Transmitter Data Register	177566 <sub>8</sub>
Receiver Interrupt Vector Address	60 <sub>8</sub>
Transmitter Interrupt Vector Address	64 <sub>8</sub>

FIGURE 8

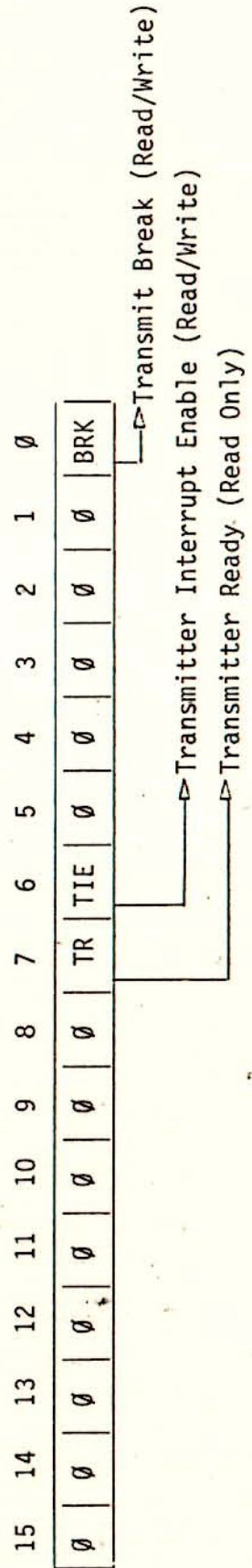
RECEIVER CSR



RECEIVER DATA REGISTER



TRANSMITTER CSR



TRANSMIT DATA REGISTER

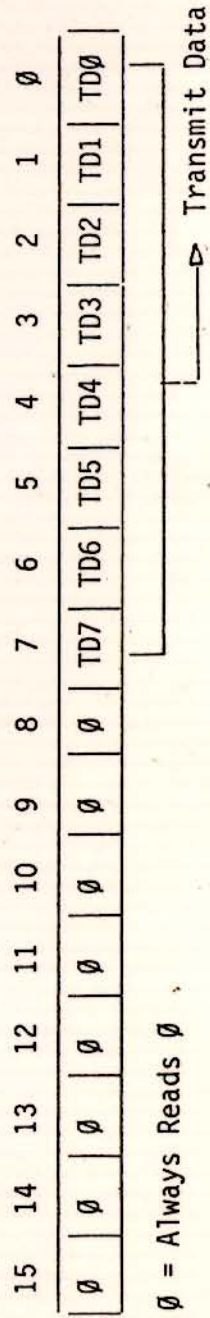


FIGURE 8 (Cont.)

Model 304 Serial I/O Port Register Formats

