MEMORY SYSTEM
CI-1103
TECHNICAL MANUAL

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CONTENTS

SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation, installation, and design of the CI-1103 dynamic read/write memory.

1.2 THE MEMORY MODULE

The CI-1103 Various options are summarized below:

OPTION	MEMORY CAPACITY	MEMORY CHIP UTILIZED
8K	8K by 16 bits	4K by 1 (4027)
16K	16K by 16 bits	16K by 1 (4116)
32K	32K by 16 bits	16K by 1 (4116)

1.2.1 CI-1103 MEMORY DESCRIPTION

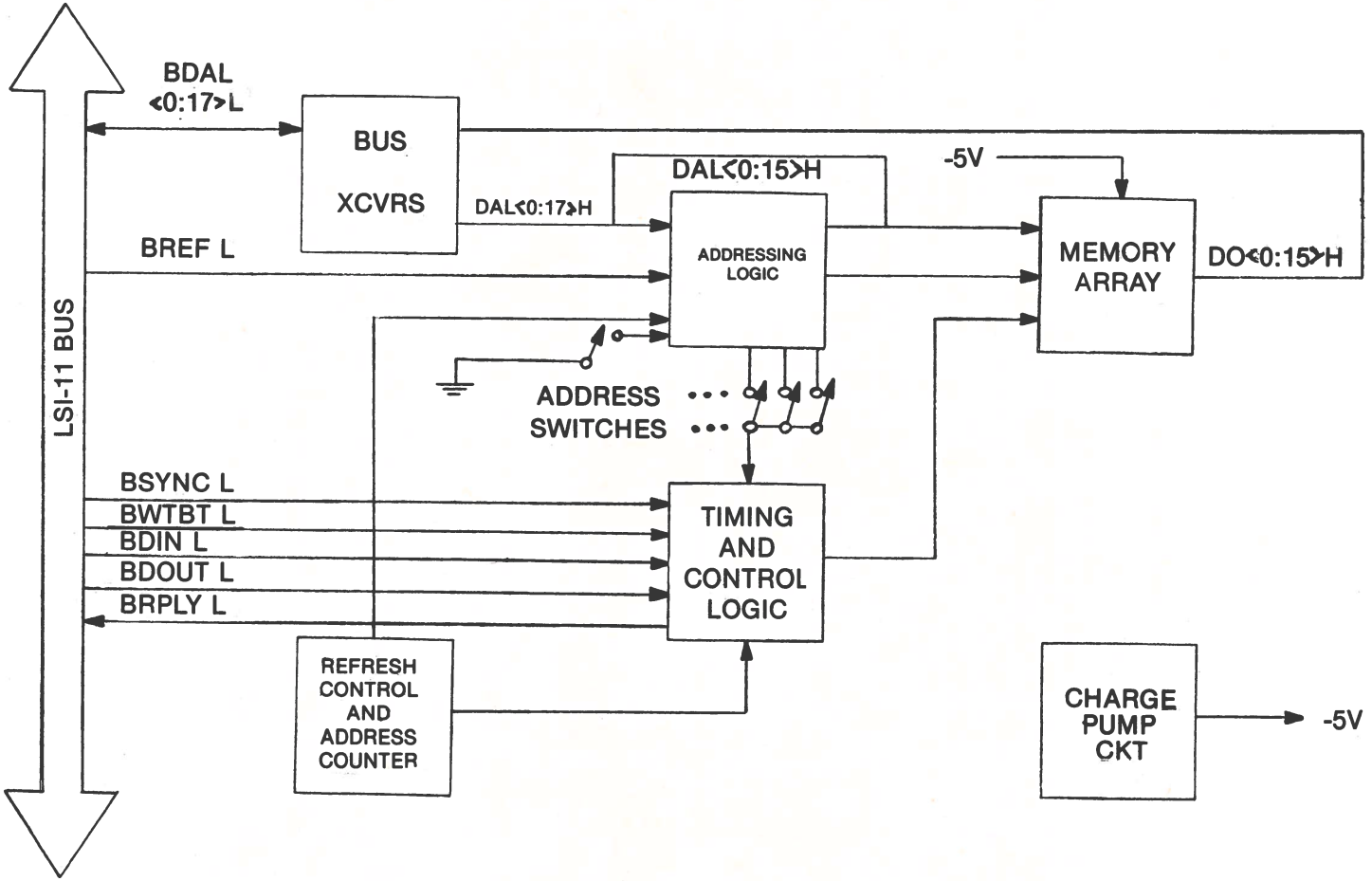
The CI-1103 is a high speed dynamic read/write memory which is plug compatible with the DEC LSI 11, LSI 11/2, and PDP-1103. Memory storage is provided by either 4K by 1 or 16K by 1 dynamic MOS memory chips depending on the option. The memory is a single package plug-in module having outline dimensions of 8.44" x 5.187".

1.2.2 OPERATIONAL FEATURES

The memory module contains its own address and data buffers. Address, data-in and data-out are multiplexed for bus compatibility with the LSI 11. The system memory address space to which the module will respond is user-configured via switches contained on the module. An address can be selected in 2K increments through the 0-128K address range. The module contains its own complete refresh control logic requiring no outside intervention. The module is available for on board distributed refresh or external refresh.

1.2.3 POWER REQUIREMENTS

The memory module uses the existing power supplies in the PDP-1103. It utilizes both the +12V and +5V supplies. It generates its own -5 Volts for the memory chips from the +12V supply.



FUNCTIONAL BLOCK DIAGRAM
FIGURE 1.1

1.3 GENERAL SPECIFICATION REQUIREMENTS

Table 1-1 lists the general specifications for the CI-1103 memory.

TABLE 1-1

CHARACTERISTICS	SPECIFICATIONS
Capacity	8K to 32K words x 16 bits
Cycle Time	525 nanoseconds
Access Time	325 nanoseconds from Sync Active
Word Size	16 bits
Address	14 bits (random access)
Data-in/Data-out	16 bits bidirectional with open collector TTL voltage compatible
Modes of Operation	DATO, DATOB, DATI, DATIO, DATIOB
Expansion	2K Memory Blocks up to 128K by selecting the proper switch
Refresh	On Board distributed or external
Interface Signals	
Inputs	TTL Compatible
Outputs	Open Collector
Operating Temperature	0 to 60°C
Storage Temperature	-20 to +70°C
Power Requirements	
	Operate / Standby
	+5.0V 1A 1A
	+12.0V 300 mA 100 mA
Dimensions	8.44" x 5.187"

1.4 MEMORY ADDRESS SELECTION

The CI-1103 has its own module select switches to choose the memory bank required. Module selection is accomplished by closing the desired switch positions as indicated in the table below and leaving all other positions open.

The memory map covers the 000000 to 177777 address field. For extended address selection in the range of 32K to 128K see appendix A.

Bank Selected	Closed Switch	Bank Selected	Closed Switch
000000 to 007777	SW1-1	100000 to 107777	SW2-1
010000 to 017777	SW1-2	110000 to 117777	SW2-2
020000 to 027777	SW1-3	120000 to 127777	SW2-3
030000 to 037777	SW1-4	130000 to 137777	SW2-4
040000 to 047777	SW1-5	140000 to 147777	SW2-5
050000 to 057777	SW1-6	150000 to 157777	SW2-6
060000 to 067777	SW1-7	160000 to 167777	SW2-7
070000 to 077777	SW1-8	170000 to 177777	SW2-8

Notes:

1. A total of 4 switches can be closed for the 8K option.
   A total of 8 switches can be closed for the 16K option.
2. On the 8K and 16K options switch 1 and switch 2 are mutually exclusive. eg. If SW1-1 is closed SW2-1 must be open and vice versa.
3. Bank 7 (1600000 thru 177777) is normally reserved for peripheral device addressing.

SECTION II

HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section details handling precautions. It includes step by step procedures to interface the CI-1103 memory module with the LSI-11 and the PDP-1103 microcomputer family.

2.2 HANDLING PRECAUTIONS

The memory IC's used on the CI-1103 are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that **no discharge** will flow through the IC. Also avoid unnecessary handling and wear cotton—rather than synthetic—clothing when you do handle these IC's.

2.3 INTERFACE SIGNALS

The input signals to the memory are TTL compatible and the output signals are open collector. The timing relationship between these signals are shown in figure 2.1.

2.4 MEMORY INTERFACE

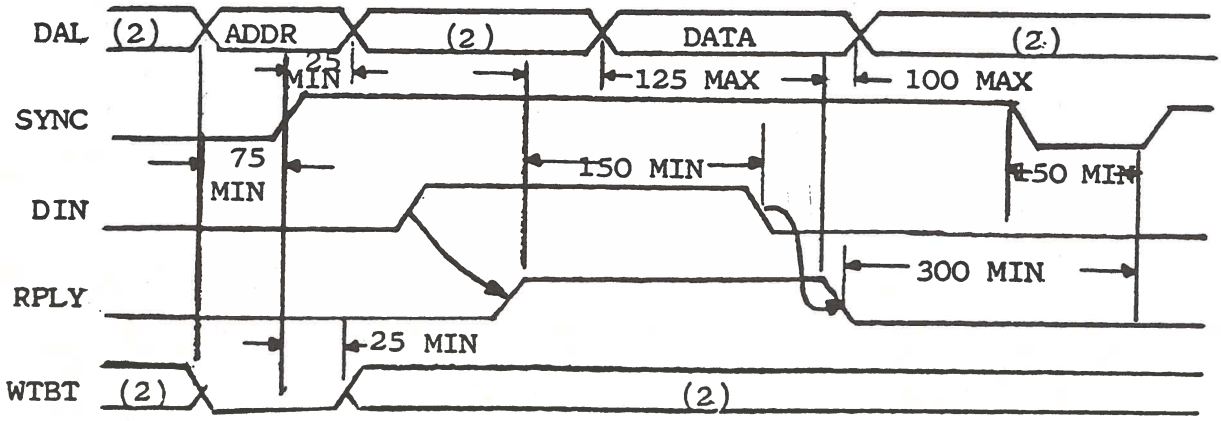
Note: If the CI-1103 is installed in a system that contains an LSI-11 processor module etch revision C or D, CS revision H2 or earlier, BDAL 16L and BDAL 17L bus lines (AC1 and AD1) respectively must be terminated.

2.4.1 INTERFACE WITH THE LSI-11, LSI-11/2, PDP-1103, or LSI-11/23

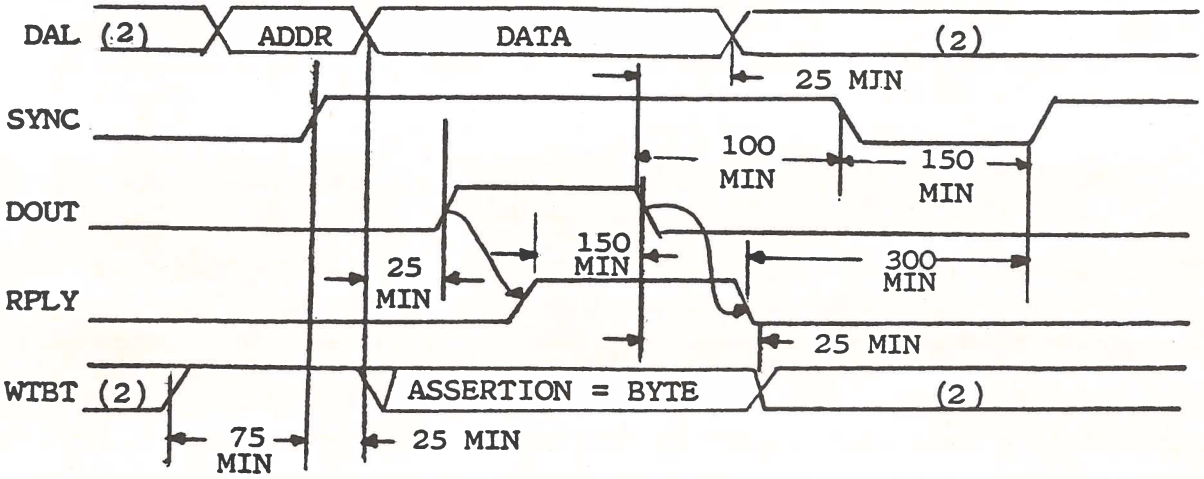
The CI-1103 memory module may be installed in any slot available in the LSI-11, LSI-11/2, PDP-1103 or LSI-11/23.

Caution: The memory module and backplane connector can be damaged if the module is installed backwards. Care should be taken to insure that the module is installed so that the component side of the module faces the same direction as other LSI-11 system modules.

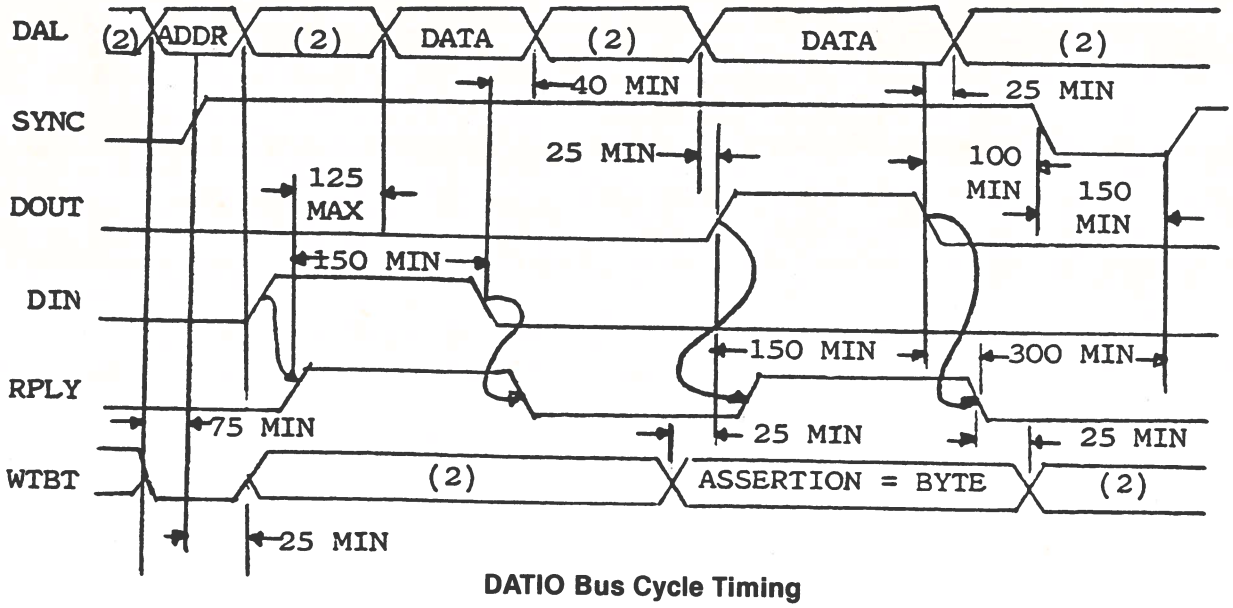
DC power must be removed from the backplane during module removal or insertion.



DATI Bus Cycle Timing



DATO or DATOB Bus Cycle Timing



DATIO Bus Cycle Timing

1. All timing signals in Nano Seconds (ns).
2. Don't care condition.

MEMORY INTERFACE DIAGRAM
FIGURE 2.1

CONNECTOR PIN ASSIGNMENT

SIGNAL NAME	COMP. SIDE	SOLDER SIDE	SOLDER SIDE
	AA1	AA2	+5V
	AB1	AB2	
BDAL16L	AC1	AC2	GND
BDAL17L	AD1	AD2	
	AE1	AE2	BDOUTL
	AF1	AF2	BRPLYL
	AH1	AH2	BDINL
GND	AJ1	AJ2	BSYNCL
	AK1	AK2	BWTBTL
	AL1	AL2	
GND	AM1	AM2	BIAKIL
	AN1	AN2	BIAKOL
	AP1	AP2	
BREFL	AR1	AR2	BDMGIL
	AS1	AS2	BDMGOL
GND	AT1	AT2	
	AU1	AU2	BDALOL
	AV1	AV2	BDALIL
BDCOKH	BA1	BA2	+5V
	BB1	BB2	
	BC1	BC2	GND
	BD1	BD2	+12V
	BE1	BE2	BDAL2L
	BF1	BF2	BDAL3L
	BH1	BH2	BDAL4L
GND	BJ1	BJ2	BDAL5L
	BK1	BK2	BDAL6L
	BL1	BL2	BDAL7L
	BM1	BM2	BDAL8L
	BN1	BN2	BDAL9L
	BP1	BP2	BDAL10L
	BR1	BR2	BDAL11L
	BS1	BS2	BDAL12L
GND	BT1	BT2	BDAL13L
	BU1	BU2	BDAL14L
+5	BV1	BV2	BDAL15L

TABLE 2-1

SECTION III

THEORY OF OPERATION

3.1 GENERAL DESCRIPTION

The CI-1103 is a high density semiconductor random access memory capable of performing all bus cycles according to LSI-11 bus protocol. In the CI-1103 a cycle is a timed sequence of events that perform one memory access. There are six kinds of cycles—DATI, DATO, DATOB, DATIO, DATIOB, and REFRESH.

The memory IC's used in the CI-1103 are dynamic memories in which the Data cells operate by stored electrical charge. Dynamic memories require stored data to be read and restored periodically. Otherwise, current leakage would eventually change the stored data. The restoring process is called "refreshing the memory," or simply refresh.

The CI-1103 provides memory refresh as required without any external intervention by the CPU or DMA device controlling the module.

3.1.1 MEMORY CYCLES OTHER THAN REFRESH

A memory cycle is first initiated by the decoding of address lines A12-A15 to determine if the memory module has been selected. If the board has been selected, and the CPU or DMA device controlling the bus is not performing a REFRESH routine (BREF is not aserted), a memory cycle will commence.

Address lines A1 thru A14 are applied to a multiplexer network U41, U49, U36, and U38, in two groups of seven. These two groups are presented in succession along with address—strobes to the memory array to determine the selected memory location.

The Row-Address-Strobe ($\overline{RAS}$) is applied to the sixteen memory IC's of one of two pages determined by A13 on the 8K option or A15 on the 32K option. It's leading edge causes these sixteen IC's to store the first group of seven address bits called the row address and starts a memory cycle.

Subsequently, Column-Address-Strobe ($\overline{CAS}$) is applied to all the memory IC's. It causes them to release their data outputs to the 3rd state (open circuited). It's leading edge causes those selected by $\overline{RAS}$ to store the second group of seven address bits, called the column address.

From this point, the control logic determines which type of cycle is to be performed eg. DATI, DATO, DATOB, or DATIOB. Each of these cycles will be described in detail in the following section.

3.2 DETAILED DESCRIPTION

3.2.1 BOARD SELECTION

Page and board selection depends on address bits A12-A15, the three decoders U34, U35, U40, and the two 8 position switches SW1 and SW2.

Address bit A13 (8K option) or $\overline{A15}$ (32K option) is applied to U44 to determine the page to be selected. This allows the $\overline{RAS}$ strobe to be applied only to that group of memory chips.

Address bits A12-A15 and $\overline{A15}$ are applied to decoders U34 and U35 with open collector outputs. These outputs are wired "or" via the two 8 position switches (SW1 and SW2) to determine the board select condition. Switch position "1" on SW1 enables the 1st 2K bank and succeeding switch positions enable the remaining 2K banks thru 32K. Thru the use of extended address bits A16 and A17 together with REF (45-9), the remaining portion of the board select condition is decoded thru U40. Thru a jumper selection guide (see appendix A) one of four 32K memory banks thru 128K can be enabled for the CI-1103 memory module. REF (45-9) is also applied to decoder U40 disabling the BS signal whenever the CPU of DMA module controlling the bus is performing a refresh cycle. BS (U50-1) is "and'ed" with the SYNC DLY LAT signal to initiate a memory cycle.

3.2.2 CYCLES

Either of two signals $\overline{MC}$ or $\overline{RC}$, can initiate a cycle. $\overline{RC}$ describes a refresh cycle and $\overline{MC}$ describes any of the LSI-11 memory cycles.

$\overline{MC}$ and $\overline{RC}$ are or'ed in U52, with the output on pin 6 being applied to DL1. DL1 is a passive delay line producing all the required timing for address strobes and enables to memory.

Each cycle is described by the signal CY which is set to "1" at the initiation of $\overline{RAS}$. It remains in this state until the completion of the cycle in progress.

3.2.2.1 DATI CYCLE (REFER to FIG. 3.1)

This cycle retrieves data from the indicated address. Approximately 75 NSEC from the assertion of BSYNC, SYNC DLY LAT(U57-5) is set. If Board Select (BS) U50-1 is set at this time $\overline{MC}$ will be set to start a cycle. $\overline{RC}$ remains at 1. After a delay of 25 NSEC, $\overline{RAS}$ occurs at the selected page of memory causing the row address to be saved, and starting a cycle within each of the sixteen memory IC's. CY goes to a "1".

After 75 NSEC, CAE (Column Address Enable) becomes active and the column address is presented to the memory array.

After 125 NSEC, CAS is set to a "1". $\overline{CAS}$ occurs at all memory IC's causing all to release their data output to the third state. Within the sixteen memory IC's selected by $\overline{RAS}$, the column address is saved. This is a read cycle. So $\overline{WR0}$ and $\overline{WR1}$ are high, and the input data is ignored.

After 175 NSEC, the reply logic is enabled (U46-4). Once BDIN becomes active, BRPLY is generated.

After 225 NSEC, the output buffers are enabled U53 thru U56 placing valid data on the bus.

Once SYNC is removed, CY will be reset 125 NSEC later allowing another cycle to occur.

3.2.2.2 **DATO CYCLE (REFER to FIG 3.2)**

This cycle stores data at the indicated address. The cycle proceeds much the same as a DATI cycle except that a BDOUT occurs instead of BDIN. This is not a DATOB cycle therefore BWTBT is not asserted. Valid new data reaches the memory array via the bus receivers U53 thru U56. BDOUT occurs which results in $\overline{WR0}$ and $\overline{WR1}$ becoming active and writing the new data at the selected address. 175 NSEC from the start of the cycle, the reply logic is enabled resulting in the assertion of BRPLY.

3.2.2.3 **DATOB CYCLE (REFER to FIG 3.2)**

This cycle proceeds the same as a DATO cycle except that BWTBT is asserted indicating the cycle is a write byte only. A0 and U58 determine whether the lower or upper byte is to be written into allowing only $\overline{WR1}$ or $\overline{WR0}$ to become active.

3.2.2.4 **DATIO OR DATIOB (REFER to FIG 3.3)**

This cycle performs a read followed by a write or write byte operation. The first portion of the cycle proceeds as a normal DATI cycle. Once the DATI portion is completed BSYNC remains active and therefore the $\overline{RAS}$ signal to the select page also remains active. At this time data is placed on the bus and BDOUT is asserted as in a DATO cycle resulting in DATA being written into the selected address location. BWTBT determines the write byte condition as before and A0 determines the lower or upper byte.

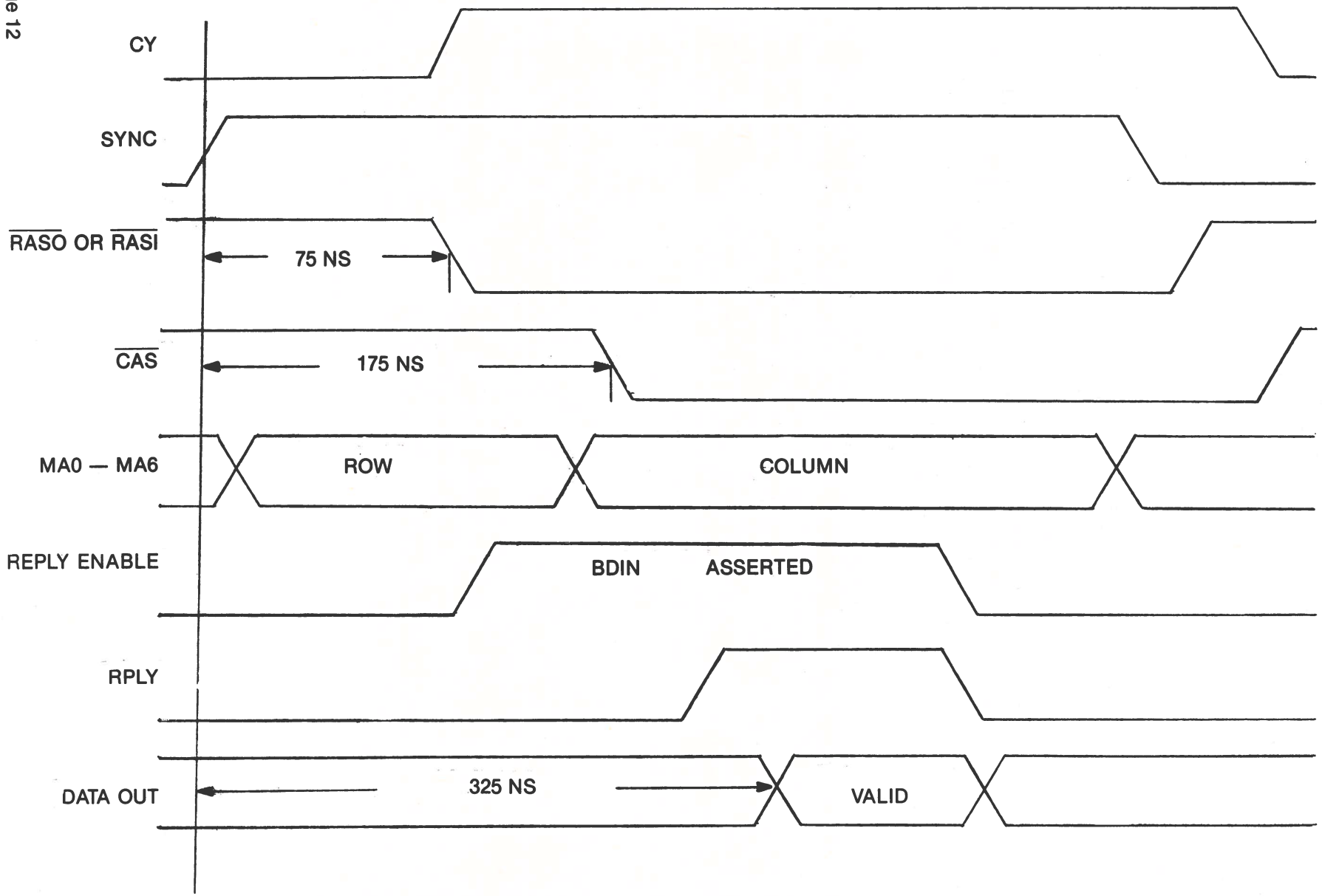
3.2.2.5 REFRESH CYCLE (REFER to FIG 3.4)

This cycle refreshes data in one row in each memory IC when it occurs.

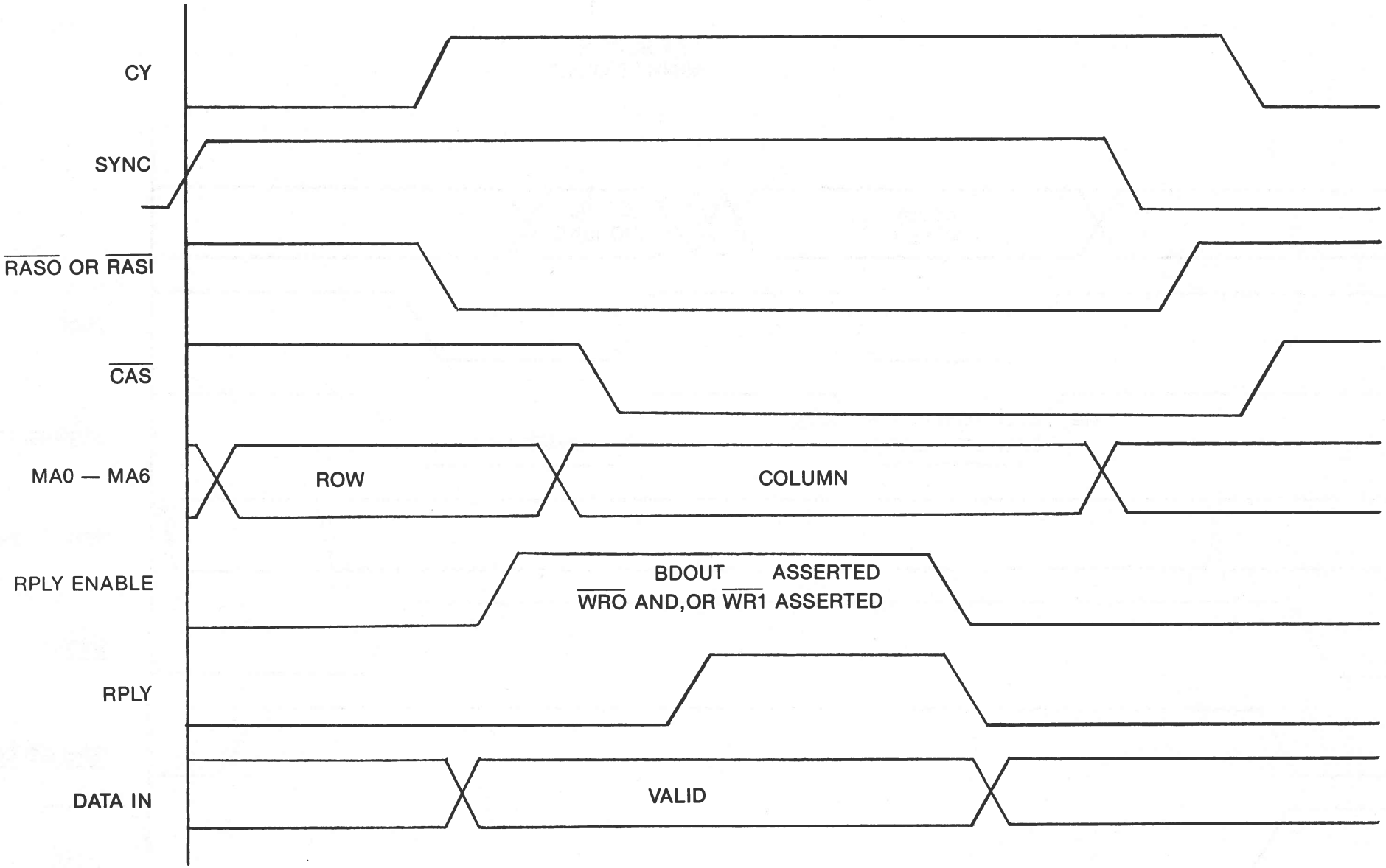
The CI-1103 is available with two refresh options, on board, or external. Each is described below:

External Refresh: When supplied with this option the CI-1103 responds to external refresh cycles initiated by BREF. BREF is latched with occurrence of SYNC resulting in REF U45-9 being set. REF in turn disables the board select function (U50-2 goes to "1"), disabling any MC cycles. The occurence of SYNC DLY LAT along with REF initiates an RC cycles (U42-6 goes low). RAS becomes active as in other cycles but because REF is a "1" $\overline{\text{RAS}}$ occurs at both pages of memory. The ROW address is strobed resulting in one of 256 ROW locations being refreshed. Again because REF is a "1" the $\overline{\text{CAS}}$ signal is disabled and no further strobing of the memory array occurs. The cycle is completed following the termination of the BSYNC signal.

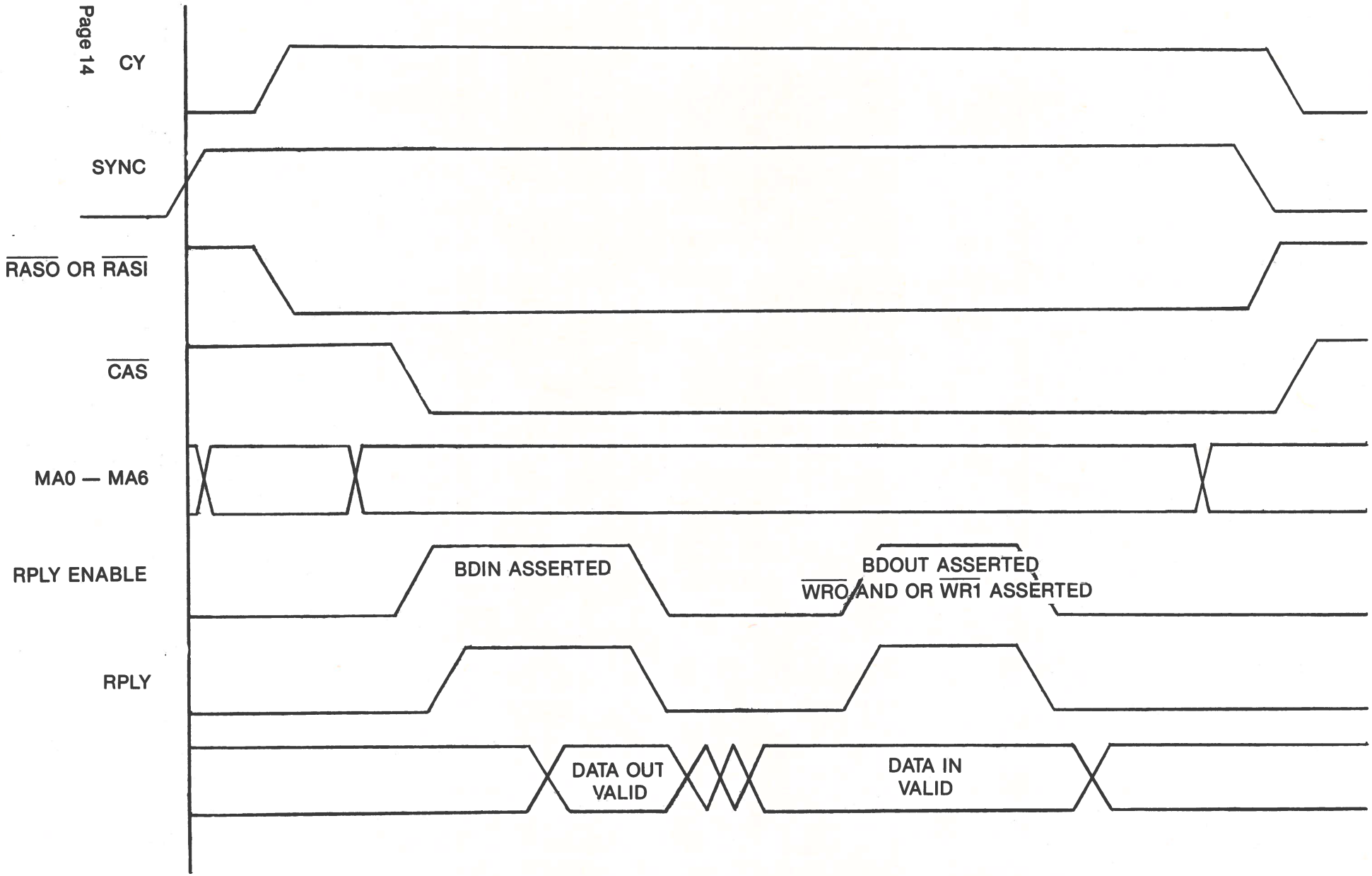
On Board Refresh: When supplied with this option the CI-1103 controls the refreshing of memory itself requiring no outside intervention. This is accomplished thru the use of the 8 bit counter U47 and one shot U60. U60 times out a 12 micro second interval at which time a refresh cycle is requested. If no cycle is in progress and the system is in a non active SYNC period, the request is granted. HREF (U45-5) is set enabling the counter address to reach the memory array and initiating an RC cycle. CY becomes a "1" disabling other cycles from occurring. RAS occurs and because this is a refresh cycle it reaches all memory IC's storing the ROW address from the 8 bit counter. After 225 NSEC $\overline{\text{RAS}}$ is terminated, the one shot is reset and the counter is increment. After 350 NSEC, CY is reset completing the refresh cycle and enabling other cycles to occur.



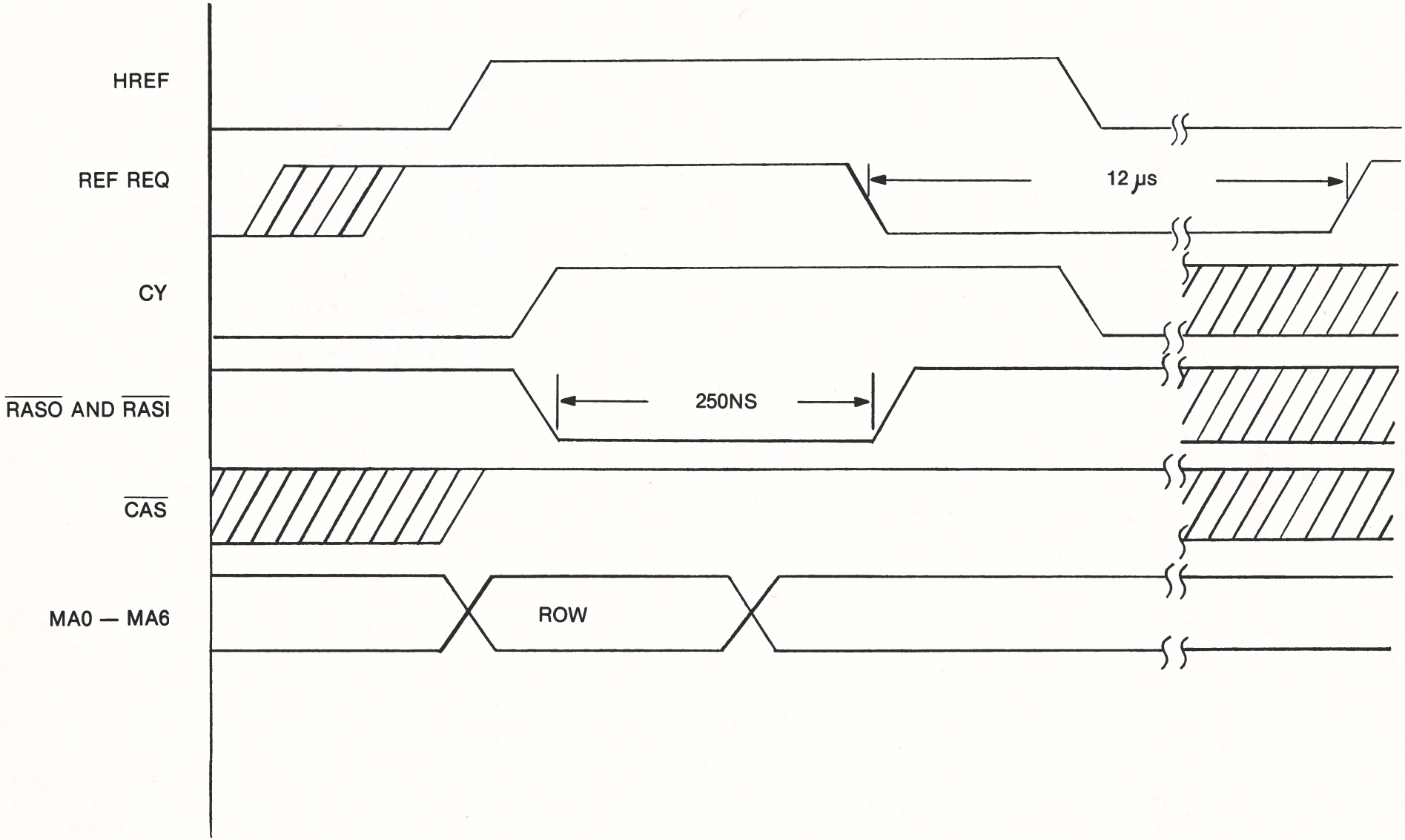
DATA CYCLE TIMING
FIGURE 3.1



DATO(B) TIMING
FIGURE 3.2



DATIO(B) TIMING
FIGURE 3.3

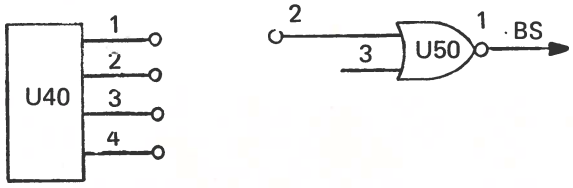


REFRESH TIMING
FIGURE 3.4

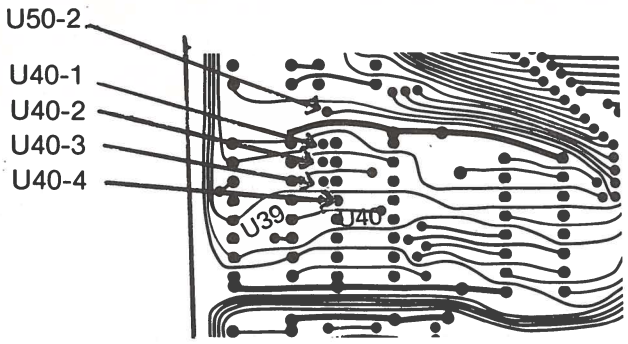
APPENDIX A

BANK SELECTION THRU 128K

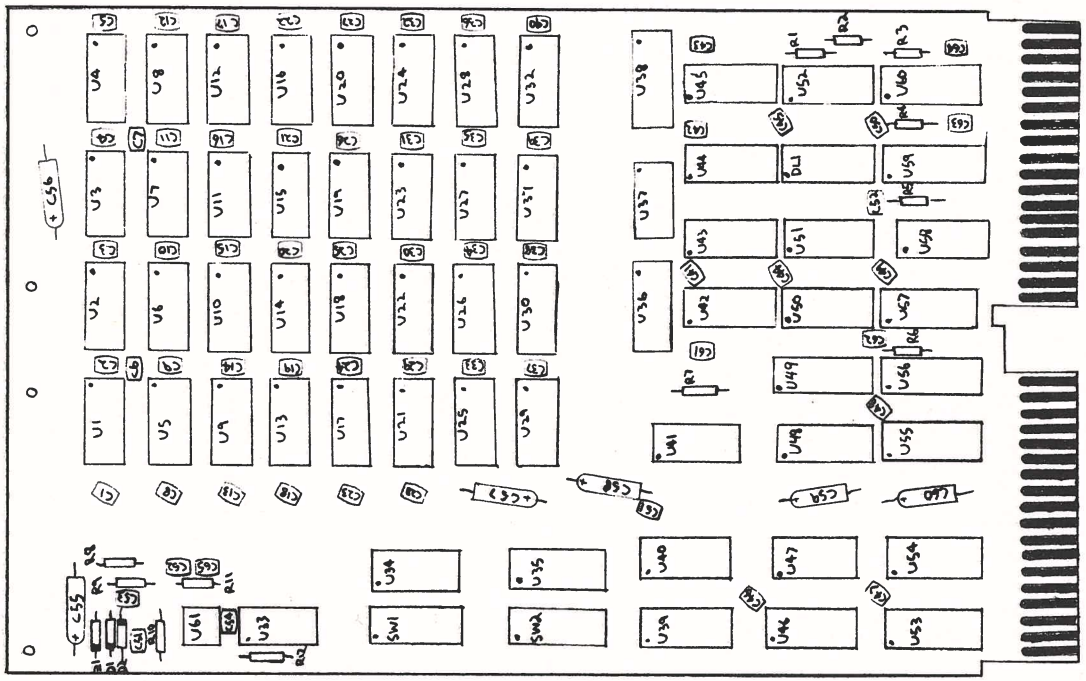
Your CI-1103 has been factory configured to operate in the 000000 177777 which is the maximum addressing capability of the LSI-11 based systems at this time. However, if the use of extended address bits BAL 16 and BAL 17 are implemented, the CI-1103 can be placed in 3 additional 32K memory banks. This gives the user up to 128K of addressable memory. Jumper configuration for the various memory banks is shown below.



Bank Selected	Jumper
00000 - 177777	U50-2 to U40-4
20000 - 377777	U50-2 to U40-3
40000 - 577777	U50-2 to U40-2
60000 - 777777	U50-2 to U40-1



COMPONENT SIDE



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SCALE: n/a	APPROVED BY:	DRAWN BY Ed Ross
DATE: 6-9-78		REVISED a

CI - 1103

DRAWING NUMBER 70054

REVISIONS				
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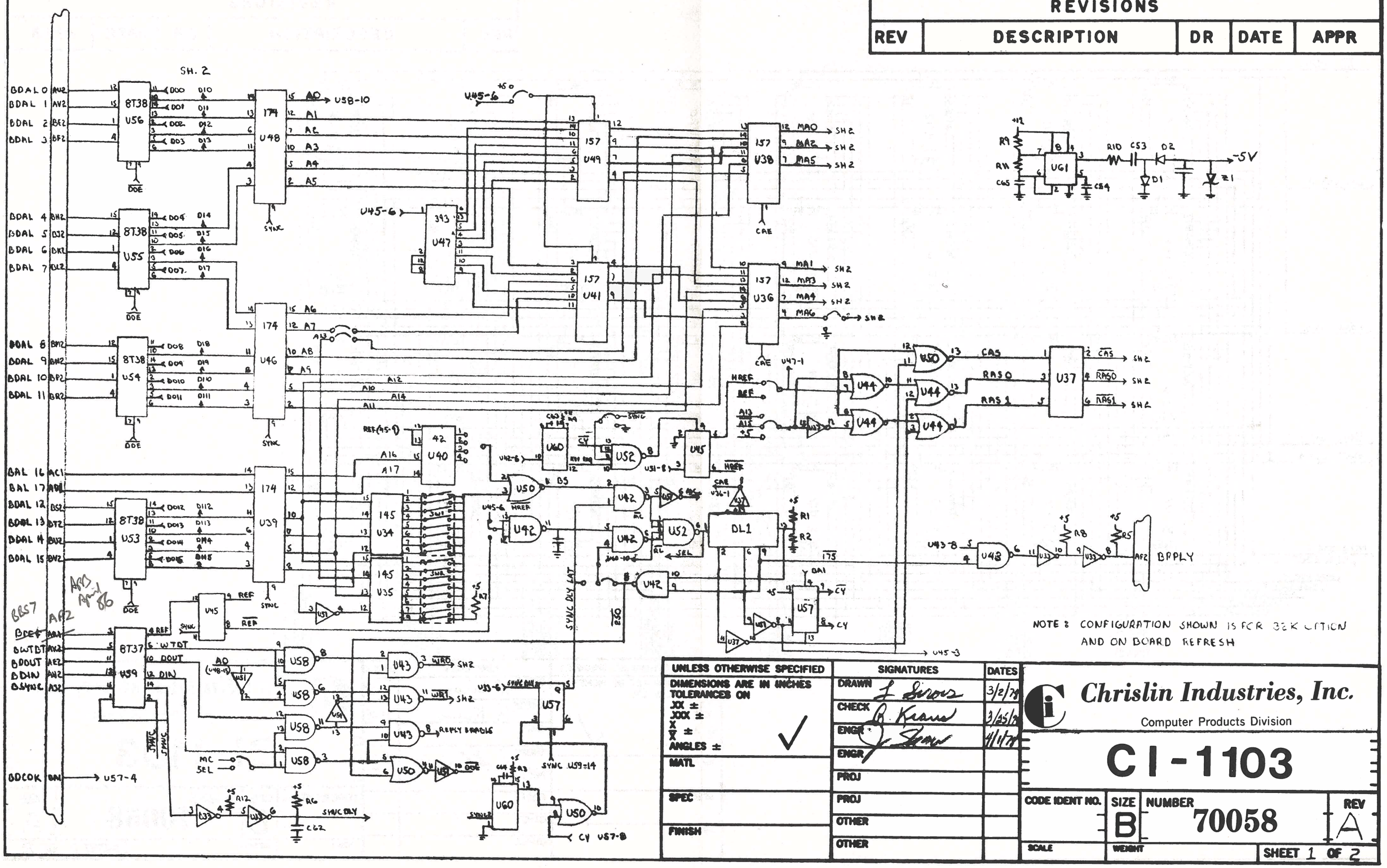

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	ENGR J. Gross	4/1/78
MATL	ENGR	
SPEC	PROJ	
FINISH	PROJ	
	OTHER	
	OTHER	

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CODE IDENT NO.	SIZE	NUMBER	REV
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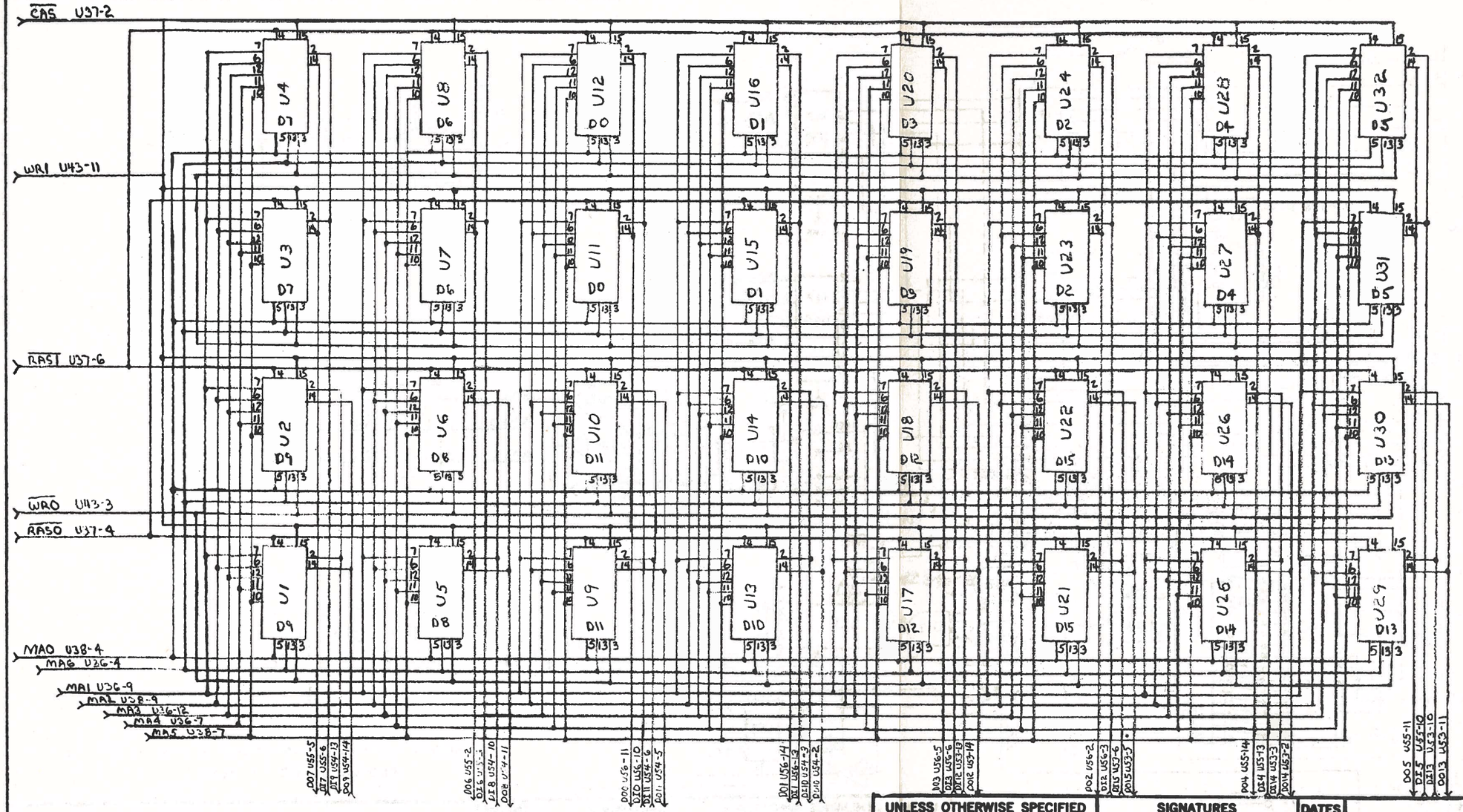
REVISIONS				
REV	DESCRIPTION	DR	DATE	APPR



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MATL	CHECK R. Kraus	3/24/78
SPEC	ENGR	
FINISH	ENGR J. Shaw	9/1/78
	PROJ	
	PROJ	
	OTHER	
	OTHER	

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CODE IDENT NO.	SIZE	NUMBER	REV
	B	70058	A
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