corporation

15 cummings park, woburn, ma. 01801 telephone (617) 935-6668 telex 949329

MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

INSTRUCTION MANUAL

IM-478
A2-10060, Rev. 2

adac corporation

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MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

GENERAL DESCRIPTION

The Model 1900 is the first bus translator that allows Digital Equipment Corporation LSI-11 peripherals to operate with a Unibus CPU (any of the PDP-11 series). The Model 1900 can be inserted directly into the Unibus. It allows peripherals located on the expander side to be communicated with in the exact manner as if the peripherals were inserted directly in the CPU bus. Peripherals on either side of the translator can transfer data to and from peripherals on its own bus or through the translator to the other bus with no significant loss of speed. Furthermore, the expander bus can be located up to 40 feet from the CPU bus.

Peripherals on the expander side of the translator can be operated under program control, program interrupt or direct memory access.

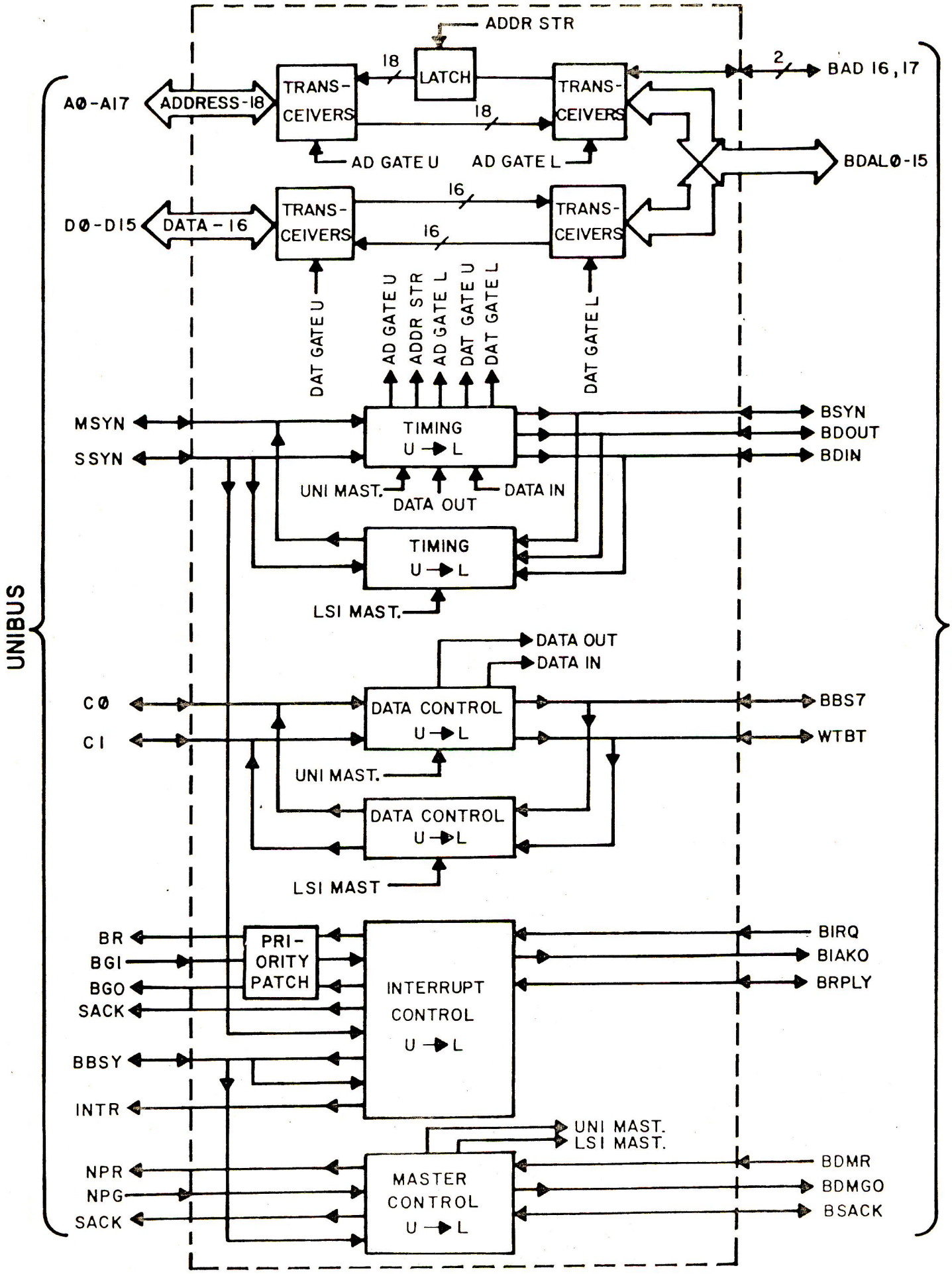
In addition to 16 bits of data, a full addressing capability of 18 bits is supplied across the translator. All inputs are buffered through low current input receivers and all outputs are either high powered open collector drivers or tri-state outputs. All inputs and outputs are terminated in 120 ohm characteristic impedances.

PHYSICAL DESCRIPTION

The Model 1900 consists of a quad size board (8 1/2" x 10") that can be plugged into the C-D-E-F positions of any of the four slots of a DEC DD11A system unit. Two 40 pin headers are mounted on the edge of the board away from the bus. Connection to the LSI-11 bus is made by means of two flat, high speed transmission cables. For connection to the ADAC System 1000 series, connectors are supplied to allow the cable to be plugged directly into its backplane. For connection to a PDP-11/03 or other LSI-11 backplanes, the cables are terminated on a half quad (8 1/2" x 5") board that plugs into one slot.

APPLICATION

The Model 1900 translator allows Unibus users to take full advantage of the substantially lower cost memories and peripherals that are available for the LSI-11 bus structure. It also allows all PDP-11 systems to operate with the ADAC System 1000 series of LSI-11 bus structured peripheral expanders. The System 1000 series can house up to 11 full quad or 22 half quad LSI-11 compatible peripherals in a 7" high rack mounted enclosure. The System 1000, which can operate with a resident LSI-11 CPU, can also be used as a slave expander chassis to any PDP-11 by inserting the Model 1900 into the Unibus and plugging the bus cable directly into its backplane.



BLOCK DIAGRAM - MODEL 1900 - BUS TRANSLATOR

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MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

THEORY OF OPERATION

The Model 1900 Bus Translator acts with the capacity of a traffic controller between a Unibus (with CPU) and an LSI-11 bus (without CPU). A master control section determines whether a module in the Unibus or a module in the LSI bus is to be master. The control is initialized so that the Model 1900 assumes that the Unibus is master unless the LSI bus requests and is granted bus mastership through a non-processor request.

When the Unibus is master, the timing and data control sections of the 1900 convert the Unibus signals such as MSYN, SSYN, CØ and C1 into properly timed LSI signals, such as BSYN, BDOUT, BDIN, BBSD and BWTBT. This allows any device in the Unibus to transfer data to and from any device in the LSI-11 bus.

The 16 address lines and 16 data lines of the Unibus are connected to the 16 multiplexed data address lines of the LSI bus through bidirectional transceivers. The two most significant address lined (A16, A17) are also carried through transceivers to the LSI extended address lines, BAD 16 and BAD 17 for future expansion capability.

The direction of signal flow through the address and data transceivers is determined by the master control section. When the Unibus is master, AD GATE L allows the address on the Unibus to be gated into the LSI bus at the beginning of MSYN. After the end of AD GATE L, either DAT GATE L or DAT GATE U is asserted, depending upon whether a Data Out or Data In operation is to be performed. These signals turn on the appropriate data drivers on the LSI bus for Data Out and on the Unibus for Data In. The timing signals, BDOUT or BDIN are also generated, with appropriate delays so that they can be used for data strobing purposes.

In all cases, and for each type of operation, complete interlocking handshaking of control signals occur between the Unibus and LSI bus to allow complete asynchronous operation. Signal delays through the translator and the bus extension cable are essentially of no significance because of the interlocking action employed. Also a minimum of 150 nanoseconds of delay is generated between data and the edge of any control signal to allow for deskewing of the address and data lines and for decoding by the bus devices.

Under program control, the PDP-11 CPU can access any device inserted in the LSI bus in the same manner as it would communicate with another device plugged into the Unibus. The addressing of memory and other peripherals located in the LSI bus have to be considered in the same vein as if the devices were plugged into the Unibus.

The interrupt control section of the Model 1900 translator allows any device plugged into the LSI bus to request an interrupt of the PDP-11. The interrupting level is jumper selectable on the 1900 to be one of four priority levels 7, 6, 5 or 4. Unless otherwise specified, the Model 1900 is shipped with the LSI bus requesting and being granted on priority level 7, which is the highest level. The request and grant signals for levels 6, 5 and 4 are jumpered through the board.

The interrupt control section supplies all the interlocking handshaking circuitry needed for proper Unibus operation. A vector produced on the LSI bus is passed through to the Unibus at the appropriate time.

The Model 1900 also allows a DMA device located in the LSI bus to request bus mastership. Once granted, the DMA device may then transfer data directly to a memory or storage device located in the LSI bus or located across the translator in the Unibus. With the LSI being granted master, the Model 1900 transforms all LSI bus control signals into appropriately timed Unibus signals. During the address portion of the LSI cycle, the address is stored in latches before driving the transceivers on the Unibus. The address and data is then presented in parallel, as required by the Unibus.

CABLE AND BUS TERMINATIONS

As mentioned earlier, the Model 1900 is a quad size card that plugs directly into the Unibus. On the side of the board opposite the Unibus are mounted two 40 pin headers that carry the LSI bus signals and allow connection to the LSI bus by means of the Model 1900-BC cable set. The 1900-BC cable set consists of two forty wire flat cables supplied in several configurations. All models have 50 pin strain relief connectors on both ends. The length and type of cable can vary. For 10' and 15' lengths the cable is supplied as 120 ohm flat ribbon cable. For 20', 30' and 40' lengths, the cable is supplied as 120 ohm flat twisted pair, with an individual ground wire twisted with each signal wire.

If the Model 1900 is operated with the ADAC System 1000 Series, the strain reliefed connector can plug directly into headers provided on its backplane. If the Model 1900 is to be used with the DEC LSI-11 backplane, or equivalent, the strain reliefed connector can plug into the ADAC Model 1900-CT cable terminator. The Model 1900-CT is a 1/2 quad board (8 1/2" x 5") that plugs directly into an LSI-11 configured backplane. The edge of the board opposite the bus contains two 40 pin headers in order to be able to accept the 1900-BC cable set.

INSTALLATION INSTRUCTIONS

The Model 1900 plugs into any slot, 1 through 4, positions C-D-E-F of a DEC DD11A or DD11B system unit. It can also be used in printed circuit backplanes such as used on the PDP 11/04. On the DD11-CK backplane, it may be inserted in any slot, 1 through 4, positions C-D-E-F. In the DD11-DK backplane, use any slot, 3 through 9, positions C-D-E-F.

On current production backplanes, DEC places a wire wrap jumper from pin CA1 to pin CB1 to preserve daisy chain continuity on the Non-Processer Grant signal. This jumper must be removed for proper operation of the 1900. On older system units, the NPG signal path is from 1AU1 to 4AU1. In this application, this wire must be removed and two wires must be added - from 1AU1 to CA1 on the 1900 slot and from CB1 on the 1900 slot to 4AU1. There must be no other wires on CA1 and CB1.

MODEL 1900

CONNECTOR J1

1.	Spare	2.	GROUND
3.	BDACL	4.	
5.	BDALØ	6.	
7.	BINIT	8.	
9.	BDMGI	10.	
11.	BREF	12.	
13.	BBS7	14.	
15.	HALT	16.	
17.	BDMR	18.	
19.	BIAK	20.	
21.	BIRQ	22.	
23.	BWTBT	24.	
25.	BSYN	26.	
27.	BDIN	28.	
29.	BRPLY	30.	
31.	BDOUT	32.	
33.	BAD 17	34.	
35.	BAD 16	36.	
37.	BUS Spare 2	38.	
39.	BUS Spare 1	40.	

MODEL 1900

CONNECTOR J2

1.	Spare	2.	GROUND
3.	BDAL 15	4.	
5.	BDAL 14	6.	
7.	BDAL 13	8.	
9.	BDAL 12	10.	
11.	BEVNT	12.	
13.	BDAL 11	14.	
15.	BUS Spare 6	16.	
17.	BDAL 1Ø	18.	
19.	BSACK	20.	
21.	BDAL 9	22.	
23.	BDAL 8	24.	
25.	BDAL 7	26.	
27.	BDAL 6	28.	
29.	BDAL 5	30.	
31.	BDAL 4	32.	
33.	BDAL 3	34.	
35.	BDAL 2	36.	
37.	BPOK	38.	
39.	BDCOK	40.	

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SPECIFICATIONS

MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

Function	Provides translation of all Unibus signals into LSI-11 bus signals (and vice versa) to allow LSI-11 peripherals to function directly with any PDP-11 Unibus computer.
Point of Insertion	Unit is plugged directly into Unibus.
Method of Connection to PDP-11/03	Connects to LSI-11 bus via Model 1900-BC Bus Cable and Model 1900-CT Cable Terminator.
Method of Connection to ADAC System 1000	Connects to bus of System 1000 Series via Model 1900-BC Bus Cable which plugs directly into backplane.
Unibus Loading	One bus load.
LSI-11 Drive Capability	15 bus loads on LSI-11 bus plus 120 ohm terminator on each line, mounted on Model 1900.
Module Types - LSI Side	All standard modules designed to interface to LSI-11 bus, except LSI-11 CPU. This includes A/D, D/A, memory floppy disc controllers, etc.
Communication Methods with LSI Peripherals	Program control, program interrupt and direct memory access.
Interfacing Technique	Completely asynchronous, interlocking handshake interface between Unibus and LSI-11 bus.

Effects on Unibus Programming	None. All PDP-11 instructions can operate across the interface. Operation is transparent to programmer.
Max Delay Through Interface	200 ns, plus cable delay.
Service Request Methods	Program interrupt, or non-processor request.
Interrupt Priority Level	A flexible jumper arrangement allows the Model 1900 to request interrupt on one of four request lines - BR7, BR6, BR5 or BR4. Unless otherwise specified, unit is wired for highest priority - BR7.
Interrupt Daisy Chain Continuity	All unused bus request lines and bus grant lines are jumpered through to preserve daisy chain integrity.
Non-processor Request	A DMA device plugged into LSI-11 bus can request bus mastership by asserting its BDMR line. This causes the NPR line to be asserted in the Unibus. Once granted mastership, the requesting device can then transfer data directly to any device on the LSI-11 bus or to any device on the Unibus.
Non-processor Grant Continuity	The NPG signal is passed through the Model 1900 unaltered if the requesting device is not on the LSI side of the translator.
Physical & Environmental Size	8 1/2" x 10" x 0.375" (standard DEC quad).
Unibus Compatibility	System Units DD11A & DD11B: Any slot, 1 through 4; Positions C-D-E-F (Use of Non-processor Request requires removal of one wire-wrap jumper and addition of one other). Backplane DD11-CK: Any slot, 1 through 4; Positions C-D-E-F Backplane DD11-DK: Any slot, 1 through 9; Positions C-D-E-F Backplane DD11-PK: Any slot, 3 through 9; Positions C-D-E-F
Power	+5V $\pm$ 5% @ 2 amps
Temperature Range of Operation	$0^{o}C$ to $55^{o}C$

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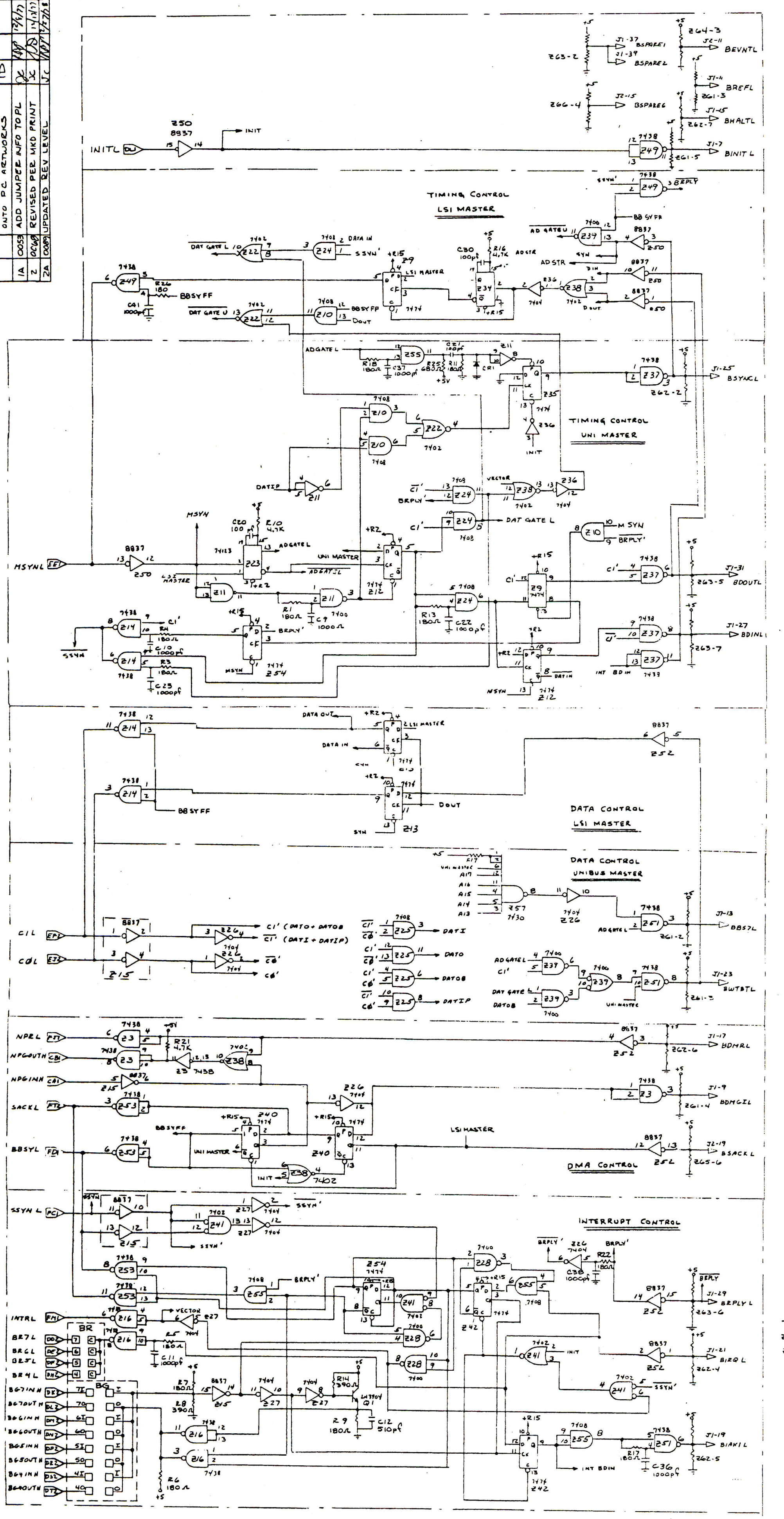
MODEL 1900

LSI-11 To UNIBUS TRANSLATOR SCHEMATIC

SIZE D — 5-10060 — REV 2A — SHEET 1 OF 2

REVISIONS

REV	ECO	DESCRIPTION	DWN	APPD	DATE
0A	—	REVISED CIRCUITRY, DELETED R12, C19	TB		
1	0028	ADDED R21, R23, R24, C38, C39, C40; INCORPORATE REV 0A CHANGES ONTO PC ARTWORKS	TB		
1A	0053	ADD JUMPER INFO TO PL	JC		12/6/77
2	0069	REVISED PER MKD PRINT	JC		1/13/77
2A	0089	UPDATED REV LEVEL	JC		



TYPICAL, ALL J1 & J2 SIGNALS: +5V, 180Ω, ZNO. - PIN NO., 390Ω. REPRESENTS ONE PIN OF 8 PIN SIP RESISTOR NETWORK ADAC # 23-000002 (PIN 1 = GND) (PIN 8 = +5V)

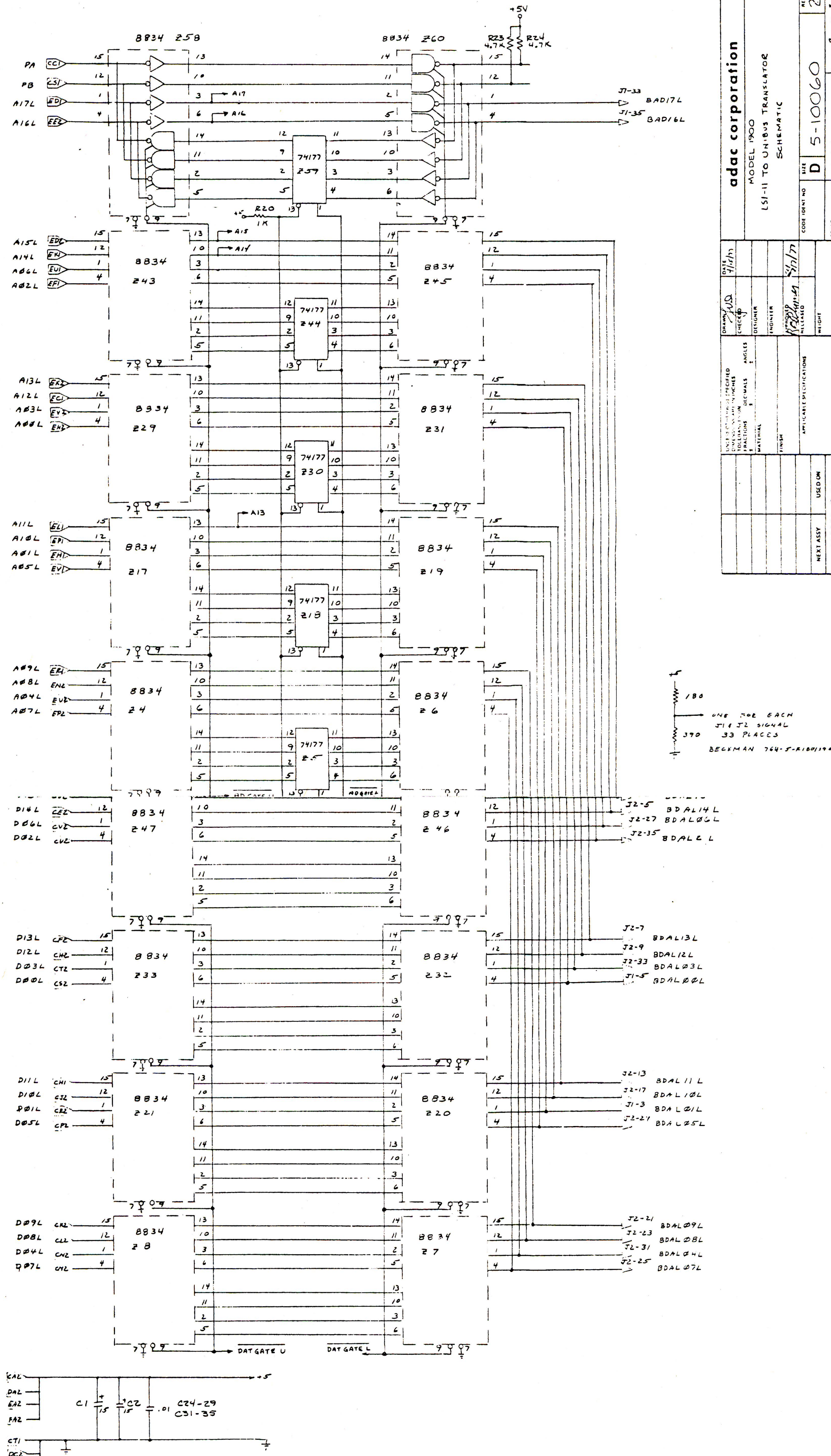
SPARE GATES

Z28	7400	12,13,11
Z27	7404	3,4

SIZE		REV
D	5-10060	2A

REVISIONS

REV	ECO	DESCRIPTION	DWN	APP'LS	DATE
		SEE SHEET 1 FOR REVISIONS			



+5V
8834 Z58
8834 Z60
R23 4.7K
R24 4.7K
74177 Z57
R20 1K
8834 Z43
8834 Z45
74177 Z44
8834 Z29
8834 Z31
74177 Z30
8834 Z17
8834 Z19
74177 Z18
8834 Z4
8834 Z6
74177 Z5
8834 Z47
8834 Z46
8834 Z33
8834 Z32
8834 Z21
8834 Z20
8834 Z8
8834 Z7
J1-33 BADI7L
J1-35 BADI6L
J2-5 BDALI4L
J2-27 BDALØ6L
J2-35 BDALØ2L
J2-7 BDALI3L
J2-9 BDALI2L
J2-33 BDALØ3L
J1-5 BDALØØL
J2-13 BDALI1L
J2-17 BDALIØL
J1-3 BDALØ1L
J2-21 BDALØ5L
J2-21 BDALØ9L
J2-23 BDALØ8L
J2-31 BDALØ4L
J2-25 BDALØ7L
180
390
ONE FOR EACH J1 & J2 SIGNAL 33 PLACES
BECKMAN 764-5-R180/390
DAT GATE U
DAT GATE L
C1 15
C2 15
.01 C24-29 C31-35

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MODEL 1900
LSI-11 TO UNIBUS TRANSLATOR
SCHEMATIC

SIZE	CODE IDENT NO		REV
D		5-10060	2A
SCALE		SHEET 2 OF 2	